Advance Information

# 256K × 4 CMOS Dynamic RAM

The MCM514258 is a 1.2μ CMOS high-speed, dynamic random access memory. It is organized as 262,144 four-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM514258 requires only nine address lines; row and column address inputs are multiplexed. The device is packaged in standard 300 mil wide packages: dual-in-line package (DIP) and J-lead small outline package.

- Three-State Data Output
- Static Column Mode Capability
- TTL-Compatible Inputs and Output
- $\overline{RAS}$ Only Refresh
- $\overline{CS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle, 8 ms Refresh
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM514258-85 = 85 ns (Maximum)
  MCM514258-10 = 100 ns (Maximum)
  MCM514258-12 = 120 ns (Maximum)
- Low Active Power Dissipation: MCM514258-85 = 413 mW (Maximum)
  MCM514258-10 = 358 mW (Maximum)
  MCM514258-12 = 303 mW (Maximum)
- Low Standby Power Dissipation: 11 mW (Maximum, TTL Levels)
  5.5 mW (Maximum, CMOS Levels)
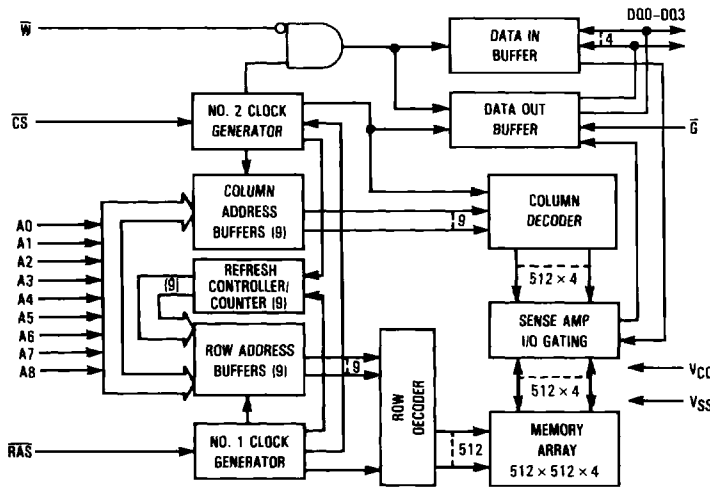
MCM514258

P PACKAGE
PLASTIC
CASE 738A

J PACKAGE
SMALL OUTLINE
CASE 822

2

PIN ASSIGNMENT
DUAL-IN-LINE

DQ0	1 ●	20	V_{SS}
DQ1	2	19	DQ3
$\overline{W}$	3	18	DQ2
$\overline{RAS}$	4	17	$\overline{CS}$
NC	5	16	$\overline{G}$
A0	6	15	A8
A1	7	14	A7
A2	8	13	A6
A3	9	12	A5
V_{CC}	10	11	A4

SMALL OUTLINE

DQ0	1	26	V_{SS}
DQ1	2	25	DQ3
$\overline{W}$	3	24	DQ2
$\overline{RAS}$	4	23	$\overline{CS}$
NC	5	22	$\overline{G}$
A0	9	18	A8
A1	10	17	A7
A2	11	16	A6
A3	12	15	A5
V_{CC}	13	14	A4

BLOCK DIAGRAM

PIN NAMES

A0–A8	Address Input
DQ0–DQ3	Data Input/Output
$\overline{G}$	Output Enable
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No Connection

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MCM514258

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-1 to $+7$	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	-1 to $+7$	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_A	0 to $+70$	°C
Storage Temperature Range	T_{stg}	-55 to $+150$	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 5.0$ V $\pm 10\%$, $T_A = 0$ to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	-1.0	—	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM514258-85, $t_{RC} = 165$ ns MCM514258-10, $t_{RC} = 190$ ns MCM514258-12, $t_{RC} = 220$ ns	I_{CC1}	 — — —	 75 65 55	mA	2
V_{CC} Power Supply Current (Standby) ($\overline{RAS} = \overline{CS} = V_{IH}$)	I_{CC2}	—	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CS} = V_{IH}$) MCM514258-85, $t_{RC} = 165$ ns MCM514258-10, $t_{RC} = 190$ ns MCM514258-12, $t_{RC} = 220$ ns	I_{CC3}	 — — —	 75 65 55	mA	2
V_{CC} Power Supply Current During Static Column Mode Cycle ($\overline{RAS} = V_{IL}$) MCM514258-85, $t_{SC} = 50$ ns MCM514258-10, $t_{SC} = 55$ ns MCM514258-12, $t_{SC} = 70$ ns	I_{CC4}	 — — —	 75 65 55	mA	2
V_{CC} Power Supply Current (Standby) ($\overline{RAS} = \overline{CS} = V_{CC} - 0.2$ V)	I_{CC5}	—	1.0	mA	
V_{CC} Power Supply Current During $\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle MCM514258-85, $t_{RC} = 165$ ns MCM514258-10, $t_{RC} = 190$ ns MCM514258-12, $t_{RC} = 220$ ns	I_{CC6}	 — — —	 75 65 55	mA	2
Input Leakage Current ($0 \leq V_{in} \leq 6.5$ V)	$I_{lkg(I)}$	-10	10	μA	
Output Leakage Current ($\overline{CS} = V_{IH}$, $0 \leq V_{out} \leq 5.5$ V)	$I_{lkg(O)}$	-10	10	μA	
Output High Voltage ($I_{OH} = -5$ mA)	V_{OH}	2.4	—	V	
Output Low Voltage ($I_{OL} = 4.2$ mA)	V_{OL}	—	0.4	V	

CAPACITANCE (f = 1.0 MHz, $T_A = 25$°C, $V_{CC} = 5$ V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0–A8	C_{in}	5	pF	3
	G, $\overline{RAS}$, $\overline{CS}$, $\overline{W}$		7	pF	3
Output Capacitance ($\overline{CS} = V_{IH}$ to Disable Output)	DQ0–DQ3	C_{out}	7	pF	3

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

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AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 5.0$ V $\pm 10\%$, $T_A = 0$ to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM514258-85		MCM514258-10		MCM514258-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	165	—	190	—	220	—	ns	5
Read-Modify-Write Cycle Time	t_{RELREL}	t_{RMW}	225	—	255	—	295	—	ns	5
Static Column Mode Cycle Time	t_{AVAV}	t_{SC}	50	—	55	—	65	—	ns	
Static Column Mode Read-Modify-Write Cycle Time	t_{AVAV}	t_{SRMW}	110	—	115	—	135	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	85	—	100	—	120	ns	6, 7
Access Time from $\overline{CS}$	t_{CELQV}	t_{CAC}	—	30	—	30	—	35	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	45	—	50	—	60	ns	6, 9
Access Time from Last Write	t_{WLQV}	t_{ALW}	—	85	—	95	—	115	ns	6, 10
$\overline{CS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	5	—	5	—	5	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	30	0	30	0	35	ns	11
Output Data Hold Time from Column Address	t_{AXQX}	t_{AOH}	5	—	5	—	5	—	ns	
Output Data Enable Time from Write	t_{WHQV}	t_{OW}	—	30	—	30	—	35	ns	
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	85	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ Pulse Width (Static Column Mode)	t_{RELREH}	t_{RASC}	85	100,000	100	100,000	120	100,000	ns	
$\overline{CS}$ to $\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	30	—	30	—	35	—	ns	
$\overline{RAS}$ to $\overline{CS}$ Hold Time	t_{RELCEH}	t_{CSH}	85	—	100	—	120	—	ns	
$\overline{CS}$ Pulse Width	t_{CELCEH}	t_{CS}	30	10,000	30	10,000	35	10,000	ns	
$\overline{CS}$ Pulse Width (Static Column Mode)	t_{CELCEH}	t_{CSC}	30	100,000	30	100,000	35	100,000	ns	
$\overline{RAS}$ to $\overline{CS}$ Delay Time	t_{RELCEL}	t_{RCD}	25	55	25	70	25	85	ns	12
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	20	40	20	50	20	60	ns	13
$\overline{CS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	10	—	10	—	10	—	ns	
$\overline{CS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	15	—	15	—	20	—	ns	
$\overline{CS}$ Precharge Time (Static Column Mode)	t_{CEHCEL}	t_{CP}	10	—	10	—	15	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	15	—	15	—	15	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	20	—	20	—	25	—	ns	
Write Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AWR}	65	—	75	—	90	—	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	100	—	115	—	140	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	45	—	50	—	60	—	ns	

(continued)

NOTES:
1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements $t_T = 5.0$ ns.
5. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
6. Measured with a current load equivalent to 2 TTL (-200 μA, $+4$ mA) loads and 100 pF with the data output trip points set at $V_{OH} = 2.0$ V and $V_{OL} = 0.8$ V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. Assumes that $t_{LWAD} \leq t_{LWAD}$ (max).
11. t_{OFF} (max) and/or t_{GZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

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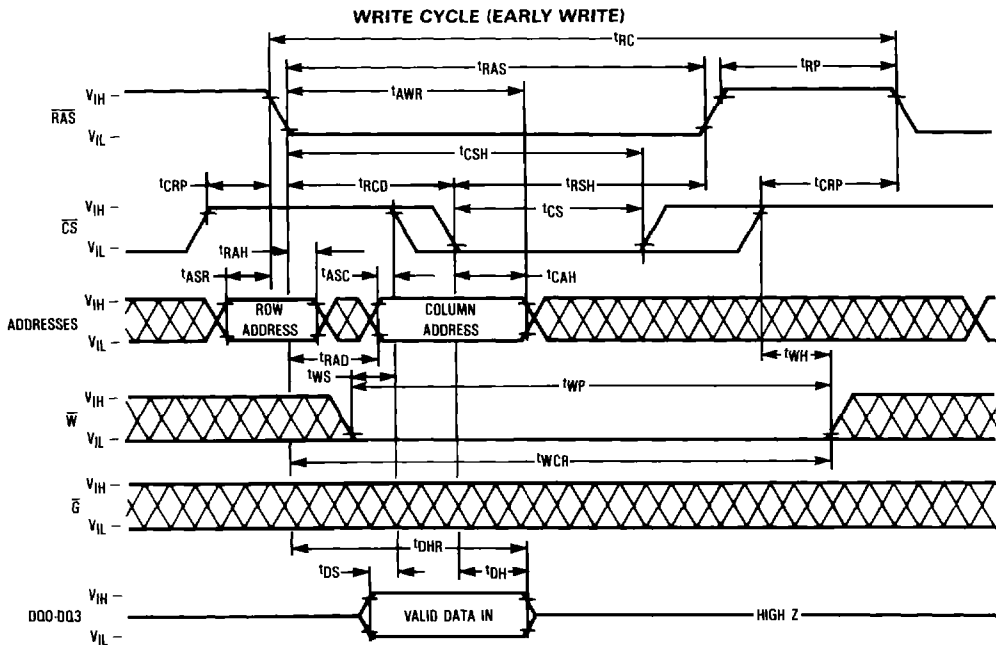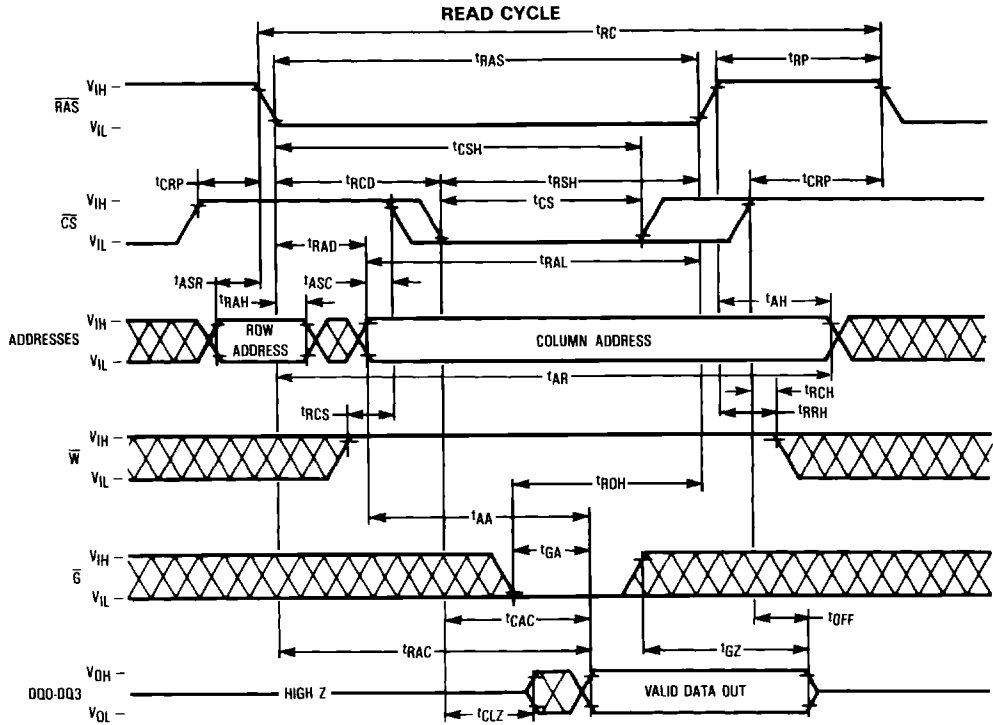## READ, WRITE, AND READ-MODIFY-WRITE CYCLES (Continued)

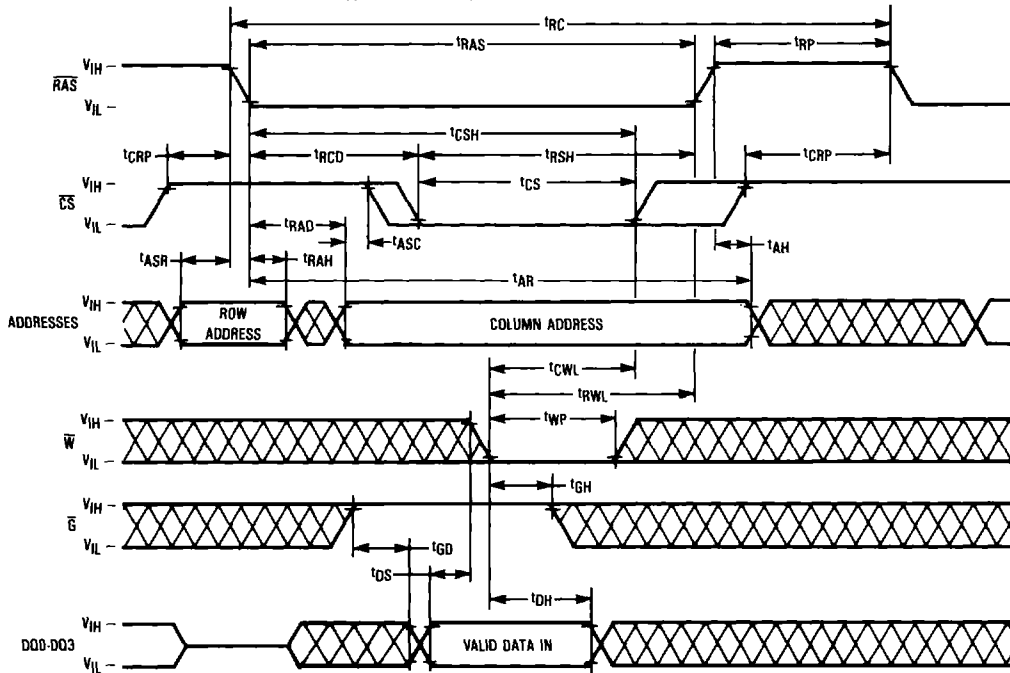| Parameter	Symbol Standard	Symbol Alternate	MCM514258-85 Min	MCM514258-85 Max	MCM514258-10 Min	MCM514258-10 Max	MCM514258-12 Min	MCM514258-12 Max	Unit	Notes
Column Address Hold Time Referenced to $\overline{RAS}$	t_{REHAX}	t_{AH}	10	—	10	—	15	—	ns	14
Last Write to Column Address Delay Time	t_{WLAV}	t_{LWAD}	25	40	25	45	30	55	ns	15
Last Write to Column Address Hold Time	t_{WLAX}	t_{AHLW}	85	—	95	—	115	—	ns	
Read Command Setup Time Referenced to $\overline{CS}$	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CS}$	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	16
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	16
Write Command Hold Time (Output Data Disable)	t_{CEHWH}	t_{WH}	0	—	0	—	0	—	ns	17
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	65	—	75	—	90	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	20	—	20	—	25	—	ns	
Write Inactive Time	t_{WHWL}	t_{WI}	10	—	10	—	15	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	25	—	30	—	ns	
Write Command to $\overline{CS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	25	—	30	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	18
Data in Hold Time	t_{CELDX}	t_{DH}	20	—	20	—	25	—	ns	18
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	65	—	75	—	90	—	ns	
Refresh Period	t_{RVRV}	t_{RFSH}	—	8	—	8	—	8	ms	
Write Command Setup Time (Output Data Disable)	t_{WLCEL}	t_{WS}	0	—	0	—	0	—	ns	17
$\overline{CS}$ to Write Delay (RMW Cycle)	t_{CELWL}	t_{CWD}	65	—	65	—	75	—	ns	17
$\overline{RAS}$ to Write Delay (RMW Cycle)	t_{RELWL}	t_{RWD}	120	—	135	—	160	—	ns	17
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	80	—	85	—	100	—	ns	17
$\overline{CS}$ Setup Time for $\overline{CS}$ Before $\overline{RAS}$ Refresh	t_{CELREL}	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CS}$ Hold Time for $\overline{CS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	—	30	—	30	—	ns	
$\overline{RAS}$ Precharge to $\overline{CS}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	ns	
$\overline{CS}$ Precharge Time for $\overline{CS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	50	—	50	—	60	—	ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{G}$	t_{GLREH}	t_{ROH}	20	—	20	—	20	—	ns	
$\overline{G}$ Access Time	t_{GLQV}	t_{GA}	—	30	—	30	—	35	ns	
$\overline{G}$ to Data Delay	t_{GHDX}	t_{GD}	25	—	25	—	30	—	ns	
Output Buffer Turn-Off Delay Time from $\overline{G}$	t_{GHQZ}	t_{GZ}	0	25	0	25	0	30	ns	11
$\overline{G}$ Command Hold Time	t_{WLGL}	t_{GH}	25	—	25	—	30	—	ns	

NOTES:
14. t_{AH} is the condition to latch the column address when $\overline{RAS}$ transitions from low to high.
15. Operation within the specified t_{LWAD} (max) limit ensures that t_{ALW} (max) can be met. t_{LWAD} (max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled exclusively by t_{AA}.
16. Enter t_{RRH} or t_{RCH} must be satisfied for a read cycle.
17. t_{WH}, t_{WS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
18. These parameters are referenced to $\overline{CS}$ leading edge in random write cycles and to $\overline{W}$ leading edge in delayed write or read-modify-write cycles.
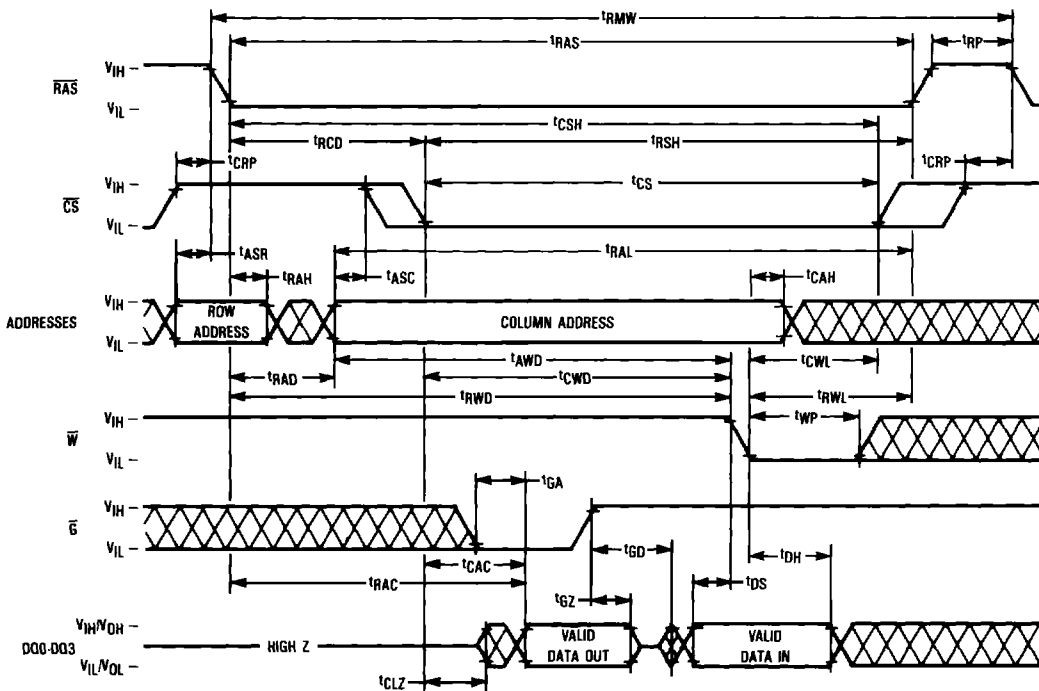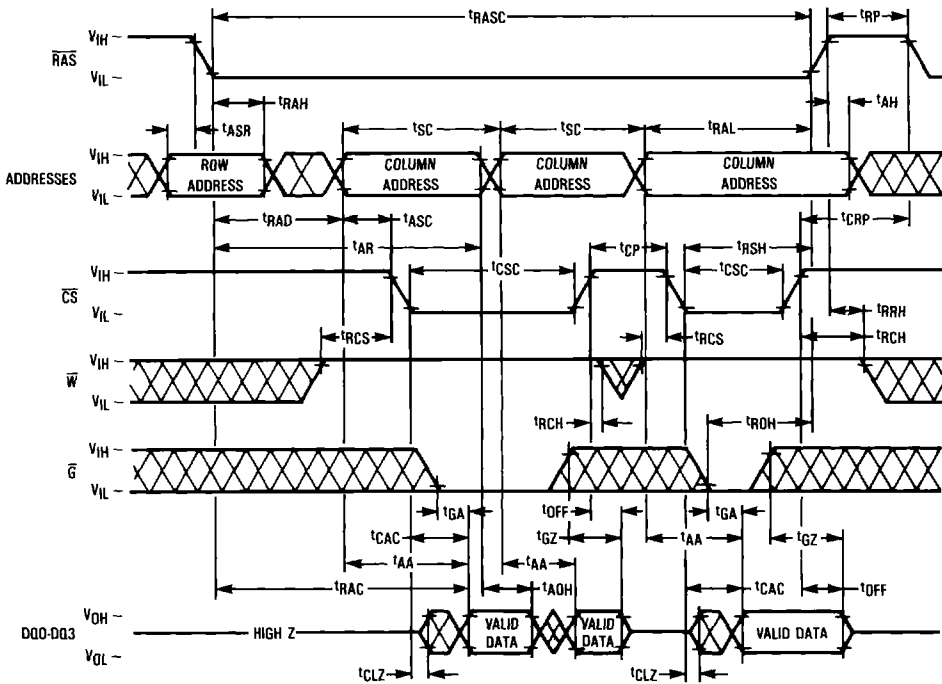
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READ CYCLE

MCM514258
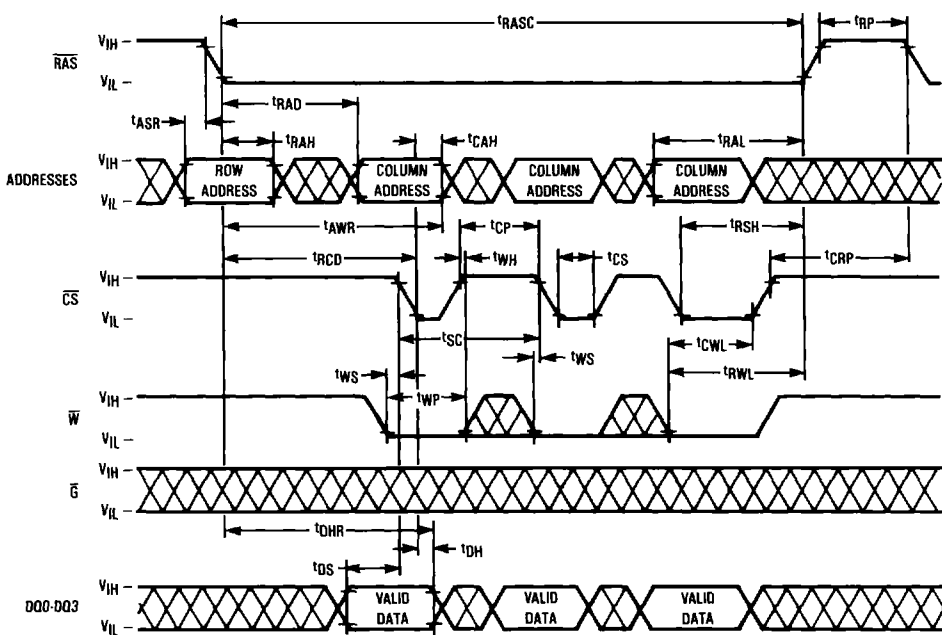
WRITE CYCLE (G̅ CONTROLLED WRITE)

READ-MODIFY-WRITE CYCLE
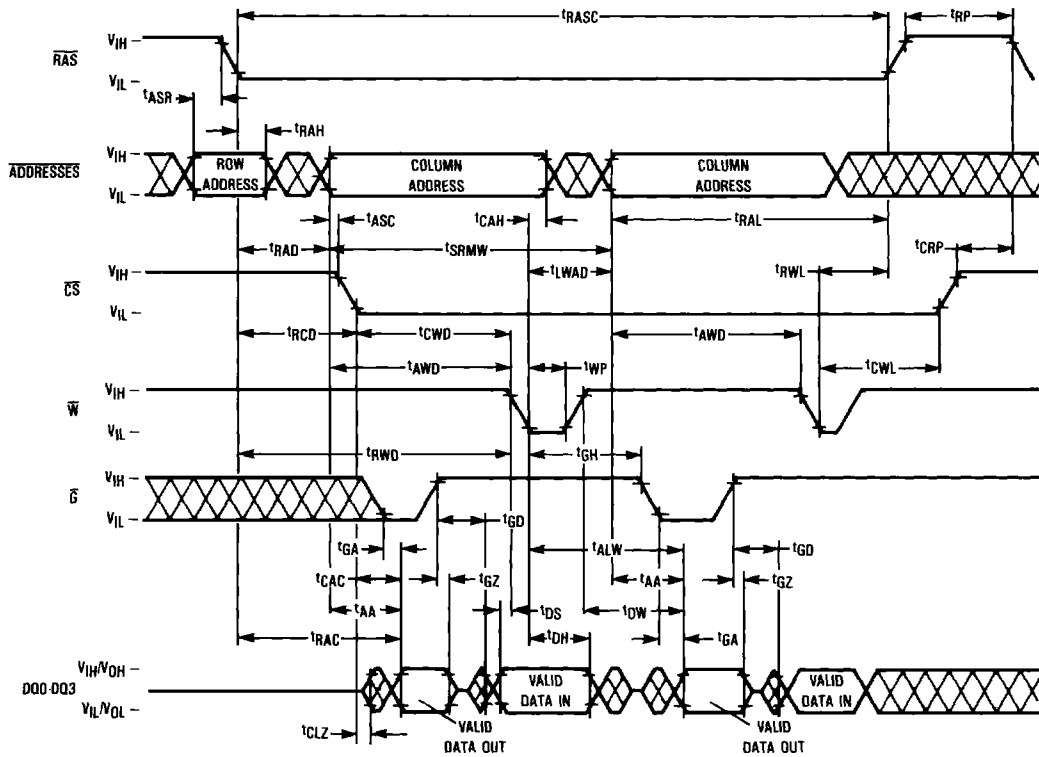
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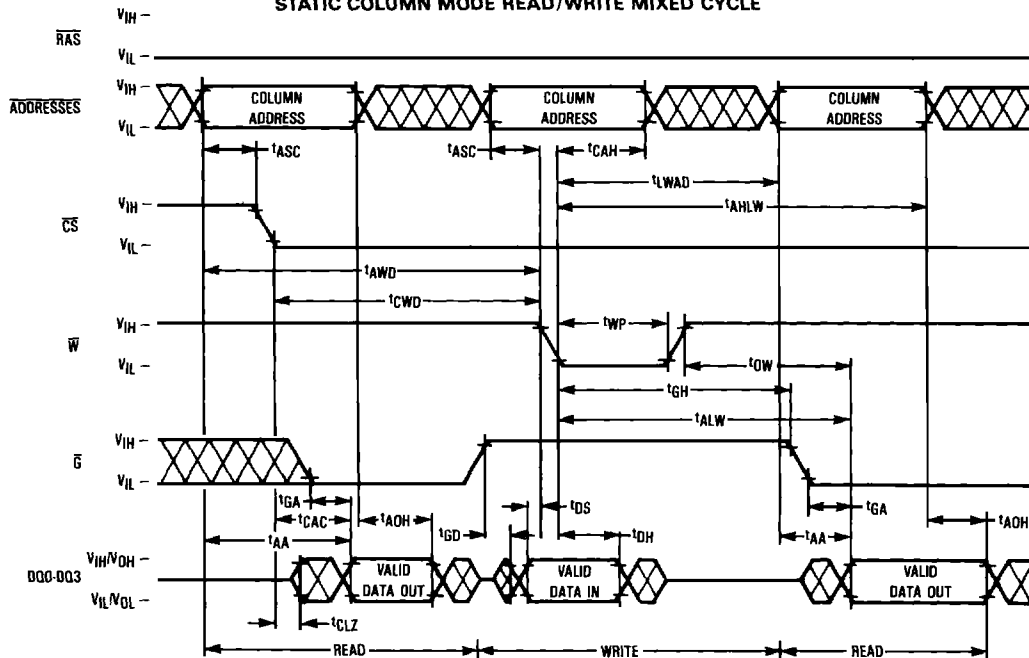## STATIC COLUMN MODE READ CYCLE

STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)
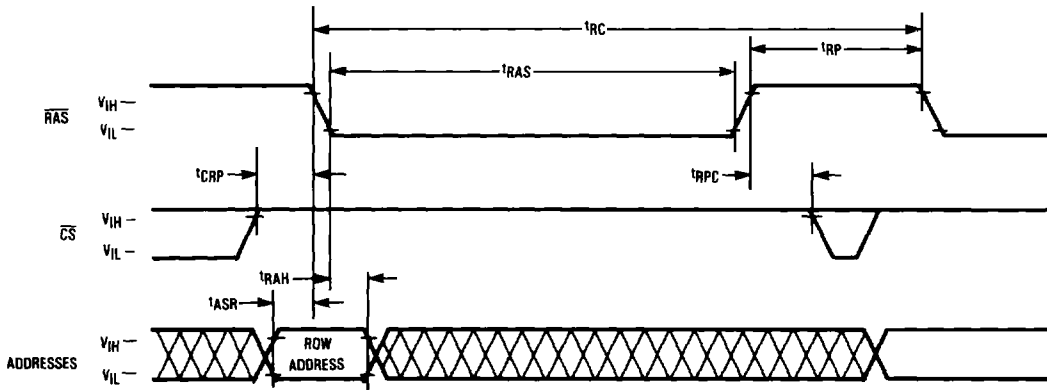
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STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE

STATIC COLUMN MODE READ/WRITE MIXED CYCLE

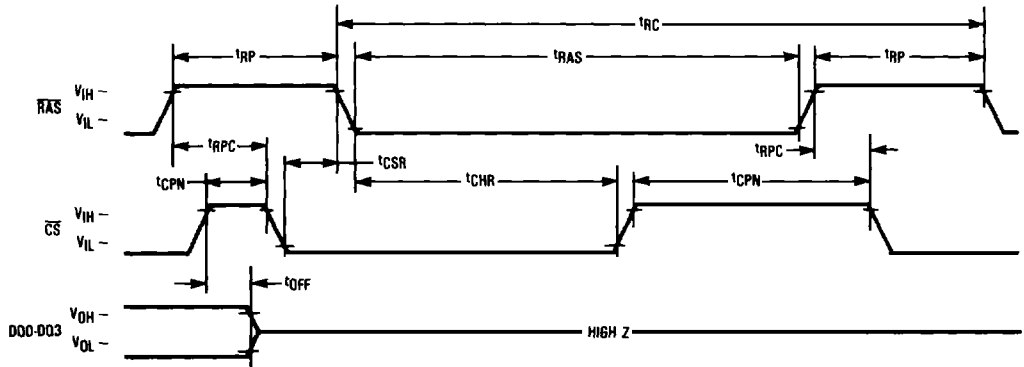# MCM514258

RAS ONLY REFRESH CYCLE
(W̄ and Ḡ are Don't Care)

C̄S̄ BEFORE R̄ĀS̄ REFRESH CYCLE
(W̄, Ḡ, and A0-A8 are Don't Care)

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HIDDEN REFRESH CYCLE (READ)

HIDDEN REFRESH CYCLE (WRITE)

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$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE

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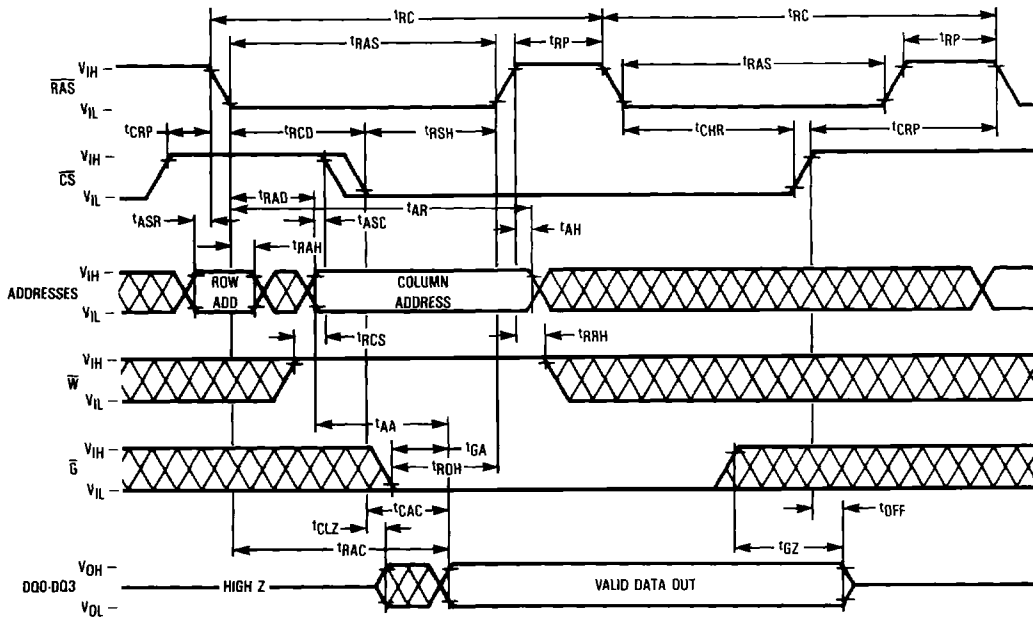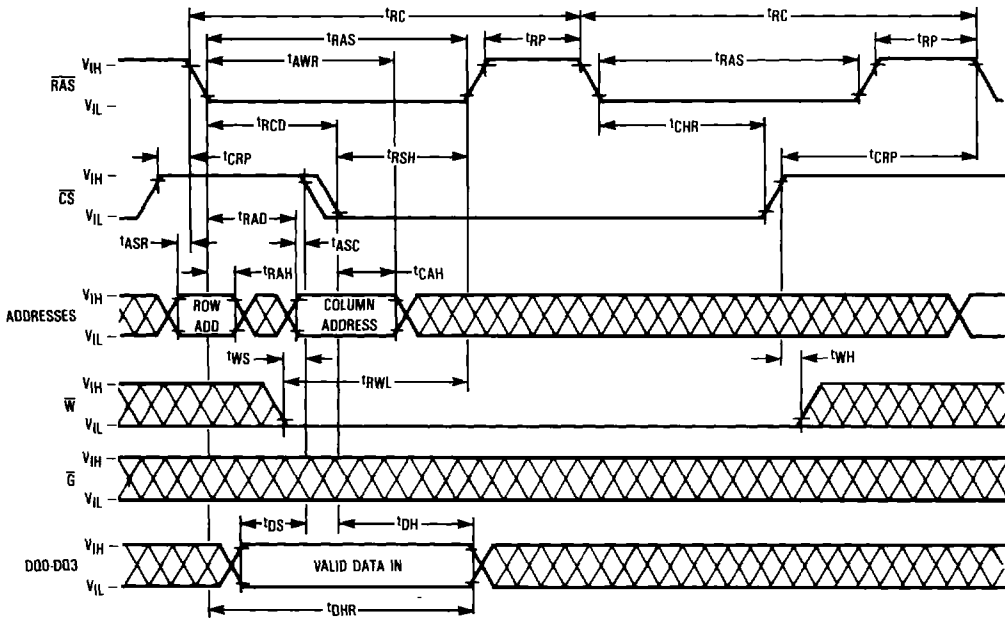
DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

ADDRESSING THE RAM

The nine address pins on the device are time multiplexed with two separate 9-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CS}$). A total of 18 address bits will decode one of the 262,144 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, other variations in addressing the RAM, the refresh modes ($\overline{RAS}$ only refresh; $\overline{CS}$ before $\overline{RAS}$ refresh; hidden refresh), another mode called static column mode allows the user to column access the 512 bits within a selected row. The refresh mode and static column mode operations are described in more detail later on.

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a static column mode read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CS}$ clock active transition will determine read access time. The external $\overline{CS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CS}$ clock will allow the external $\overline{CS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CS}) period for the $\overline{CS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CS}$ and $\overline{G}$ clocks are active; the output will switch to the three-state mode when either the $\overline{CS}$ or $\overline{G}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{CS}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisfied before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write ($\overline{W}$) clock can occur much later in time with respect to the active transition of the $\overline{CS}$ clock. This time could be as long as 10 microseconds— ($t_{RWL} + t_{RP} + 2t_T$).

In a late write or a ready-modify-write cycle, $\overline{G}$ must be at the V_{IH} level to bring the output buffers to high impedance prior to data-in being valid.

At the start of an early write cycle, the data out is in a high impedance condition and remains inactive throughout the cycle. The data out remains three-state because the active transition of the write ($\overline{W}$) clock prevents the $\overline{CS}$ clock from enabling the data-out buffers. The three-state condition (high impedance) of the data out pin during a write cycle can be effectively utilized in systems that have a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE CYCLE

As the name implies, both a read and a write cycle are accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{W}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{W}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

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STATIC COLUMN MODE CYCLES

Output buffers are always on when the device is in the static column mode and $\overline{CS}$ clock is not cycled, resulting in fewer transients and simpler operation. The static column mode allows faster access (t_{AA}) to any of the 512 column addresses on a given row, typically at half the standard (t_{RAC}) rate for randomly performed operations. Static column mode operation consists of changing column addresses while holding the $\overline{RAS}$ and $\overline{CS}$ clocks active. A new column location can be accessed with each static column cycle (t_{SC}).

Static column mode operation is initiated with a standard read or write cycle. The row address is latched by the $\overline{RAS}$ clock transition to active, followed by column addresses and $\overline{CS}$ clock. Performing an address cycle (t_{SC}) while $\overline{RAS}$ and $\overline{CS}$ clocks remain active constitutes the first static column cycle. Subsequent static column cycles can be performed as long as the $\overline{RAS}$ and $\overline{CS}$ clocks are held active. The first access (data out) occurs at the standard (t_{RAC}) rate. All of the read operations in static column mode following the initial operation are measured at the faster rate (t_{AA}), provided all other timing minimums are maintained. Static column cycle time determines how fast successive bits are read.

Any combination of read, write, or read-modify-write operations can be performed in the static column mode. The conditions normal to each operation apply when the device is operated in this mode.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 8 milliseconds. This is accomplished by sequentially cycling through the 512 row address locations every 8 milliseconds, (i.e., at least one row every 15.6 microseconds). A normal read or write operation to the RAM will serve to refresh all the bits associated with the particular rows decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 512 row addresses every 8 milliseconds. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CS}$ clock is not required and must be inactive or at a V_{IH} level.

$\overline{CS}$ Before $\overline{RAS}$ Refresh

$\overline{CS}$ before $\overline{RAS}$ refreshing available on the MCM514258 offers an alternate refresh method. If $\overline{CS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place.

After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh

An optional feature of the MCM514258 is that refresh cycle may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CS}$ before $\overline{RAS}$ refresh cycle. (see Figure 1 below)

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh operation of MCM514258 can be tested by $\overline{CS}$ before $\overline{RAS}$ refresh counter test. This cycle performs read/write operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{CS}$ before $\overline{RAS}$ cycles as initialization cycles. The test procedure is as follows.

1. Write a "0" into all memory cells.
2. Select any column address and read the "0"s written in step 1. Write a "1" into each cell of the selected column by performing $\overline{CS}$ before $\overline{RAS}$ Refresh Counter Test Read-Write Cycle (see timing diagram). Repeat 512 times.
3. Read the "1"s (use a normal read mode) written in step 2.
4. Select the same column address as step 2, read the "1"s and write a "0" into each cell by performing $\overline{CS}$ before $\overline{RAS}$ Refresh Counter Test Read-Write Cycle (see timing diagram). Repeat 512 times.
5. Read the "0"s (use a normal read mode) written in step 4.
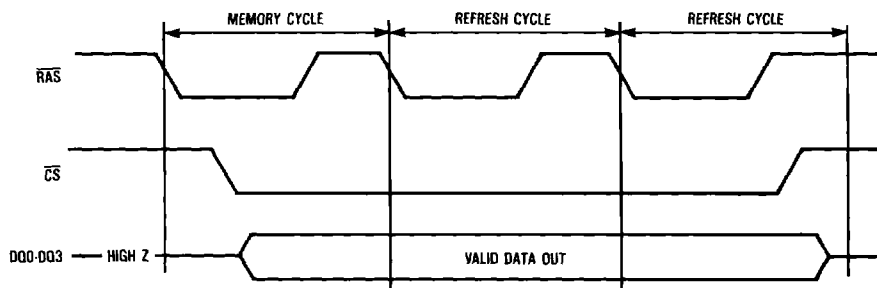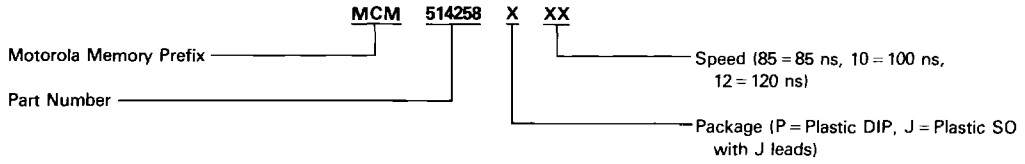6. Repeat steps 1 through 5 using complement data.

Figure 1. Hidden Refresh Cycle

MCM514258

ORDERING INFORMATION
(Order by Full Part Number)

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        MCM   514258   X   XX
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Motorola Memory Prefix ─────────────────

Part Number ────────────────────

Speed (85 = 85 ns, 10 = 100 ns, 12 = 120 ns)

Package (P = Plastic DIP, J = Plastic SO with J leads)

Full Part Numbers—	MCM514258P85	MCM514258J85
	MCM514258P10	MCM514258J10
	MCM514258P12	MCM514258J12