CCD 153A
512-Element High Speed Linear Image Sensor

FEATURES

- **512 x 1 photosite array**
- **13 µm x 13 µm photosites on 13µm pitch**
- **High speed: up to 20 MHz data rate**
- **Enhanced spectral response**
- **Low dark signal**
- **High responsivity**
- **On-chip clock drivers**
- **Dynamic range typical: 5000:1**
- **Over 1 V peak-to-peak outputs**
- **Dark and white references contained in sample-and-held output**

GENERAL DESCRIPTION

The CCD153A is a 512-photoelement linear image sensor utilizing charge-coupled device technology. It is designed for visible and very-near-IR imaging applications such as page scanning, facsimile, optical character recognition, earth-resources-satellite telescopes, and other applications which require high resolution, high responsivity, high data rates, and high dynamic range.

The CCD153A has been improved and is pin-for-pin compatible with the CCD153 except for the deletion of the end-of-Scan Waveform (EOS_{OUT}). The CCD153A has several new features which may be implemented at the user's option by supplying input voltages and wave forms different than those required for standard CCD153-type operation.

Photoelement size is 13 µm (0.51mils) x 13 µm (0.51 mils) on 13 µm (0.51 mils) centers. The devices are manufactured using Fairchild Imaging's advanced second-generation n-channel Isoplanar buried-channel technology.

PIN NAMES	DESCRIPTION
V_{OUT_A}	Output Amplifier A Source
ϕSH_{GA}	Sample-and-Hold Gate A
ϕSH_{CA}	Sample-and-Hold Clock A
V_{CD}	Clock Driver Drain
NC	No Connection (Do Not Ground)
V_T	Transport Register DC Electrode
V_{EI}	Electrical Input Bias
V_{SS}	Substrate Ground
V_{PG}	Photogate
ϕX	Transfer Clock
ϕT	Transport Clock
V_{RD}	Reset Transistor Drain
ϕSH_{CB}	Sample-and-Hold Clock B
ϕSH_{GB}	Sample-and-Hold Gate B
V_{OUT_B}	Output Amplifier B Source
V_{DD}	Output Amplifier Drain

PIN CONNECTION DIAGRAM
(TOP VIEW)

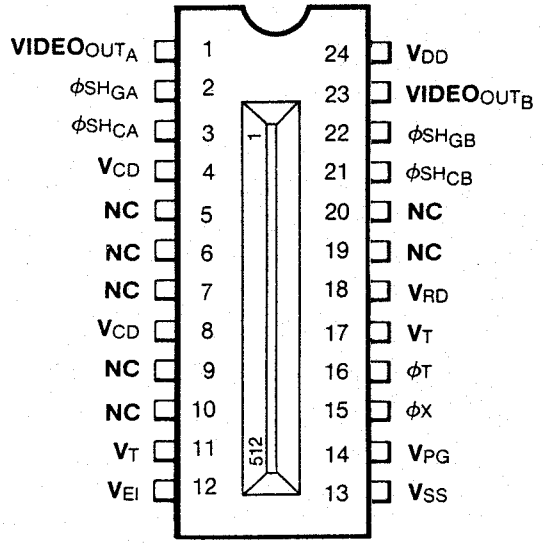

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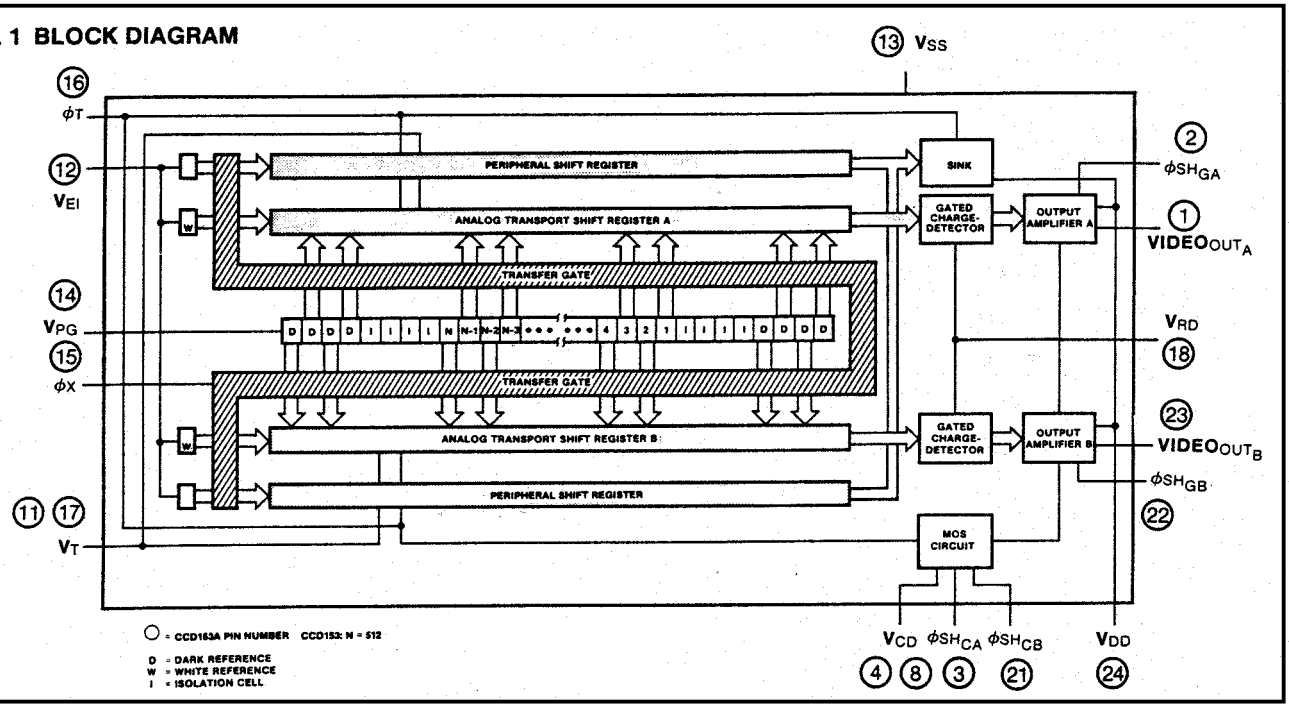
Fig. 1 BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The CCD153A consists of the following functional elements illustrated in the Block Diagram and Circuit Diagram (Fig1.).

Photosites: A row of 512 image sensor elements separated by a diffused channel stop and covered by a silicon dioxide surface passivation layer. Image photons pass through the transparent silicon creating hole-electron pairs. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated in each photosite is a linear function of the incident illumination intensity and the integration period. The output signal will vary in an analog manner from a thermally generated background level at zero illumination to a maximum at saturation under bright illumination.

Photogate: The photogate structure, located at the edge of the photosites, provides a bias voltage for the photosites.

Transfer Gate: The transfer gate structure separates the outer edge of the photogates from the analog shift registers. Charge-packets generated and accumulated in the photosites are transferred into the transport analog shift registers whenever the transfer gate voltage goes “High”. All odd-numbered charge packets are transferred into the “A” transport analog shift register: all even-numbered charge packets are transferred into the “B” transport analog shift register. The transfer gate also controls the input of charge from V_{EI} into the white reference cells (described below). The time inteval between successive transfer pulses determines the integration time.

Analog Shift Registers: Four 273-element analog shift registers transport charge towards the output end of the chip. the two inner registers, the transport registers, move the image generated charge packets serially to the two gated charge detectors and amplifiers. The two outer shift registers, the peripheral registers, accumulate charge generated at the chip periphery (by photons passing through unavoidable gaps in the light shield layer, etc.) and transport it to charge sinks. The primary shift register clock is ϕ_T. The complementary phase relationship of the secondary shift register clocks $\overline{\phi_T}$ and $\overline{\overline{\phi_T}}$, generated on-chip, provide alternate delivery of charge packets from “A” and “B” shift registers to their amplifiers so that the original serial sequential string of video information may be easily demutiplexed off-chip.

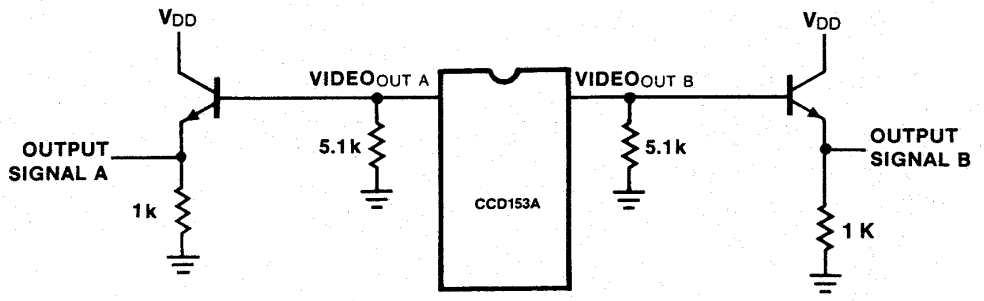
Gated Charge Detectors & Reset Gates: Each transport analog shift register delivers charge packets to a precharged diode. The change in diode potential is linearly proportional to the amount of charge delivered in the charge packet. This potential is applied to the input gate of a MOS transistor amplifier (see below), which linearly amplifies the input potential. The diode is reset to the reset drain bias voltage (V_{RD}) by the reset gate structure. Reset occurs when both the internal reset clocks ($\overline{\overline{\phi_T}}$ on the “A: side, $\overline{\phi_T}$ on the “B” side) are “High.” Each side is reset just before the next charge packet is delivered from its respective transport analog shift register.

Output Amplifiers and Sample-and Hold Gates: Each sides’ gated charge integrator drives the input of a two-stage linear MOS-transistor amplifier. A schematic diagram of this circuit is shown in Figure 9 below. The two stages of each amplifier are separated by sample-and-hold gates. The output of the first stage is connected to the input of the second stage whenever the sample-and-hold gates is “High”. The output of the second stage is connected to the $VIDEO_{OUT}$ pin. The sample-and-hold gates are switching MOS transistors: clocking these gates results in a sampled-and-held output, thus eliminating the reset clock feedthrough. When on-chip sample-and-hold is used, pin 2 is to be tied to pin 3 and pin 21 is to be tied to pin 22. Off-chip sample-and hold pulses can be supplied through pins 2 and 22. The sample-and-hold operation can be disabled by tying pins 2 and 22 to V_{DD}. Whenever on-chip sample-and hold is not used, pins 3 and 21 should be left unconnected.

Clock Driver Circuits: Two MOSFET clock-driver circuits on-chip allow sample-and-held operation of the CCD153A with only two externally-supplied clocks: the square-wave primary shift register transport clock ϕ_T, which determines the output data rate, and the transfer clock ϕ_X, which determines the integration time.

Dark and White Reference Cells and Circuitry — At each

Fig. 2 TEST LOAD CONFIGURATION



end of the 512-photosite array there are four additional sensing elements covered by opaque metallization. These "Dark Reference Cells" provide four charge packets (two on each side) at each end of the serial video output which indicate the typical dark (non-illuminated) signal level. In addition, two "white Reference Cells" (one per side) are input into the serial video outputs after the last pixel (#512) and the dark reference cells. (Refer to the section on the transfer gate, above) Each white reference cell generates an output signal pulse approximately 80% of the amplitude of a photosite saturation (maximum) signal. These cells may be used as inputs to external DC restoration and/or automatic gain control circuits. White reference amplitude is slightly dependent on exposure, especially at infrared wavelengths

DEFINITION OF TERM

Charge-Coupled Device — A Charge-coupled device is a semiconductor device in which finite isolated charge-packets are transported from one position in the semiconductor to an adjacent position by sequential clocking of an array of gates. The charge-packets are minority carriers with respect to the semiconductor substrate.

Transfer Clock ϕX **—** The transfer clock is the voltage waveform applied to the transfer gate to move the accumulated charge from the image sensor elements to the CCD transport shift registers.

Transport Clock ϕT **—** The transport clock is the clock applied to the gates of the CCD transport shift registers to move the charge-packets received from the image sensor elements to the gate charge-detector/amplifiers.

Sample-and-Hold Clock ($\phi SHCA$, $\phi SHCB$) **—** The voltage waveform applied to the sample-and-hold gates in the output amplifiers to create a continuous sampled video signal at the output. The sample-and-hold feature may be defeated by connecting $\phi SH(A+B)$ to V_{DD}.

Isolation Cell — A site on-chip producing an element in the video output that serves as a buffer between valid video data and dark reference signals. The output from an isolation cell contains no valid information and should be ignored.

Dynamic Range — The saturation exposure divided by the rms temporal noise equivalent exposure. Dynamic range is sometimes defined in terms of peak-to-peak noise. To compare the two definitions a factor of four to six is generally appropriate in that peak-to-peak noise is approximately equal to four to six times rms noise.

RMS Noise Equivalent Exposure — The exposure level that gives an output signal to the rms noise level at the output in the dark.

Saturation Exposure — The minimum exposure level that will provide a saturation output signal. Exposure is equal to the light intensity times the photosites integration time.

Charge Transfer Efficiency — Percentage of valid charge information that is transferred between each successive stage of the transport registers.

Responsivity — The output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure.

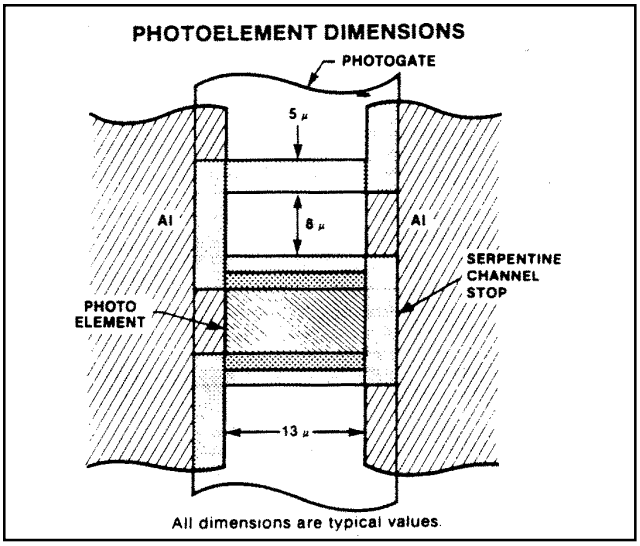
Total Photoresponse Non-uniformity — The difference of the response levels of the most and the least sensitive element under uniform illumination. Measurement of PRNU excludes first and last elements.

Dark Signal — The output signal in the dark caused by thermally generated electrons that is a linear function of the integration time and highly sensitive to temperature. (See accompanying photos for details of definition.)

Saturation Output Voltage — The maximum usable signal output voltage. Charge transfer efficiency decreases sharply when the saturation output voltage is exceeded.

Integration Time — The time interval between the falling edge of any two successive transfer pulses (ϕX). The integration is the time allowed for the photosites to collect charge.

Pixel - A picture element (photosite).



ABSOLUTE MAXIMUM RATINGS (Above which useful life may be impaired)

Storage Temperature	−25°C to +125°C
Operating Temperature (See Curves)	−25°C to +70°C
CCD153A Pins 2, 3, 4, 8, 11, 12, 14, 15, 16, 17, 18, 21, 22, 24	−0.3V to +18V
Pin 13	0V
Pins 5, 6, 7, 9, 10, 19, 20	NC
Pins 1, 23	See Caution Note

CAUTION NOTE: These devices have limited built-in gate protection. It is recommended that static discharge be controlled and minimized. Care must be taken to avoid shorting pins V_{OUT} A&B to V_{SS} or V_{DD} during operation of these devices. Shorting these pins temporarily to V_{SS} or V_{DD} may destroy the output amplifiers.

DC CHARACTERISTICS: T_P = 25° C (Notes 1, 2)

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
V_{CD}	Clock Driver Drain Supply Voltage	13.5	14	14.5	V	Note 3
I_{CD}	Clock Driver Drain Supply Current		7.0	15	mA	
V_{DD}	Output Amplifier Drain Supply Voltage	13.5	14	14.5	V	Note 3
I_{CD}	Output Amplifier Drain Supply Current		15	25	mA	
V_{PG}	Photogate Bias Voltage	8.5	9.0	9.5	V	
V_T	DC Electrode Bias Voltage	5.5	6.0	6.5	V	Note 4
V_{EI}	Electrical Input Bias Voltage		6.0		V	Note 5
V_{SS}	Substrate (Ground)		0.0		V	Note 6
V_{RD}	Reset Drain Supply	12	13	14.5	V	Note 18

CLOCK CHARACTERISTICS: T_P = 25° C (Note 1)

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
$V\phi XL$, $V\phi TL$	Transfer & Transport Clock LOW	0.0	0.3	0.5	V	Notes 6, 7
$V\phi XH$, $V\phi 1_r$,	Transfer & Transport Clock HIGH	11	11.5	12	V	Note 7
$f_{DATA\ MAX}$	Maximum Output Data Rate	12	20		MHz	Notes 8, 9

NOTES:
1. T_P is defined as the package temperature, measured on a copper block in good thermal contact with the entire backside of the package.
2. ALL V_{SS} pins must be grounded. All NC pins must be left unconnected.
3. V_{DD} pins may be connected to V_{CD} and/or V_{RD} pins.
4. $V_T = 0.55\ \phi X_{HIGH} = 0.55\ \phi T_{HIGH}$
5. V_{EI} is used to generate the white reference output. These two signals can be eliminated by connecting V_{EI} to V_{DD}.
6. Negative transients on any clock pin going below 0.0 volts may cause charge injection, which results in an increase in apparent DS.
7. C ϕT = 180 pF; C ϕX = 50 pF.
   All clock rise and fall times should be > 30ns.
8. The minimum clock frequency is limited by increases in dark signal.
9. $f_{DATA} = 2\ (f\ \phi T)$
10. OCLI WBHM = Optical Coating Laboratory, Inc. Wide Bant Hot Mirror.
11. CTE is the measurement for a one-stage transfer.
12. See photographs for PRNU definitions.
13. Video mismatch is the difference in ac amplitudes between $V_{OUT\ A}$ and $V_{OUT\ B}$ under uniform illumination. It can be eliminated by attenuation/amplification of one of the video outputs.
14. DC mismatch is the difference in dc output level V_O between $V_{OUT\ A}$ and $V_{OUT\ B}$.
15. See photographs for dark signal definitions.
16. Dark signal component approximately doubles for every 5-10 °C in T_P.
17. Each SPDSNU is measured from the DS level adjacent to the base of the SPDSNU. The SPDSNU approximately doubles for every 5-15 °C in T_P.
18. V_{RD} voltages in the lower range improves amplifier linearity.

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AC CHARACTERISTICS: (Note 1)
T_P = 25° C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms, Light Source* = 2854° K + 2.0 mm thick
Schott BG-38 and OCLI WBHM filters
All operating voltages nominal specified values

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
DR	Dynamic Range (relative to peak-to-peak noise) (relative to rms noise)		1500:1 7500:1			
NEE	RMS Noise Equivalent Exposure		0.00009		$\mu j/cm^2$	
SE	Saturation Exposure		0.67		$\mu j/cm^2$	
CTE	Charge Transfer Efficiency	0.99995	0.99999			Note 11
V_O	Output DC Level	4.0	8.0	11.0	V	
Z	Output Impedance		0.75	1.5	kΩ	
P	On-Chip Power Dissipation Clock Drivers Amplifiers		 100 170	 215 325	 mW mW	
N	Peak-to-Peak Temporal Noise		1.0		mV	

PERFORMANCE CHARACTERISTICS: (Note 1)
T_P = 25° C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms, Light Source* = 2854° K + 2.0 mm thick
Schott BG-38 and OCLI WBHM filters
All operating voltages nominal specified values

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
PRNU**	Photoresponse Non-Uniformity:					Note 12
	Peak-to-Peak		60	160	mV	
	Peak-to-Peak Without Single-Pixel Positive & Negative Pulses		40		mV	
	Single-Pixel Positive Pulses		10		mV	
	Single-Pixel Negative Pulses		20		mV	
M_{VIDEO}	Video Mismatch		10	100	mV	Note 13
M_{DC}	DC Mismatch		0.5	2.0	V	Note 14
DS	Dark Signal:					Note 15, 16
	DC Component		1.0	2.0	mV	
	Low Frequency Component		1.0	2.0	mV	
SPDSNU	Single-Pixel DS Non-Uniformity		1.0	2.0	mV	Note 17
R	Responsivity	1.8	3.0	5.5	Volts per $\mu j/cm^2$	
V_{SAT}	Saturation Output Voltage	1.0	1.5	2.5	V	

* OCLI WBHM = Optical Coating Laboratory, Inc. Wide Band Hot Mirror

** PRNU measurements include both register outputs but exclude the outputs from the first and last elements of the array. Also excluded from the measurement are video and dc mismatch.
All PRNU measurements are taken at a 800 mV output level using an f/5.0 lens.
The "f" number is defined as the distance from the lens to the array divided by the diameter of the lens aperture. As the "f" number increases, the resulting more highly collimated light causes the package window imperfections to dominate and increase PRNU. A lower "f" number results in less collimated light causing device photosite blemishes to dominate the PRNU.

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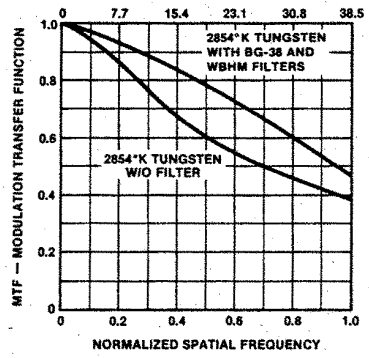
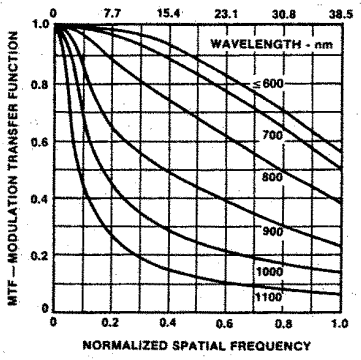
Fig. 3 TEST LOAD CONFIGURATION **TYPICAL PERFORMANCE CURVES**

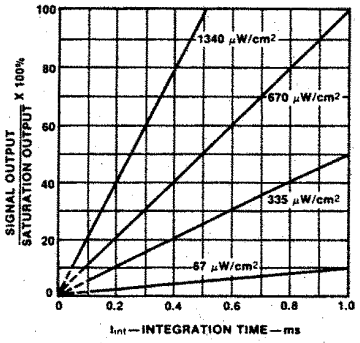
MODULATION TRANSFER FUNCTIONS FOR TWO BROADBAND ILLUMINATION SOURCES



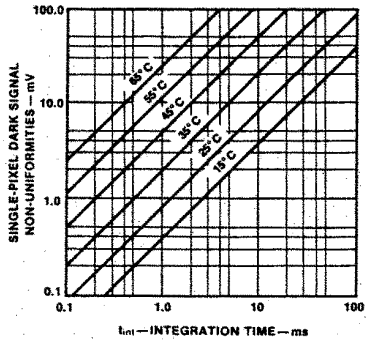
MODULATION TRANSFER FUNCTIONS FOR NARROW BAND ILLUMINATION SOURCES



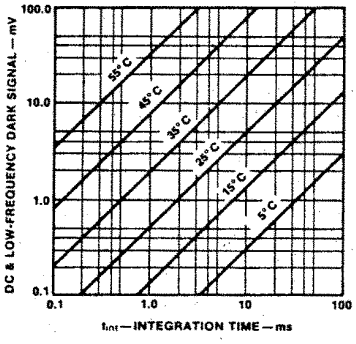
OUTPUT SIGNAL LEVEL VERSUS INTEGRATION TIME 2854°K TUNGSTEN SOURCE WITH BG-38 AND WBHM FILTERS



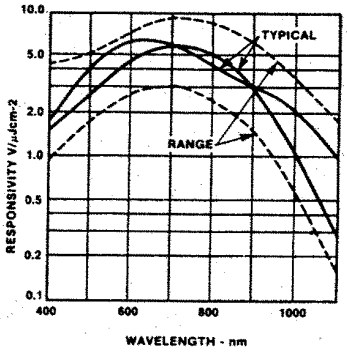
SINGLE-PIXEL DARK SIGNAL NON-UNIFORMITIES VERSUS INTEGRATION TIME



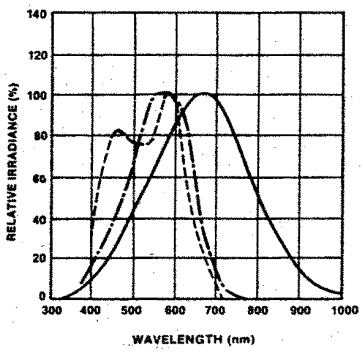
DC AND LOW-FREQUENCY DARK SIGNAL VS INTEGRATION TIME



TYPICAL SPECTRAL RESPONSE

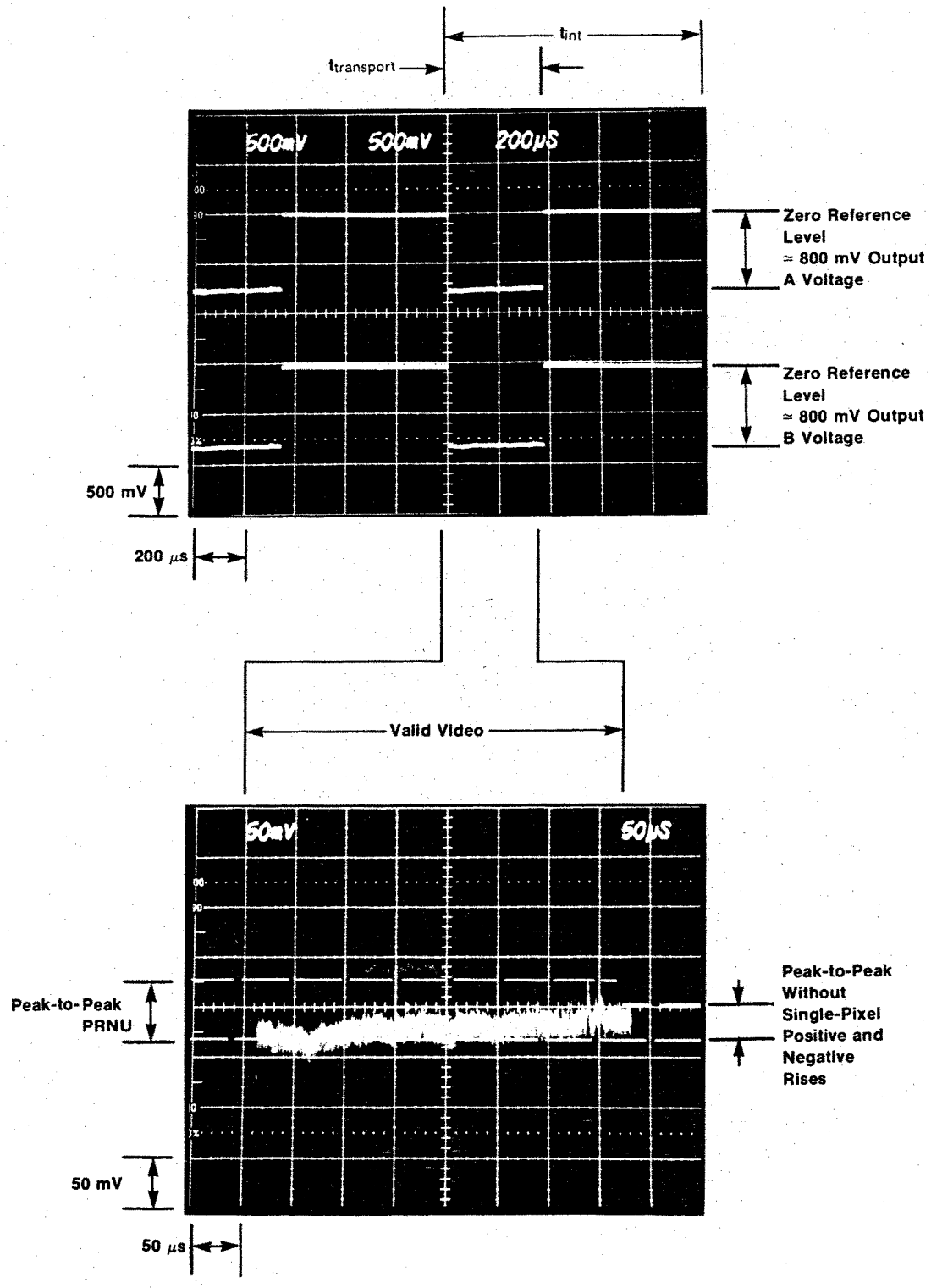


***RELATIVE RADIANT FLUX VS WAVELENGTH**



TYPICAL "DAYLIGHT FLUORESCENT" BULB
2854°K LIGHT SOURCE +WBHM + 2.0 mm THICK BG-38
2854°K LIGHT SOURCE + 3.0 mm THICK 1-75

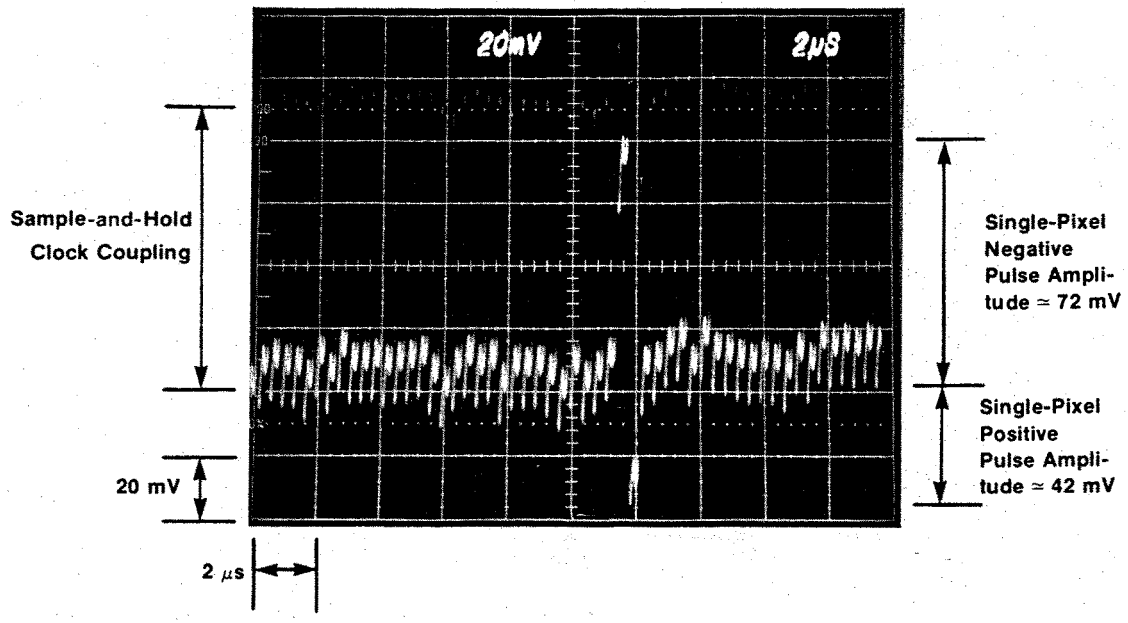
Fig. 4 PHOTORESPONSE NON-UNIFORMITY PARAMETERS (PRNU)



TEST CONDITIONS

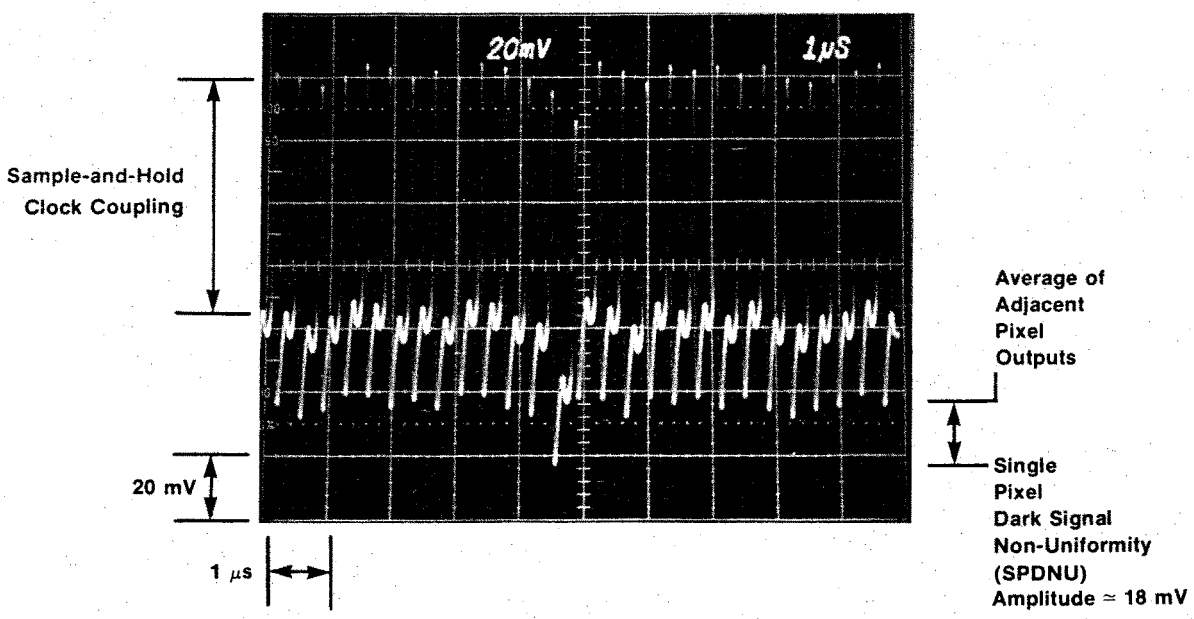
T_P = +25°C, f_{DATA} = 1.25 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Light source = 2854°K tungsten + 2.0 mm thick Schott BG-38 and OCLI WBHM filters. PRNU measurements taken at an output voltage of ≃ 800 mV. Output fed through 5 MHz low pass filter.

Fig. 5 PHOTORESPONSE NON-UNIFORMITY PARAMETERS (PRNU)



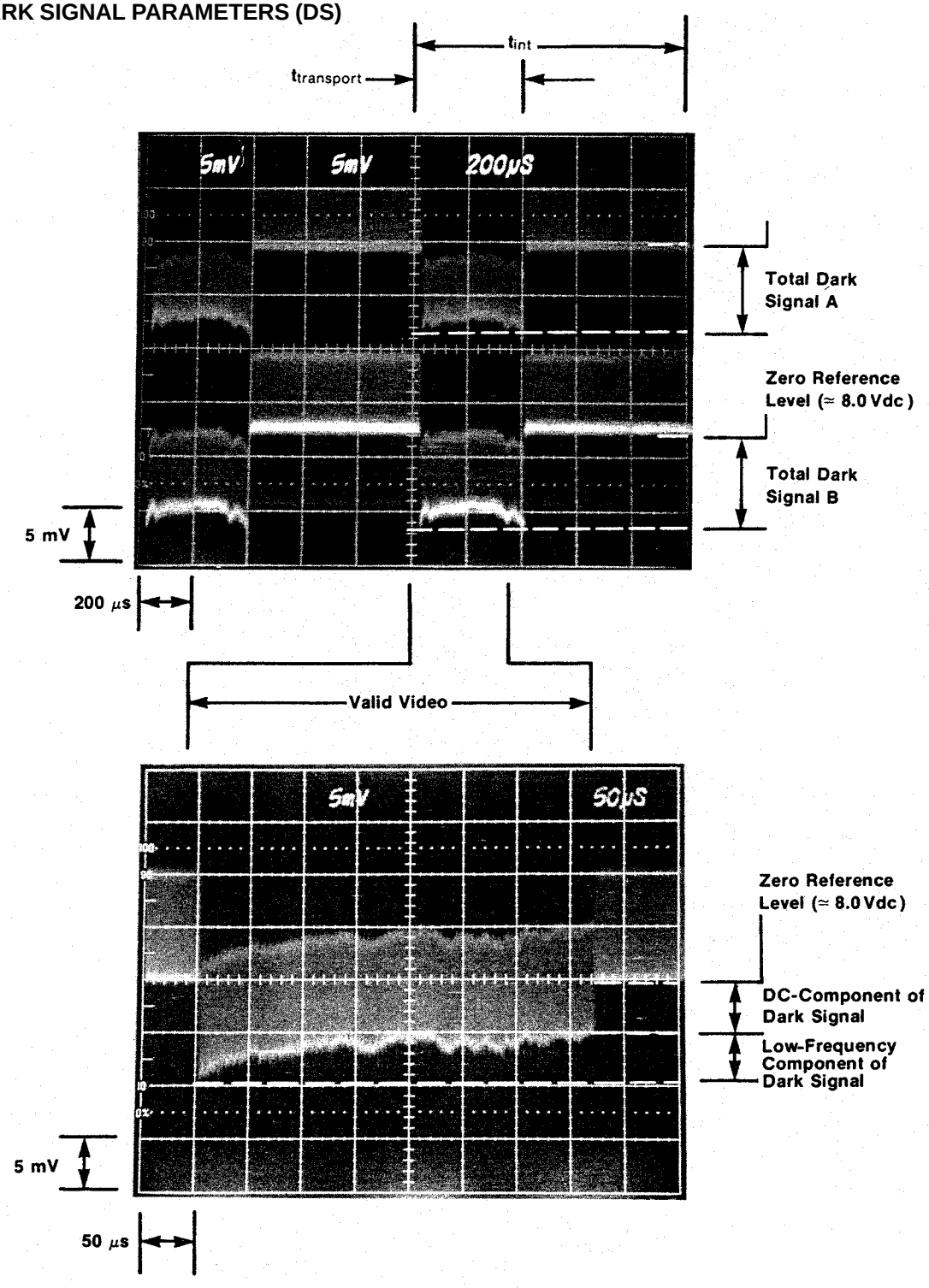
TEST CONDITIONS
T_P = +25°C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Light source = 2854°K tungsten +2.0 mm thick Schott BG-38 and OCLI WBHM filters. PRNU measurements taken at an output voltage of ≃ 800 mV. Output fed through 5 MHz low pass filter.

Fig. 6 DARK SIGNAL PARAMETERS (DS)



TEST CONDITIONS
T_P = +25°C, f_{DATA} = 5 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Output fed through 5 MHz low pass filter.

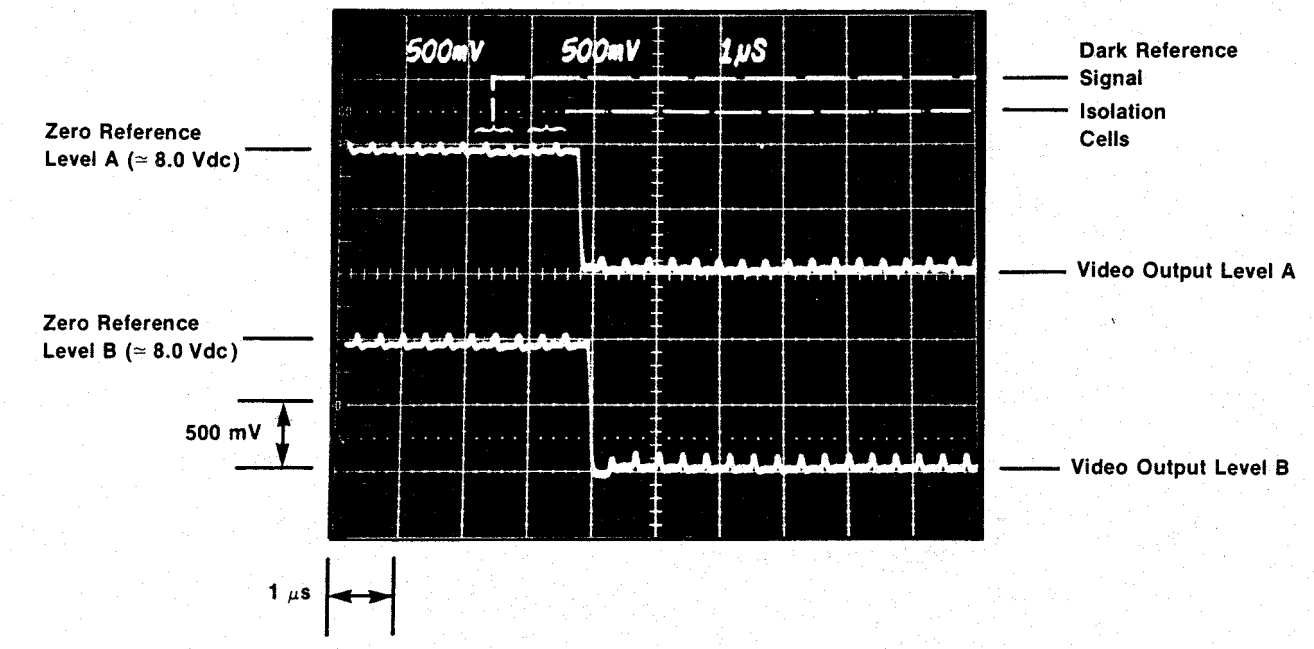
Fig. 6 DARK SIGNAL PARAMETERS (DS)



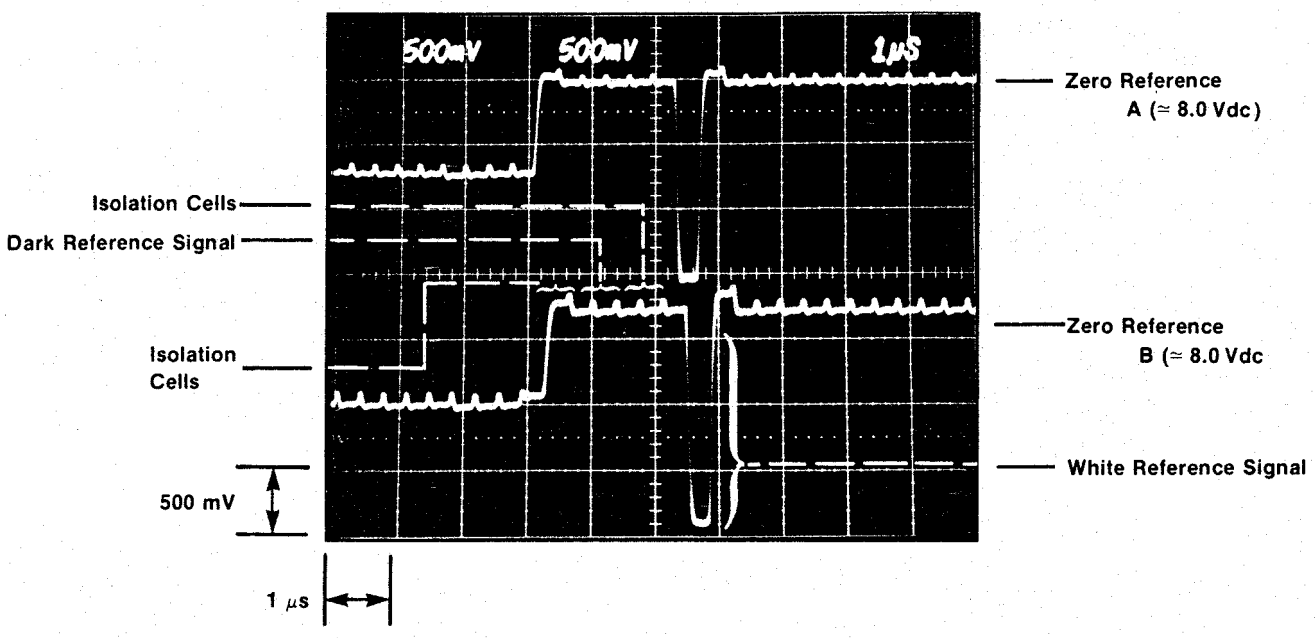
TEST CONDITIONS

T_P = +25°C, f_{DATA} =1.25 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Output fed through 5 MHz low pass filter.

Fig. 7 VIDEO OUTPUT TIMING PHOTOGRAPHS



Start of One Scan Video Output

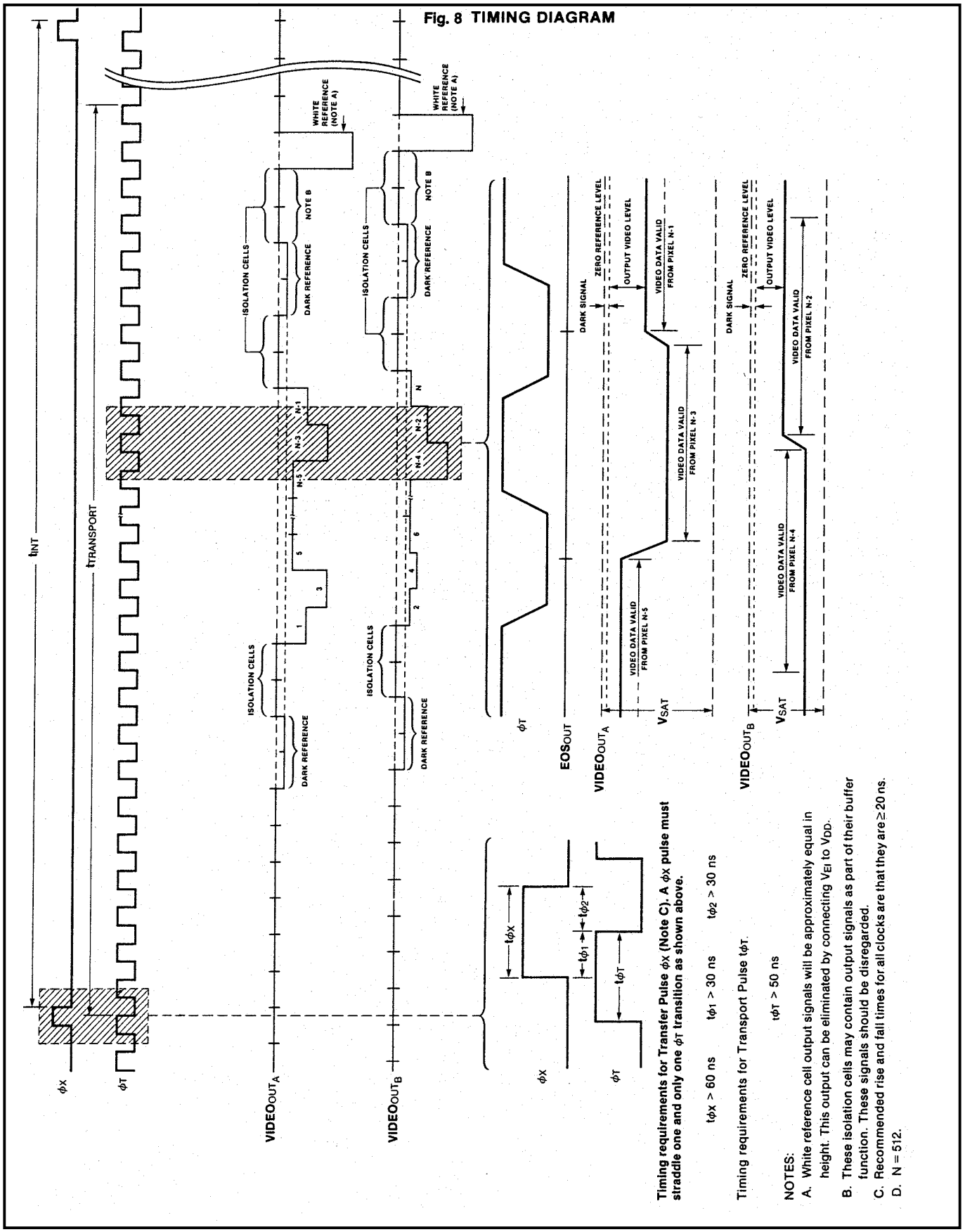


End of One Scan Video Output

TEST CONDITIONS

T_P = +25°C, f_{DATA} = 5 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Light source = 2854°K tungsten with 2.0 mm thick Schott BG-38 and OCLI WBHM filters. Output fed through 5 MHz low pass filter.

Fig. 8 TIMING DIAGRAM



Timing requirements for Transfer Pulse ϕX (Note C). A ϕX pulse must straddle one and only one ϕT transition as shown above.

$t\phi X > 60$ ns $t\phi 1 > 30$ ns $t\phi 2 > 30$ ns

Timing requirements for Transport Pulse tϕT.

$t\phi T > 50$ ns

NOTES:

A. White reference cell output signals will be approximately equal in height. This output can be eliminated by connecting V_{EI} to V_{DD}.

B. These isolation cells may contain output signals as part of their buffer function. These signals should be disregarded.

C. Recommended rise and fall times for all clocks are that they are ≥ 20 ns.

D. N = 512.

DEVICE CARE AND OPERATION

Glass may be cleaned by saturating a cotton swab in alcohol and lightly wiping the surface. Rinse off the alcohol with deionized water. Allow the glass to dry, preferably by blowing with filtered dry N_2 or air.

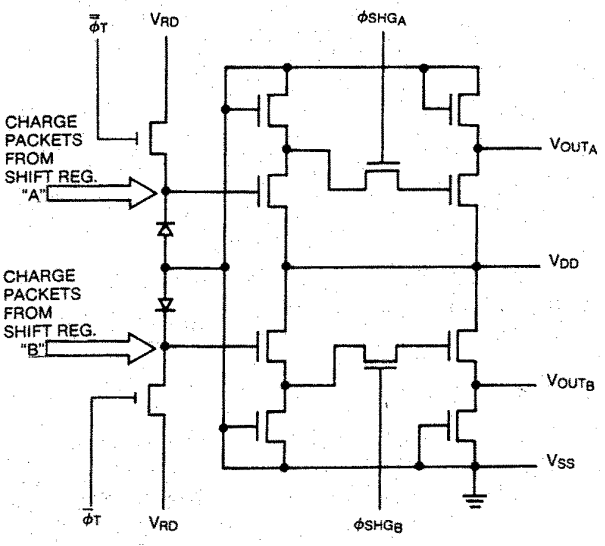
It is important to note in design and applications considerations that the devices are very sensitive to thermal conditions. The dark signal dc and low frequency components approximately double for every 5º C temperature increase and single-pixel dark signal non-uniformities approximately double for every 8º C temperature increase. The devices may be cooled to achieve very long integration times and very low light level capability.

ORDER INFORMATION

Order CCD153ADC where “D” stands for a ceramic package and “C” for commercial temperature range.

Also available are printed circuit boards that include all the necessary clocks, logic drivers and video amplifiers to operate the CCD153A. The boards are fully assembled and tested and require only one power supply for operation (+20V). The printed circuit board order codes are CCD153DB. The CCD153A,143A and 133A can be operated in the same printed circuit board. The 24 pin CCD133A and 153A devices are to be placed at the center of the 28 pin socket on the printed circuit board.

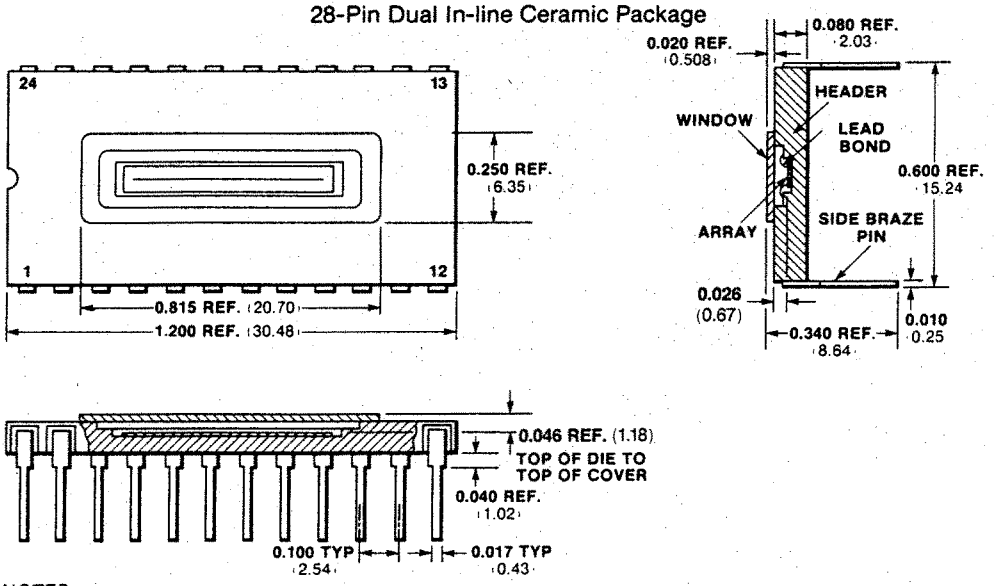
Fig. 9 OUTPUT AMPLIFIER SCHEMATIC



NOTE: $\overline{\phi T}$ AND $\overline{\overline{\phi T}}$ ARE INTERNALLY GENERATED RESET CLOCKS.

PACKAGE OUTLINE

28-Pin Dual In-line Ceramic Package



NOTES:
All dimensions in inches (**bold**) and millimeters (parentheses). Header is black ceramic (Al_2O_3). Window is glass. The amplifier of the device is located near the notched end of the package.

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