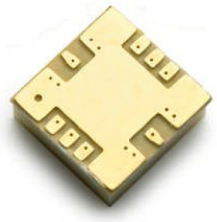
AMMP-5618
6–20 GHz General Purpose Amplifier

Data Sheet



Description

Avago's AMMP-5618 is a high power, medium gain amplifier that operates from 6 GHz to 20 GHz. The amplifier is designed to be an easy-to-use component for any surface mount PCB application. In communication systems, it can be used as a LO buffer, or as a transmit driver amplifier. During typical operation with a single 5V supply, each gain stage is biased for Class-A operation for optimal power output with minimal distortion. The amplifier has integrated 50Ω I/O match, DC blocking, self-bias and choke to eliminate complex tuning and assembly processes typically required by hybrid (discrete-FET) amplifiers. The package is fully SMT compatible with backside grounding and I/O to simplify assembly.

Note: These devices are ESD sensitive. The following precautions are strongly recommended. Ensure that an ESD approved carrier is used when dice are transported from one destination to another. Personal grounding is to be worn at all times when handling these devices.

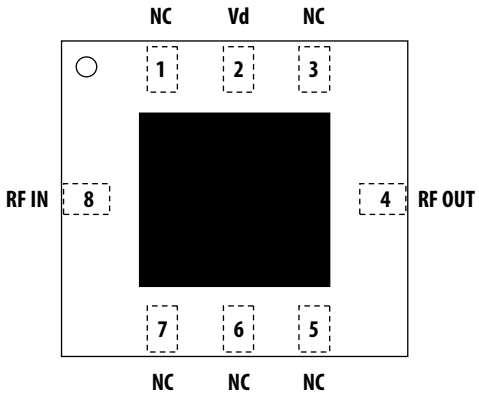
Features

- 5 x 5 mm surface mount package
- Broad band performance 6–20 GHz
- High +19 dBm output power
- Medium 13 dB typical gain
- 50Ω input and output match
- Single 5V (107 mA) supply bias

Applications

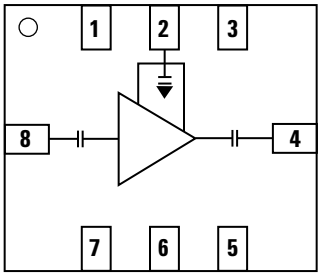
- Microwave radio systems
- Satellite VSAT
- Commercial grade military

Package Diagram



Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model (Class A) = 50V
ESD Human Body Model (Class 0) = 150V
Refer to Avago Application Note A004R: Electrostatic Discharge Damage and Control.

Functional Block Diagram



Pin	Function
1	NC
2	Vd
3	NC
4	RF_out
5	NC
6	NC
7	NC
8	RF_in

Electrical Specifications

1. Small/Large -signal data measured in a fully de-embedded test fixture form TA = 25°C, Vd=5V, Idq=107mA.
2. Pre-assembly into package performance verified 100% on-wafer per AMMC-5618 published specifications
3. This final package part performance is verified by a functional test correlated to actual performance at one or more frequencies
4. Specifications are derived from measurements in a 50Ω test environment. Aspects of the amplifier performance may be improved over a more narrow bandwidth by application of additional conjugate, linearity, or low noise (Γopt) matching.

Table 1. RF Electrical Characteristics (T_A= 25°C, V_d= 5.0V, I_{dq}=107 mA, Zo=50 Ω)

Parameter	Typ.	Sigma	Unit	Frequency
Small-signal Gain, Gain	12 13	0.40	dB	5-6 GHz
Noise Figure into 50 Ω, NF	4.4	0.2	dB	
Output Power at 1dB Gain Compression, P1dB	19	0.9	dBm	
Third Order Intercept Point; Δf=100MHz; Pin=-20dBm, OIP3	25 30	1.2	dBm	5-6 GHz
Input Return Loss, RLin	-12	0.7	dB	
Output Return Loss, Rlout	-12	0.6	dB	
Reverse Isolation, Isolation	-40	1.2	dB	

Table 2. Recommended Operating Range

1. Ambient operational temperature T_A = 25°C unless otherwise noted.
2. Channel-to-backside Thermal Resistance (Tchannel (Tc) = 34°C) as measured using infrared microscopy. Thermal Resistance at backside temperature (Tb)= 25°C calculated from measured data.

	Specifications				
Description	Min.	Typical	Max.	Unit	Comments
Drain Supply Current, Id		107	140	mA	(Vd = 5 V, Under any RF power drive and temperature

Table 3. Thermal Properties

Parameter	Test Conditions	Value
Thermal Resistance, θ_{ch-b}	Backside Temperature, T_A =25°C	θ_{ch-b} = 34 °C/W

Absolute Minimum and Maximum Ratings

Table 4. Minimum and Maximum Ratings

	Specifications			
Description	Min.	Max.	Unit	Comments
Positive Drain Voltage, Vd		7	V	
Drain Current, Id		150	mA	
RF Input Power (Pin), RFin		20	dBm	CW
Channel Temperature, Tch		+150	°C	
Storage Temperature, Tstg	-65	+150	°C	
Max. Assembly Temp, Tmax	+300		°C	30 second maximum

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to this device.

Selected performance plots

These measurements are in 50Ω test environment at TA = 25°C, Vd = 5V, Id = 107 mA. Aspects of the amplifier performance may be improved over a narrower bandwidth by application of additional conjugate, linearity or low noise (Γopt) matching.

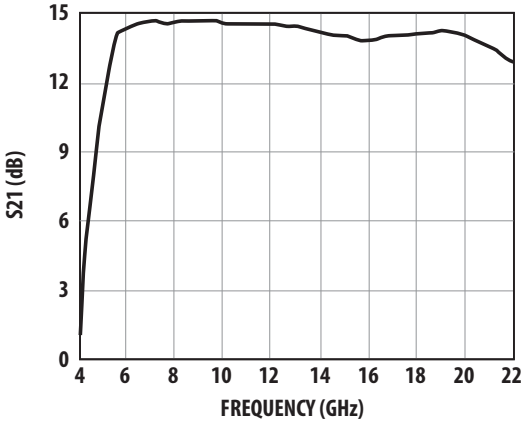


Figure 1. Gain.

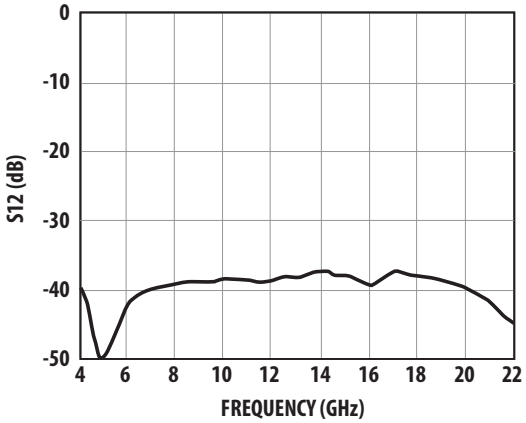


Figure 2. Isolation.

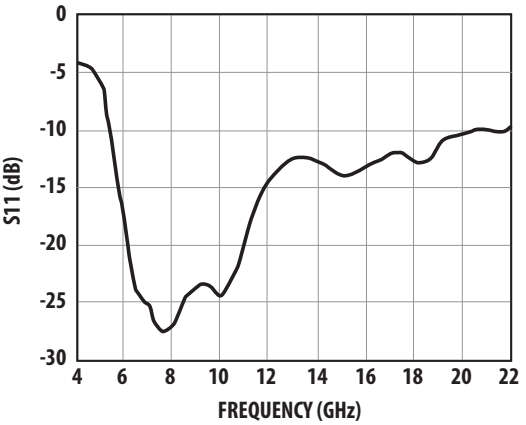


Figure 3. Input Return Loss.

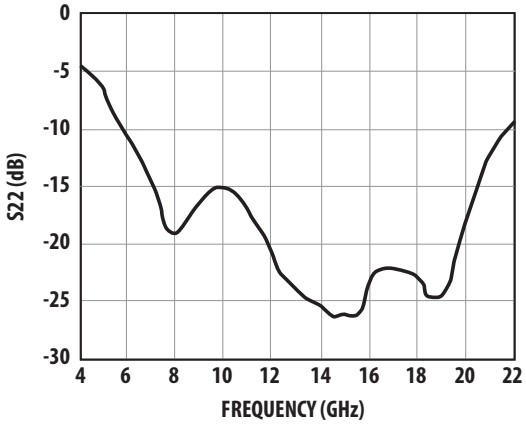


Figure 4. Output Return Loss.

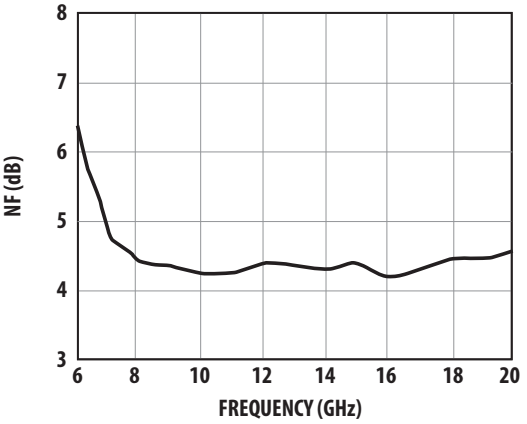


Figure 5. Noise Figure.

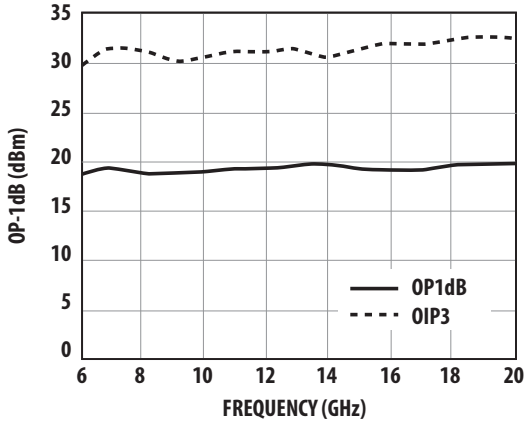


Figure 6. Typical Power, OP-1dB and OIP3.

Over Temperature Performance Plots

These measurements are in 50Ω test environment at TA = 25°C, Vd = 5V, Id = 107 mA. Aspects of the amplifier performance may be improved over a narrower bandwidth by application of additional conjugate, linearity or low noise (Γopt) matching.

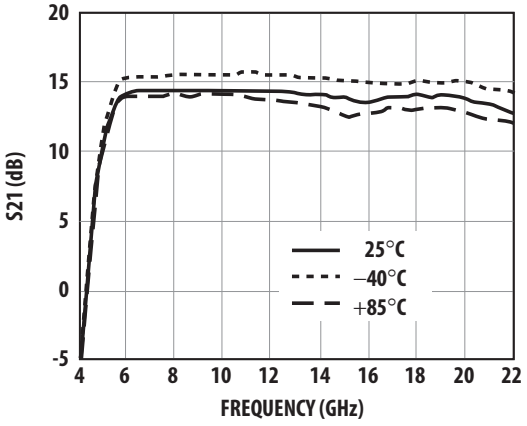


Figure 7. Gain Over Temperature.

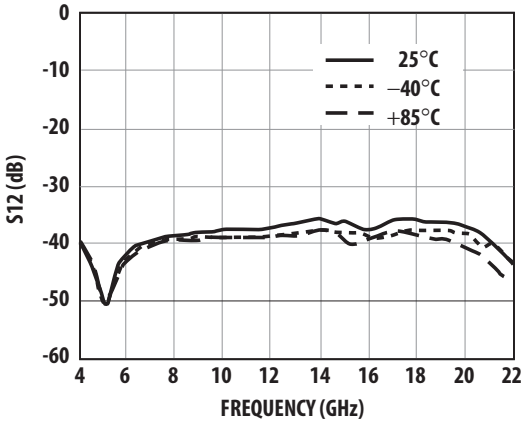


Figure 8. Isolation Over Temperature.

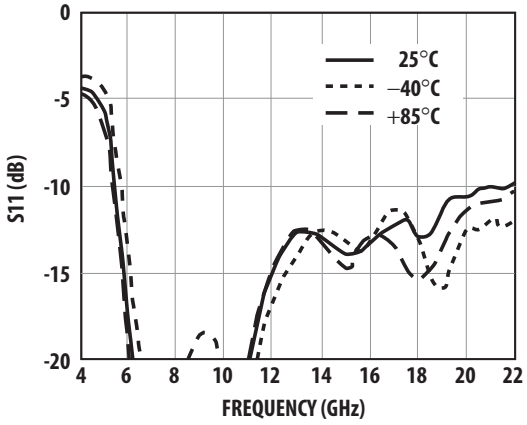


Figure 9. Input RL Over Temperature.

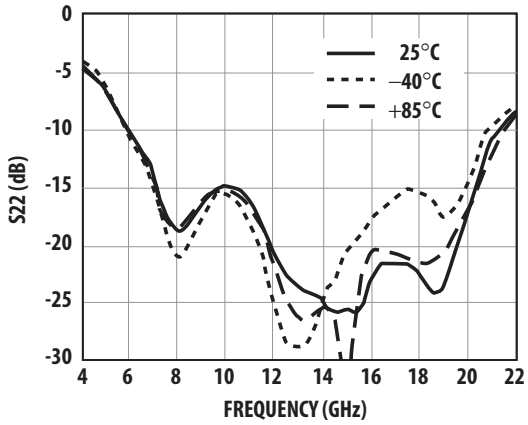


Figure 10. Output Return Loss Over Temperature.

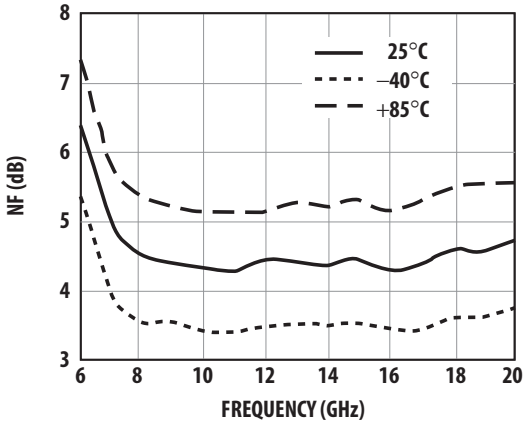


Figure 11. NF Over Temperature.

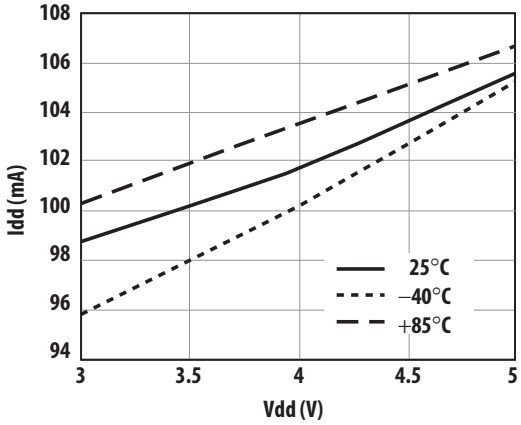


Figure 12. Bias Current Over Temperature.

Over Voltage plots

These measurements are in 50Ω test environment at TA = 25°C, Vd = 5V, Id = 107 mA. Aspects of the amplifier performance may be improved over a narrower bandwidth by application of additional conjugate, linearity or low noise (Γopt) matching.

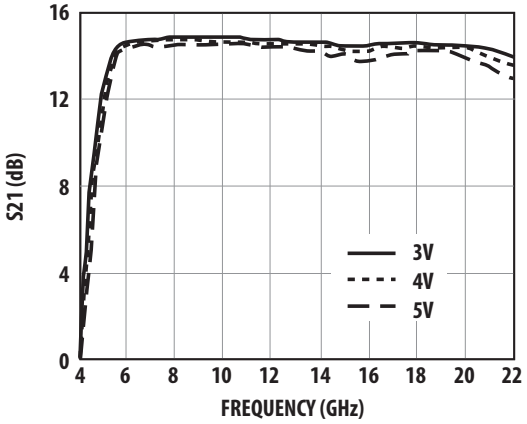


Figure 13. Gain Over Vdd.

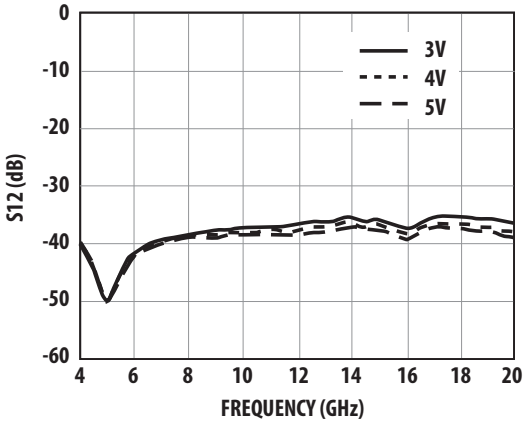


Figure 14. Isolation Over Vdd.

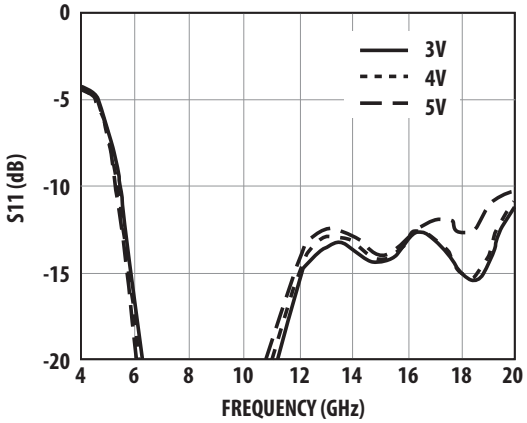


Figure 15. Input RL Over Vdd.

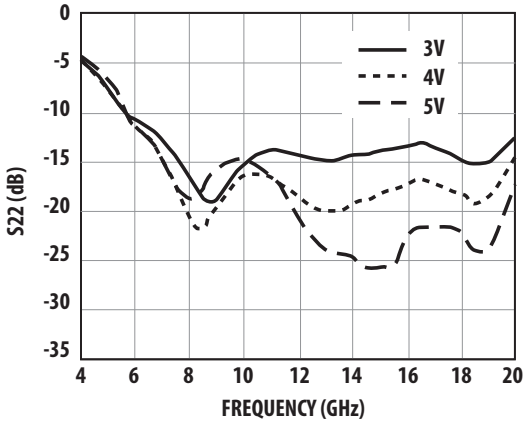


Figure 16. Output Return Loss Over Vdd.

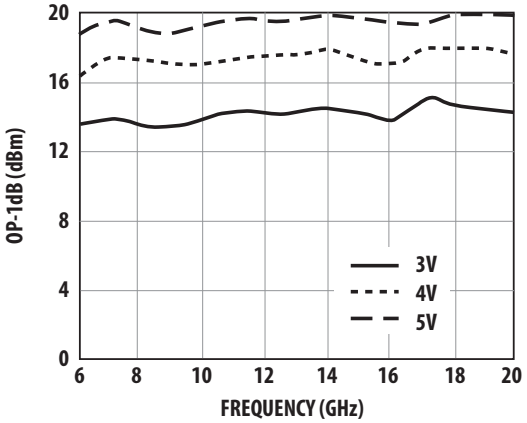


Figure 17. Output Power Over Vdd.

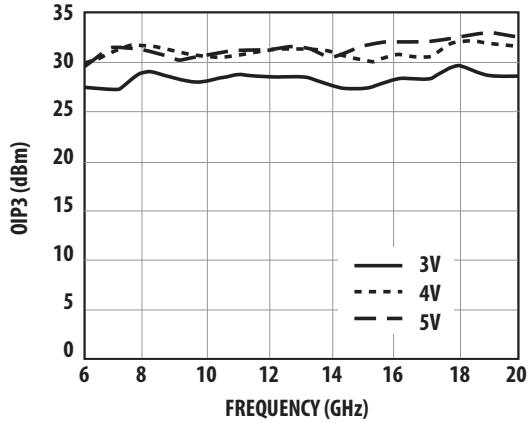


Figure 18. OIP3 Over Vdd.

Typical Scattering Parameters

Please refer to <http://www.avagotech.com> for typical scattering parameters data.

Biasing and Operation

The AMMC-5618 is normally biased with a single positive drain supply connected to both V_D pins through bypass capacitors as shown in Figure 19. The recommended supply voltage is 5V. It is important to have 0.1 µF bypass capacitor, and the capacitor should be placed as close to the component as possible.

The AMMC-5618 does not require a negative gate voltage to bias any of the two stages. No ground wires are needed because all ground connections are made with plated through-holes to the backside of the package.

Refer to the Absolute Maximum Ratings table for allowed DC and thermal conditions.

Application Circuit

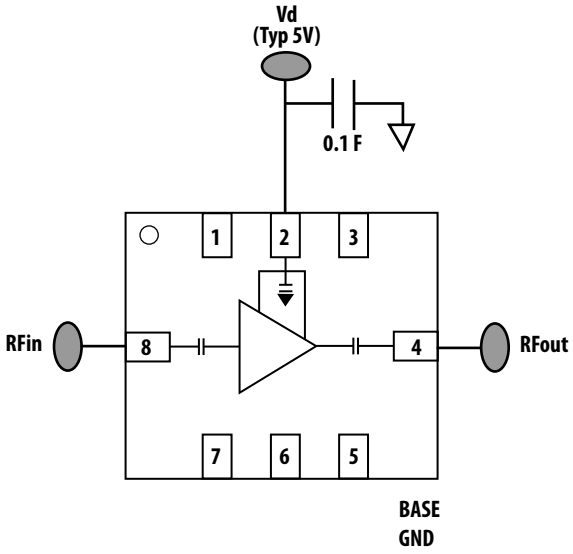


Figure 19. Typical Application.

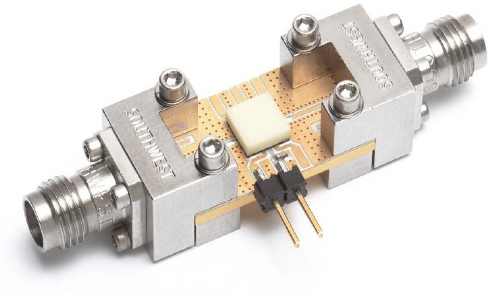


Figure 21. Demonstration Board (available upon request).

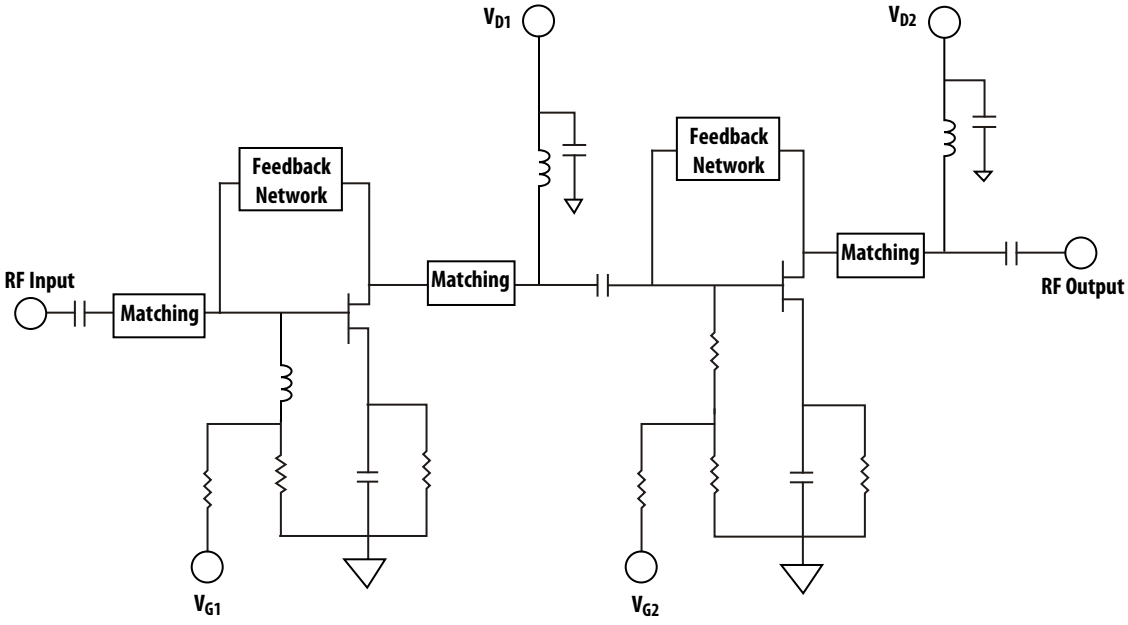


Figure 20. Simplified MMIC Schematic.

Package Dimension, PCB Layout and Tape and Reel information

Please refer to Avago Technologies Application Note 5520, AMxP-xxxx production Assembly Process (Land Pattern A).

Part Number Ordering Information

Part Number	Devices per Container	Container
AMMP-5618-BLK	10	antistatic bag
AMMP-5618-TR1	100	7″ Reel
AMMP-5618-TR2	500	7″ Reel

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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