

Distinctive Features

- Provides random logic and high current drive for VMEbus interrupt generator in 300 mil 24 pin DIP or 28 pin LCC package
- IRQ* can be connected to any single interrupt request level
- Includes interrupter arbitration logic
- Drives 48mA IRQ* signal
- Input hysteresis filters bus noise
- VME 3000 provides Release on Acknowledge operation
- VME 3010 provides Release on Register Access or Release on Acknowledge operation
- Available in Commercial, Industrial and Military temperature ranges

Programmable Version Available

If the VME 3000/3010 does not match the requirements of the design, a programmable version is available (the PLX 448) which allows the user to customize all inputs, outputs and logic. Programming is performed using industry standard tools such as ABEL™ or CUPL™ software and commonly available PLD programming hardware. Contact PLX for a data sheet on the PLX 448 and other information.

Applications

- Single level interrupt generator logic for VMEbus slave modules generating an 8 bit interrupt vector

T-52-33-13

General Description

The VME 3000/3010 is a CMOS single level interrupt generator for the VMEbus which is packaged in a compact 24 pin 300 mil wide DIP or 28 pin LCC. The protocols of the VME 3000 meet the VMEbus IEEE 1014 timing requirements. The device buffers and drives the VMEbus signals to the IEEE 1014 electrical specifications.

The VME 3000/3010 will respond to an interrupt cycle when it receives IACKIN* from the daisy chain. It arbitrates between IACKIN* and the interrupt request signal, compares priority levels and generates an interrupt acknowledge or IACKOUT* depending on which is appropriate.

The VME 3000 provides the Release on Acknowledge interrupter operation, while the VME 3010 provide both Release on Acknowledge and Release on Register Access.

This part will function with any interrupt handler and master module which meets the IEEE 1014 VMEbus specification.

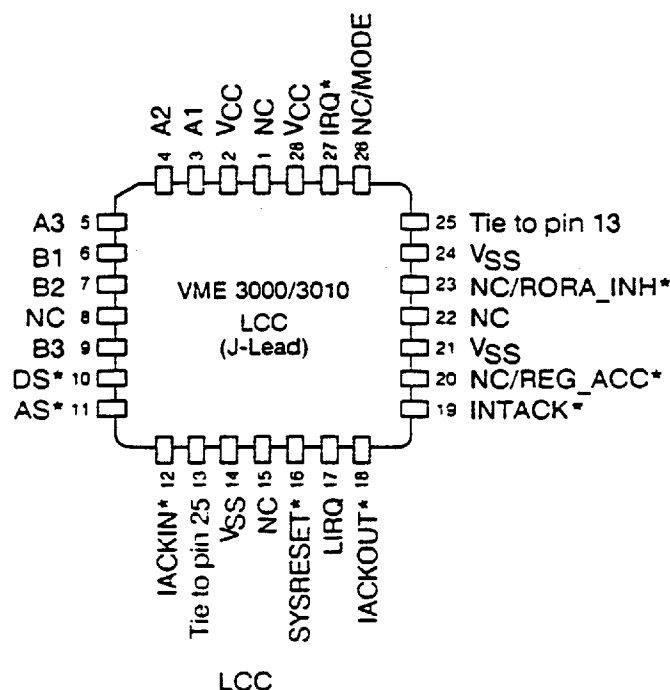
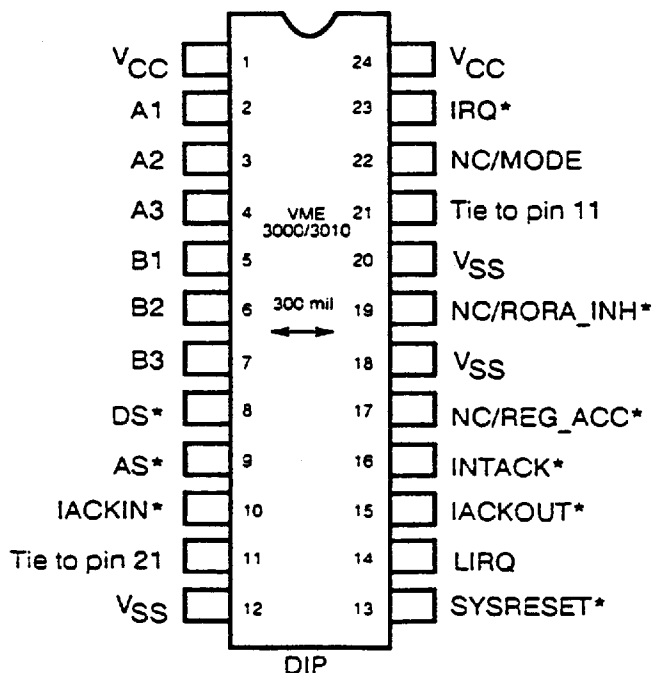


Figure 1. Pinout of VME 3000/3010

ABEL is a trademark of Data I/O Corp
CUPL is a trademark of Logical Devices, Inc
Patent Pending

T-52-33-13

28 Pin LCC	24 Pin DIP	Signal	Type	Function
2	1	V _{CC}	—	5V Power Supply.
3	2	A ₁	I	Active high. Address bit 1; VME address bit.
4	3	A ₂	I	Active high. Address bit 2; VME address bit.
5	4	A ₃	I	Active high. Address bit 3; VME address bit.
6	5	B ₁	I	Active high. Encode level bit 1; Encode bit for IRQ* priority level.
7	6	B ₂	I	Active high. Encode level bit 2; Encode bit for IRQ* priority level.
9	7	B ₃	I	Active high. Encode level bit 3; Encode bit for IRQ* priority level.
10	8	DS*	I	Active low. Data Strobe; DS0* for interrupt vector size.
11	9	AS*	I	Active low. VMEbus Address Strobe; Indicates valid address.
12	10	IACKIN*	I	Active low. Interrupt Acknowledge In; VMEbus IACK* daisy chain input.
13	11		I	Tie to pin 21 (DIP) or 25 (LCC).
14	12	V _{SS}	—	Chip Ground.
16	13	SYSRESET*	I	Active low. System Reset; VMEbus System Reset.
17	14	LIRQ	I	Active high. Local Interrupt Request; Interrupt Request from local slave.
18	15	IACKOUT*	O	Active low. Interrupt Acknowledge Out; IACK* daisy chain output if interrupt cycle does not belong to local slave.
19	16	INTACK*	O	Active low. Interrupt Acknowledge; VME 3000 generates INTACK* if interrupt cycle belongs to local slave.
20	17	NC/REG_ACC*	I	No connect on VME 3000. Register accessed input on VME 3010. Input used only in RORA mode. Indicates when the STATUS/ID register on the slave has been read to complete the RORA interrupt handling process. Assertion of this input causes IRQ* to be negated. Tie to GND if using VME 3010 in ROAK mode.
21	18	V _{SS}	—	Chip Ground.
23	19	NC/RORA_INH*	I	No connect on VME 3000. LIRQ inhibit input to VME 3010. Input used only in RORA mode. Indicates when the 2 msec window after the STATUS/ID register has been read is up. This window causes LIRQ from the slave to be ignored. When this input is negated, LIRQ will be sampled again by the VME 3010. Tie to GND if using the VME 3010 in ROAK mode.
24	20	V _{SS}	—	Chip Ground.
25	21		O	Tie to pin 11 (DIP) or pin 13 (LCC).
26	22	NC/MODE	I	No connect on VME 3000. Mode input to VME 3010. Indicates VME 3010 mode of operation: tie to GND to operate VME 3010 in ROAK mode; tie to V _{CC} to operate VME 3010 in RORA mode.
27	23	IRQ*	O	Active low. Interrupt Request; Interrupt request can be connected to any priority level. 48 mA OC.
28	24	V _{CC}	—	5V Power Supply.
1 8 15.22	—	NC	—	No Connect

Note OC is Open Collector

Detailed Description

The VME 3000/3010 generates an interrupt request, IRQ^* , and will respond to an interrupt cycle when it receives $IACKIN^*$. The VME 3000/3010 will then assert $IACKOUT^*$ or $INTACK^*$ depending on whether or not it was selected to participate in the interrupt cycle.

Figure 2 contains a block diagram of a typical interrupt generator configuration. Figure 3 shows the critical timing relationships.

The local slave generates an interrupt request by asserting $LIRQ$ high. The VME 3000/3010, in turn, drives IRQ^* low, which indicates to the VME system interrupt handler that an interrupt request is pending. The IRQ^* output of the VME 3000/3010 should be hardwired or connected through jumpers to the desired VMEbus interrupt request level IRQ_n^* ($n = 1$ to 7). If multiple interrupt request levels or dynamic selection of the interrupt request levels is required, contact PLX for information on how to meet these requirements.

After receiving one or more interrupt requests, the system interrupt handler will drive $IACKIN^*$ down the $IACK$ daisy chain, which indicates the beginning of a VMEbus interrupt cycle. When the VME 3000/3010 receives $IACKIN^*$, it will arbitrate between $IACKIN^*$ and the interrupt request it generates (IRQ^*) to determine which occurred first.

If the VME 3000/3010 receives $IACKIN^*$ before it has asserted IRQ^* , then the local slave has "lost" the arbitration and must generate $IACKOUT^*$ down the $IACK^*$ daisy chain. The local slave will not participate in this interrupt cycle. Another slave in the system will participate in the cycle. In this case, the VME 3000/3010 will continue to assert IRQ^* until it is eventually selected to participate.

If the VME 3000/3010 receives $IACKIN^*$ after it has asserted IRQ^* then the VME 3000/3010 will compare the valid addresses $A1-A3$ to the encoded priority levels $B1-B3$. If these do not match, the VME 3000/3010 will not participate in the interrupt cycle and must generate $IACKOUT^*$ down the daisy

chain. As in the case described in the previous paragraph, the VME 3000/3010 will continue to assert IRQ^* until it is eventually selected to participate.

T-52-33-13
If the VME 3000/3010 receives $IACKIN^*$ after it asserts IRQ^* and $A1-A3$ matches $B1-B3$ then the local slave has been selected to participate in the interrupt cycle. In this case the VME 3000/3010 asserts the interrupt acknowledge signal, $INTACK^*$. It does not pass $IACKOUT^*$ down the daisy chain.

$DS0^*$ is connected to DS^* to generate an 8 bit interrupt vector. Please contact factory for information on generating a 16/32 bit interrupt vector generator device.

When the VME 3000/3010 asserts $INTACK^*$, the local slave enables the data buffers for the interrupt vector. To complete the interrupt cycle, the local slave asserts $DTACK^*$.

The VME 3000 provides Release on Acknowledge operation (ROAK). Thus when $INTACK^*$ is asserted to the slave, IRQ^* is de-asserted from the bus. The VME 3010 provides both ROAK operation and Release on Register Access operation (RORA). By controlling the mode pin input, the VME 3010 switches between ROAK and RORA. In RORA mode, IRQ^* will not be de-asserted until the REG_ACC^* and $RORA_INH^*$ inputs are asserted. This indicates that the local STATUS/ID register has been read. The $RORA_INH^*$ input guarantees that the VME 3010 will ignore $LIRQ$ for 2 msec after reading the STATUS/ID register.

NOTE: The VME3000/3010 is edge triggered. The assertion of $INTACK^*$ releases IRQ^* . Also, the assertion of SYS_RESET^* clears the pending interrupt request, IRQ^* . Please contact the factory for information on level sensitive devices.

If the VME 3000/3010 is used in conjunction with PLX Technology's VME 2000 slave module selector, then the $INTACK^*$ output from the VME 3000/3010 can be connected to the $INTACK^*$ input of the VME 2000. Once the VME 2000 receives $INTACK^*$, it will enable $MODSEL^*$ which enables the data buffers for the interrupt vector. The VME 2000 will also generate $DTACK^*$ to finish the cycle. (See the VME 2000 data sheet).

T-52-33-13

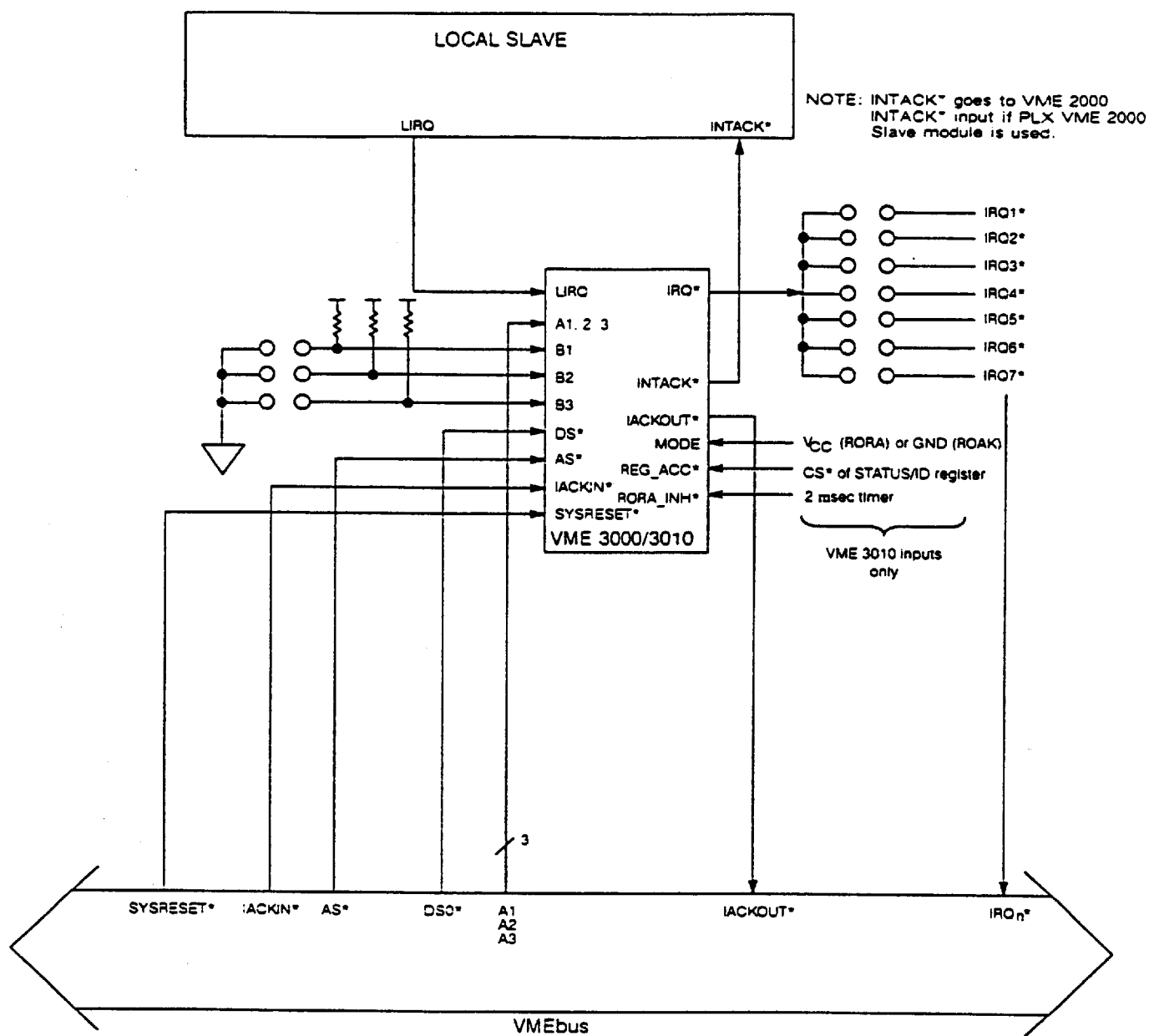


Figure 2. Interrupt Generator

T-52-33-13

INTERRUPT GENERATOR TIMING

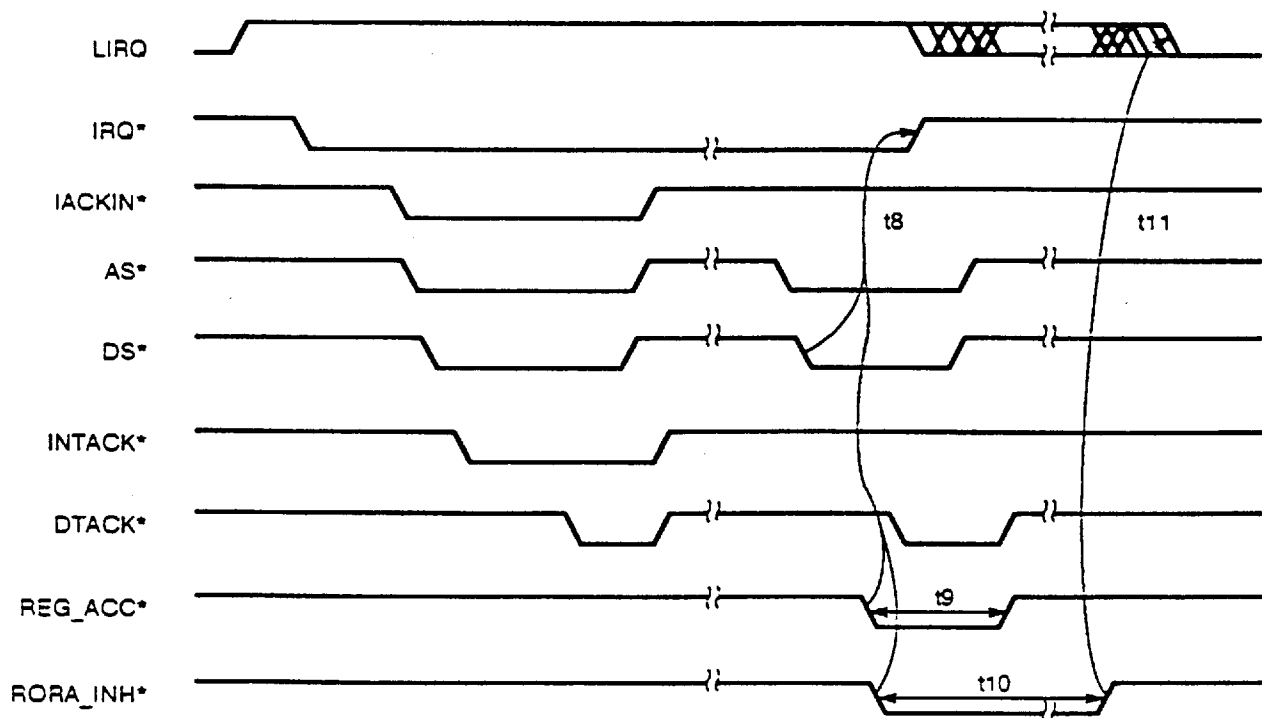
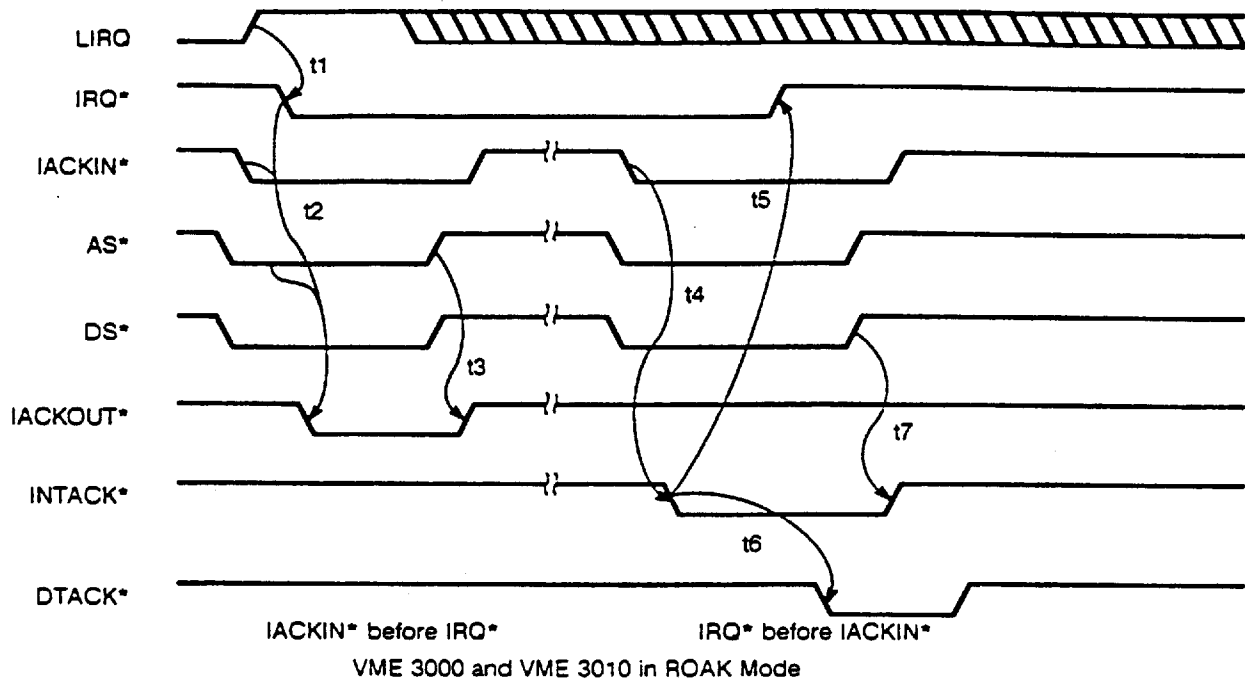
*MODE input pin tied to V_{CC} .

Figure 3. VMEbus Interrupt Generator Timing Diagram

Timing Parameter	Signals	Max. Time (ns) unless otherwise specified		Description
		C-45	I-55, M-65	
t1	LIRQ to IRQ* enable	30	40, 50	LIRQ is positive edge sensitive. LIRQ needs to be high for min. of 40 ns for -45 parts to enable IRQ*
t2	IRQ* to IACKOUT* enable	45	55, 65	If IACKIN* is received min. 140 ns to a Max. 225 ns before IRQ*. AS* must be low.
	IACKIN* to IACKOUT*	Min. 140 Max. 225	Min. 100, 140 Max. 240, 285	If IRQ* and IACKIN* are received at the same time. This allows for worst case arbitration timing. AS* must be low.
t3	AS* to IACKOUT* disable	45	55, 65	
t4	IACKIN* to INTACK* enable	Min. 140 Max. 225	Min. 100, 140 Max. 240, 285	
t5	INTACK* (or SYSRESET*) to IRQ* disable	90	110, 130	
t6	INTACK* to DTACK* enable	@ local slave	@ local slave	DTACK* finishes the interrupt cycle.
t7	DS* to INTACK* disable	45	55, 65	
t8	DS*, REG_ACC*, RORA_INH* to IRQ* negated	137	170, 195	Latest assertion of DS*, REG_ACC*, or RORA_INH* signal to IRQ* output negated.
t9	REG_ACC* pulse width	45 min	55, 65 min	Minimum pulse width on REG_ACC* input.
t10	RORA_INH* pulse width	2 msec min	2 msec min	Minimum time to ignore LIRQ input as required by VME specification.
t11	RORA_INH* negated to LIRQ input valid	90	110, 130	Time from RORA_INH* negated to the time VME 3010 starts sensing LIRQ valid.

Absolute Maximum Ratings

Storage Temperature -65°C to +150°C
 Ambient Temperature with
 Power Applied -55°C to +125°C
 Supply Voltage to Ground
 (pin 24 to pins 12, 18, & 20 on DIP) ... -0.5V to +7.0V
 DC Voltage to Outputs in
 High Z State -0.5V to +7.0V

Operating Ranges

T-5233-13

	Ambient Temperature	Supply Voltage (V _{CC})
Commercial	0°C to +70°C	5V ± 5%
Industrial (I)	-40°C to +85°C	5V ± 10%
Military (M)	-55°C to +125°C	5V ± 10%

Electrical Characteristics Tested over Operating Range

Parameter	Description	Test Conditions	Min	Max	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL} I _{OH} = -3.0mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL} Output pins I _{OL} = 24mA (Com'l)		0.5	V
				0.6	V
				0.5	V
				0.6	V
V _{IH}	Input HIGH Level		2.0		V
V _{IL}	Input LOW Level			0.8	V
I _{IX}	Input Leakage Current	V _{SS} ≤ V _{IN} ≤ V _{CC} , V _{CC} = Max	-10	10	mA
I _{OZ}	Output Leakage Current	V _{CC} = Max, V _{SS} ≤ V _{OUT} ≤ V _{CC}	-40	40	mA
I _{SC}	Output Short Circuit Current	V _{CC} = Max, V _{OUT} = 0.5V	-30	-90	mA
I _{CC}	Power Supply Current	V _{CC} = Max, V _{IN} = GND Outputs Open (Com'l)		80	mA
		V _{CC} = Max, V _{IN} = GND Outputs Open (MIL)		90	mA

Capacitance (sample tested only)

Parameter	Test Conditions	Pins	Typ	Units
C _{IN}	V _{IN} = 2.0V @ f = 1MHz	2-11, 14 (DIP)	5	pF
		13, 15-17, 18, 20-23 (DIP)	10	pF
C _{OUT}	V _{IN} = 2.0V @ f = 1MHz	13, 15-17, 18, 20-23 (DIP)	10	pF

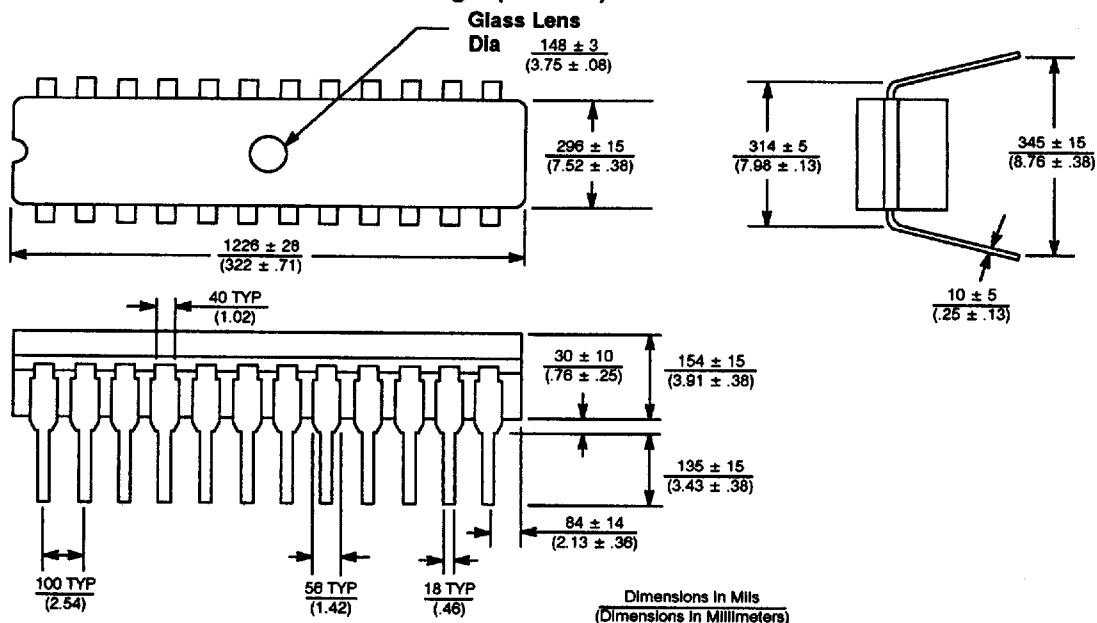
Package Information

The devices are available in 24 pin slimline DIP (300 mil wide) or 28 pin LCC.

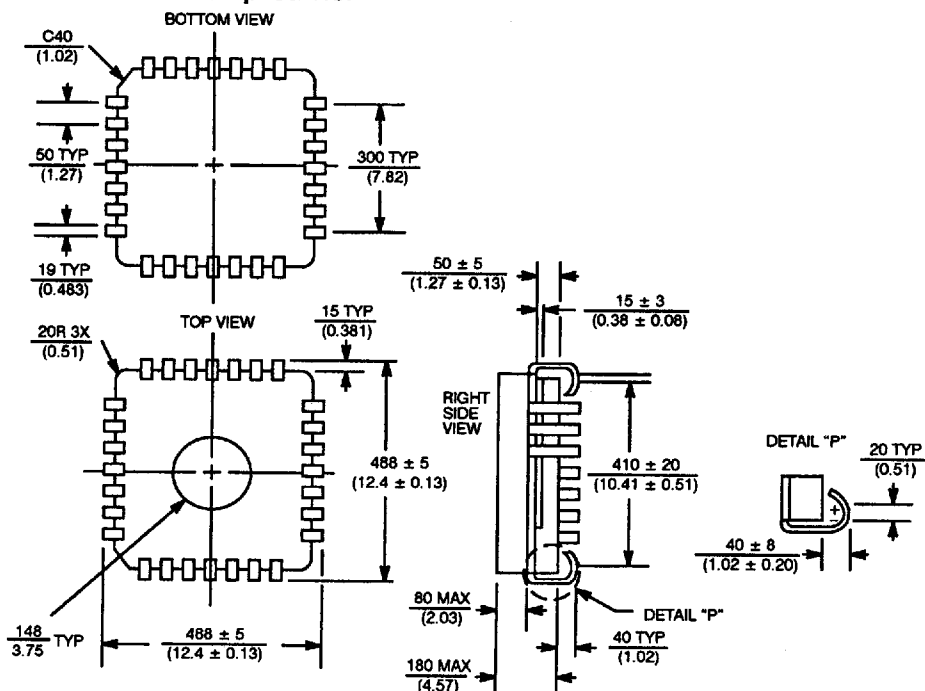
See PLX 448 or PLX 464 January 1989 or later data sheets for package dimensions. Contact PLX for further packaging information.

PLX reserves the right to make changes in its products without notice. For further information on specifications, contact PLX directly.

24-Lead Ceramic Dual In-line Package (CERDIP)



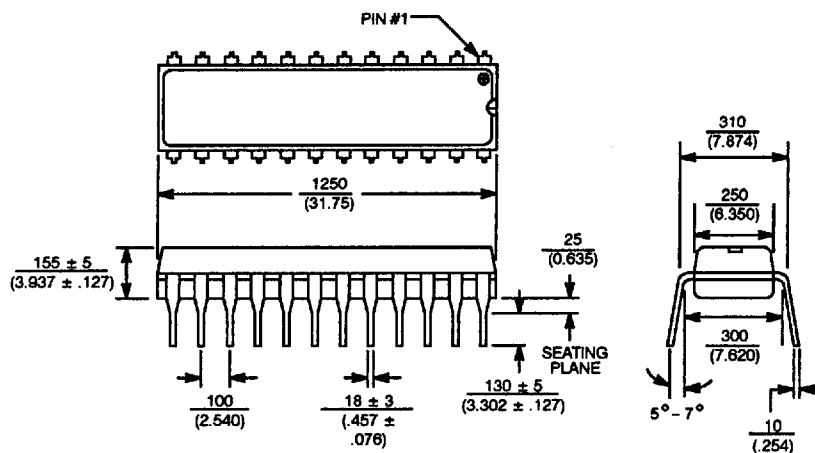
28-Pin J Lead Ceramic Chip Carrier



PLX 464

T-46-19-09

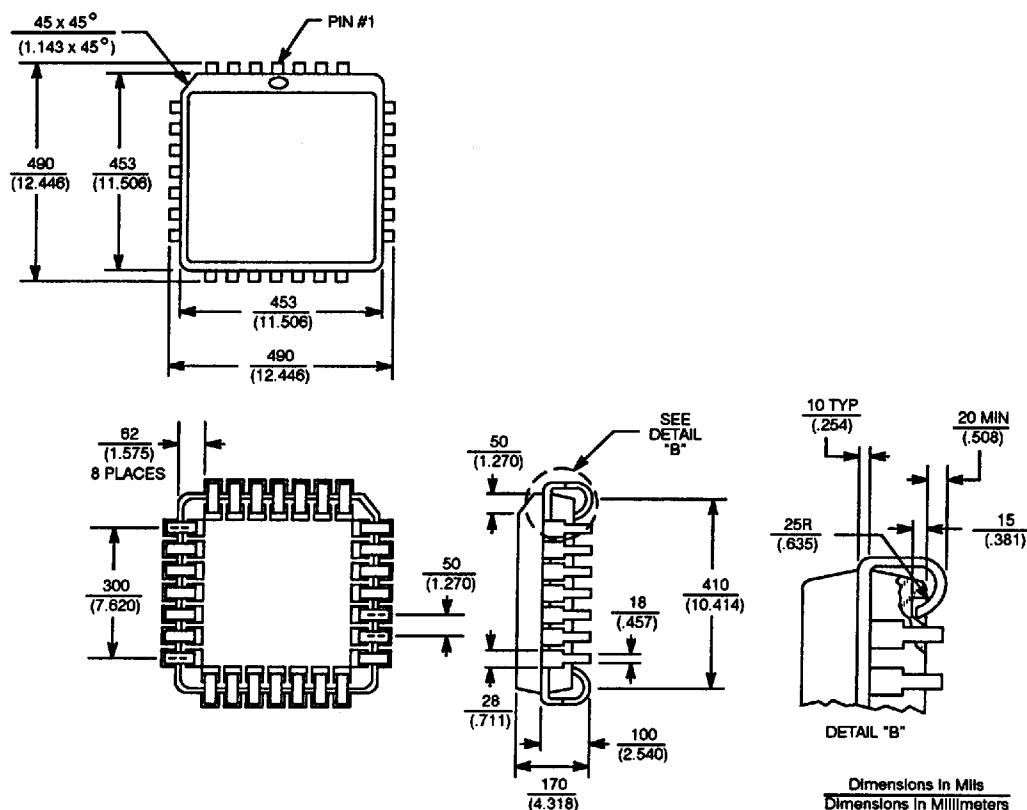
24-Pin DIP Plastic



Dimensions in Mils
Dimensions in Millimeters

Tolerances are ± 10 unless otherwise specified
(± 0.254)

28-Pin LCC Plastic



Dimensions in Mils
Dimensions in Millimeters

Tolerances are ± 10 unless otherwise specified
(± 0.254)