VRAM

128K x 8 DRAM WITH 256 x 8 SAM

FEATURES

- Industry standard pinout, timing and functions
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power: 15mW standby; 275mW active, typical
- Inputs and outputs are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 512-cycle refresh within 8ms
- No refresh required for serial access memory
- Optional FAST PAGE MODE access cycles
- Dual port organization: 128K x 8 DRAM port
  256 x 8 SAM port
- Fast access times - 70ns random, 22ns serial

SPECIAL FUNCTIONS

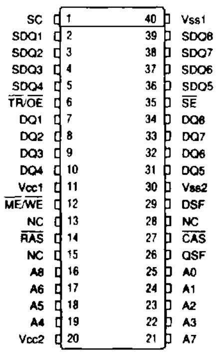
- JEDEC Standard Function set
- PERSISTENT MASKED WRITE
- SPLIT READ TRANSFER
- WRITE TRANSFER/SERIAL INPUT
- ALTERNATE WRITE TRANSFER
- BLOCK WRITE

OPTIONS

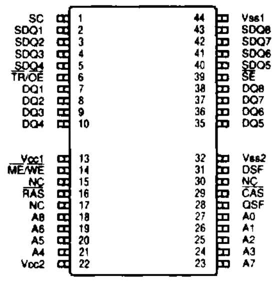
OPTIONS	MARKING
• Timing [DRAM, SAM (cycle/access)]	
70ns, 25ns/22ns	- 7
80ns, 30ns/25ns	- 8
100ns, 30ns/27ns	-10
• Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG
• 32ms low power/extended refresh	L

PIN ASSIGNMENT (Top View)

40-Pin SOJ (Q-6)



40/44-Pin TSOP* (R-5)



*Consult factory on TSOP availability.

MULTIPORT DRAM

GENERAL DESCRIPTION

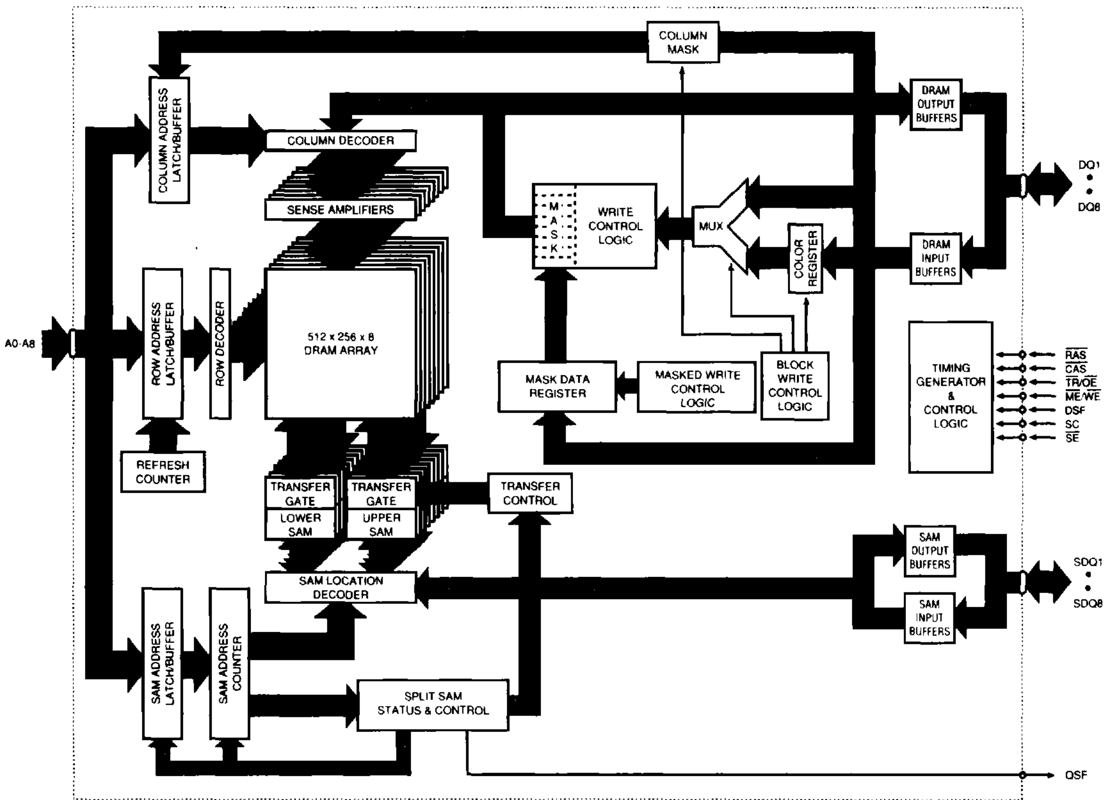
The MT42C8128 is a high-speed, dual port CMOS dynamic random access memory or video RAM (VRAM) containing 1,048,576 bits. These bits may be accessed either by an 8-bit wide DRAM port or by a 256 x 8-bit serial access memory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM. An extended refresh (32ms), low power option is available as the MT42C8128 L.

The DRAM portion of the VRAM is functionally identical to the MT4C4256 (256K x 4 DRAM). Eight 256-bit data registers make up the SAM portion of the VRAM. Data I/O and internal data transfer are accomplished using three separate bidirectional data paths: the 8-bit random access I/O port, the eight internal 256 bit wide paths between the DRAM and the SAM, and the 8-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing and address decoding logic.

Each port may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 8ms, or 32ms for the MT42C8128 L, (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and requires no refresh.

The operation and control of the MT42C8128 is optimized for high performance graphics and communication designs. The dual port architecture is well suited to buffering the sequential data used in raster graphics display, serial/parallel networking and data communications. Special features such as SPLIT READ TRANSFER and BLOCK WRITE, allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1	1	SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
6	6	TR/OE	Input	Transfer Enable: Enables an internal TRANSFER operation at RAS (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after RAS goes LOW (CAS must also be LOW), otherwise the output buffers are in a High-Z state.
12	14	ME/WE	Input	Mask Enable: If ME/WE is LOW at the falling edge of RAS, a MASKED WRITE cycle is performed, or Write Enable: ME/WE is also used to select a READ (ME/WE = H) or WRITE (ME/WE = L) cycle when accessing the DRAM. This includes a READ TRANSFER (ME/WE = H) or WRITE TRANSFER (ME/WE = L).
35	39	SE	Input	Serial Port Enable: SE enables the serial I/O buffers and allows a serial READ or WRITE operation to occur, otherwise the output buffers are in a High-Z state. SE is also used during a WRITE TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL INPUT MODE ENABLE cycle is performed.
29	31	DSF	Input	Special Function Select: DSF is used to indicate which special functions (BLOCK WRITE, MASKED WRITE vs. PERSISTENT MASKED WRITE, etc.) are used for a particular access cycle.
14	16	RAS	Input	Row Address Strobe: RAS is used to clock in the 9 row-address bits and strobe the ME/WE, TR/OE, DSF, SE, CAS and DQ inputs. It acts as master chip enable, and must fall to initiate any DRAM or TRANSFER cycle
27	29	CAS	Input	Column Address Strobe: CAS is used to clock-in the 8 column-address bits, enable the DRAM output buffers (along with TR/OE), and strobe the DSF input.
25, 24, 23, 22, 19, 18, 17, 21, 16	27, 26, 25, 24, 21, 20, 19, 23, 18	A0-A8	Input	Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by RAS and CAS to select one 8-bit word out of the 128K available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when RAS goes LOW) and A0-A7 indicate the SAM start address (when CAS goes LOW). A7, A8 = "don't care" for the start address when during SPLIT TRANSFER.

PIN DESCRIPTIONS (continued)

SOJ PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
7, 8, 9, 10, 31, 32, 33, 34	7, 8, 9, 10, 35, 36, 37, 38	DQ1-DQ8	Input/ Output	DRAM Data I/O: Data input/output for DRAM cycles; inputs for Mask Data Register and Color Register load cycles, and DQ and Column Mask inputs for BLOCK WRITE.
2, 3, 4, 5, 36, 37, 38, 39	2, 3, 4, 5, 40, 41, 42, 43	SDQ1-SDQ8	Input/ Output	Serial Data I/O: Input, output, or High-Z.
26	28	QSF	Output	Split SAM Status: QSF indicates which half of the SAM is being accessed. LOW if address is 0-127, HIGH if address is 128-255.
15, 28	17, 30	NC	–	No Connect: This pin should be either left unconnected or tied to ground.
11, 20	13, 22	Vcc	Supply	Power Supply: +5V ±10%
30, 40	32, 44	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT42C8128 may be divided into three functional blocks: the DRAM, the transfer circuitry, and the SAM. All of the operations described below are shown in the AC Timing Diagrams section of this data sheet and summarized in the Truth Table.

Note: *For dual-function pins, the function that is not being discussed will be surrounded by parentheses. For example, the TR/OE pin will be shown as TR/(OE) in references to transfer operations.*

DRAM OPERATION

DRAM REFRESH

Like any DRAM-based memory, the MT42C8128 VRAM must be refreshed to retain data. All 512 row address combinations must be accessed within 8ms. The MT42C8128 supports CAS-BEFORE-RAS, RAS-ONLY and HIDDEN types of refresh cycles.

For the CAS-BEFORE-RAS REFRESH cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data, and simply must perform 512 CAS-BEFORE-RAS cycles within the 8ms time period.

The refresh address must be generated externally and applied to A0-A8 inputs for RAS-ONLY REFRESH cycles. The DQ pins remain in a High-Z state for both the RAS-ONLY and CAS-BEFORE-RAS cycles.

HIDDEN REFRESH cycles are performed by toggling RAS (and keeping CAS LOW) after a READ or WRITE cycle. This performs CAS-BEFORE-RAS cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row that is being accessed. The SAM portion of the MT42C8128 is fully static and does not require any refreshing.

DRAM READ AND WRITE CYCLES

The DRAM portion of the VRAM is nearly identical to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or in "don't care" states for the DRAM are specified for the VRAM. These conditions are highlighted in the following discussion. In addition, the VRAM has several special functions that can be used when writing to the DRAM.

The 17 address bits used to select an 8-bit word from the 131,072 available are latched into the chip using the A0-A8, RAS and CAS inputs. First, the 9 row-address bits are set up on the address inputs and clocked into the part when RAS transitions from HIGH-to-LOW. Next, the 8 column address bits are set up on the address inputs and clocked-in when CAS goes from HIGH-to-LOW.

Note: *RAS also acts as a "master" chip enable for the VRAM. If RAS is inactive, HIGH; all other DRAM control pins (CAS, TR/OE, ME/WE, etc.) are a "don't care" and may change state without effect. No DRAM or TRANSFER cycles will be initiated without RAS falling.*

For single port DRAMS, the OE pin is a "don't care" when RAS goes LOW. For the VRAM, when RAS goes LOW, TR/(OE) selects between DRAM access or TRANSFER cycles. TR/(OE) must be HIGH at the RAS HIGH-to-LOW transition for all DRAM operations (except CAS-BEFORE-RAS).

If (ME)/WE is HIGH when CAS goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1-DQ8 port. To enable the DRAM output port, the (TR)/OE input must transition from HIGH-to-LOW some time after RAS falls.

For single port normal DRAMs, WE is a "don't care" when RAS goes LOW. For the VRAM, ME/(WE) is used, when RAS goes LOW, to select between a MASKED WRITE cycle and a normal WRITE cycle. If ME/(WE) is LOW at the RAS HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any DRAM access cycle (READ or WRITE), ME/(WE) must be HIGH at the RAS HIGH-to-LOW transition. If (ME)/WE is LOW before CAS goes LOW, a DRAM EARLY-WRITE operation is performed and the data present on the DQ1-DQ8 data port will be written into the selected memory cells. If (ME)/WE goes LOW after CAS goes LOW, a DRAM LATE-WRITE operation is performed. Refer to the AC timing diagrams.

The VRAM can perform all the normal DRAM cycles including READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE (Late or Early), and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

MULTIPORT DRAM

NONPERSISTENT MASKED WRITE

The MASKED WRITE feature eliminates the need for a READ-MODIFY-WRITE cycle when changing only specific bits within an 8-bit word. The MT42C8128 supports two types of MASKED WRITE cycles, NONPERSISTENT MASKED WRITE and PERSISTENT MASKED WRITE.

If $\overline{ME}/(\overline{WE})$ and DSF are LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a NONPERSISTENT MASKED WRITE is performed and the data (mask data) present on the DQ1-DQ8 inputs will be written into the mask data register. The mask data acts as an individual write enable for each of the eight DQ1-DQ8 pins. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operation to proceed. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ goes LOW, the bits present on the DQ1-DQ8 inputs will be either written to the DRAM (if the mask data bit is HIGH) or ignored (if the mask data bit is LOW). The DRAM contents that correspond to masked input bits will not be changed during the WRITE cycle. The MASKED WRITE is nonpersistent (must be re-entered at every $\overline{RAS}$ cycle) if DSF is LOW when $\overline{RAS}$ goes LOW. The mask data register is cleared at the end of every NONPERSISTENT MASKED WRITE. FAST PAGE MODE can be used with NONPERSISTENT MASKED WRITE to write several column locations in an addressed row. The same mask is used during the entire FAST-PAGE-MODE $\overline{RAS}$ cycle. An example NONPERSISTENT MASKED WRITE cycle is shown in Figure 1.

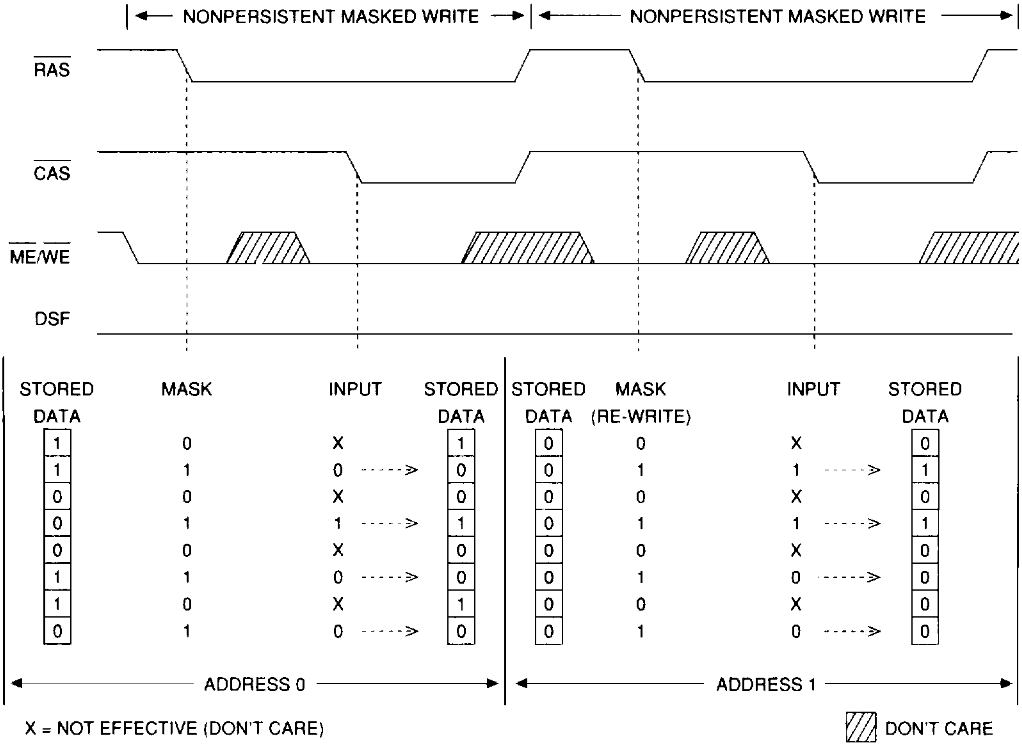


Figure 1
NONPERSISTENT MASKED WRITE EXAMPLE

PERSISTENT MASKED WRITE

The PERSISTENT MASKED WRITE feature eliminates the need to rewrite the mask data before each MASKED WRITE cycle if the same mask data is being used repeatedly. To initiate a PERSISTENT MASKED WRITE, a LOAD MASK REGISTER cycle is performed by taking $\overline{ME}/(\overline{WE})$ and DSF HIGH when $\overline{RAS}$ goes LOW. The mask data is loaded into the internal register when $\overline{CAS}$ goes LOW.

PERSISTENT MASKED WRITE cycles may then be performed by taking $\overline{ME}/(\overline{WE})$ LOW and DSF HIGH when $\overline{RAS}$ goes LOW. The contents of the mask data register will then be used as the mask data for the DRAM inputs. Unlike the NONPERSISTENT MASKED WRITE cycle, the data present on the DQ inputs is not loaded into the mask register when $\overline{RAS}$ falls, and the mask data register will not be cleared at the end of the cycle. Any number of PERSISTENT MASKED WRITE cycles, to any address, may be performed without having to reload the mask data register. Figure 2 shows the LOAD MASK REGISTER and two PERSISTENT MASKED WRITE cycles in operation. The LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycles allow controllers that cannot provide mask data to the DQ pins at $\overline{RAS}$ time to perform MASKED WRITE operations. PERSISTENT MASKED WRITE operations can be performed during FAST PAGE MODE cycles and the same mask will apply to all addressed columns in the addressed row.

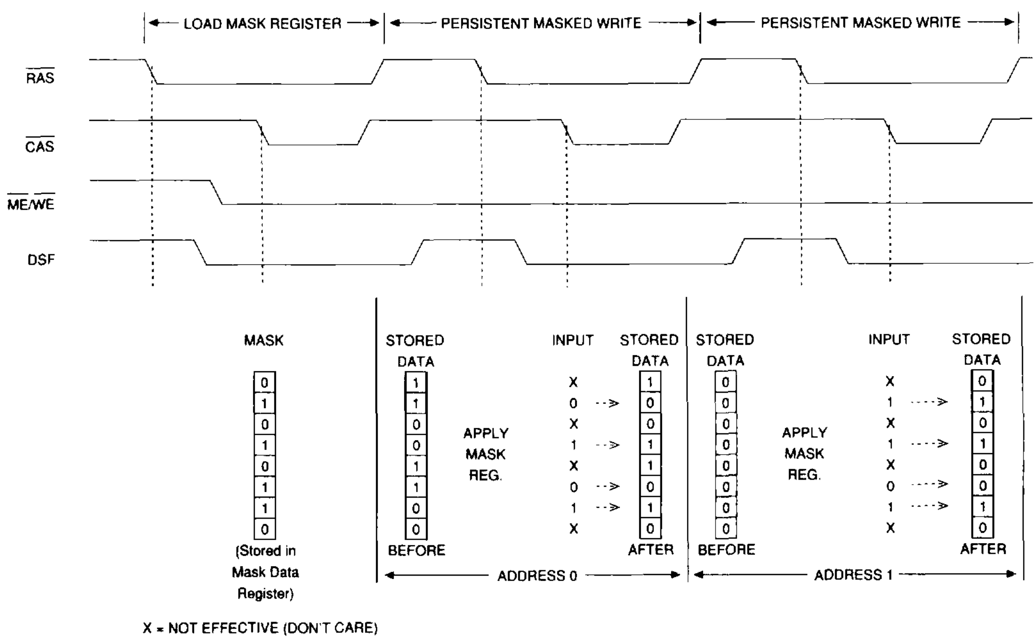


Figure 2
PERSISTENT MASKED WRITE EXAMPLE

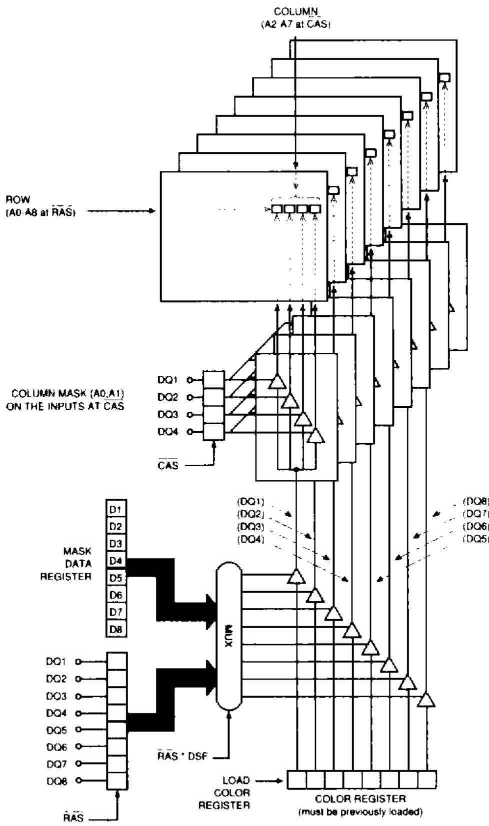


Figure 3
BLOCK WRITE EXAMPLE

BLOCK WRITE

If DSF is HIGH when $\overline{CAS}$ goes LOW, the MT42C8128 will perform a BLOCK WRITE cycle instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register are directly written to four adjacent column locations (see Figure 3). The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER). Each DQ location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane.

The row is addressed as in a normal DRAM WRITE cycle. However when $\overline{CAS}$ goes LOW, only the A2-A7 inputs are used. A2-A7 specify the "block" of four adjacent column locations that will be accessed. The DQ inputs (DQ1, 2, 3, and 4) are then used to determine what combination of the four column locations will be changed. The table on this page illustrates how each of the DQ inputs is used to selectively enable or disable individual column locations within the block. The write enable controls are active HIGH; a logic "1" enables the WRITE function and a logic "0" disables the WRITE function.

INPUTS	COLUMN ADDRESS CONTROLLED	
	A0	A1
DQ1	0	0
DQ2	1	0
DQ3	0	1
DQ4	1	1

NONPERSISTENT MASKED BLOCK WRITE

The MASKED WRITE functions can also be used during BLOCK WRITE cycles. NONPERSISTENT MASKED BLOCK WRITE operates exactly like the normal NONPERSISTENT MASKED WRITE except the mask is now applied to four column locations instead of just one.

Like NONPERSISTENT MASKED WRITE, the combination of $\overline{\text{ME}}/(\overline{\text{WE}})$ LOW and DSF LOW when $\overline{\text{RAS}}$ goes LOW initiates a NONPERSISTENT MASK cycle. The DSF pin must be driven HIGH when $\overline{\text{CAS}}$ goes LOW, to perform a NONPERSISTENT MASKED BLOCK WRITE. Using the column mask input and MASKED WRITE function allows any combination of the eight bit planes or four column locations to be masked.

PERSISTENT MASKED BLOCK WRITE

This cycle is also performed exactly like the normal PERSISTENT MASKED WRITE except that DSF is HIGH when $\overline{\text{CAS}}$ goes LOW to indicate the BLOCK WRITE function. Both the mask data register and the color register must be loaded with the appropriate data prior to starting a PERSISTENT MASKED BLOCK WRITE.

LOAD MASK DATA REGISTER

The LOAD MASK REGISTER operation and timing are identical to a normal WRITE cycle except that DSF is HIGH when $\overline{\text{RAS}}$ goes LOW. As shown in the Truth Table, the combination of $\overline{\text{TR}}/(\overline{\text{OE}})$, $\overline{\text{ME}}/(\overline{\text{WE}})$, and DSF being HIGH when $\overline{\text{RAS}}$ goes LOW indicates the cycle is a LOAD REGISTER cycle. DSF is used when $\overline{\text{CAS}}$ goes LOW to select the register to be loaded, and must be LOW for a LOAD MASK REGISTER cycle. The data present on the DQ lines will then be written to the mask data register.

Note: *For a normal DRAM WRITE cycle, the mask data register is disabled but not modified. The mask data register contents will not be changed unless a NONPERSISTENT MASKED WRITE cycle or a LOAD MASK REGISTER cycle is performed.*

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK REGISTER cycle.

The mask data register contents are used during PERSISTENT MASKED WRITE and PERSISTENT MASKED BLOCK WRITE cycles to selectively enable writes to the eight DQ planes.

LOAD COLOR REGISTER

The LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF is HIGH when $\overline{\text{CAS}}$ goes LOW. The contents of the color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.

TRANSFER OPERATIONS

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW then $\overline{RAS}$ goes LOW. The state of $(\overline{ME})/\overline{WE}$ when $\overline{RAS}$ goes LOW indicates the direction of the TRANSFER (to or from the DRAM), and DSF is used to select between NORMAL TRANSFER, SPLIT READ TRANSFER, and ALTERNATE WRITE TRANSFER cycles. Each of the TRANSFER cycles available is described below.

READ TRANSFER (DRAM-TO-SAM TRANSFER)

If $(\overline{ME})/\overline{WE}$ is HIGH and DSF is LOW when $\overline{RAS}$ goes LOW, a READ TRANSFER cycle is selected. The row address bits indicate the eight 256-bit DRAM row planes that are to be transferred to the eight SAM data register planes. The column address bits indicate the start address (or Tap address) of the serial output cycle from the SAM data registers. $\overline{CAS}$ must fall for every TRANSFER in order to load a valid Tap address. A read transfer may be accomplished two ways. If the transfer is to be synchronized with SC (REAL-TIME READ TRANSFER), $\overline{TR}/(\overline{OE})$ is taken HIGH after $\overline{CAS}$ goes LOW. If the transfer does not have to be synchronized with SC (READ TRANSFER), $\overline{TR}/(\overline{OE})$ may go HIGH before $\overline{CAS}$ goes LOW (refer to the AC Timing Diagrams). The 2,048 bits of DRAM data are written into the SAM data registers and the serial shift start address is stored in an internal 8-bit register. QSF will be LOW if access is from the lower half (addresses 0 through 127), and HIGH if access is from the upper half (128 through 255). If $\overline{SE}$ is LOW, the first bits of the new row data will appear at the serial outputs with the first SC clock pulse. $\overline{SE}$ enables the serial outputs and may be either HIGH or LOW during this operation. The SAM address pointer will increment with the SC LOW-to-HIGH transition, regardless of the state of $\overline{SE}$. Performing a READ TRANSFER cycle sets the direction of the SAM I/O buffers to the output mode.

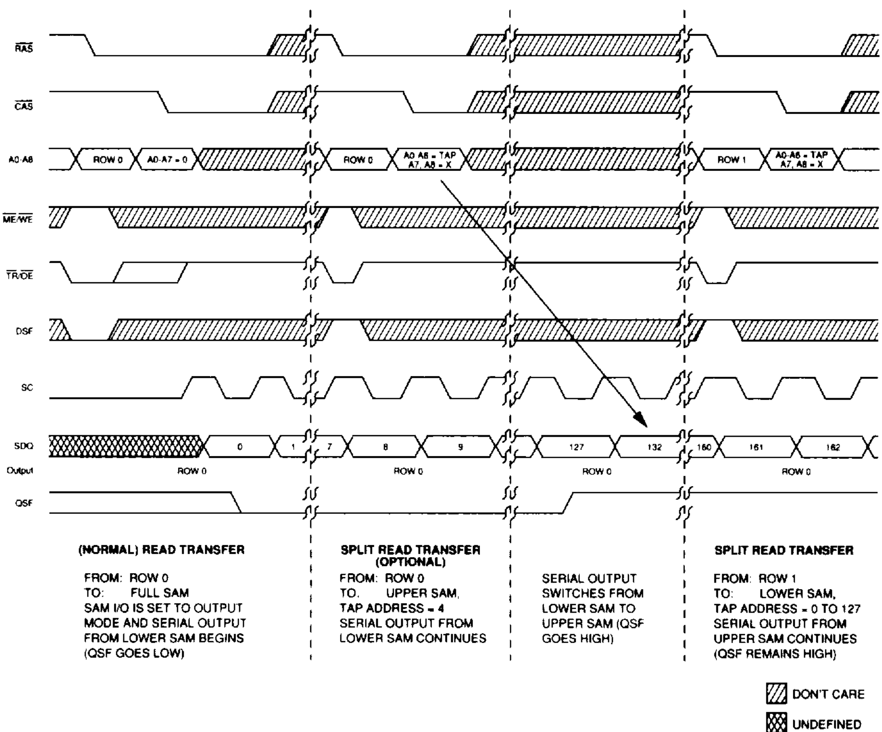


Figure 4
TYPICAL SPLIT-READ-TRANSFER INITIATION SEQUENCE

SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)

The SPLIT READ TRANSFER (SRT) cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream. When using normal TRANSFER cycles, the REAL-TIME READ TRANSFER cycle has to occur immediately after the last bit of "old data" was clocked out of the SAM port.

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data may be transferred to the other half. The transfer may occur at any time while the other half is sending data, and need not be synchronized with the SC clock.

The $\overline{TR}/(\overline{OE})$ timing is also relaxed for SPLIT TRANSFER cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle and therefore is independent of the rising edges of $\overline{RAS}$ or $\overline{CAS}$. The transfer timing is generated internally for SPLIT TRANSFER cycles. A SPLIT READ TRANSFER does not change the direction of the SAM port.

A normal, non-split READ TRANSFER cycle must precede any sequence of SPLIT READ TRANSFER cycles to provide a reference to which half of the SAM the access will begin, and to set SAM I/O direction. Then SPLIT READ TRANSFERS may be initiated by taking DSF HIGH when $\overline{RAS}$ goes LOW during the TRANSFER cycle. As in nonsplit transfers, the row address is used to specify the DRAM row to be transferred. The column address, A0-A6, is used to input the SAM Tap address. Address pin A7 is a "don't care" when the Tap address is loaded at the HIGH-to-LOW transition of $\overline{CAS}$. It is internally generated so that the SPLIT TRANSFER will be to the SAM half not currently being accessed.

Figure 4 shows a typical SPLIT READ TRANSFER initiation sequence. The normal READ TRANSFER is first performed, followed by a SPLIT READ TRANSFER of the same row to the upper half of the SAM. The SRT to the upper half is optional, it is only needed if the Tap for the upper half is ≠ 0. Serial access continues, and when the SAM address counter reaches 127 ("A7" = 0, A0-A6 = 1) the new Tap address is loaded for the next half ("A7" = 1, A0-A6 = Tap) and the QSF output goes HIGH. Once the serial access has switched to the upper SAM, new data may be transferred to the lower SAM. The controller must wait for the state of QSF to change and then the new data may be transferred to the SAM half not being accessed. For example, the next step in Figure 4 would be to wait until QSF went LOW (indicating that row-1 data is shifting out of the lower SAM) and then transfer the upper half of row 1 to the upper SAM. If the half boundary is reached, before an SRT is done for the half, a Tap address of "0" will be used. Access will start at 0 if going to the lower half, and 128 if going to the upper half. See Figure 5.

WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the WRITE TRANSFER is identical to that of the READ TRANSFER described previously except $(\overline{ME})/\overline{WE}$ and $\overline{SE}$ must be LOW when $\overline{RAS}$ goes LOW. The row address indicates the DRAM row to which the SAM data registers will be written. The column address (Tap) indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. A WRITE TRANSFER changes the direction of the SAM I/O buffers to the input mode. QSF is LOW if access is to the lower half of the SAM, and HIGH if to access the upper half.

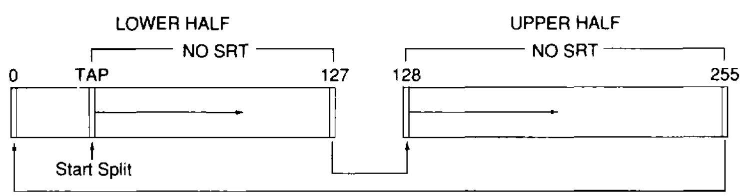


Figure 5
SPLIT SAM TRANSFER

PSEUDO WRITE TRANSFER (SERIAL-INPUT-MODE ENABLE)

The PSEUDO WRITE TRANSFER cycle is used to change the direction of the SAM port from output to input without performing a WRITE TRANSFER cycle. A PSEUDO WRITE TRANSFER cycle is a WRITE TRANSFER cycle with $\overline{SE}$ held HIGH instead of LOW. The DRAM data will not be disturbed and the SAM will be ready to accept input data.

ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the ALTERNATE WRITE TRANSFER is identical to the WRITE TRANSFER except that the DSF pin is HIGH and ($\overline{ME}$)/$\overline{WE}$ is LOW when $\overline{RAS}$ goes LOW, allowing $\overline{SE}$ to be a "don't care." This allows the outputs to be disabled using $\overline{SE}$ during a WRITE TRANSFER cycle. ALTERNATE WRITE TRANSFER will change the SAM I/O direction to an input condition.

SERIAL INPUT AND SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUTPUT are SC and $\overline{SE}$. The rising edge of SC increments the serial address counter and provides access to the next SAM location. $\overline{SE}$ enables or disables the serial input/output buffers.

Serial output of the SAM contents will start at the serial start address that was loaded in the SAM address counter during a READ or SPLIT READ TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the 8-bit port. $\overline{SE}$ is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether $\overline{SE}$ is HIGH or LOW. The address progresses through the SAM and will wrap around (after count 127 or 255) to the Tap address of the next half, for split modes. If an SRT was not performed before the half boundary is reached, the count will progress as illustrated in Figure 5. Address count will wrap around (after count 255) to Tap address 0 if in the "full" SAM modes.

SC is also used to clock-in data when the device is in the serial input mode. As in the serial output operation, the contents of the SAM address counter (loaded when the serial input mode was enabled) will determine the serial address of the first 8-bit word written. $\overline{SE}$ acts as a write enable for serial input data and must be LOW for valid serial input. If $\overline{SE}$ = HIGH, the data inputs are disabled and the SAM contents will not be modified. The serial address counter is incremented with every LOW-to-HIGH transition of SC, regardless of the logic level on the $\overline{SE}$ input.

POWER-UP AND INITIALIZATION

After Vcc is at specified operating conditions, for 100µs minimum, eight $\overline{RAS}$ cycles must be executed to initialize the dynamic memory array. Micron recommends that $\overline{RAS}$ = ($\overline{TR}$)/$\overline{OE}$ ≥ V_{IH} during power up to ensure that the DRAM I/O pins (DQs) are in a High-Z state. The DRAM array will contain random data.

The SAM portion of the MT42C8128 is completely static in operation and does not require refresh or initialization. The SAM port will power-up in the serial input mode (WRITE TRANSFER) and the I/O pins (SDQs) will be High- Z, regardless of the state of $\overline{SE}$. The mask and color register will contain random data after power-up. QSF initializes in the LOW state.

MULTIPORT DRAM

TRUTH TABLE

CODE	FUNCTION	RAS FALLING EDGE					CAS FALL	A0-A8[1]		DQ1-DQ8[2]		REGISTERS	
		CAS	TR/OE	ME/WE	DSF	SE	DSF	RAS	CAS, A8=X	RAS	CAS, WE[3]	MASK	COLOR
	DRAM OPERATIONS												
CBR	CAS-BEFORE-RAS REFRESH	0	X	X	X	X	X	—	X	—	X	X	X
ROR	RAS-ONLY REFRESH	1	1	X	X	X	—	ROW	—	X	—	X	X
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	X	0	ROW	COLUMN	X	VALID	X	X
RWNM	NONPERSISTENT (LOAD AND USE) MASKED WRITE TO DRAM	1	1	0	0	X	0	ROW	COLUMN	WRITE MASK	VALID DATA	LOAD & USE	X
RWOM	PERSISTENT (USE REGISTER) MASKED WRITE TO DRAM	1	1	0	1	X	0	ROW	COLUMN	X	VALID DATA	USE	X
BW	BLOCK WRITE TO DRAM (NO DATA MASK)	1	1	1	0	X	1	ROW	COLUMN (A2-A7)	X	COLUMN MASK	X	USE
BWNM	NONPERSISTENT (LOAD & USE) MASKED BLOCK WRITE TO DRAM	1	1	0	0	X	1	ROW	COLUMN	WRITE MASK	COLUMN MASK	LOAD & USE	USE
BWOM	PERSISTENT (USE MASK REGISTER) MASKED BLOCK WRITE TO DRAM	1	1	0	1	X	1	ROW	COLUMN (A2-A7)	X	COLUMN MASK	USE	USE
	REGISTER OPERATIONS												
LMR	LOAD MASK REGISTER	1	1	1	1	X	0	ROW[4]	X	X	WRITE MASK	LOAD	X
LCR	LOAD COLOR REGISTER	1	1	1	1	X	1	ROW[4]	X	X	COLOR DATA	X	LOAD
	TRANSFER OPERATIONS												
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	X	X	ROW	TAP[5]	X	X	X	X
SRT	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	X	X	ROW	TAP[5]	X	X	X	X
WT	WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	0	0	X	ROW	TAP[5]	X	X	X	X
PWT	PSEUDO WRITE TRANSFER (SERIAL-INPUT- MODE ENABLE)	1	0	0	0	1	X	ROW[4]	TAP[5]	X	X	X	X
AWT	ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	1	X	X	ROW	TAP[5]	X	X	X	X

NOTE:
1. These columns show what must be present on the A0-A8 inputs when RAS falls and A0-A7 when CAS falls.
2. These columns show what must be present on the DQ1-DQ8 inputs when RAS falls and when CAS falls.
3. On WRITE cycles (except BLOCK WRITE), the input data is latched at the falling edge of CAS or ME/WE, whichever is later. Similarly, on READ cycles, the output data is activated at the falling edge of CAS or TR/OE, whichever is later.
4. The ROW that is addressed will be refreshed, but no particular ROW address is required.
5. This is the SAM location that the first SC cycle will access. For split SAM transfers, the Tap will be the first address location accessed of the "new" SAM half after the boundary of the current half is reached (127 for lower half, 255 for upper half).

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (Ambient) ....0°C to +70°C
Storage Temperature (Plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	VIH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1

MULTIPORT DRAM

DC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le 70°C$; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT Any input (0V ≤ VIN ≤ Vcc); all other pins not under test = 0V	IL	-10	10	µA	
OUTPUT LEAKAGE CURRENT (DQ, SDQ disabled, 0V ≤ VOUT ≤ Vcc)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -2.5mA)	VOH	2.4		V	1
Output Low Voltage (IOUT = 2.5mA)	VOL		0.4	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	CI1		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, SC, $\overline{SE}$, DSF	CI2		7	pF	2
Input/Output Capacitance: DQ, SDQ	CI/O		9	pF	2
Output Capacitance: QSF	CO		9	pF	2

CURRENT DRAIN, SAM IN STANDBY

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX -7	MAX -8	MAX -10	UNITS	NOTES
OPERATING CURRENT (RAS and CAS = Cycling: ᵗRC = ᵗRC (MIN))	I_{CC1}	95	85	75	mA	3, 4 26
OPERATING CURRENT: FAST PAGE MODE (RAS = V_{IL}; CAS = Cycling: ᵗPC = ᵗPC (MIN))	I_{CC2}	85	75	65	mA	3, 4 27
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current (RAS = CAS = V_{IH} after 8 RAS cycles (MIN); other inputs ≥ V_{IH} or ≤ V_{IL})	I_{CC3}	8	8	8	mA	4
STANDBY CURRENT: CMOS INPUT LEVELS (MT42C8128 L only) (RAS = CAS ≥ Vcc -0.2V, other inputs ≥ Vcc -0.2V or ≤ 0.2V)	I_{CC4}	500	500	500	µA	4
REFRESH CURRENT: RAS-ONLY (RAS = Cycling; CAS = V_{IH})	I_{CC5}	95	85	75	mA	3, 26
REFRESH CURRENT: CAS-BEFORE-RAS (RAS and CAS = Cycling)	I_{CC6}	95	85	75	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) MT42C8128 L only Average power supply current during BATTERY BACKUP refresh: CAS ≤ 0.2V or CAS-BEFORE-RAS cycling; RAS = ᵗRAS (MIN) to 300ns; ME/WE, A0-A8 and DQs ≥ Vcc - 0.2V or ≤ 0.2V (DQs may be left open), ᵗRC = 62.5µs (512 rows at 62.5µs = 32ms)	I_{CC7}	600	600	600	µA	3, 5
SAM/DRAM DATA TRANSFER	I_{CC8}	105	95	90	mA	3

CURRENT DRAIN, SAM ACTIVE (ᵗSC = MIN)

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX -7	MAX -8	MAX -10	UNITS	NOTES
OPERATING CURRENT (RAS and CAS = Cycling: ᵗRC = ᵗRC (MIN))	I_{CC9}	150	130	120	mA	3, 4, 26
OPERATING CURRENT: FAST PAGE MODE (RAS = V_{IL}; CAS = Cycling: ᵗPC = ᵗPC (MIN))	I_{CC10}	140	120	110	mA	3, 4, 27
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current (RAS = CAS = V_{IH} after 8 RAS cycles (MIN); other inputs ≥ V_{IH} or ≤ V_{IL})	I_{CC11}	55	45	45	mA	3, 4
REFRESH CURRENT: RAS-ONLY (RAS = Cycling; CAS = V_{IH})	I_{CC12}	150	130	120	mA	3, 4, 26
REFRESH CURRENT: CAS-BEFORE-RAS (RAS and CAS = Cycling)	I_{CC13}	150	130	120	mA	3, 4, 5
SAM/DRAM DATA TRANSFER	I_{CC14}	160	130	125	mA	3, 4

MULTIPORT DRAM

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^{t}RC	130		150		180		ns	
READ-MODIFY-WRITE cycle time	^{t}RWC	175		190		230		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	45		50		55		ns	
FAST-PAGE-MODE READ-MODIFY-WRITE cycle time	^{t}PRWC	90		95		110		ns	
Access time from $\overline{RAS}$	^{t}RAC		70		80		100	ns	14
Access time from $\overline{CAS}$	^{t}CAC		20		25		25	ns	15
Access time from ($\overline{TR}$)/$\overline{OE}$	^{t}OE		20		20		25	ns	
Access time from column address	^{t}AA		35		40		45	ns	
Access time from $\overline{CAS}$ precharge	^{t}CPA		40		45		50	ns	
$\overline{RAS}$ pulse width	^{t}RAS	70	20,000	80	20,000	100	20,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^{t}RASP	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	^{t}RSH	20		20		25		ns	
$\overline{RAS}$ precharge time	^{t}RP	50		60		70		ns	
$\overline{CAS}$ pulse width	^{t}CAS	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time	^{t}CSH	70		80		100		ns	
$\overline{CAS}$ precharge time	^{t}CP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^{t}RCD	20	50	20	55	20	75	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^{t}CRP	10		10		10		ns	
Row address setup time	^{t}ASR	0		0		0		ns	
Row address hold time	^{t}RAH	10		10		15		ns	
$\overline{RAS}$ to column address delay time	^{t}RAD	20	45	15	40	20	50	ns	18
Column address setup time	^{t}ASC	0		0		0		ns	
Column address hold time	^{t}CAH	15		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^{t}AR	45		55		70		ns	
Column address to $\overline{RAS}$ lead time	^{t}RAL	35		40		50		ns	
Read command setup time	^{t}RCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^{t}RCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^{t}RRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^{t}CLZ	3		3		3		ns	
Output buffer turn-off delay	^{t}OFF	3	20	3	20	3	20	ns	20, 23
Output disable	^{t}OD	3	10	3	10	3	20	ns	20, 23
Output disable hold time from start of WRITE	^{t}OEH	10		10		20		ns	27
$\overline{OE}$ LOW to $\overline{RAS}$ HIGH delay time	^{t}ROH	0		0		0		ns	

DRAM TIMING PARAMETERS (continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command setup time	ᵗWCS	0		0		0		ns	21
Write command hold time	ᵗWCH	15		15		15		ns	
Write command hold time (referenced to RAS)	ᵗWCR	45		55		70		ns	
Write command pulse width	ᵗWP	15		15		15		ns	
Write command to RAS lead time	ᵗRWL	20		20		20		ns	
Write command to CAS lead time	ᵗCWL	20		20		20		ns	
Data-in setup time	ᵗDS	0		0		0		ns	22
Data-in hold time	ᵗDH	15		15		15		ns	22
Data-in hold time (referenced to RAS)	ᵗDHR	45		55		65		ns	
RAS to WE delay time	ᵗRWD	90		100		130		ns	21
Column address to WE delay time	ᵗAWD	55		65		75		ns	21
CAS to WE delay time	ᵗCWD	40		45		55		ns	21
Transition time (rise or fall)	ᵗT	3	35	3	35	3	35	ns	9, 10
Refresh period (512 cycles)	ᵗREF		8(32)		8(32)		8(32)	ms	29
RAS to CAS precharge time	ᵗRPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS REFRESH)	ᵗCSR	10		10		10		ns	5
CAS hold time (CAS-BEFORE-RAS REFRESH)	ᵗCHR	10		10		10		ns	5
ME/WE to RAS setup time	ᵗWSR	0		0		0		ns	
ME/WE to RAS hold time	ᵗRWH	15		15		15		ns	
Mask Data to RAS setup time	ᵗMS	0		0		0		ns	
Mask Data to RAS hold time	ᵗMH	15		15		15		ns	

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
TR/(OE) LOW to RAS setup time	tTLS	0		0		0		ns	
TR/(OE) LOW to RAS hold time	tTLH	15	10,000	15	10,000	15	10,000	ns	
TR/(OE) LOW to RAS hold time (REAL-TIME READ-TRANSFER only)	tRTH	65	10,000	70	10,000	80	10,000	ns	
TR/(OE) LOW to CAS hold time (REAL-TIME READ-TRANSFER only)	tCTH	25		25		25		ns	
TR/(OE) HIGH to SC lead time	tTSL	5		5		5		ns	
TR/(OE) HIGH to RAS precharge time	tTRP	50		60		70		ns	
TR/(OE) to precharge time	tTRW	20		20		30		ns	
First SC edge to TR/(OE) HIGH delay time	tTSD	15		15		15		ns	
Serial output buffer turn-off delay from RAS	tSDZ	7	40	7	40	7	40	ns	
SC to RAS setup time	tSRS	25		30		30		ns	
Serial data input to SE delay time	tSZE	0		0		0		ns	
Serial data input delay from RAS	tSDD	50		50		50		ns	
Serial data input to RAS delay time	tSZS	0		0		0		ns	
Serial-input-mode enable (SE) to RAS setup time	tESR	0		0		0		ns	
Serial-input-mode enable (SE) to RAS hold time	tREH	15		15		15		ns	
TR/(OE) HIGH to RAS setup time	tYS	0		0		0		ns	
TR/(OE) HIGH to RAS hold time	tYH	15		15		15		ns	
DSF to RAS setup time	tFSR	0		0		0		ns	
DSF to RAS hold time	tRFH	15		15		15		ns	
SC to QSF delay time	tSQD		30		30		30	ns	
SPLIT TRANSFER setup time	tSTS	25		30		30		ns	
SPLIT TRANSFER hold time	tSTH	0		0		0		ns	
RAS to QSF delay time	tRQD		75		75		75	ns	
DSF to RAS hold time	tFHR	45		60		65		ns	
DSF to CAS setup time	tFSC	0		0		0		ns	
DSF to CAS hold time	tCFH	15		15		20		ns	
TR/OE to QSF delay time	tTQD		25		25		25	ns	
CAS to QSF delay time	tCQD		35		35		35	ns	
RAS to first SC delay	tRSD	80		80		80		ns	
CAS to first SC delay	tCSD	30		30		30		ns	

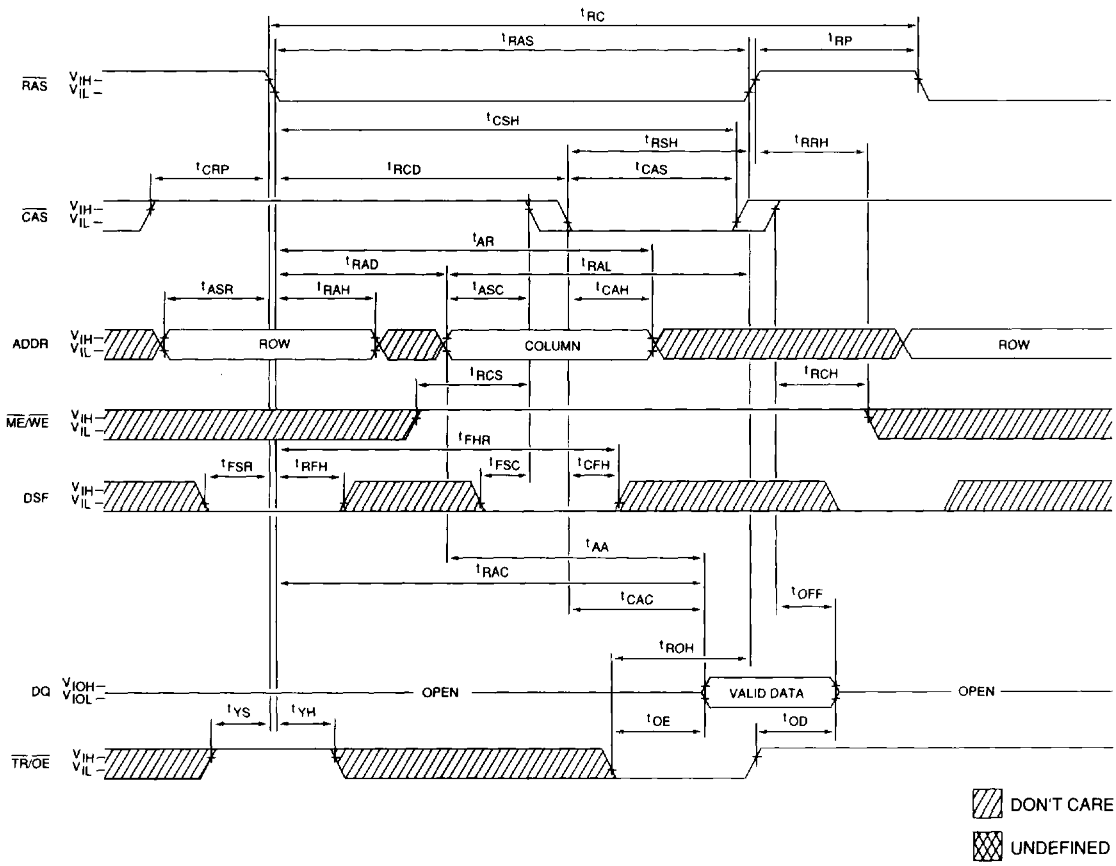
SAM TIMING PARAMETERS
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Serial clock cycle time	^tSC	25		30		30		ns	
Access time from SC	^tSAC		22		25		27	ns	24
SC precharge time (SC LOW time)	^tSP	8		10		10		ns	
SC pulse width (SC HIGH time)	^tSAS	8		10		10		ns	
Access time from $\overline{SE}$	^tSEA		15		15		15	ns	24
$\overline{SE}$ precharge time	^tSEP	20		20		20		ns	
$\overline{SE}$ pulse width	^tSE	20		20		20		ns	
Serial data-out hold time after SC high	^tSOH	5		5		5		ns	24
Serial output buffer turn-off delay from $\overline{SE}$	^tSEZ	3	12	3	12	3	12	ns	20, 24
Serial data-in setup time	^tSDS	0		0		0		ns	
Serial data-in hold time	^tSDH	10		10		10		ns	
Serial input (Write) Enable setup time	^tSWS	0		0		0		ns	
Serial input (Write) Enable hold time	^tSWH	15		15		15		ns	
Serial input (Write) disable setup time	^tSWIS	0		0		0		ns	
Serial input (Write) disable hold time	^tSWIH	15		15		15		ns	

NOTES

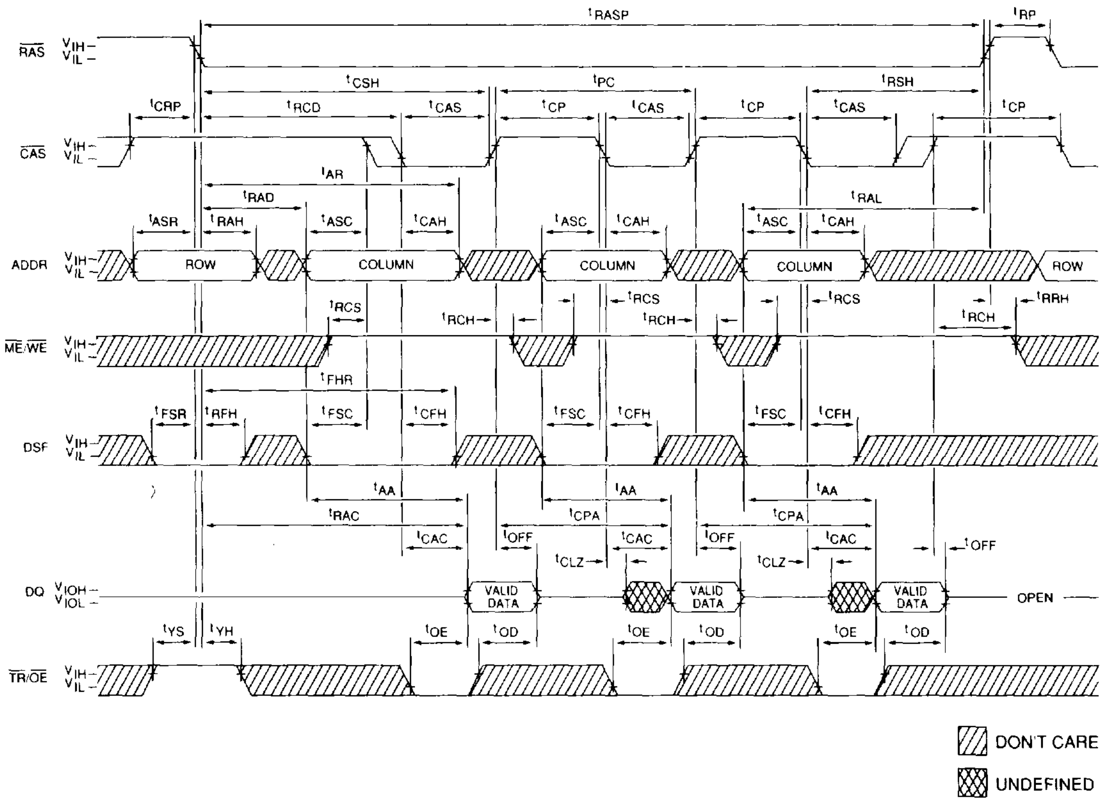
1. All voltages referenced to Vss.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on I/O loading. Specified values are obtained with minimum cycle time and the I/Os open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}). Input signals transition between 0V and 3V for AC testing.
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, DRAM data output (DQ1-DQ8) is High-Z.
12. If $\overline{CAS}$ = V_{IL}, DRAM data output (DQ1-DQ8) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to 1 TTL gate and 50pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OD, ^{t}OFF and ^{t}SEZ define the time when the output achieves open circuit (V_{OH} -200mV, V_{OL} +200mV). This parameter is sampled and not 100% tested.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If ^{t}WCS ≤ ^{t}WCS (MIN), the cycle is a LATE-WRITE and $\overline{TR}/\overline{OE}$ must control the output buffers during the write to avoid data contention. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of the output buffers (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate but the WRITE will be valid, if ^{t}OD and ^{t}OEH are met. See the LATE-WRITE AC Timing diagram.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{ME}/\overline{WE}$ leading edge in LATE-WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW then taken HIGH, DQ goes open. The DQs will go open with $\overline{OE}$ or $\overline{CAS}$, whichever goes HIGH first.
24. SAM output timing is measured with a load equivalent to 1 TTL gate and 30pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
25. LATE-WRITE and READ-MODIFY-WRITE cycles must have ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken LOW after ^{t}OEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
26. Address (A0-A8) may be changed two times or less while $\overline{RAS}$ = V_{IL}.
27. Address (A0-A8) may be changed once or less while $\overline{CAS}$ = V_{IH} and $\overline{RAS}$ = V_{IL}.
28. ^{t}SAC is MAX at 70° C and 4.5V Vcc; ^{t}SOH is MIN at 0°C and 5.5V Vcc. These limits will not occur simultaneously at any given voltage or temperature ^{t}SOH = ^{t}SAC - output transition time, this is guaranteed by design.
29. Values in parenthesis apply to the "L" version.

DRAM READ CYCLE



MULTIPORT DRAM

DRAM FAST-PAGE-MODE READ CYCLE



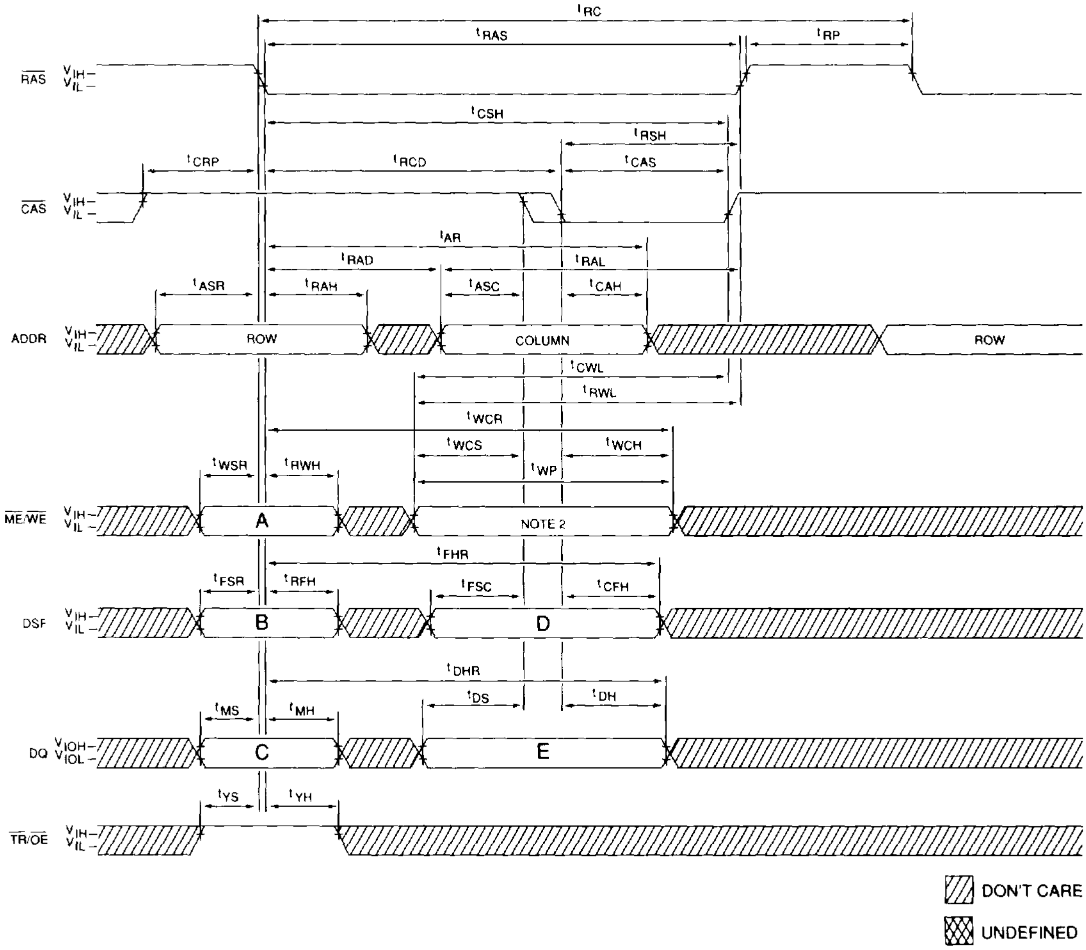
NOTE: WRITE cycles or READ-MODIFY-WRITE cycles may be mixed with READ cycles while in FAST PAGE MODE.

WRITE CYCLE FUNCTION TABLE [1]

FUNCTION	LOGIC STATES				
	RAS Falling Edge			CAS Falling Edge	
	A ME/WE	B DSF	C DQ (Input)	D DSF	E[2] DQ (Input)
Normal DRAM WRITE (or READ)	1	0	X	0	DRAM Data
NONPERSISTENT (Load and Use) MASKED WRITE to DRAM	0	0	Write Mask	0	DRAM Data (Masked)
PERSISTENT (Use Register) MASKED WRITE to DRAM	0	1	X	0	DRAM Data (Masked)
BLOCK WRITE to DRAM (No Data Mask)	1	0	X	1	Column Mask[3]
NONPERSISTENT (Load and Use) MASKED BLOCK WRITE to DRAM	0	0	Write Mask	1	Column Mask[3]
PERSISTENT (Use Register) MASKED BLOCK WRITE to DRAM	0	1	X	1	Column Mask[3]
Load Mask Register	1	1	X	0	Write Mask
Load Color Register	1	1	X	1	Color Data

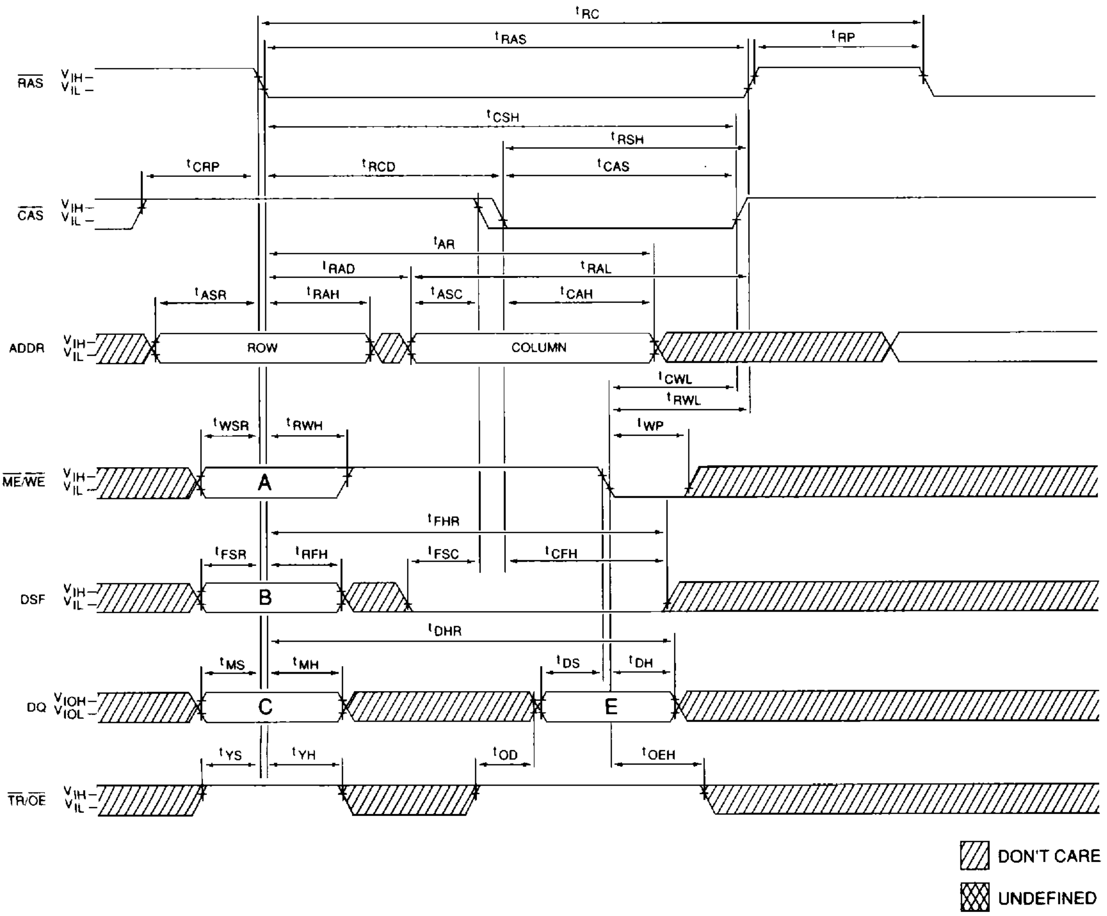
NOTE:
1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for the WRITE cycle timing diagrams on the following pages.
2. CAS or ME/WE, whichever occurs later (except for BLOCK WRITE).
3. WE = "don't care" for BLOCK WRITE. The DQ column-mask data will be latched at the falling edge of CAS, regardless of the state of ME/WE.

DRAM EARLY-WRITE CYCLE [1]



NOTE:
1. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.
2. For BLOCK WRITE, $\overline{ME}/\overline{WE}$ = "don't care." For all other EARLY-WRITE cycles, $\overline{ME}/\overline{WE}$ = LOW.

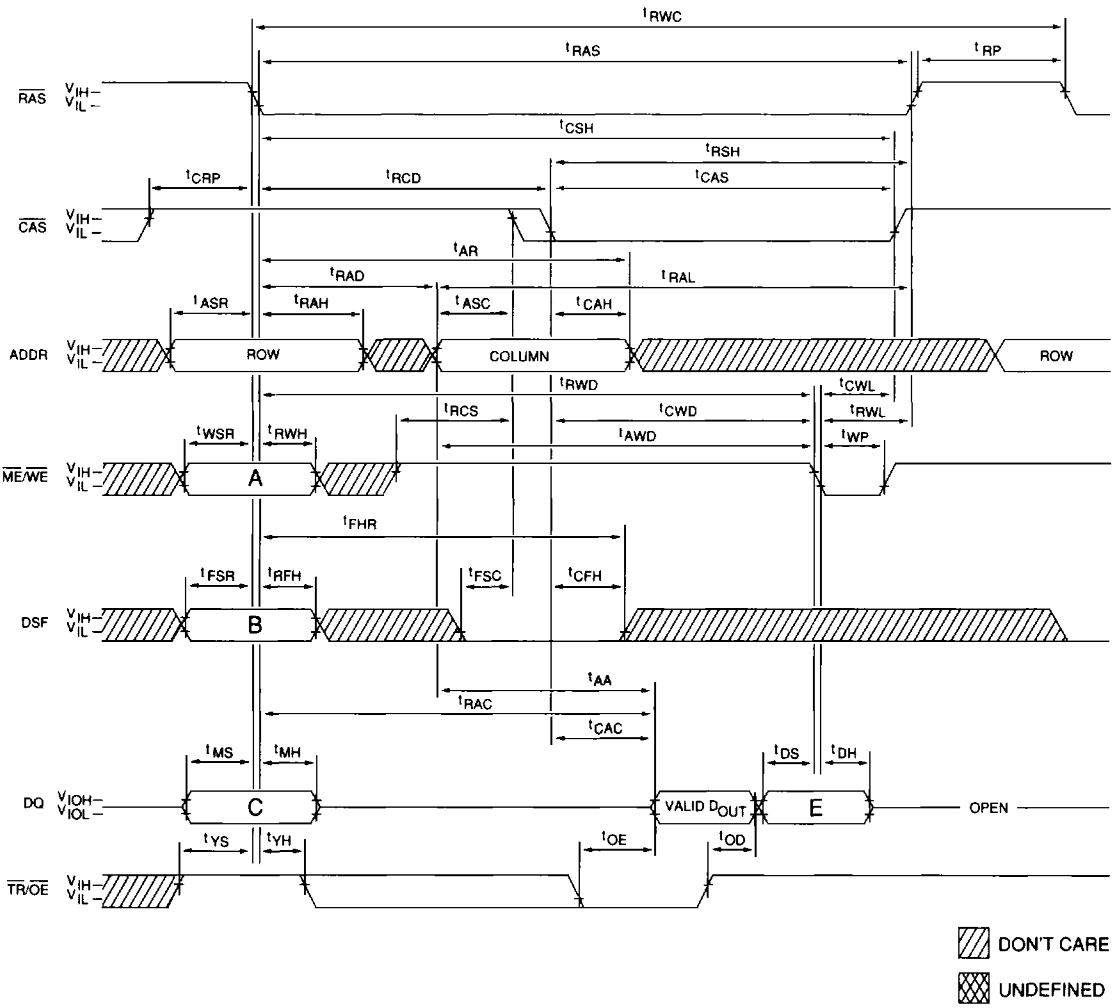
DRAM LATE-WRITE CYCLE



NOTE: The logic states of "A", "B", "C" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

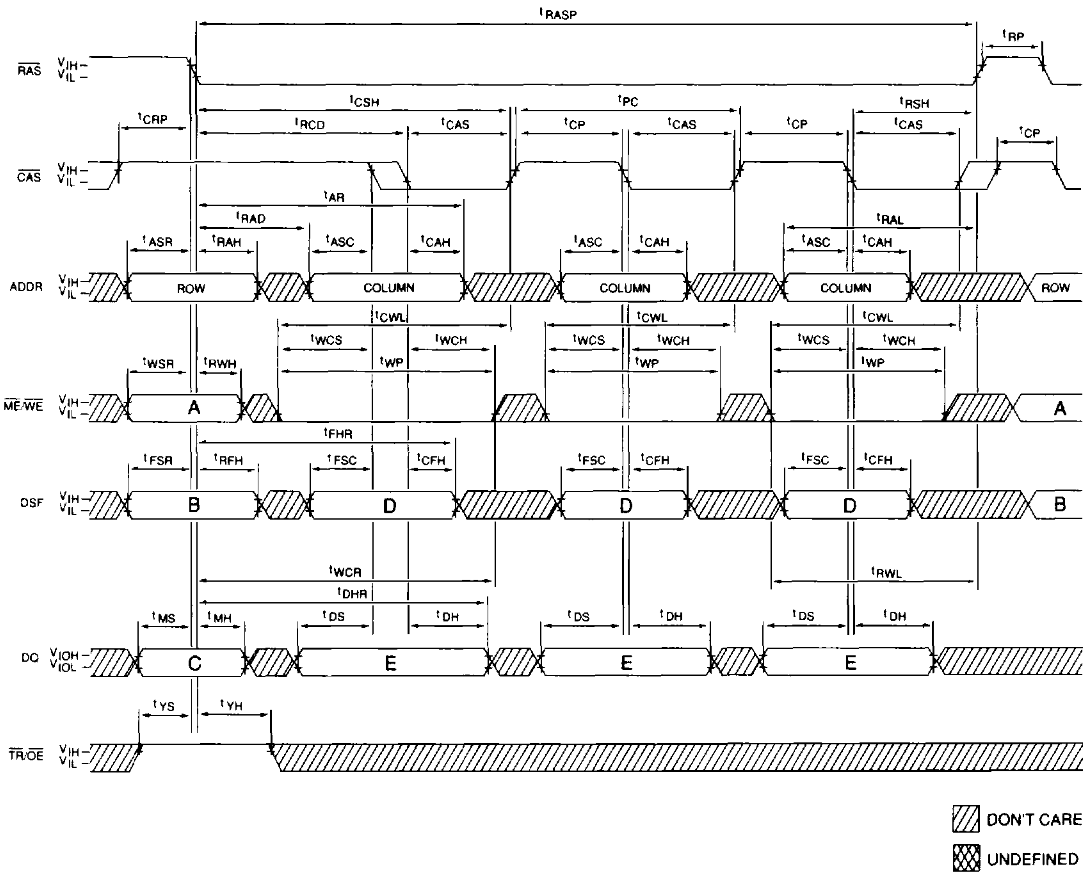
MULTIPORT DRAM

DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



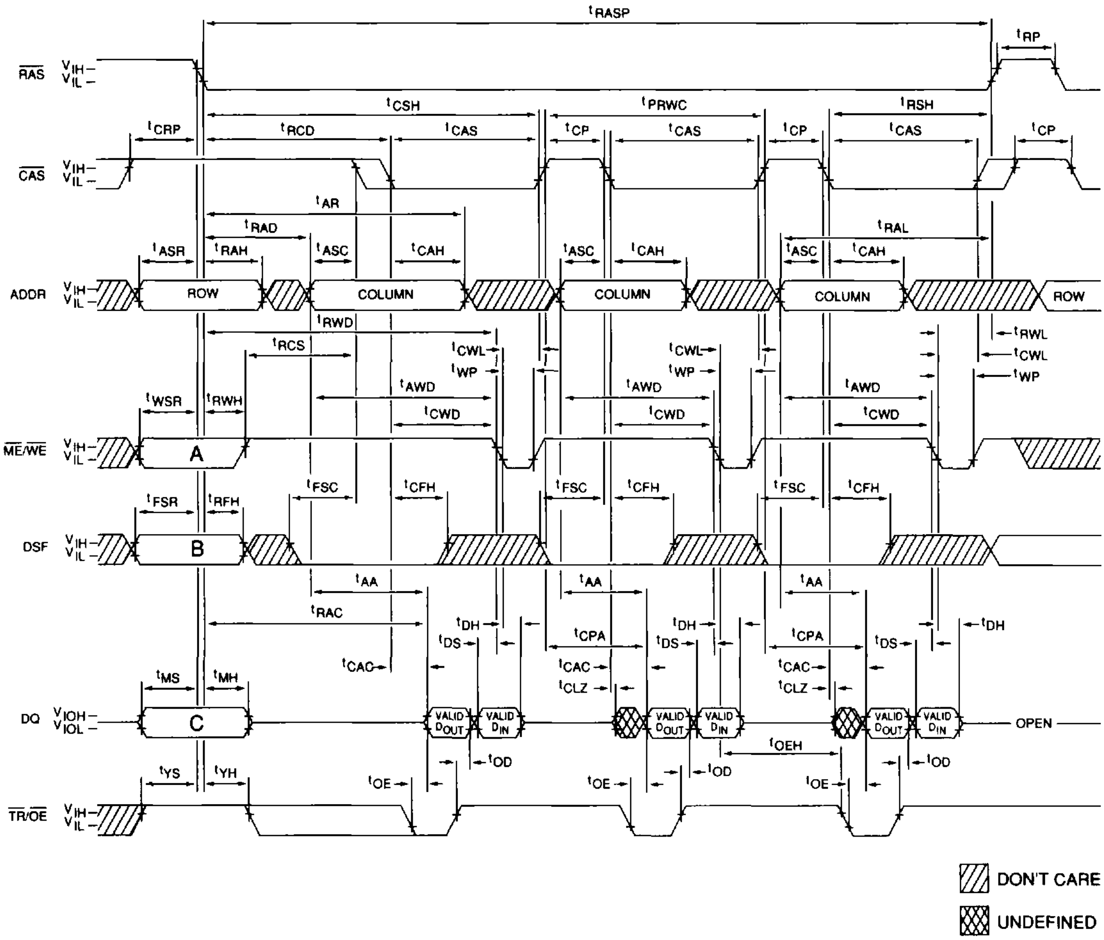
NOTE: The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE



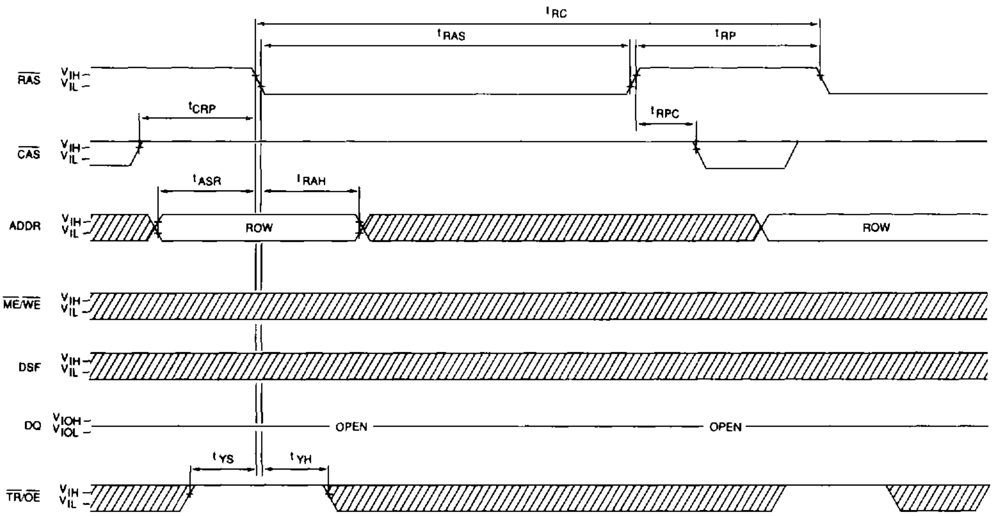
NOTE:
1. READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in FAST PAGE MODE.
2. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE READ-WRITE CYCLE
(READ-MODIFY-WRITE OR LATE-WRITE CYCLES)

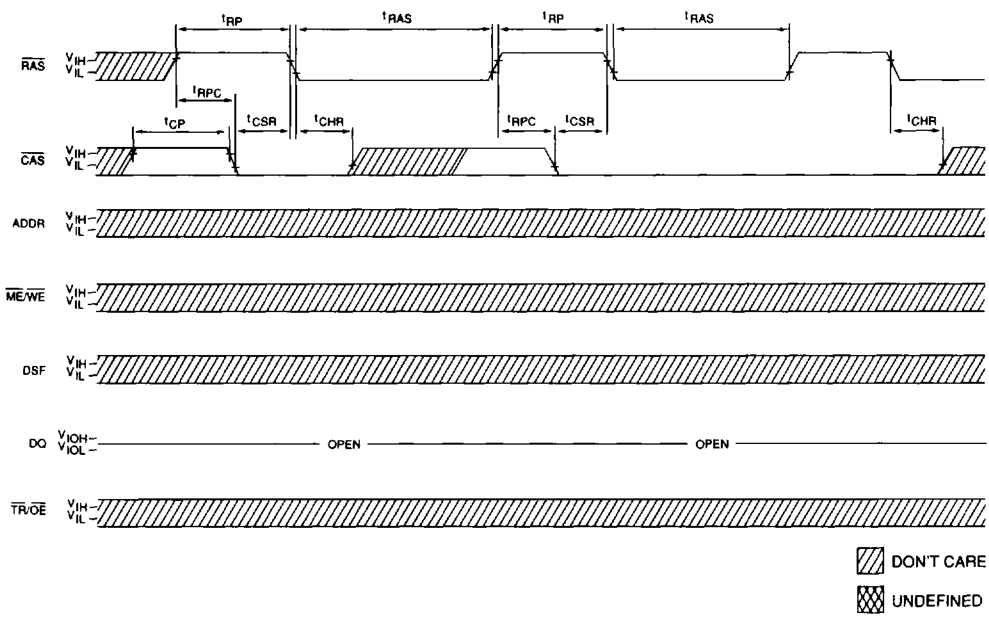


NOTE:
1. READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in FAST PAGE MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.
2. The logic states of "A", "B" and "C" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM $\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8)

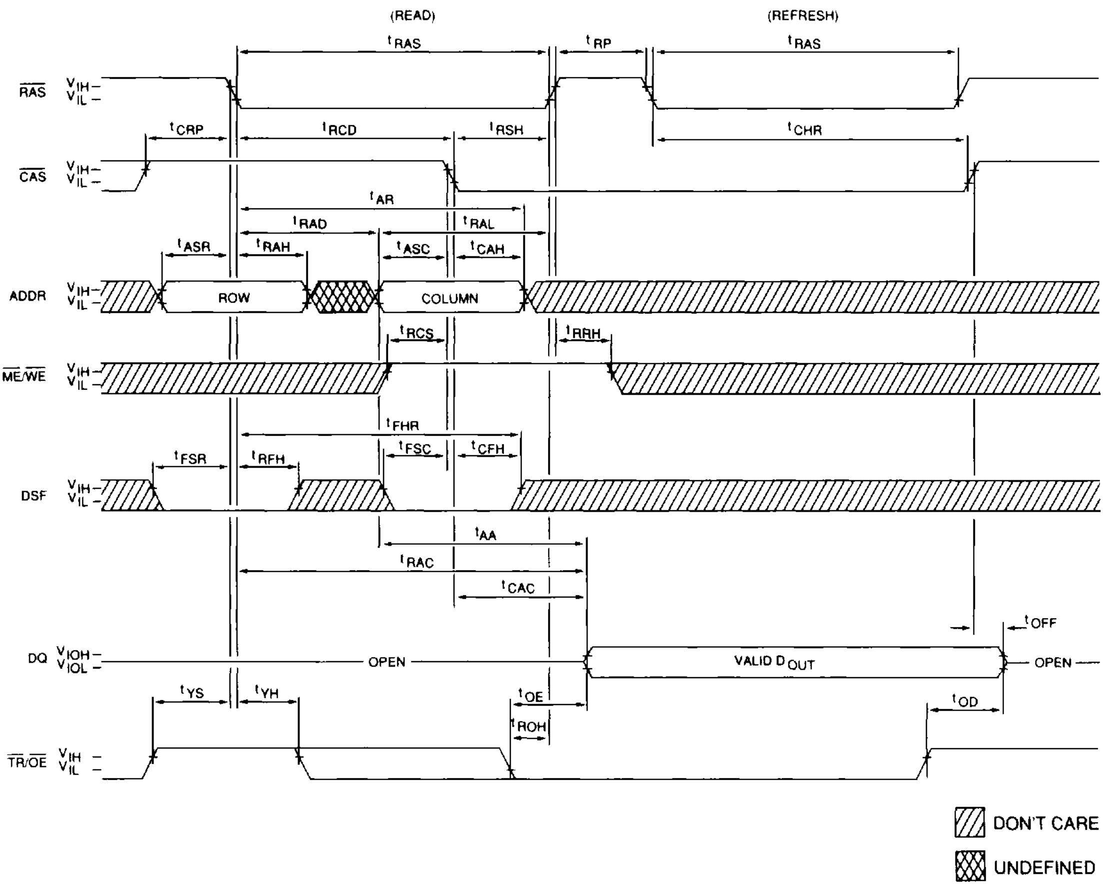


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



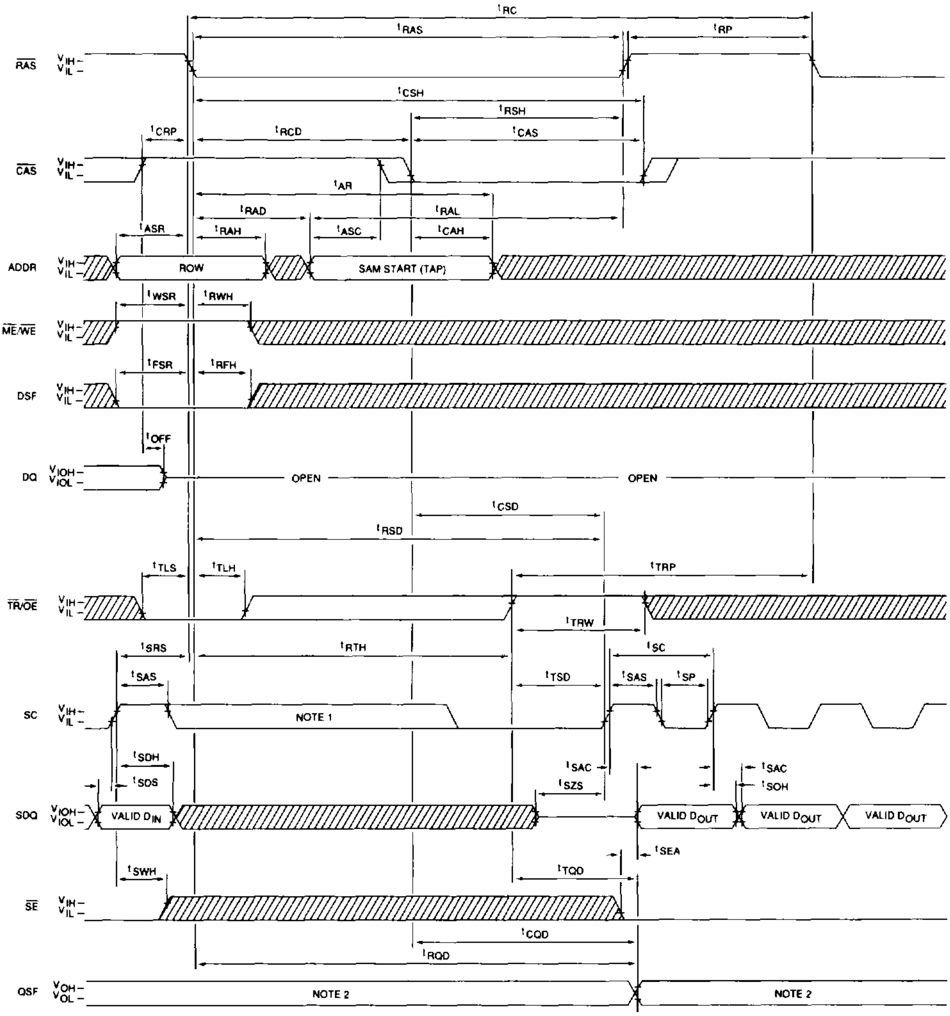
MULTIPORT DRAM

DRAM HIDDEN-REFRESH CYCLE



NOTE: A HIDDEN REFRESH may also be performed after a WRITE or TRANSFER cycle. In the WRITE case, $\overline{ME}/\overline{WE}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}/\overline{OE}$ = HIGH and the DQ pins stay High-Z. In the TRANSFER case, $\overline{TR}/\overline{OE}$ = LOW (when $\overline{RAS}$ goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of $\overline{TR}/\overline{OE}$.

READ TRANSFER 3
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL INPUT mode or SC idle)

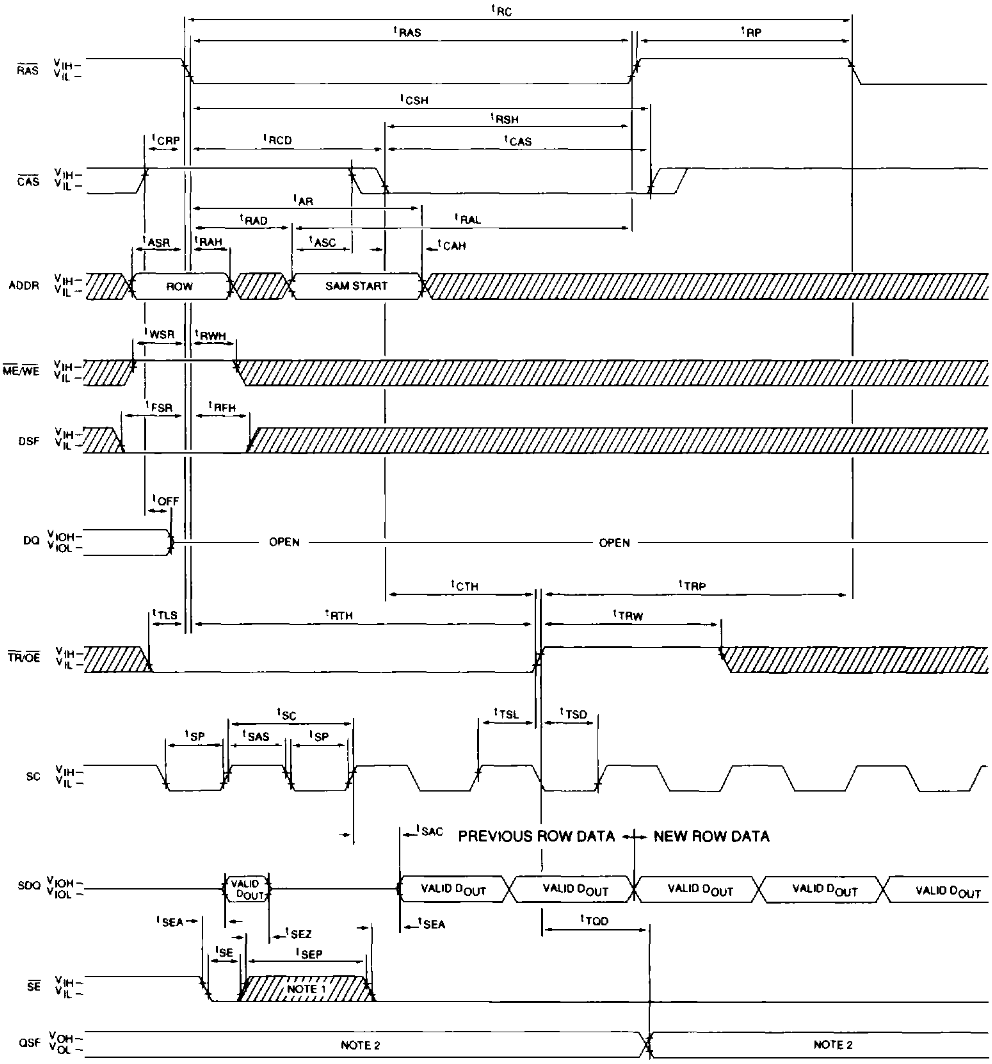


DON'T CARE
UNDEFINED

NOTE: 1. There must be no rising edges on the SC input during this time period.
2. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
QSF = 1 when the Upper SAM (bits 128–255) is being accessed.
3. If ᵗTLH is timing for the $\overline{TR}/(\overline{OE})$ rising edge, the transfer is self-timed and the ᵗCSD and ᵗRSD times must be met. If ᵗRTH is timing for the $\overline{TR}/(\overline{OE})$ rising edge, the transfer is done off of the $\overline{TR}/(\overline{OE})$ rising edge and ᵗTSD must be met.

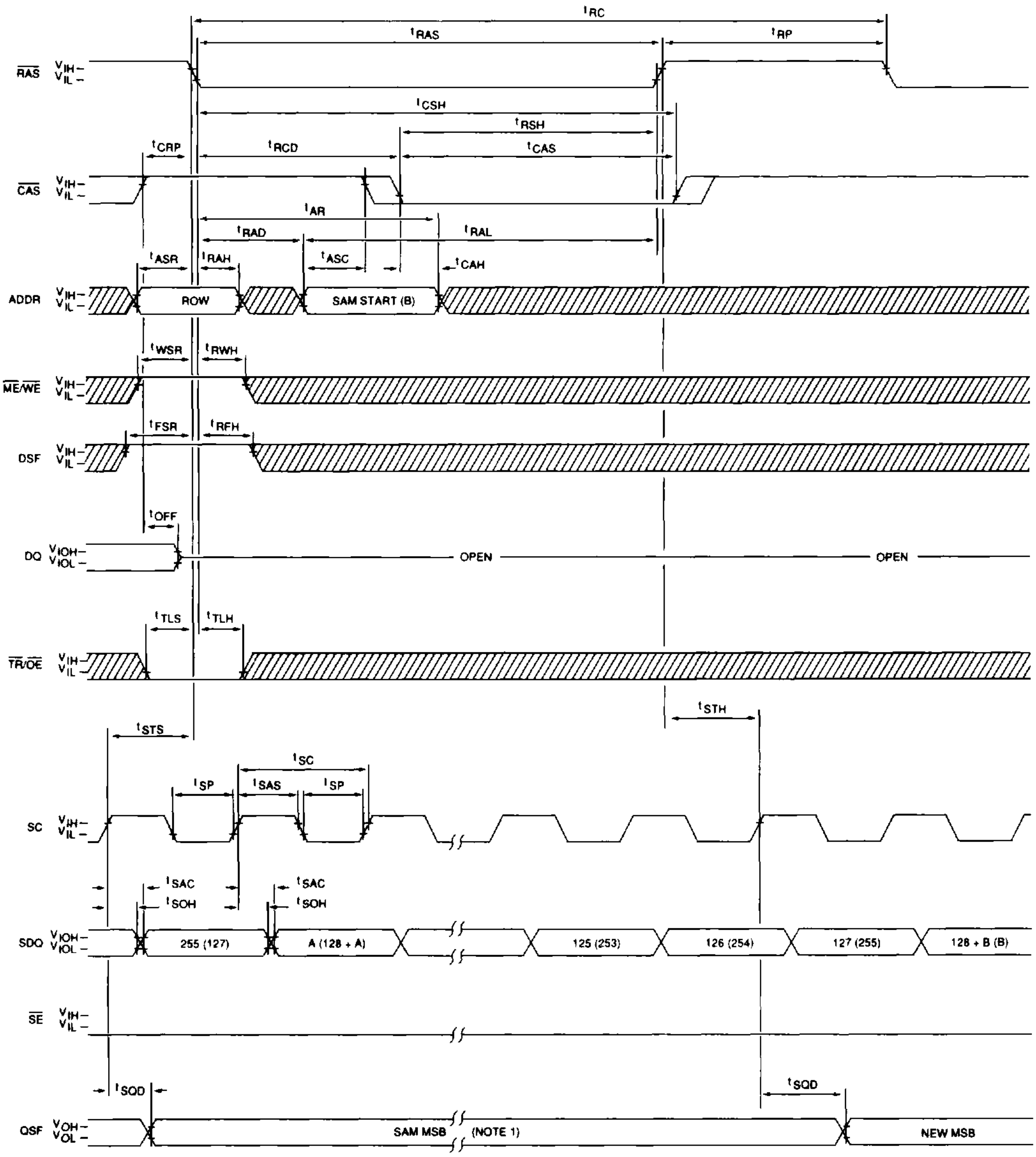
REAL-TIME READ TRANSFER (DRAM-TO-SAM TRANSFER)

(When part was previously in the SERIAL OUTPUT mode)



NOTE:
1. The $\overline{SE}$ pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.
2. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

SPLIT READ TRANSFER
(SPLIT DRAM-TO-SAM TRANSFER)

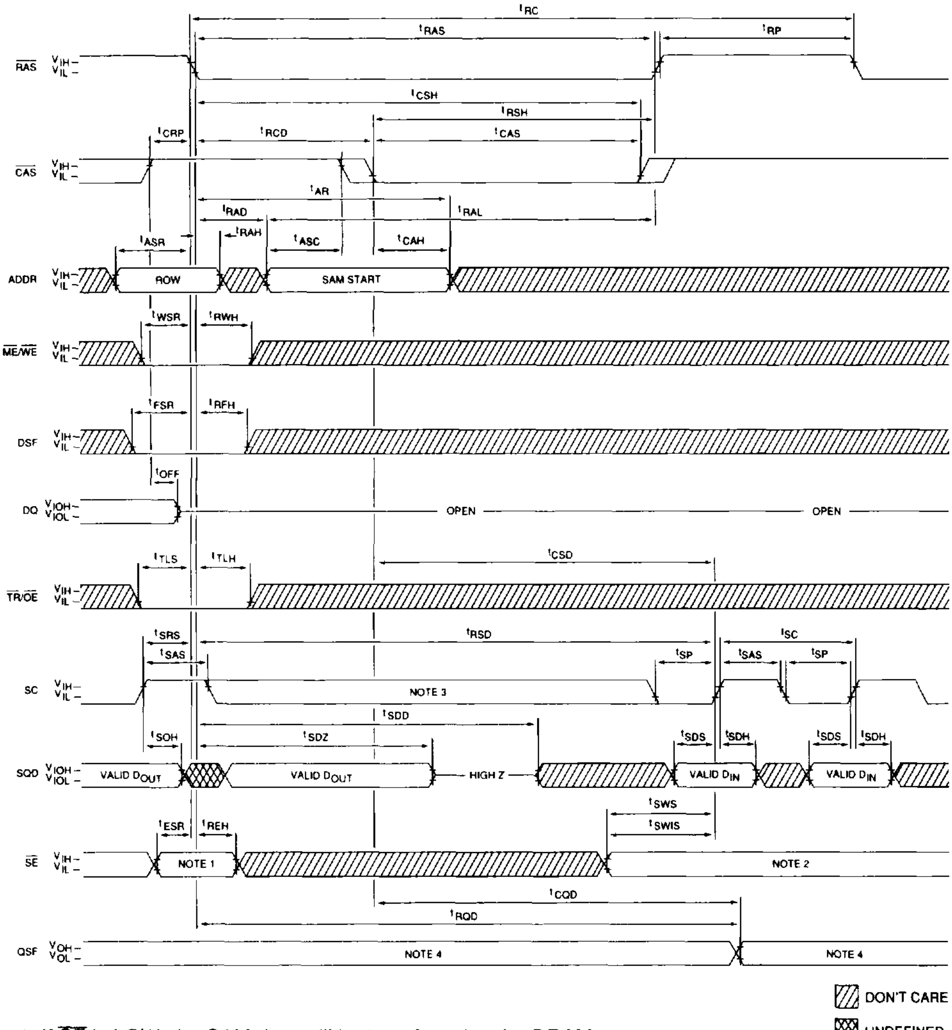


NOTE: 1. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

MULTIPORT DRAM

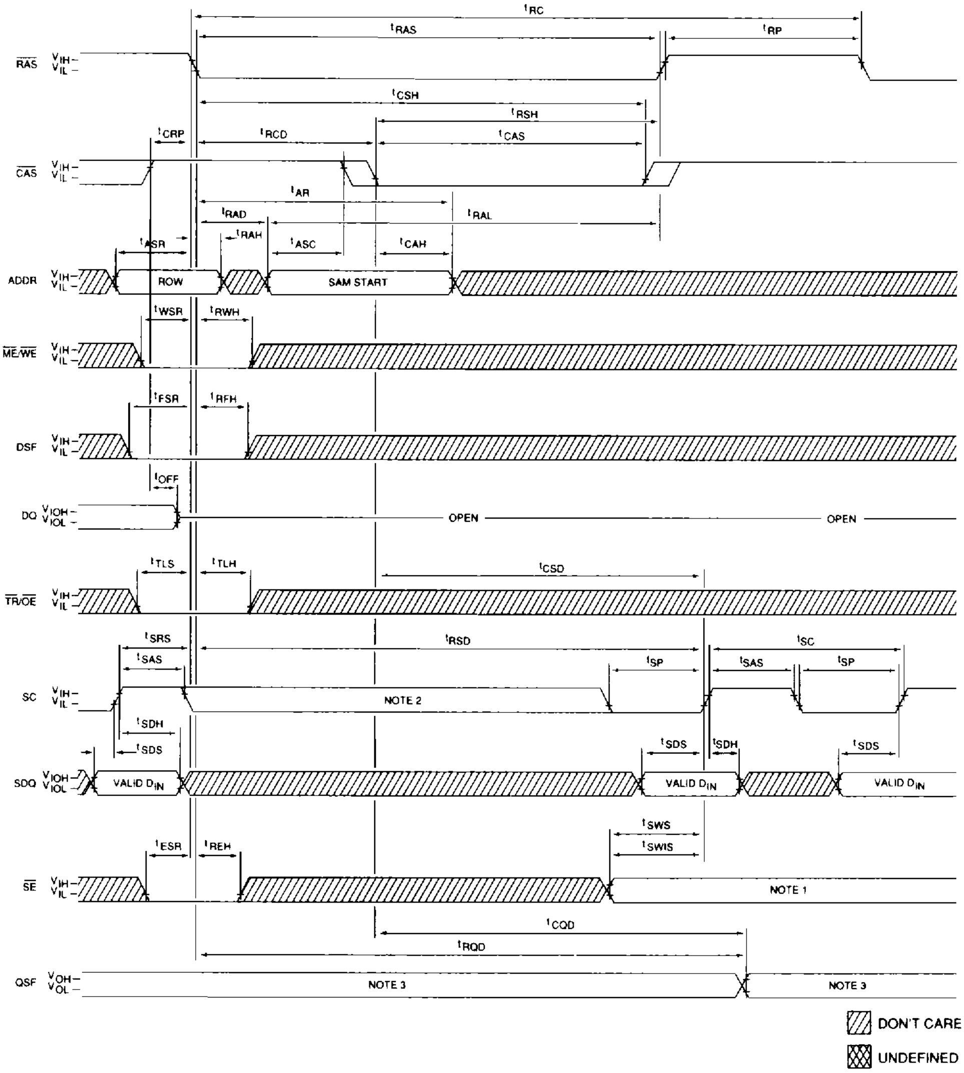
WRITE TRANSFER and PSEUDO WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

(When part was previously in the SERIAL OUTPUT mode)



NOTE:
1. If $\overline{SE}$ is LOW, the SAM data will be transferred to the DRAM. If $\overline{SE}$ is HIGH, the SAM data will not be transferred to the DRAM (SERIAL-INPUT-MODE ENABLE cycle).
2. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
3. There must be no rising edges on the SC input during this time period.
4. QSF = 0 when the Lower SAM (bits 0–127) is being accessed. QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

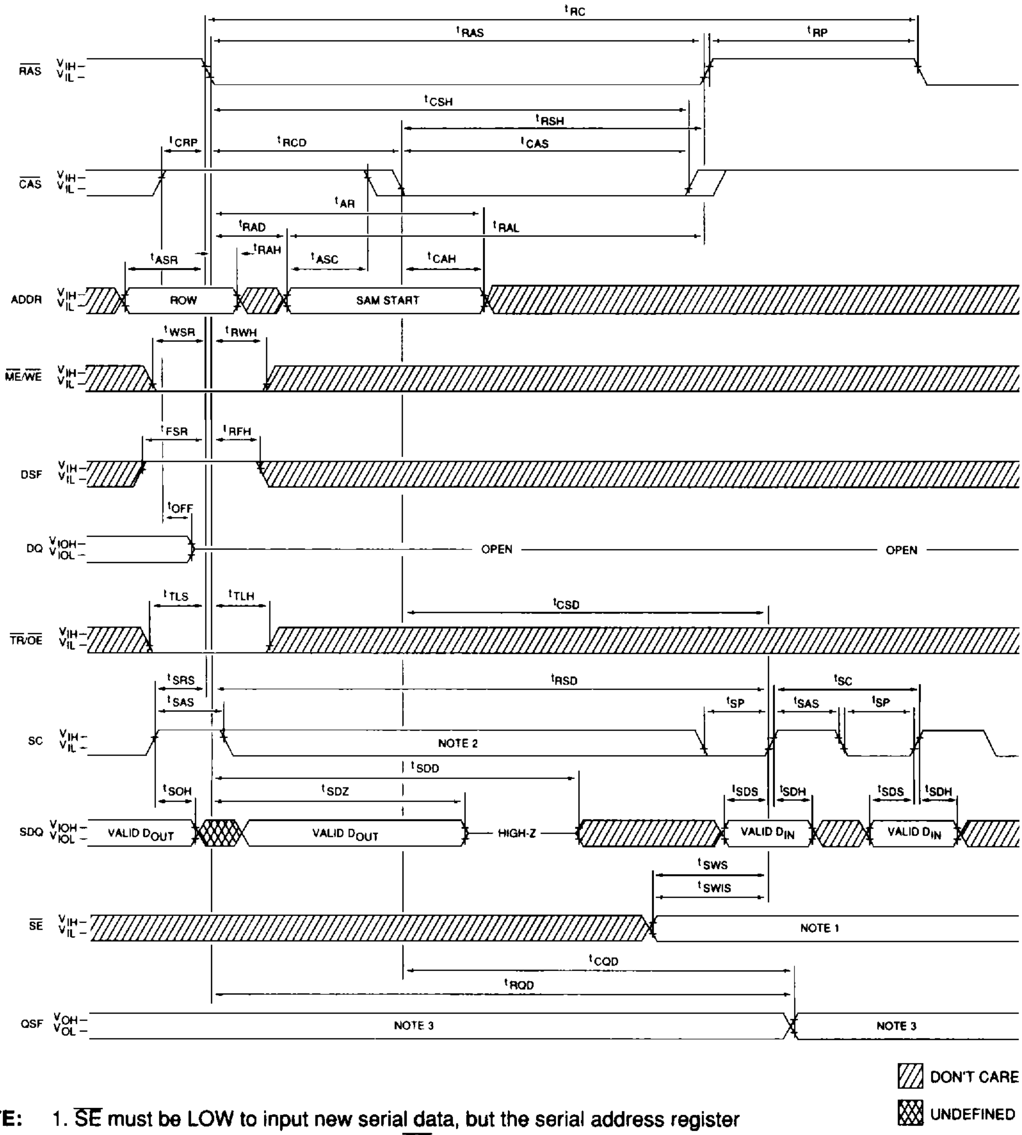
WRITE TRANSFER
(SAM-TO-DRAM TRANSFER)
(When part was previously in the SERIAL INPUT mode)



NOTE:
1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

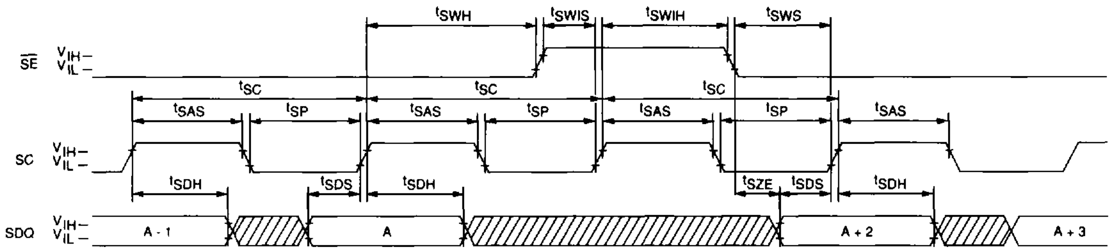
MULTIPORT DRAM

ALTERNATE WRITE TRANSFER
(SAM-TO-DRAM TRANSFER)

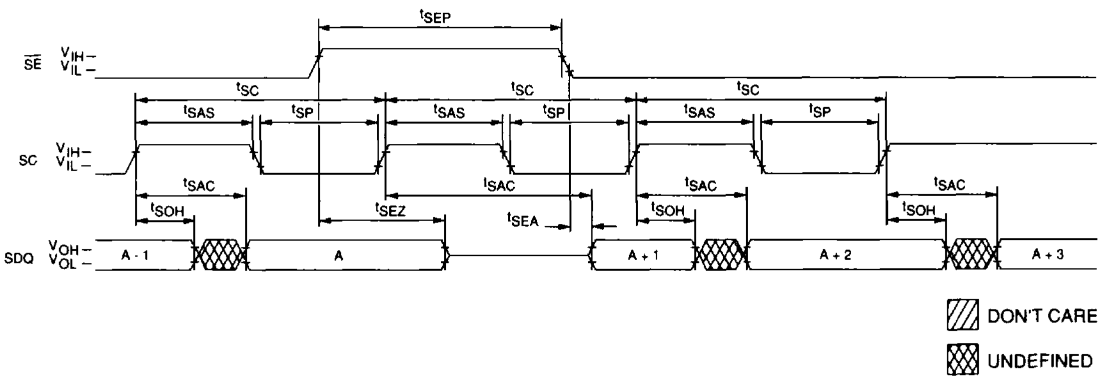


NOTE:
1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

SAM SERIAL INPUT



SAM SERIAL OUTPUT



MULTIPORT DRAM