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Mosaic Semiconductor Inc.

512K X 8 EEPROM

ME8512SC-15/20

Issue 1.3 : April 1993

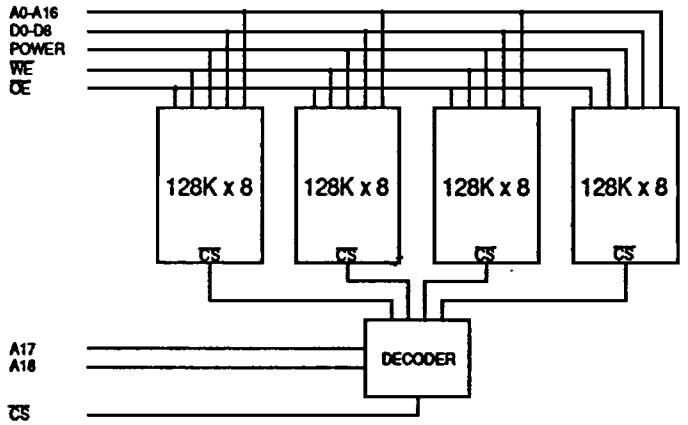
ADVANCE PRODUCT INFORMATION

524,288x 8 CMOS EEPROM

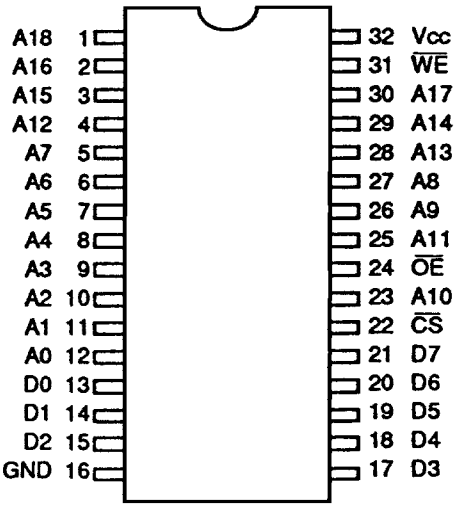
Features

Very Fast Access Times of 150/200 ns
JEDEC 4M EEPROM Standard 32 pin DIL footprint
Operating Power 350 mW (max)
Standby Power 11 mW (max)
Hardware and Software Data Protection
Byte and Page Write Cycle: 10ms
$\overline{\text{DATA}}$ Polling for End of Write Detection
10^4 Erase/Write cycles & 10 year Data Retention
Completely Static Operation
May be Processed to MIL-STD-883, Method 5004

Block Diagram



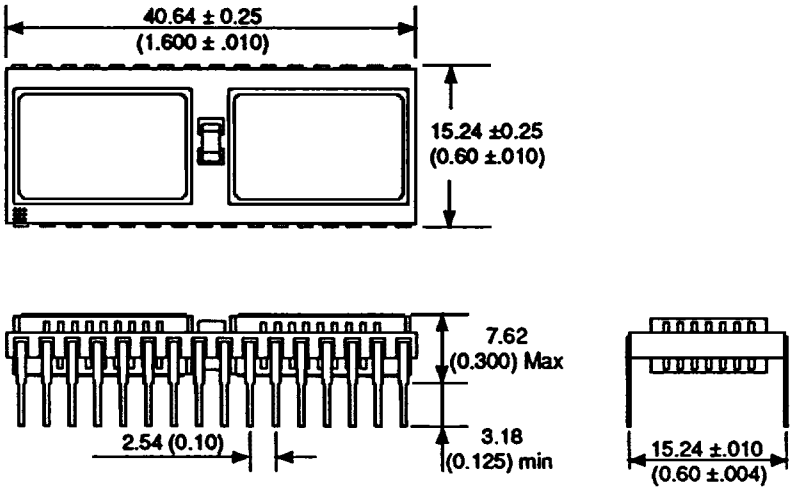
Pin Definition



Pin Functions

A0-A18	Address Inputs
D0-D7	Data Input/Output
$\overline{\text{CS}}$	Chip Select
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
NC	No Connect
V_{CC}	Power (+5V)
GND	Ground

Package Details Dimensions in mm (inches).



MOSCS021

Absolute Maximum Ratings

Voltage on any pin relative to GND	V_T	-1.0 to +7.0	V
Power Dissipation	P_T	1	W
Storage Temperature	T_{STG}	-65 to +150	°C
Temperature Under Bias	T_{BAS}	-55 to +125	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

		min	*typ*	*max*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+1	V
Input Low Voltage	V_{IL}	-0.1	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AL}	-40	-	85	°C (ME8512SCI)
	T_{AM}	-55	-	125	°C (ME8512SCM,MB)

DC Electrical Characteristics

Parameter	*Symbol*	*Test Condition*	*min*	*max*	*Unit*
Input Leakage Current	I_{LI1}	$0V \le V_{IN} \le V_{CC}$	-	40	µA
Output Leakage Current	I_{LO}	$\overline{CS}=V_{IH}$, $V_{I/O}$=GND to V_{CC}	-	40	µA
Average Current	I_{CC1}	f=5 MHz, $I_{I/O}$=0mA	-	64	mA
Standby Current	I_{SB}	TTL Levels	-	14	mA
Standby Current	I_{SB1}	CMOS Levels	-	2	mA
Output Voltage	V_{OL}	I_{OL}= 2.1mA	-	0.4	V
	V_{OH}	I_{OH}=-400 µA	2.4	-	V

Capacitance (V_{CC}=5V±10%,T_A=25°C, f=1MHz)

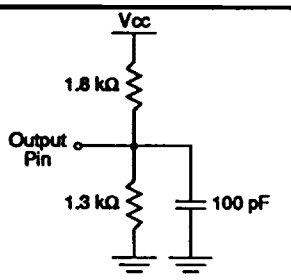
Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance ($\overline{CS}$, A15, A16)	C_{IN1}	V_{IN} = 0V	-	10	pF
($\overline{WE}$, $\overline{OE}$,A0-14)	C_{IN2}	V_{IN} = 0V	-	40	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	-	40	pF

Note: Capacitance calculated, not measured.

AC Test Conditions

- Input pulse levels: 0V to 3.0V
- Input rise and fall times: 10ns
- Input and Output timing reference levels: 1.5V
- Output load: 1 TTL gate + 100pF
- V_{CC}=5V±10%

Output Test Load



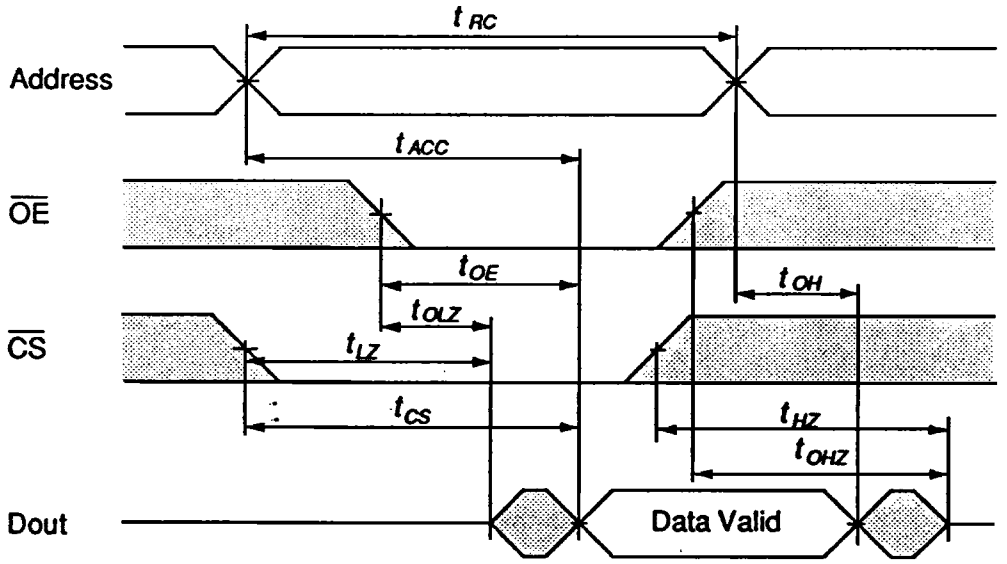
AC READ CHARACTERISTICS

Read Cycle

Parameter	Symbol	-15 min	-15 max	-20 min	-20 max	Unit	Notes
Read Cycle Time	t_{RC}	150	-	200	-	ns	
Address to Output Delay	t_{ACC}	-	150	-	200	ns	
$\overline{CS}$ to Output Delay	t_{CS}	-	150	-	200	ns	
$\overline{OE}$ to Output Delay	t_{OE}	-	50	-	50	ns	
$\overline{CS}$,$\overline{OE}$ High to High Z Output	t_{HZ},t_{OHZ}	-	50	-	50	ns	2
$\overline{CS}$,$\overline{OE}$ Low to Active Output	t_{LZ},t_{OLZ}	0	-	0	-	ns	2

Notes: (1) t_{HZ} and t_{OHZ} are specified from $\overline{OE}$ or $\overline{CS}$ whichever occurs first (C_L = 5pF).
(2) This parameter is only sampled and is not 100% tested.

Read Cycle Timing Waveform

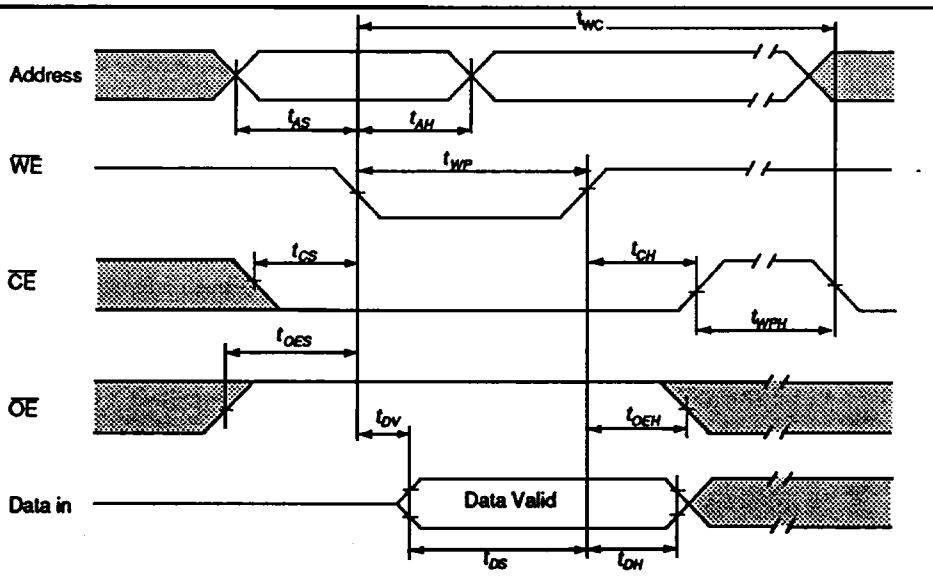


AC WRITE CHARACTERISTICS

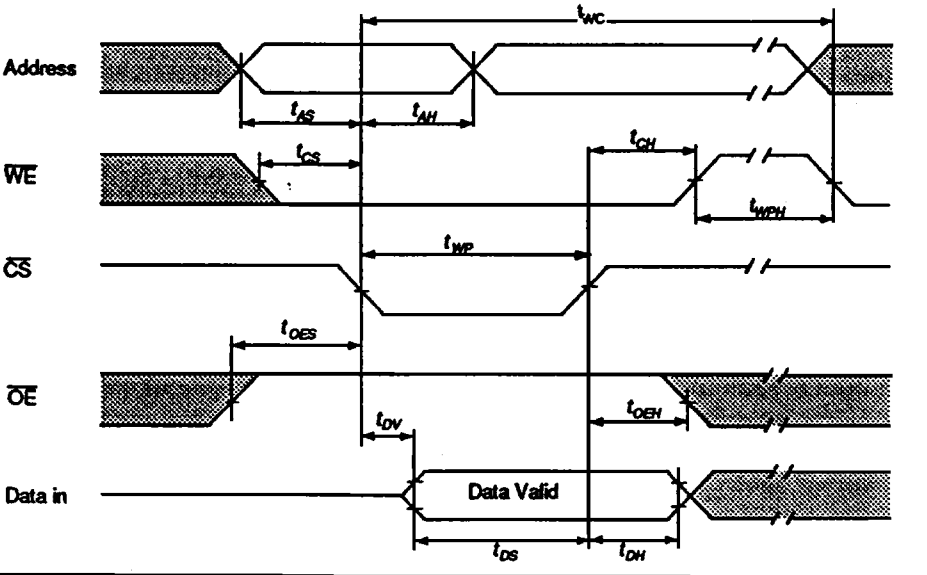
Write Cycle

Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Address Set-up Time	t_{AS}	0	-	-	ns
Address Hold Time	t_{AH}	50	-	-	ns
Chip Select Set-up Time	t_{CS}	0	-	-	ns
Chip Select Hold Time	t_{CH}	0	-	-	ns
Write Pulse Width ($\overline{WE}$ or $\overline{CS}$)	t_{WP}	100	-	-	ns
Data Set-up Time	t_{DS}	50	-	-	ns
Data Hold Time	t_{DH}	10	-	-	ns
Time to Data Valid	t_{DV}	-	-	1	µs
Write Cycle Time	t_{WC}	-	-	10	ms
Write Pulse Width High	t_{WPH}	100	-	-	ns
$\overline{OE}$ Set-up Time	t_{OES}	10	-	-	ns
$\overline{OE}$ Hold Time	t_{OEH}	10	-	-	ns

AC Write Waveform - $\overline{WE}$ Controlled



AC Write Waveform - $\overline{CS}$ Controlled

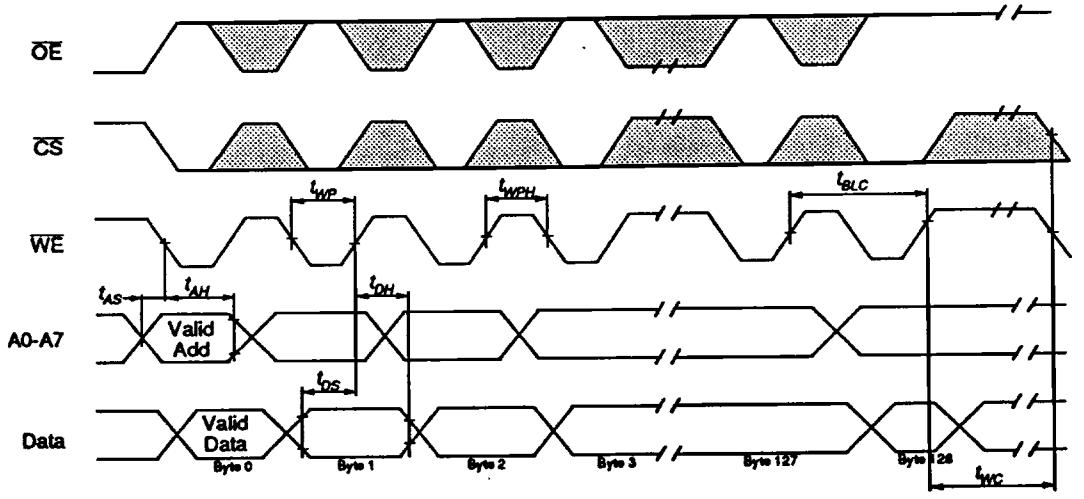


PAGE MODE WRITE CHARACTERISTICS

Write Cycle

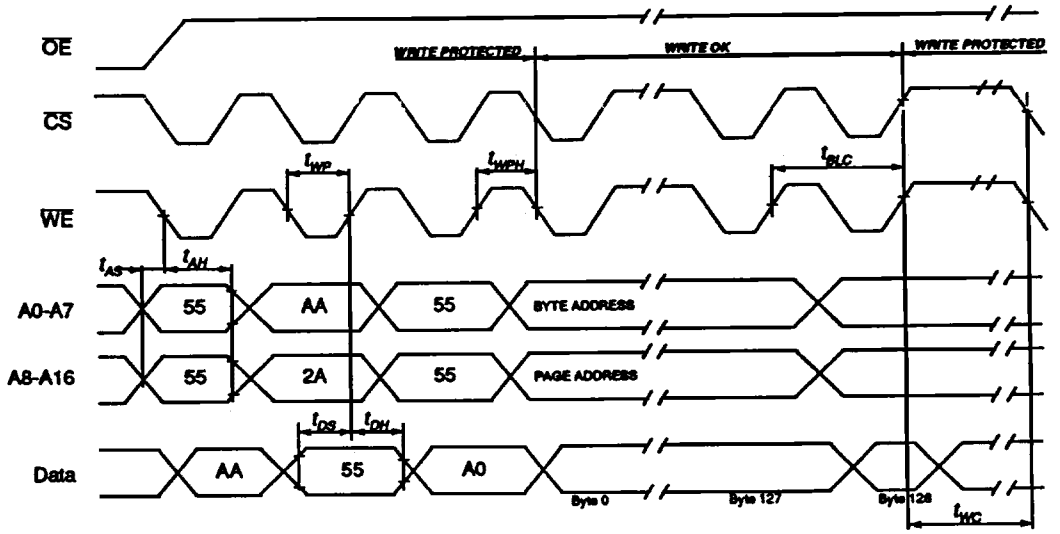
Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Write Cycle Time	t_{WC}	-	-	10	ms
Address Set-up Time	t_{AS}	0	-	-	ns
Address Hold Time	t_{AH}	50	-	-	ns
Data Set-up Time	t_{DS}	50	-	-	ns
Data Hold Time	t_{DH}	10	-	-	ns
Write Pulse Width	t_{WP}	100	-	-	ns
Byte Load Cycle Time	t_{BLC}	0.2	-	100	µs
Write Pulse Width High	t_{WPH}	100	-	-	ns

Page Mode Write Waveform



Note: A8 through A16 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CS}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CS}$ are both low.

Software Protected Write Waveform



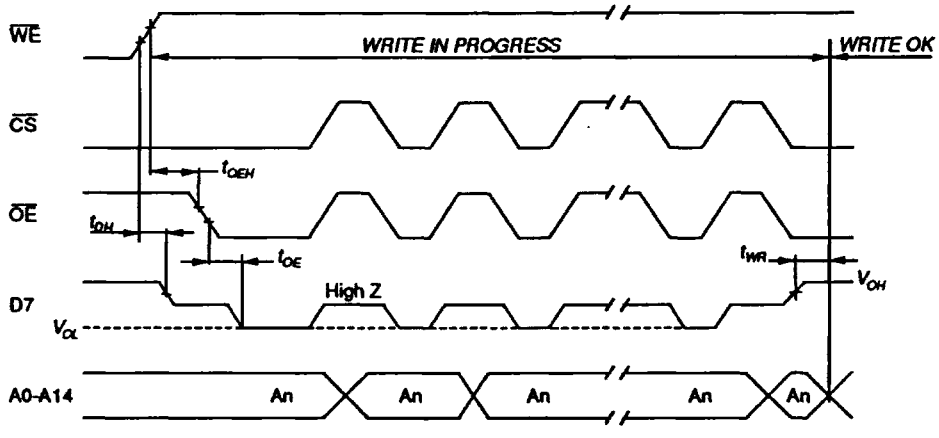
Note: A8 through A16 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CS}$).
The example addresses above are for EEPROM 1 on the module - see page 8 for full details.
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CS}$ are both low.

$\overline{\text{DATA}}$ Polling Characteristics (1)

Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Data Hold Time	t_{DH}	10	-	-	ns
$\overline{\text{OE}}$ Hold Time	t_{OEH}	0	-	-	ns
$\overline{\text{OE}}$ to Output Delay	t_{OE}	-	-	100	ns
Write Recovery Time	t_{WR}	0	-	-	ns

Note : (1) These parameters are sampled and not 100% tested.

$\overline{\text{DATA}}$ Polling Waveform

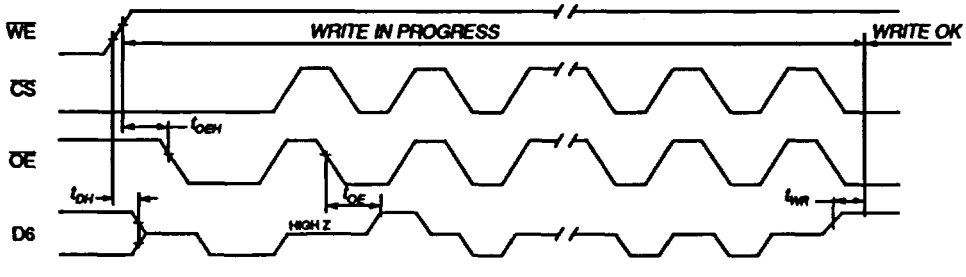


Toggle Bit Characteristics (1)

Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Data Hold Time	t_{DH}	10	-	-	ns
$\overline{\text{OE}}$ Hold Time	t_{OEH}	10	-	-	ns
$\overline{\text{OE}}$ to Output Delay	t_{OE}	-	-	100	ns
Write Recovery Time	t_{WR}	0	-	-	ns

Note : (1) These parameters are sampled and not 100% tested.

Toggle Bit Waveform



Notes : (1) Toggling either $\overline{\text{OE}}$ or $\overline{\text{CS}}$ or both $\overline{\text{OE}}$ and $\overline{\text{CS}}$ will operate toggle bit.
(2) Beginning and ending state of D6 may vary.
(3) Any address location may be used but the address should not vary.

DEVICE OPERATION

Read

The ME8512SC is accessed in the same way as a static RAM, with the data stored at the memory location determined by the address being placed on the output pins when $\overline{CS}$ and $\overline{OE}$ are low, and $\overline{WE}$ is high. Whenever $\overline{CS}$ or $\overline{OE}$ are high, the outputs are in the OFF or high impedance state.

Write

A low pulse on $\overline{WE}$ with $\overline{CS}$ low or a low pulse on $\overline{CS}$ with $\overline{WE}$ low indicates a Write Cycle. The address is latched on the falling edge of $\overline{CS}$ or $\overline{WE}$, and the data is latched on the first rising edge of $\overline{CS}$ or $\overline{WE}$. Once a Byte Write has begun it will automatically time itself to completion.

Page Mode Write

This mode allows 2 to 256 bytes of data to be loaded into an EEPROM, which are then simultaneously written. Once the first byte has been written, each subsequent byte must have the high to low transition of $\overline{WE}$ (or $\overline{CS}$) within 100µs of the same transition of the previous byte. If this 100µs time is exceeded, the load period ends and internal programming starts. A8 to A16 specify the page address (which must be valid during the above transitions) and A0 to A7 specify which bytes within the page are to be written. Note that the bytes may be loaded in any order and may be changed within the same load period.

Operating Modes

MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	*OUTPUTS*
Read	0	0	1	Data Out
Write (1)	0	I	0	Data in
Standby	1	X	X	Floating
Write Inhibit	X	X	1	
	X	0	X	
Output Disable	X	1	X	Floating
Chip Erase	0	V_H	0	Floating

1 = V_{IH} 0 = V_{IL} X = Don't care V_H = 12.0V±0.5V

DATA Polling

In order to detect the end of a Write Cycle, two methods are provided. During a Write operation (Byte or Page) an attempt to Read the device will result in the complement of the written data appearing on D7. Once the Write Cycle is complete true data appears on the outputs and the next Write Cycle may begin.

TOGGLE bit

In addition to DATA polling, another method is provided to determine the end of a Write Cycle. During a write operation successive attempts to read data will result in D6 toggling between 1 and 0. Once a write is complete, this toggling will stop and valid data will be read.

Hardware Data Protection

Four types of harware protection give high security against accidental writes:

(a) If V_{CC} < 3.8V write is inhibited

(b) At power on, the device times out 5ms before allowing a Write.

(c) $\overline{OE}$ low, $\overline{CS}$ or $\overline{WE}$ high inhibits writes.

(d) Pulses of less than 15ns on $\overline{WE}$ or $\overline{CS}$ do not initiate a write cycle.

Software Data Protection

Software controlled data protection, once enabled by the user, necessitates the use of a software algorithm before any Write can be performed. To enable this feature a special sequence of Writes must be performed, and must be reused for each subsequent Write cycle. Once set the data protection remains operational until it is disabled by using a second algorithm; power transitions will not reset this feature.

Note that the ME8512SC is supplied with the Software Data Protection feature **disabled.**

The ME8512SC consists of four 128K x 8 EEPROMs; which device is active at a particular time and $\overline{CS}$ inputs are controlled by address lines A17 and A18. The Memory Map of this module is arranged as follows:

EEPROM NUMBER	*ADDRESSING RANGE*	
	START	*END*
1	00000	1FFFF
2	20000	3FFFF
3	40000	5FFFF
4	60000	7FFFF

The Software Data Protection operation mode is available on a single device independent from the mode of the others e.g. one EEPROM could be protected while the others were not. However this situation is undesireable because the current mode of each EEPROM would have to be recorded during operation in order to avoid trying to Write to a device without first issuing the correct command codes.Because of this it is advisable that if this feature is to be used then all four devices on each module are either disabled or enabled at the same time. Software Data Protection Enable for any device can be achieved by using the following table:

ACTION PERFORMED	EEPROM NUMBER			
	1	2	3	4
LOAD DATA (1)	AA	AA	AA	AA
TO ADDRESS (1)	05555	25555	45555	65555
LOAD DATA	55	55	55	55
TO ADDRESS	02AAA	22AAA	42AAA	62AAA
LOAD DATA	A0	A0	A0	A0
TO ADDRESS	05555	25555	45555	65555
	WRITES ENABLED (2)			
LOAD DATA (3)	ANY	ANY	ANY	ANY
TO ADDRESS	ANY VALID FOR PAGE WRITE			
LOAD LAST DATA	ANY	ANY	ANY	ANY
TO LAST ADDRESS	ANY VALID FOR PAGE WRITE			
	ENTER DATA PROTECTED STATE			

Notes : (1) Data D7 - D0 (hex); Address A16 - A0 (hex).
(2) Write Protect Mode will be activated at end ofWrite even if no other data is loaded.
(3) 1 to 64 bytes of data may be loaded.

In order to enable Data Protection for the entire ME8512SC module, the sequence of three loads shown above must be performed for each EEPROM in turn, totalling 12 loads in all. Once activated, the same three bytes must be loaded to the same addresses before any Writes will occur to a particular device. **All software write commands must obey the Page Write timing specifications.**

The process of disabling the Data Protection mode is very similar to that described for enable, except 6 bytes must be loaded to specific locations for each EEPROM as shown in the table below:

ACTION PERFORMED	EEPROM NUMBER			
	1	2	3	4
LOAD DATA (1)	AA	AA	AA	AA
TO ADDRESS (1)	05555	25555	45555	65555
LOAD DATA	55	55	55	55
TO ADDRESS	02AAA	22AAA	42AAA	62AAA
LOAD DATA	80	80	80	80
TO ADDRESS	05555	25555	5556	65555
LOAD DATA	AA	AA	AA	AA
TO ADDRESS	06666	25555	45555	65555
LOAD DATA	55	55	55	55
TO ADDRESS	02AAA	22AAA	42AAA	62AAA
LOAD DATA	20	20	20	20
TO ADDRESS	06666	25666	45666	66666
	EXIT DATA PROTECTED STATE (2)			
LOAD DATA (3)	ANY	ANY	ANY	ANY
TO ADDRESS	ANY VALID FOR PAGE WRITE			
LOAD LAST DATA	ANY	ANY	ANY	ANY
TO LAST ADDRESS	ANY VALID FOR PAGE WRITE			

Notes : (1) Data D7 - D0 (hex); Address A16 - A0 (hex).
(2) Write Protect Mode will be activated at end of Write even if no other data is loaded.
(3) 1 to 64 bytes of data may be loaded.

Thus, to disable the Software Data Protection mode for the module 24 bytes have to be loaded.

Note here the use of the word 'load' to describe enabling and disabling the protection modes is in preference to write'. Although it may seem that if the Write command sequence is performed to enable protection then the three bytes at those addresses will be overwritten with AA,55,A0, this is not the case. This is because these Writes obey Page Write parameters, where A8 - A16 must remain valid to specify the page address, but during this enable sequence they change. Actual Writes therefore never occur, and data is not corrupted during an enable sequence.

For the same reasons no Writes are performed during the disable routine, in addition to the fact that since Data Protection is enabled no Writes can occur without the correct bytes being loaded in sequence.

Ordering Information

ME8512SCMB-15

Speed	15	= 150 ns
	20	= 200 ns
Temp. range/screening	Blank	= Commercial Temp.
	I	= Industrial Temp.
	M	= Military Temp.
	MB	= Processed to MIL-STD-883 Method 5004, non-compliant
Package	SC	= 32 Pin 600 mil Ceramic DIP

The policy of the company is one of continuous development and while the information presented in this data sheet is believed to be accurate, no liability is assumed for any data contained within. The company reserves the right to make changes without notice at any time.

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