

1M x 16Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 1,048,576 x 16 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage (+5.0V or +3.3V), refresh cycle (1K Ref. or 4K Ref.), access time (-5 or -6), power consumption(Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ -only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in L-version. This 1Mx16 Fast Page Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as graphic memory unit for microcomputer, personal computer and portable machines.

FEATURES

• Part Identification

- KM416C1000C/C-L (5V, 4K Ref.)
- KM416C1200C/C-L (5V, 1K Ref.)
- KM416V1000C/C-L (3.3V, 4K Ref.)
- KM416V1200C/C-L (3.3V, 1K Ref.)

• Active Power Dissipation

Unit : mW

Speed	3.3V		5V	
	4K	1K	4K	1K
-5	324	504	495	770
-6	288	468	440	715

• Refresh Cycles

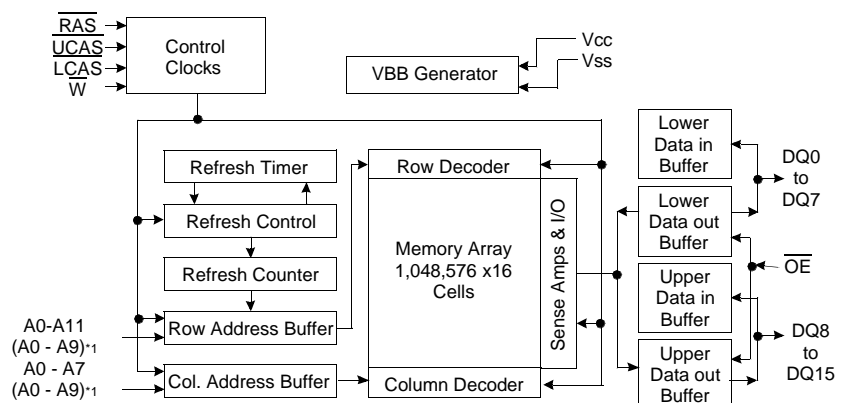
Part NO.	VCC	Refresh cycle	Refresh period	
			Normal	L-ver
C1000C	5V	4K	64ms	128ms
V1000C	3.3V			
C1200C	5V	1K	16ms	
V1200C	3.3V			

• Performance Range

Speed	t _{TRAC}	t _{CAC}	t _{RC}	t _{PC}	Remark
-5	50ns	15ns	90ns	35ns	5V/3.3V
-6	60ns	15ns	110ns	40ns	5V/3.3V

- Fast Page Mode operation
- 2 $\overline{\text{CAS}}$ Byte/Word Read/Write operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL(5V)/LVTTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in 42-pin SOJ 400mil and 50(44)-pin TSOP(II) 400mil packages
- Single +5V±10% power supply (5V product)
- Single +3.3V±0.3V power supply (3.3V product)

FUNCTIONAL BLOCK DIAGRAM



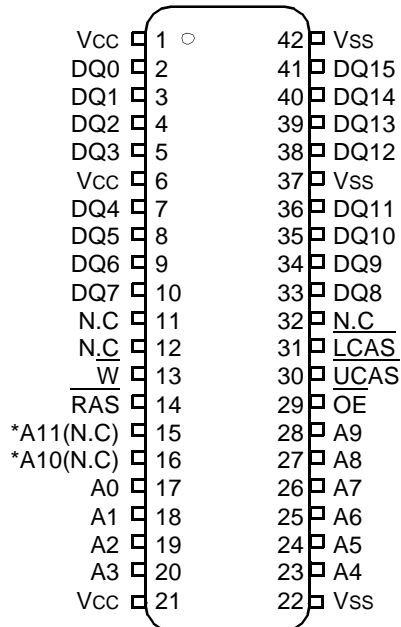
Note) *1 : 1K Refresh

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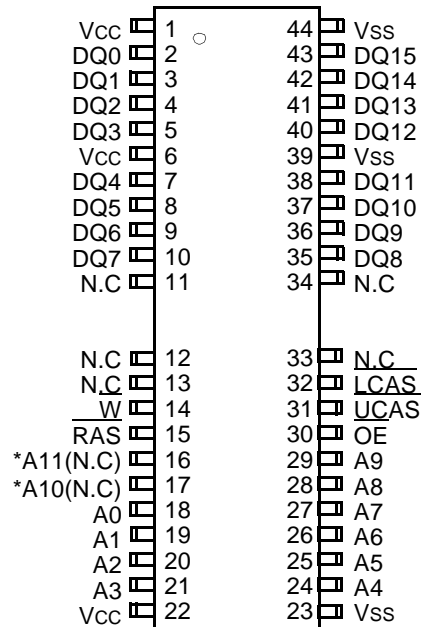


PIN CONFIGURATION (Top Views)

• KM416C/V10(2)00CJ



• KM416C/V10(2)00CT



*A10 and A11 are N.C for KM416C/V1200C(5V/3.3V, 1K Ref. product)

J : 400mil 42 SOJ
T : 400mil 50(44) TSOP II

Pin Name	Pin Function
A0 - A11	Address Inputs (4K Product)
A0 - A9	Address Inputs (1K Product)
DQ0 - 15	Data In/Out
Vss	Ground
RAS	Row Address Strobe
UCAS	Upper Column Address Strobe
LCAS	Lower Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
Vcc	Power(+5V)
	Power(+3.3V)
N.C	No Connection

KM416C1000C, KM416C1200C KM416V1000C, KM416V1200C

CMOS DRAM

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to Vss	V _{IN} ,V _{OUT}	-0.5 to +4.6	-1.0 to +7.0	V
Voltage on Vcc supply relative to Vss	V _{CC}	-0.5 to +4.6	-1.0 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	-55 to +150	°C
Power Dissipation	P _D	1	1	W
Short Circuit Output Current	I _{OS} Address	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A= 0 to 70°C)

Parameter	Symbol	3.3V			5V			Units
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V _{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} +0.3* ¹	2.4	-	V _{CC} +1.0* ¹	V
Input Low Voltage	V _{IL}	-0.3* ²	-	0.8	-1.0* ²	-	0.8	V

*1 : V_{CC}+1.3V/15ns(3.3V), V_{CC}+2.0V/20ns(5V), Pulse width is measured at V_{CC}

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at V_{SS}

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Max	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V _{IN} ≤V _{IN} +0.3V, all other input pins not under test=0 Volt)	I _{I(L)}	-5	5	uA
	Output Leakage Current (Data out is disabled, 0V≤V _{OUT} ≤V _{CC})	I _{O(L)}	-5	5	uA
	Output High Voltage Level(I _{OH} =-2mA)	V _{OH}	2.4	-	V
	Output Low Voltage Level(I _{OL} =2mA)	V _{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V _{IN} ≤V _{IN} +0.5V, all other input pins not under test=0 Volt)	I _{I(L)}	-5	5	uA
	Output Leakage Current (Data out is disabled, 0V≤V _{OUT} ≤V _{CC})	I _{O(L)}	-5	5	uA
	Output High Voltage Level(I _{OH} =-5mA)	V _{OH}	2.4	-	V
	Output Low Voltage Level(I _{OL} =4.2mA)	V _{OL}	-	0.4	V



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CMOS DRAM

DC AND OPERATING CHARACTERISTICS (Continued)

Symbol	Power	Speed	Max				Units
			KM416V1000C	KM416V1200C	KM416C1000C	KM416C1200C	
I _{CC1}	Don't care	-5	90	140	90	140	mA
		-6	80	130	80	130	
I _{CC2}	Normal L	Don't care	1	1	2	2	mA
			1	1	1	1	
I _{CC3}	Don't care	-5	90	140	90	140	mA
		-6	80	130	80	130	
I _{CC4}	Don't care	-5	90	90	90	90	mA
		-6	80	80	80	80	
I _{CC5}	Normal L	Don't care	0.5	0.5	1	1	mA
			200	200	200	200	
I _{CC6}	Don't care	-5	90	140	90	140	mA
		-6	80	130	80	130	
I _{CC7}	L	Don't care	300	200	350	250	uA
I _{CCS}	L	Don't care	150	150	200	200	uA

I_{CC1}* : Operating Current ($\overline{\text{RAS}}$ and $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$ cycling @t_{RC}=min.)

I_{CC2} : Standby Current ($\overline{\text{RAS}}=\overline{\text{UCAS}}=\overline{\text{LCAS}}=\overline{\text{W}}=\text{V}_{\text{IH}}$)

I_{CC3}* : RAS-only Refresh Current ($\overline{\text{UCAS}}=\overline{\text{LCAS}}=\text{V}_{\text{IH}}$, $\overline{\text{RAS}}$ cycling @t_{RC}=min.)

I_{CC4}* : Fast Page Mode Current ($\overline{\text{RAS}}=\text{V}_{\text{IL}}$, $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$, Address cycling @t_{PC}=min.)

I_{CC5} : Standby Current ($\overline{\text{RAS}}=\overline{\text{UCAS}}=\overline{\text{LCAS}}=\overline{\text{W}}=\text{V}_{\text{CC}}-0.2\text{V}$)

I_{CC6}* : CAS-Before-RAS Refresh Current ($\overline{\text{RAS}}$, $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ cycling @t_{RC}=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}=0.2\text{V}$,

DQ=Don't care, T_{RC}=31.25us(4K/L-ver), 125us(1K/L-ver),

T_{RA}S=T_{RA}S_{min}~300ns

I_{CCS} : Self Refresh Current

$\overline{\text{RAS}}=\overline{\text{UCAS}}=\overline{\text{LCAS}}=\text{V}_{\text{IL}}$, $\overline{\text{W}}=\overline{\text{OE}}=\text{A}0 \sim \text{A}11=\text{V}_{\text{CC}}-0.2\text{V}$ or 0.2V,

DQ0 ~ DQ15=V_{CC}-0.2V, 0.2V or Open

***Note** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3} and I_{CC6}, address can be changed maximum once while $\overline{\text{RAS}}=\text{V}_{\text{IL}}$. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time, t_{PC}.



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CMOS DRAM

CAPACITANCE (TA=25°C, VCC=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Units
Input capacitance [A0 ~ A11]	CIN1	-	5	pF
Input capacitance [$\overline{\text{RAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{W}}$, $\overline{\text{OE}}$]	CIN2	-	7	pF
Output capacitance [DQ0 - DQ15]	CDQ	-	7	pF

AC CHARACTERISTICS (0°C ≤ TA ≤ 70°C, See note 1,2)

Test condition (5V device) : VCC=5.0V±10%, VIH/VIL=2.4/0.8V, VOH/VOL=2.4/0.4V

Test condition (3.3V device) : VCC=3.3V±0.3V, VIH/VIL=2.2/0.7V, VOH/VOL=2.0/0.8V

Parameter	Symbol	-5		-6		Units	Notes
		Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		ns	
Read-modify-write cycle time	tRWC	133		155		ns	
Access time from $\overline{\text{RAS}}$	tRAC		50		60	ns	3,4,10
Access time from $\overline{\text{CAS}}$	tCAC		15		15	ns	3,4,5
Access time from column address	tAA		25		30	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	ns	6
Transition time (rise and fall)	tT	3	50	3	50	ns	2
$\overline{\text{RAS}}$ precharge time	tRP	30		40		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	50	10K	60	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	13		15		ns	
$\overline{\text{CAS}}$ hold time	tCSH	50		60		ns	
$\overline{\text{CAS}}$ pulse width	tCAS	13	10K	15	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	tRCD	20	37	20	45	ns	4
$\overline{\text{RAS}}$ to column address delay time	tRAD	15	25	15	30	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		ns	
Row address set-up time	tASR	0		0		ns	
Row address hold time	tRAH	10		10		ns	
Column address set-up time	tASC	0		0		ns	11
Column address hold time	tCAH	10		10		ns	11
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		ns	
Read command set-up time	tRCS	0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		ns	8
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		ns	8
Write command hold time	tWCH	10		10		ns	
Write command pulse width	tWP	10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	13		15		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	13		15		ns	



AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		Units	Notes
		Min	Max	Min	Max		
Data set-up time	tDS	0		0		ns	9,17
Data hold time	tDH	10		10		ns	9,17
Refresh period (1K, Normal)	tREF		16		16	ms	
Refresh period (4K, Normal)	tREF		64		64	ms	
Refresh period (L-ver)	tREF		128		128	ms	
Write command set-up time	twCS	0		0		ns	7
CAS to \overline{W} delay time	tcWD	36		40		ns	7,13
RAS to \overline{W} delay time	trWD	73		85		ns	7
Column address to \overline{W} delay time	tAWD	48		55		ns	7
CAS precharge to \overline{W} delay time	tcpWD	53		60		ns	7
CAS set-up time (CAS-before-RAS refresh)	tCSR	5		5		ns	15
CAS hold time (CAS-before-RAS refresh)	tCHR	10		10		ns	16
RAS to CAS precharge time	trPC	5		5		ns	
Access time from CAS precharge	tCPA		30		35	ns	3
Fast Page mode cycle time	tPC	35		40		ns	
Fast Page read-modify-write cycle time	tPRWC	76		80		ns	
CAS precharge time (Fast Page cycle)	tCP	10		10		ns	12
RAS pulse width (Fast Page cycle)	trASP	50	200K	60	200K	ns	
RAS hold time from CAS precharge	trHCP	30		35		ns	
\overline{OE} access time	toEA		13		15	ns	3
\overline{OE} to data delay	toED	13		15		ns	
Output buffer turn off delay time from \overline{OE}	toEZ	0	13	0	15	ns	
\overline{OE} command hold time	toEH	13		15		ns	
RAS pulse width (\overline{C} -B- \overline{R} self refresh)	trASS	100		100		us	18,19,20
RAS precharge time (\overline{C} -B- \overline{R} self refresh)	trPS	90		110		ns	18,19,20
CAS hold time (\overline{C} -B- \overline{R} self refresh)	tCHS	-50		-50		ns	18,19,20

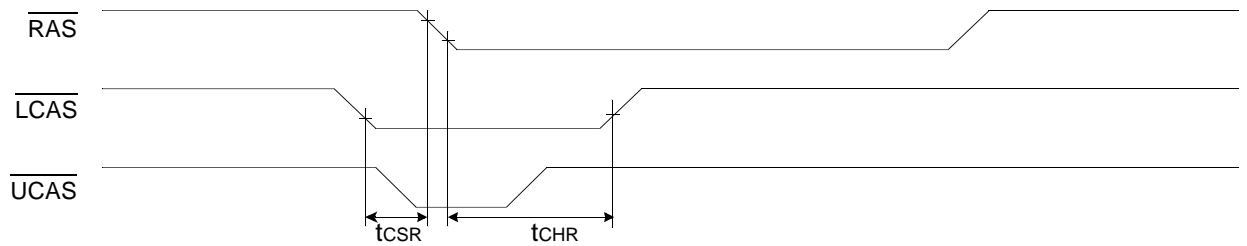
NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{ih}/V_{il} . $V_{ih}(\text{min})$ and $V_{il}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{ih}(\text{min})$ and $V_{il}(\text{max})$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1TTL(3.3V) loads and 100pF.
4. Operation within the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol} .
7. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ and $t_{\text{CPWD}} \geq t_{\text{CPWD}}(\text{min})$, then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to $\overline{\text{CAS}}$ falling edge in early write cycles and to $\overline{\text{W}}$ falling edge in $\overline{\text{OE}}$ controlled write cycle and read-modify-write cycles.
10. Operation within the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled by t_{AA} .
11. t_{ASC} , t_{CAH} are referenced to the earlier $\overline{\text{CAS}}$ falling edge.
12. t_{CP} is specified from the later $\overline{\text{CAS}}$ rising edge in the previous cycle to the earlier $\overline{\text{CAS}}$ falling edge in the next cycle.

KM416C/V10(2)00C/C-L Truth Table

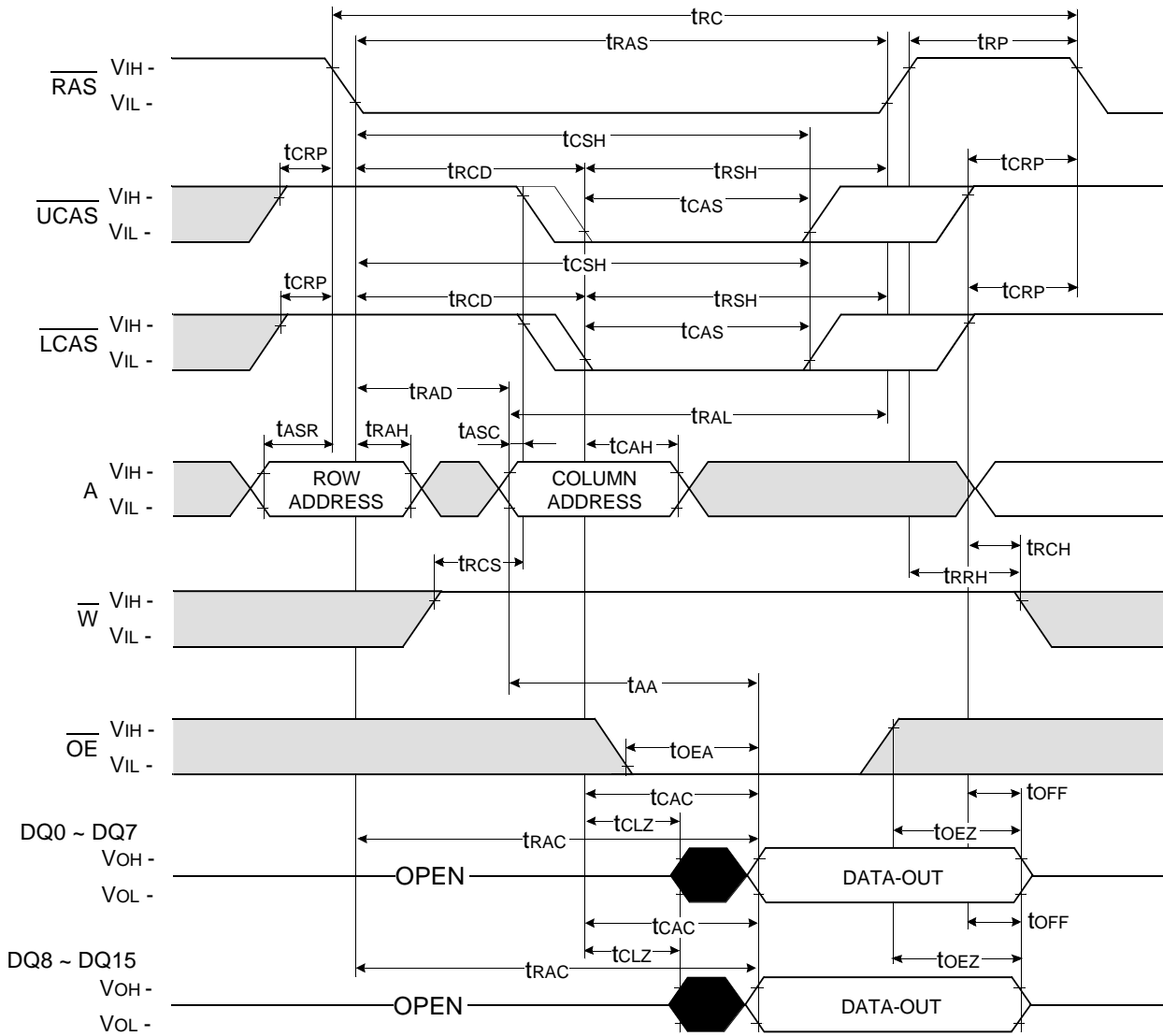
RAS	LCAS	UCAS	W	OE	DQ0 - DQ7	DQ8-DQ15	STATE
H	X	X	X	X	Hi-Z	Hi-Z	Standby
L	H	H	X	X	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

13. t_{CWD} is referenced to the later \overline{CAS} falling edge at word read-modify-write cycle.
14. t_{CWL} is specified from \overline{W} falling edge to the earlier \overline{CAS} rising edge.
15. t_{CSR} is referenced to the earlier \overline{CAS} falling edge before \overline{RAS} transition low.
16. t_{CHR} is referenced to the later \overline{CAS} rising edge after \overline{RAS} transition low.



17. t_{DS} , t_{DH} is independently specified for lower byte DQ(0-7), upper byte DQ(8-15)
18. If $t_{RAS} \geq 100\mu s$, then \overline{RAS} precharge time must use t_{RPS} instead of t_{RP} .
19. For \overline{RAS} -only refresh and burst \overline{CAS} -before- \overline{RAS} refresh mode, 4096(4K)/1024(1K) cycles of burst refresh must be executed within 64ms/16ms before and after self refresh, in order to meet refresh specification.
20. For distributed \overline{CAS} -before- \overline{RAS} with 15.6 μs interval \overline{CAS} -before- \overline{RAS} refresh should be executed with in 15.6 μs immediately before and after self refresh in order to meet refresh specification.

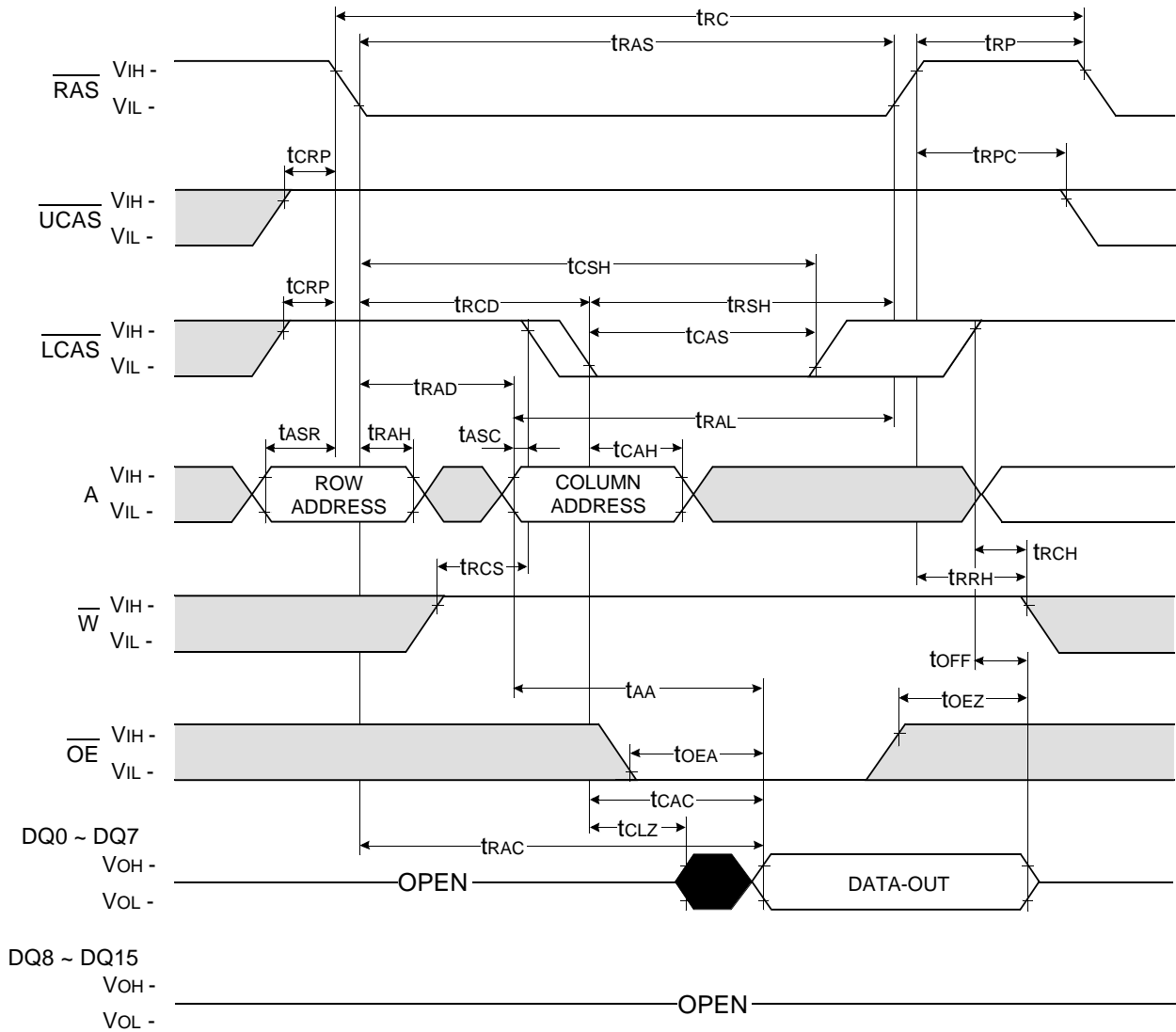
WORD READ CYCLE



□ Don't care
 ■ Undefined

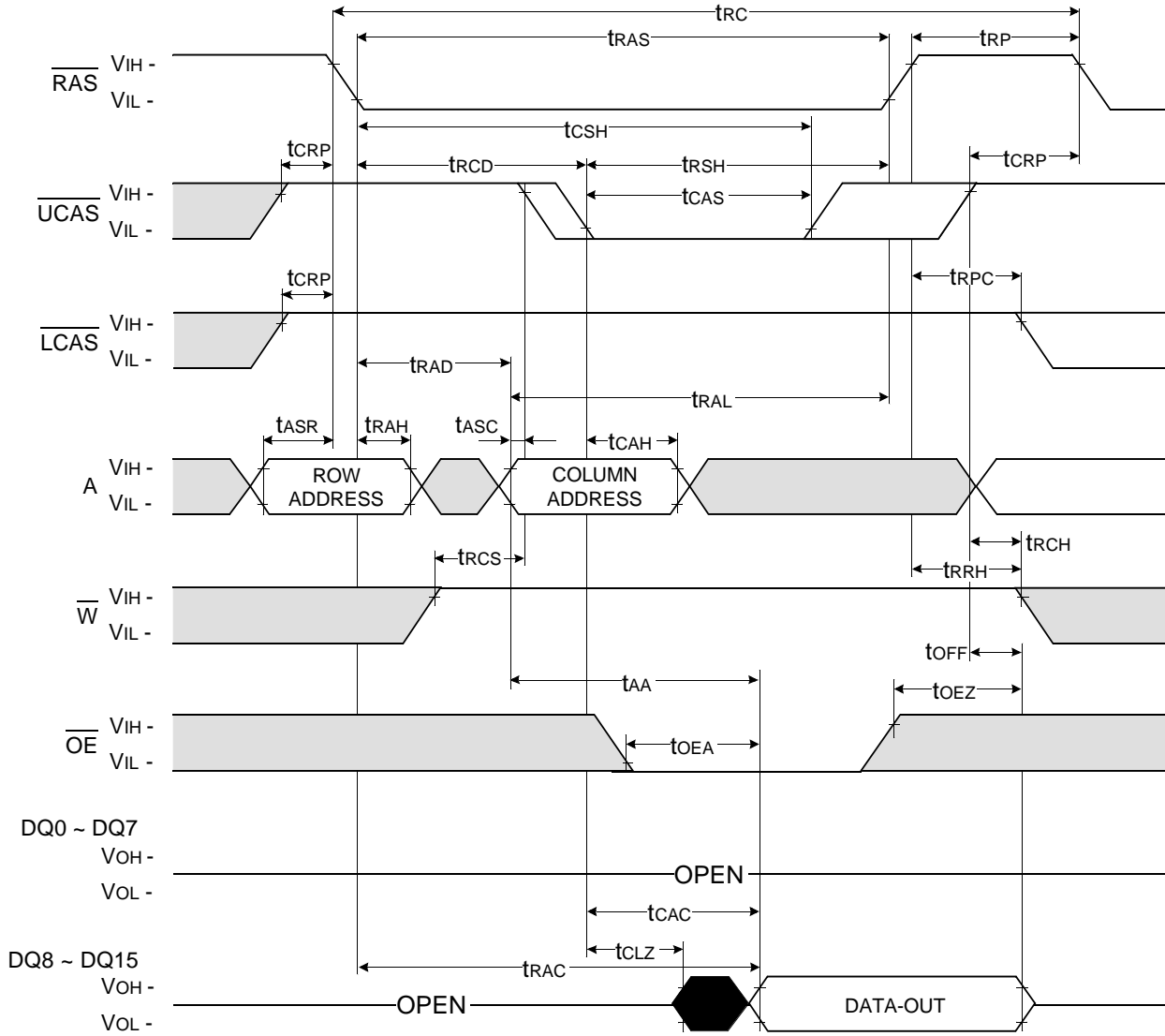
LOWER BYTE READ CYCLE

NOTE : DIN = OPEN



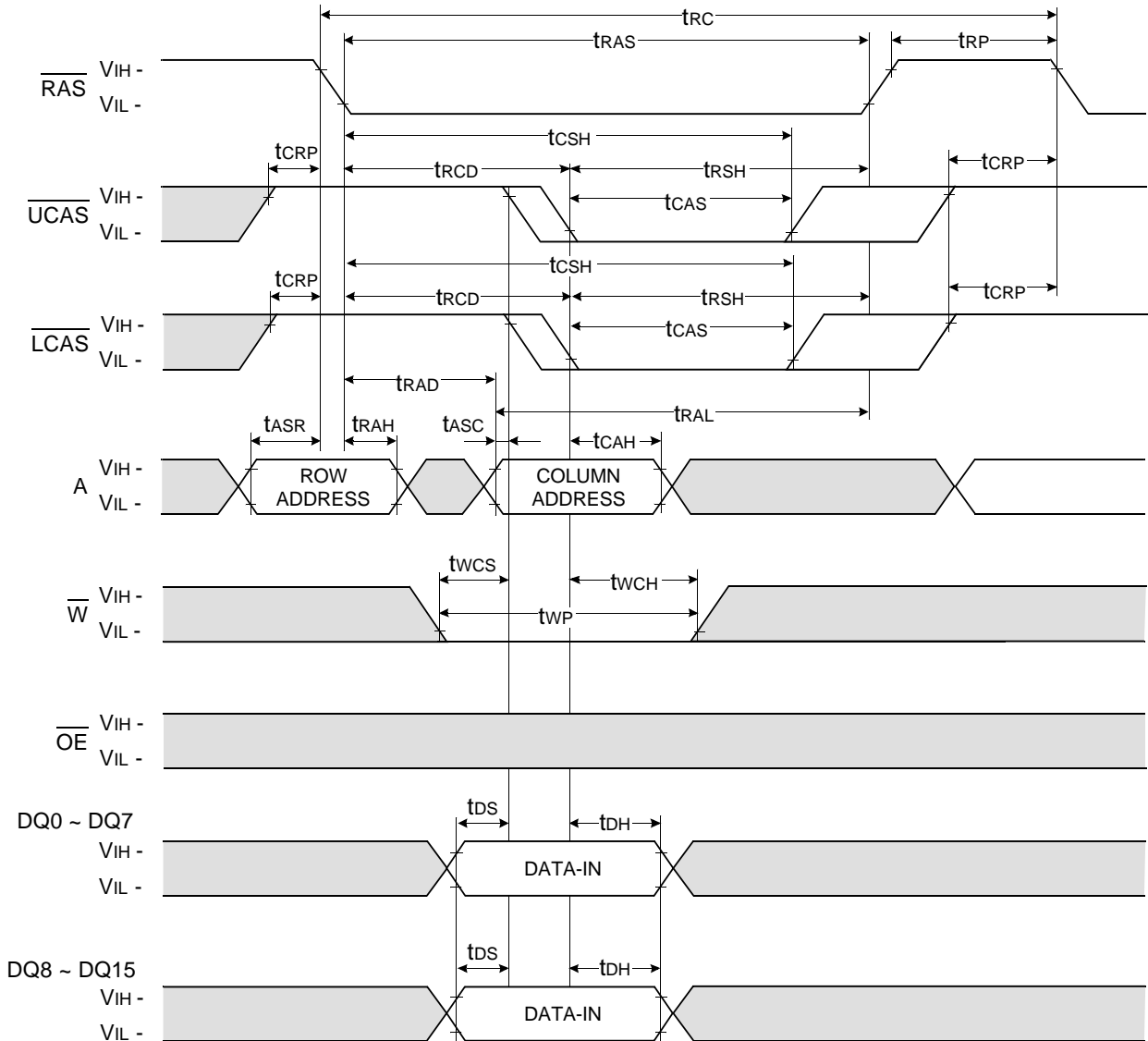
UPPER BYTE READ CYCLE

NOTE : DIN = OPEN



WORD WRITE CYCLE (EARLY WRITE)

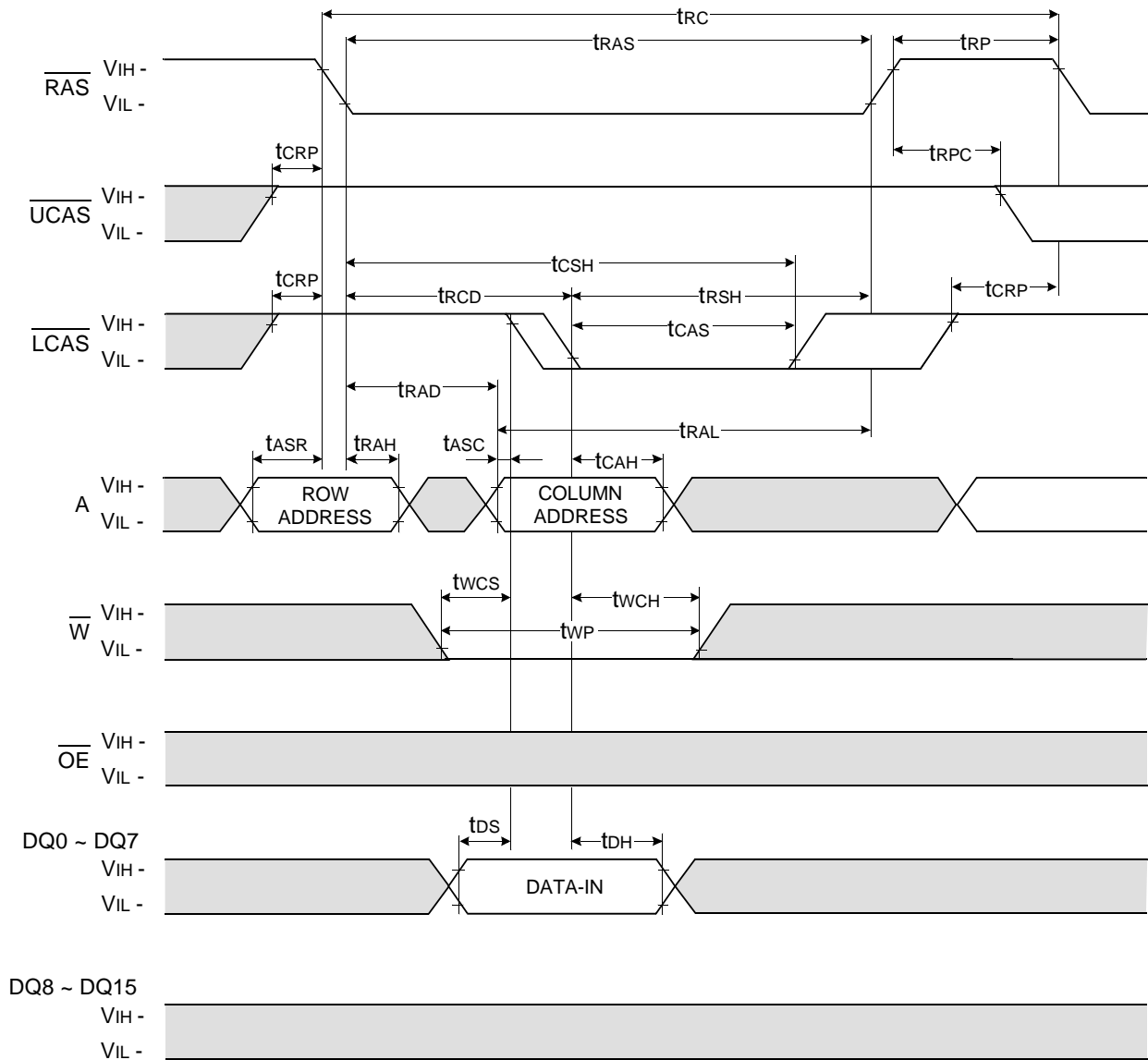
NOTE : DOUT = OPEN



□ Don't care
 ■ Undefined

LOWER BYTE WRITE CYCLE (EARLY WRITE)

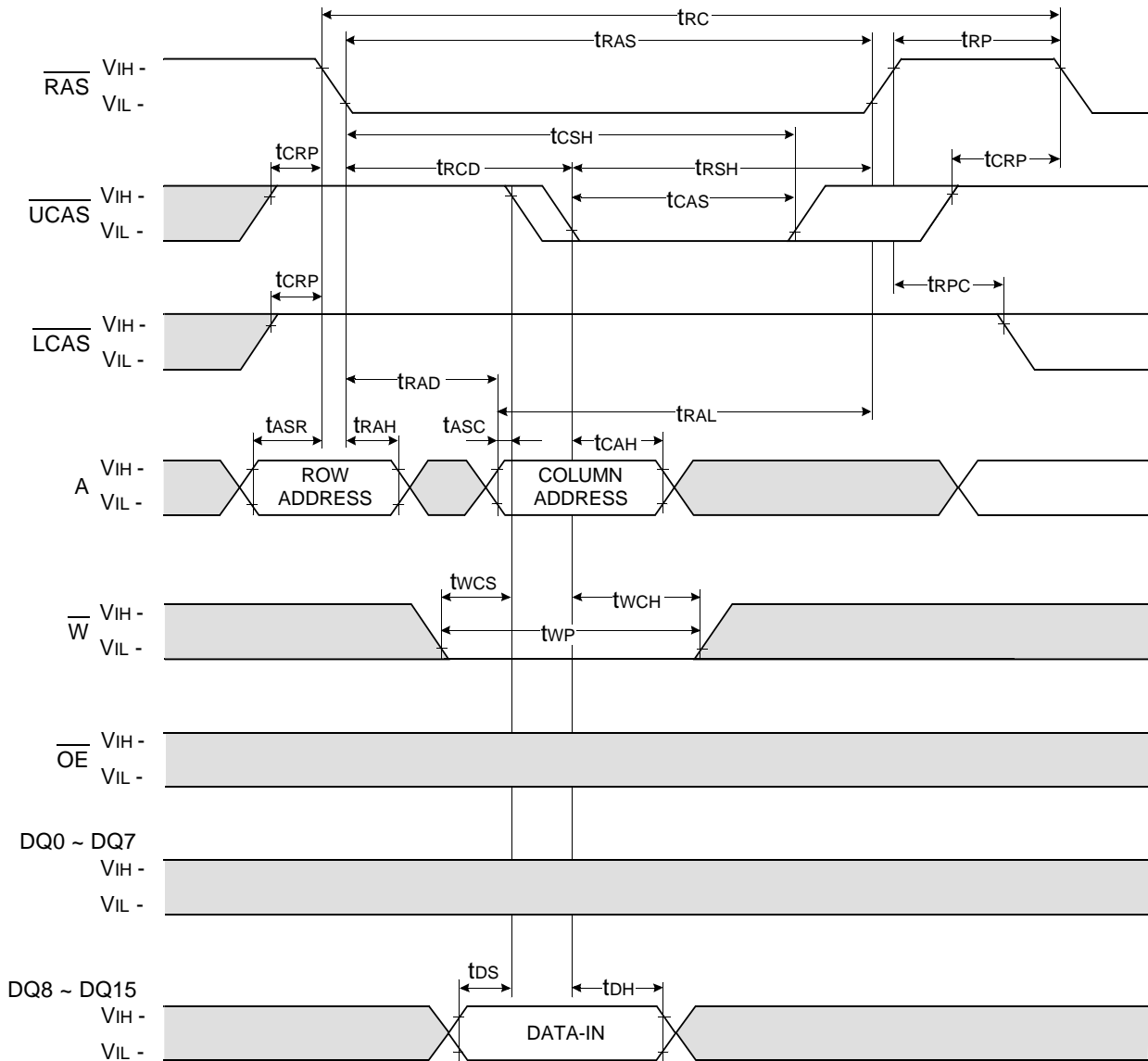
NOTE : DOUT = OPEN



□ Don't care
 ■ Undefined

UPPER BYTE WRITE CYCLE (EARLY WRITE)

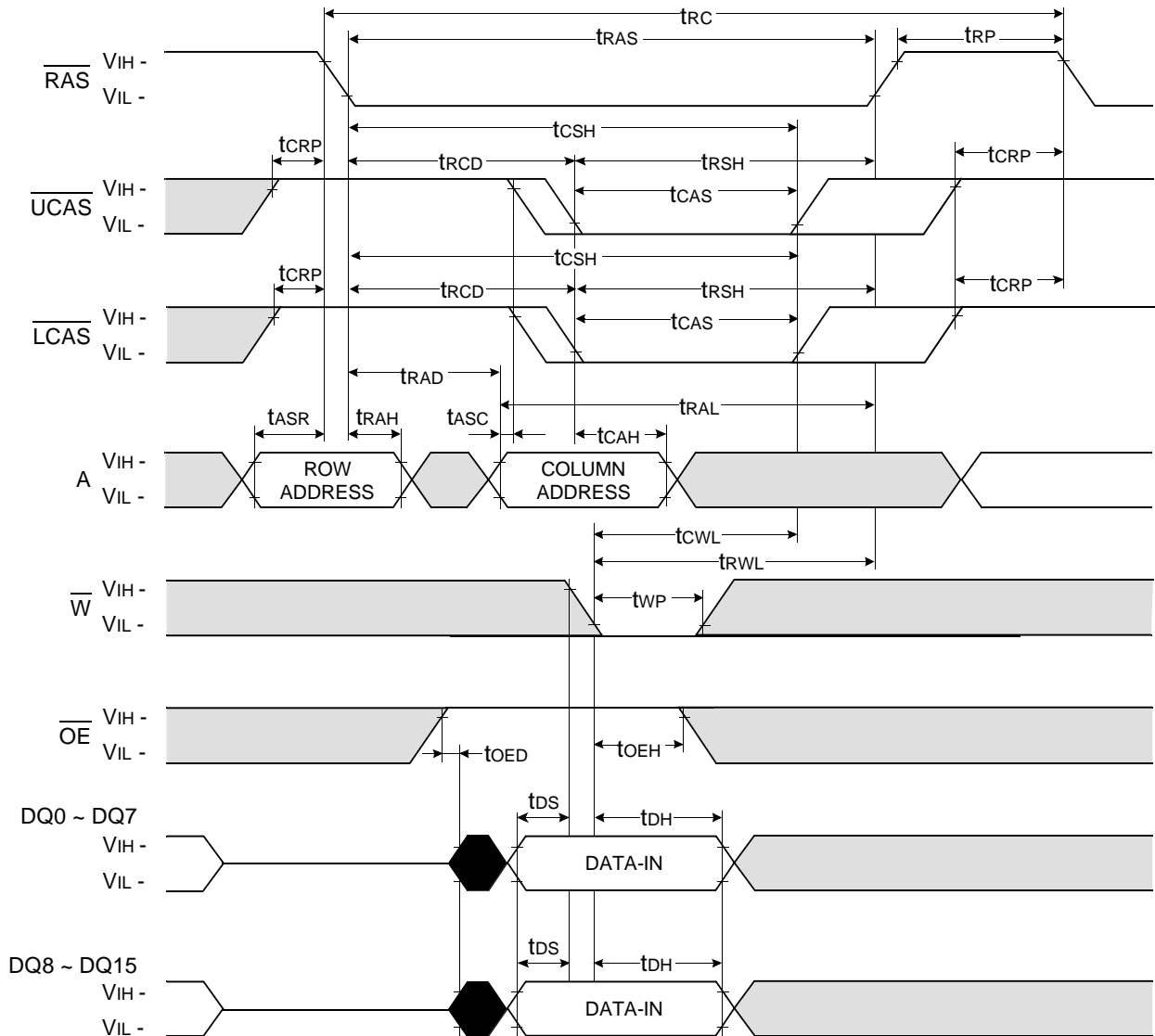
NOTE : DOUT = OPEN



□ Don't care
 ■ Undefined

WORD WRITE CYCLE ($\overline{\text{OE}}$ CONTROLLED WRITE)

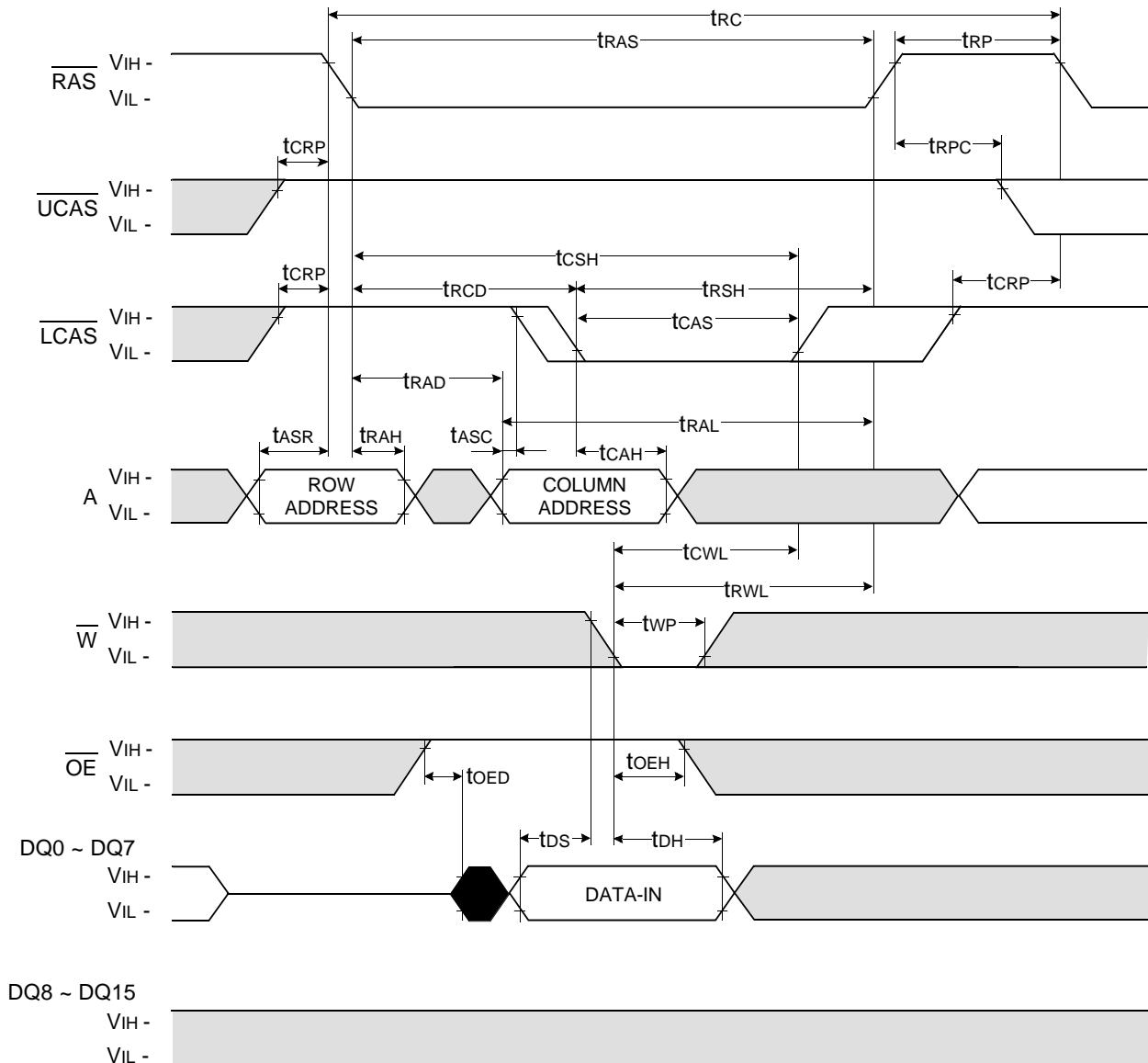
NOTE : DOUT = OPEN



Don't care
 Undefined

LOWER BYTE WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

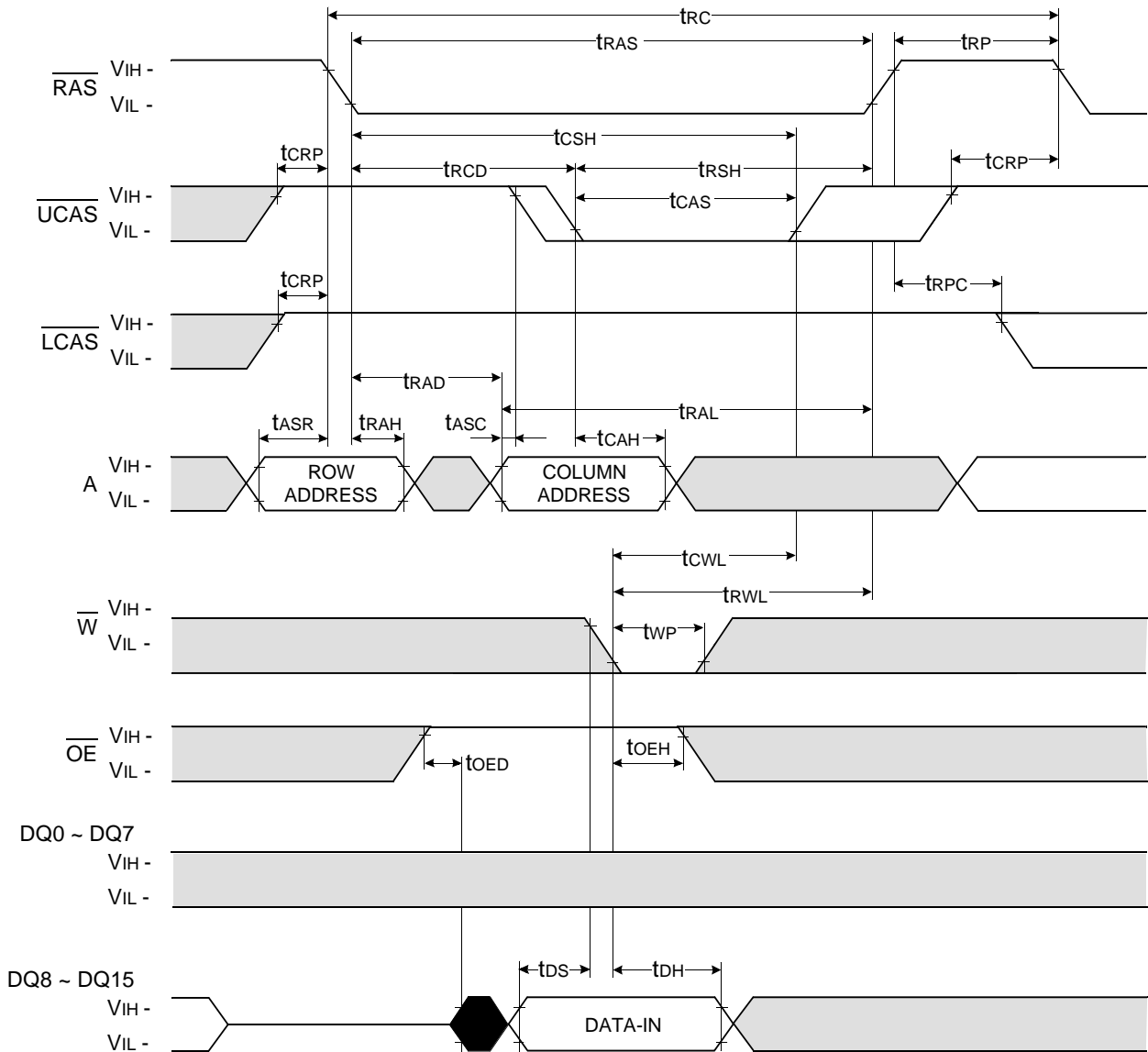
NOTE : DOUT = OPEN



□ Don't care
 ■ Undefined

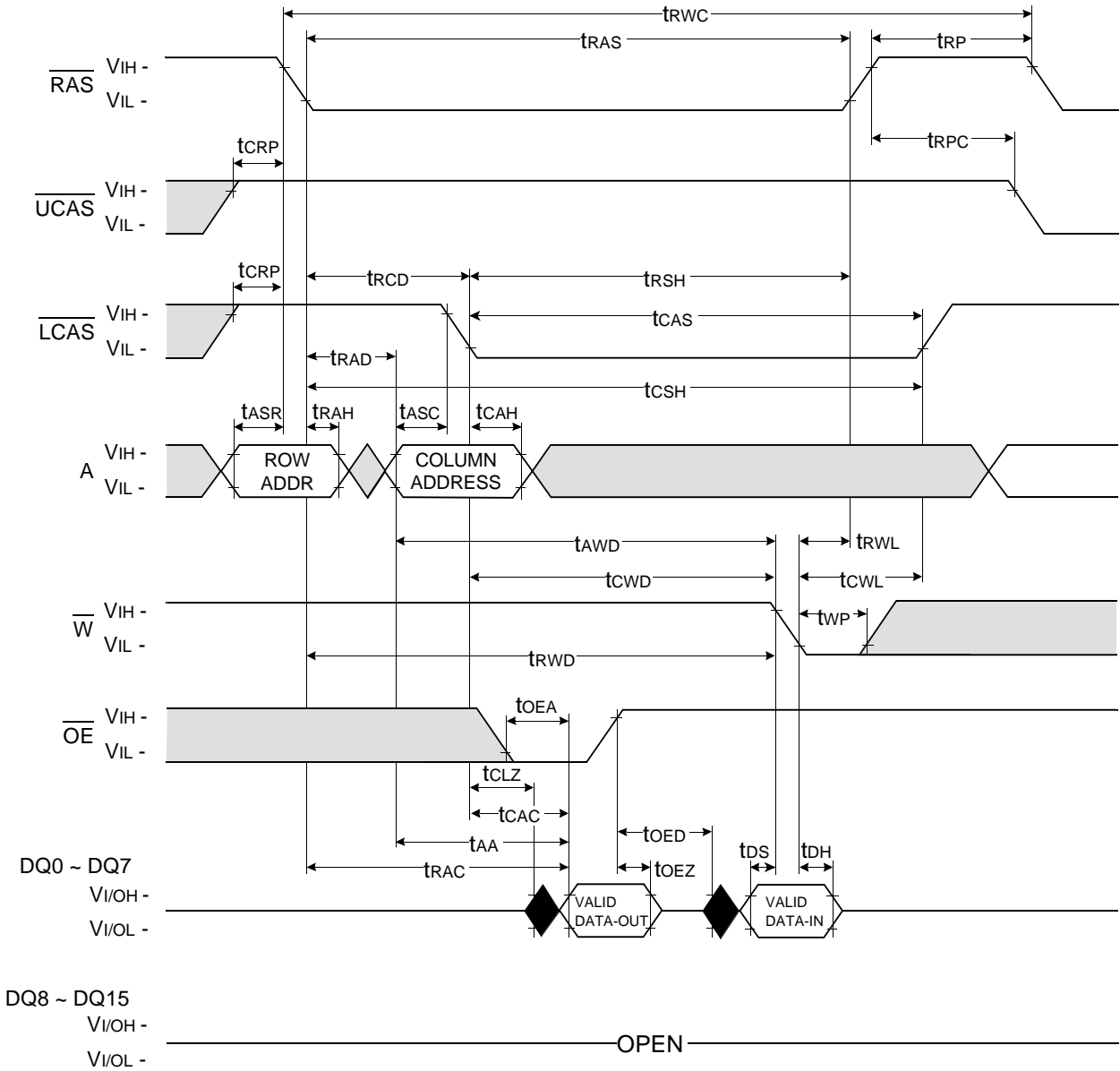
UPPER BYTE WRITE CYCLE ($\overline{\text{OE}}$ CONTROLLED WRITE)

NOTE : DOUT = OPEN

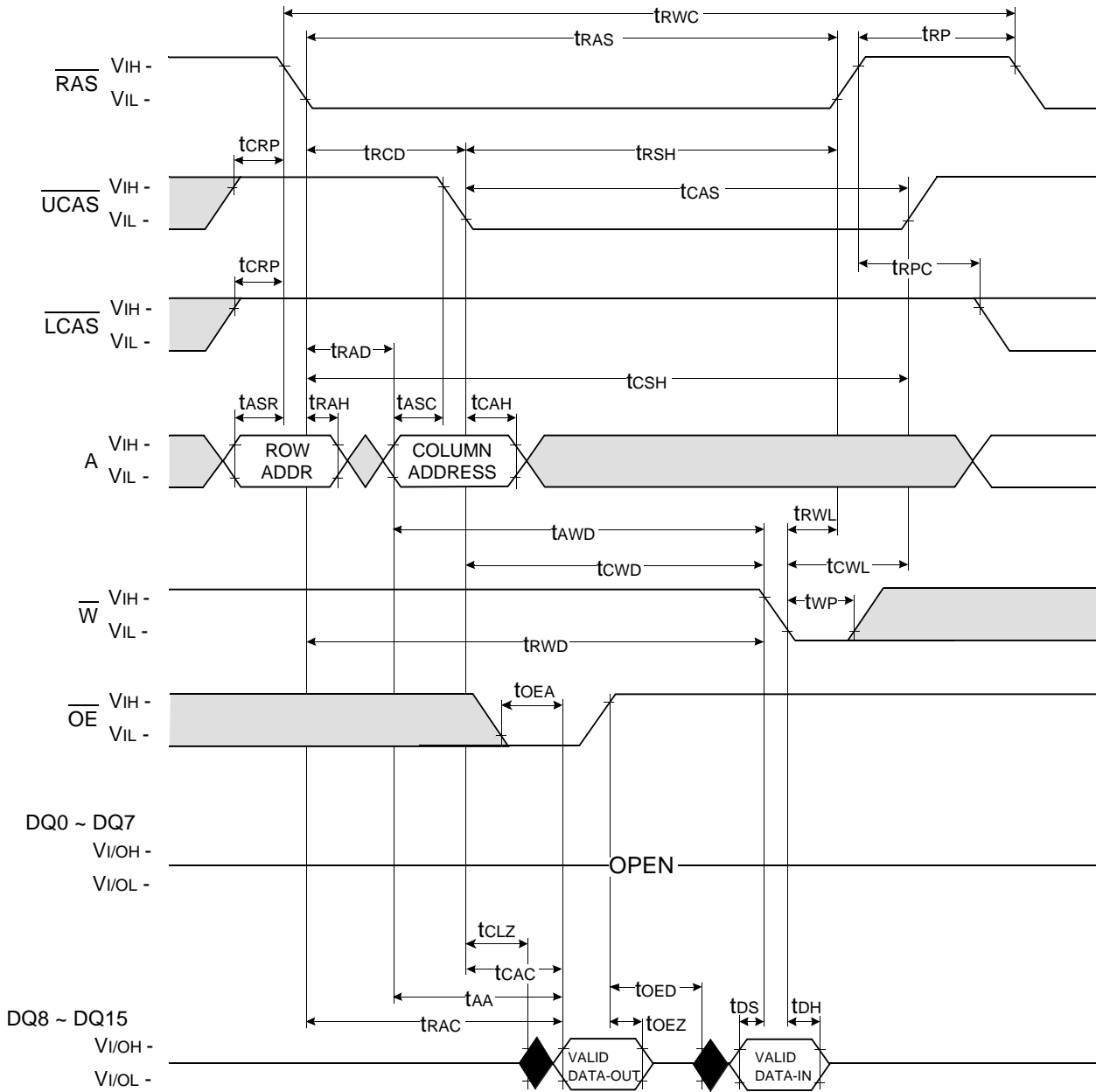


□ Don't care
 ■ Undefined

LOWER-BYTE READ - MODIFY - WRITE CYCLE

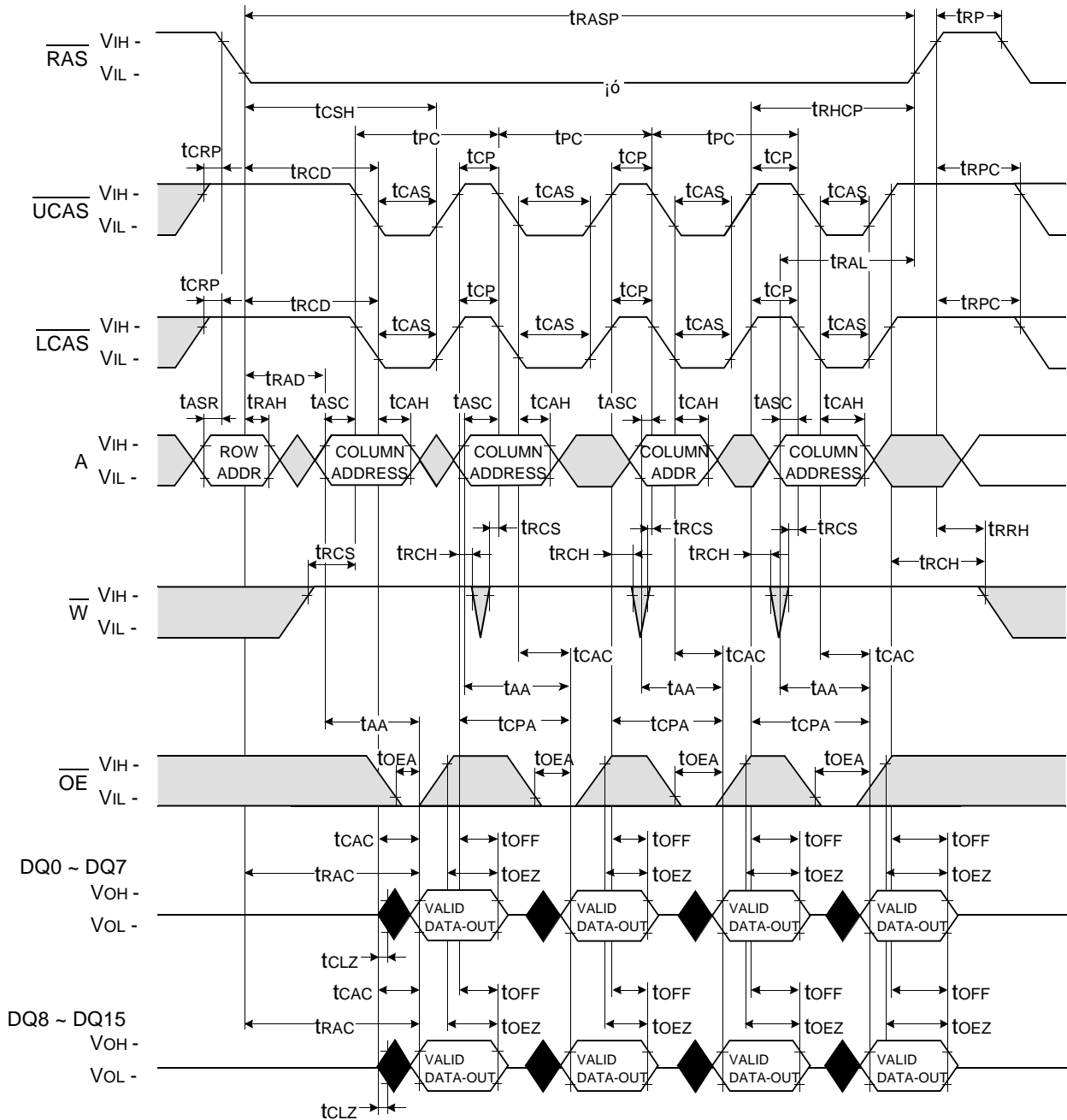


UPPER-BYTE READ - MODIFY - WRITE CYCLE



Don't care
 Undefined

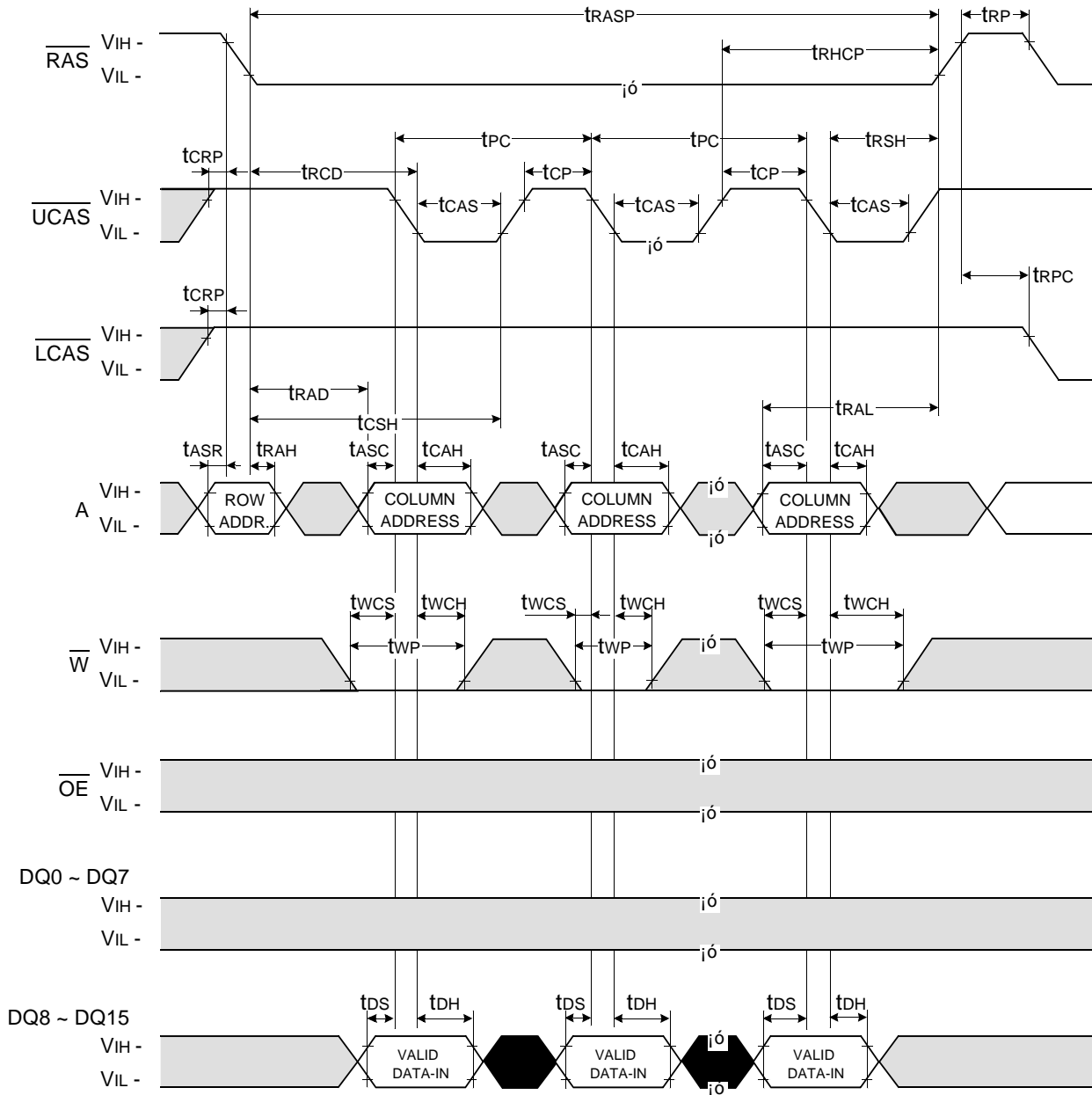
FAST PAGE MODE WORD READ CYCLE



Don't care
 Undefined

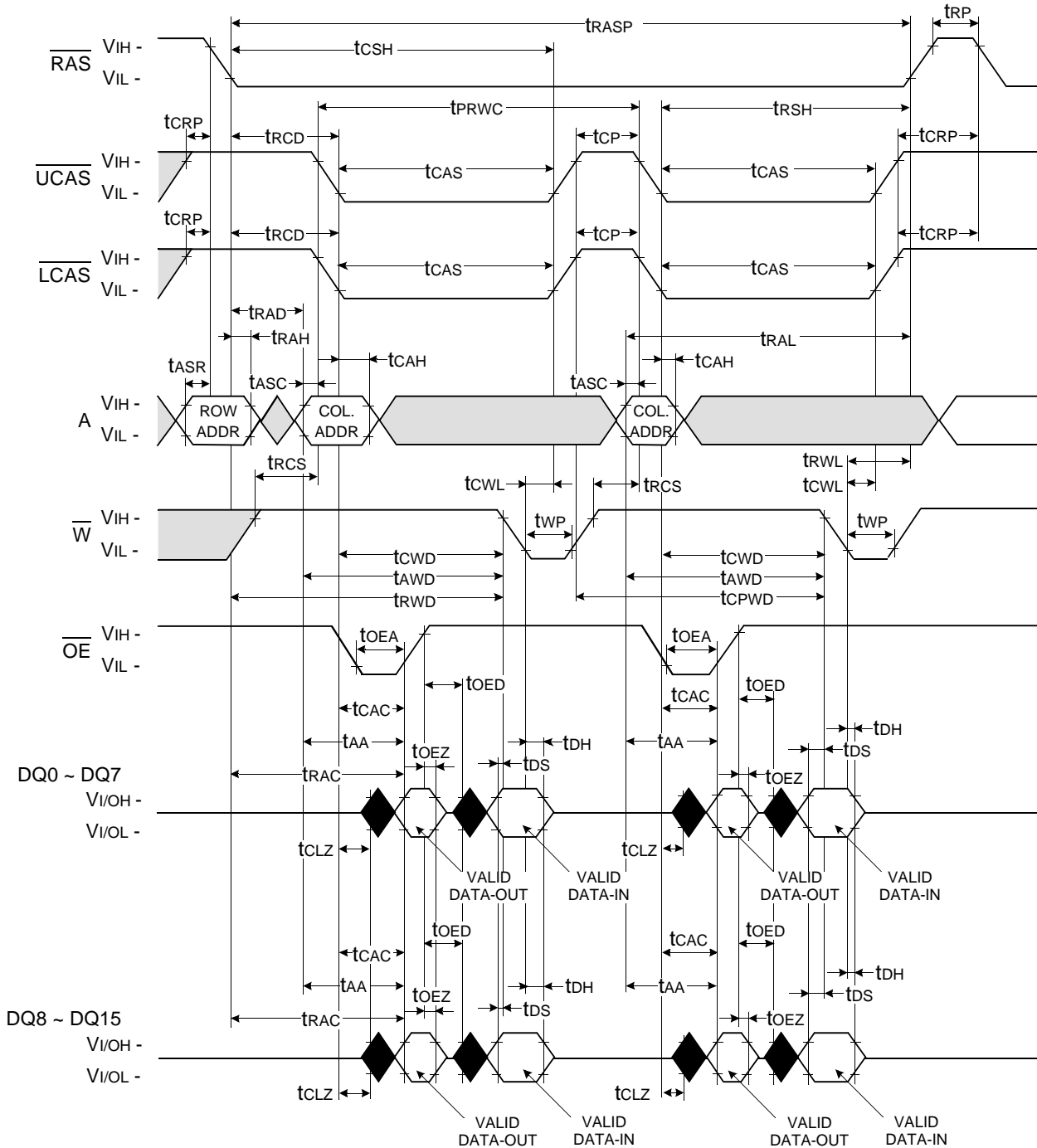
FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



□ Don't care
 ■ Undefined

FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE

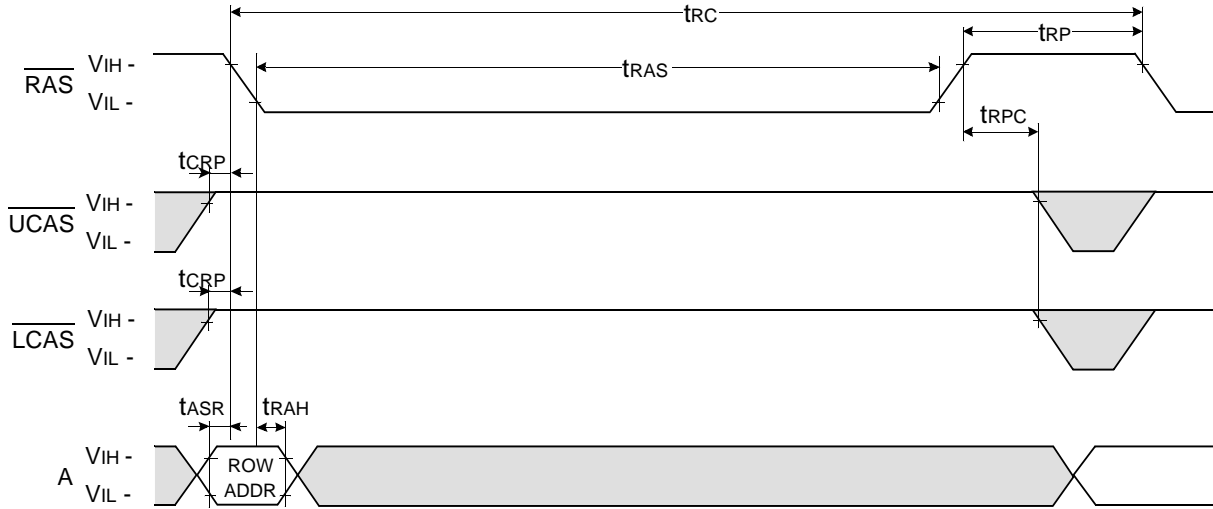


□ Don't care
 ■ Undefined

$\overline{\text{RAS}}$ - ONLY REFRESH CYCLE

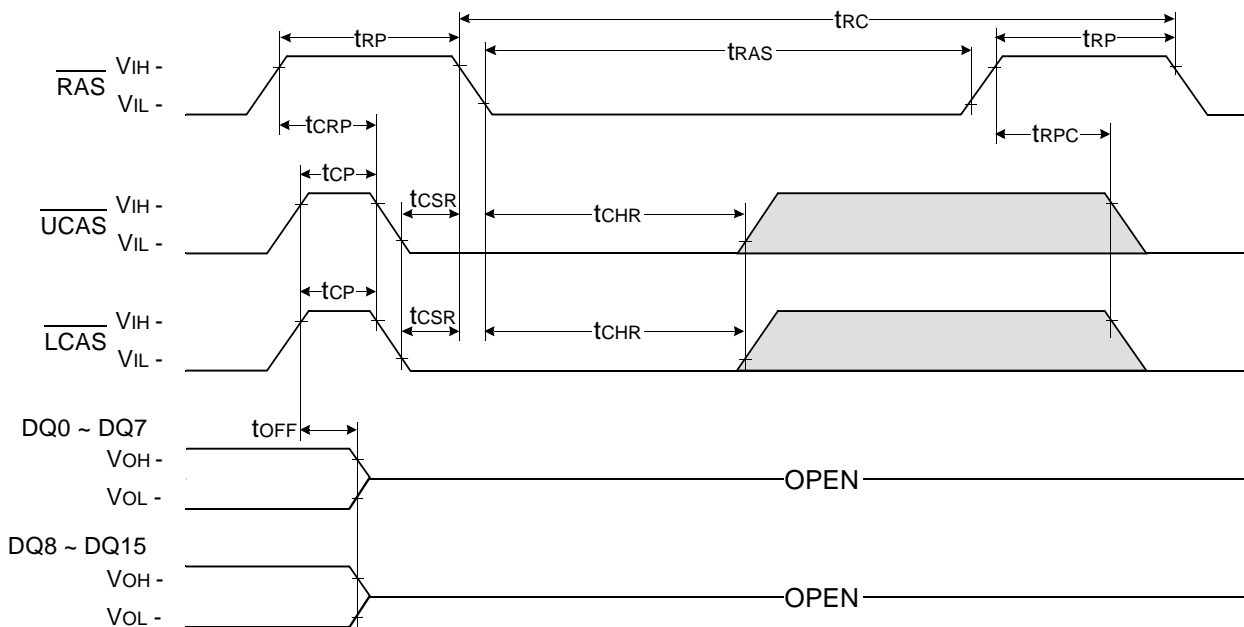
NOTE : $\overline{\text{W}}$, $\overline{\text{OE}}$, DIN = Don't care

DOUT = OPEN



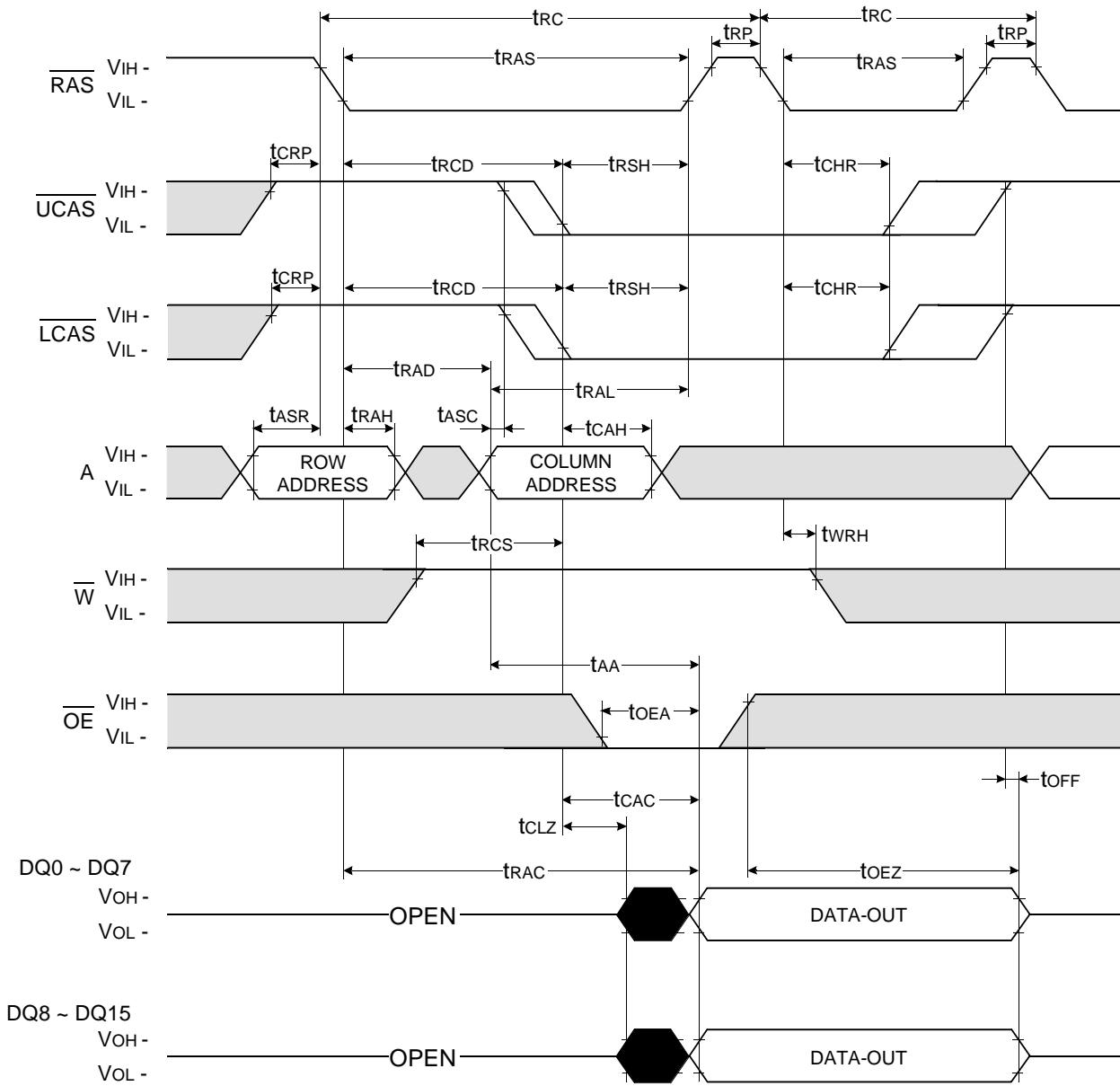
$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ REFRESH CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



□ Don't care
■ Undefined

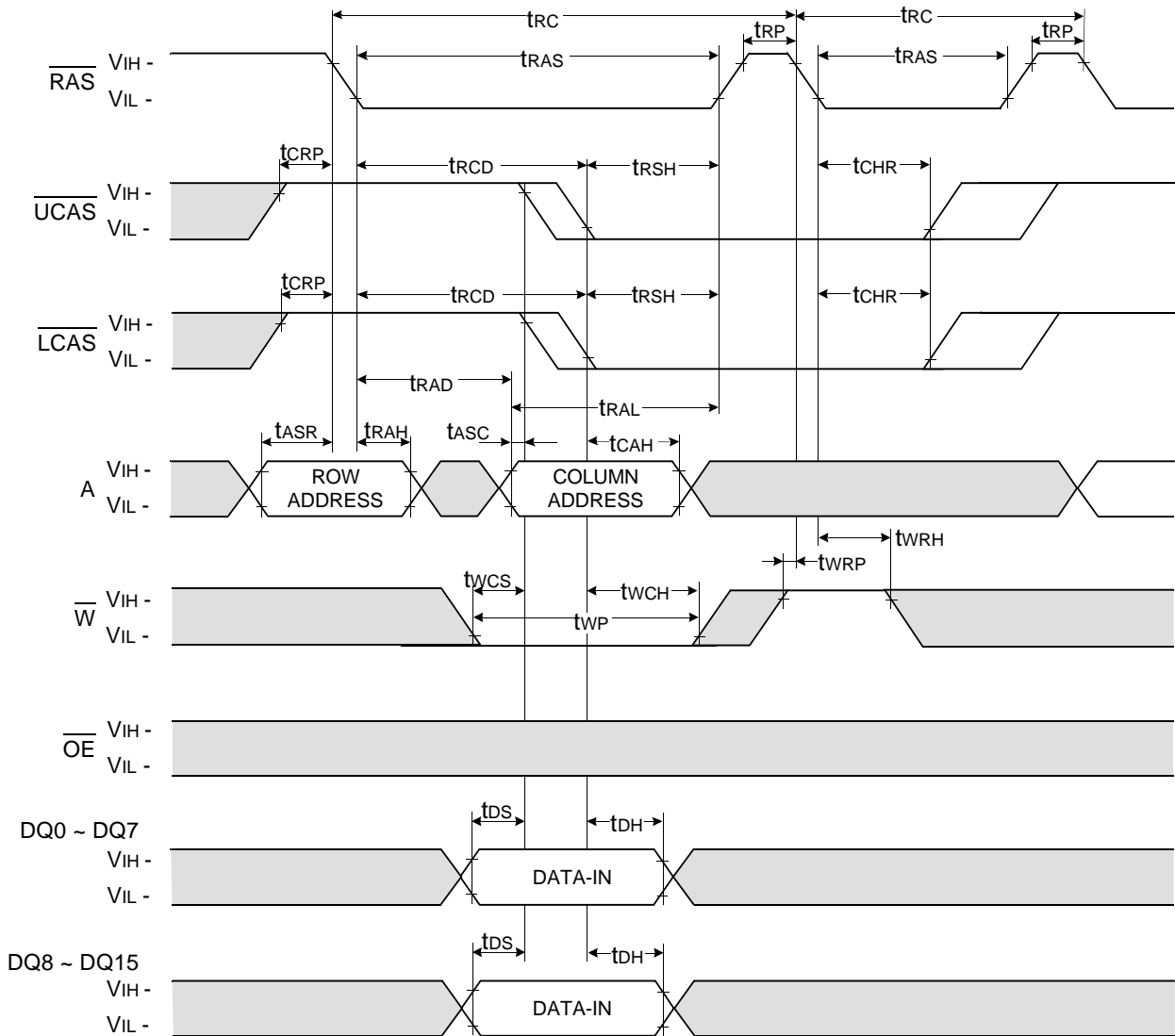
HIDDEN REFRESH CYCLE (READ)



□ Don't care
 ■ Undefined

HIDDEN REFRESH CYCLE (WRITE)

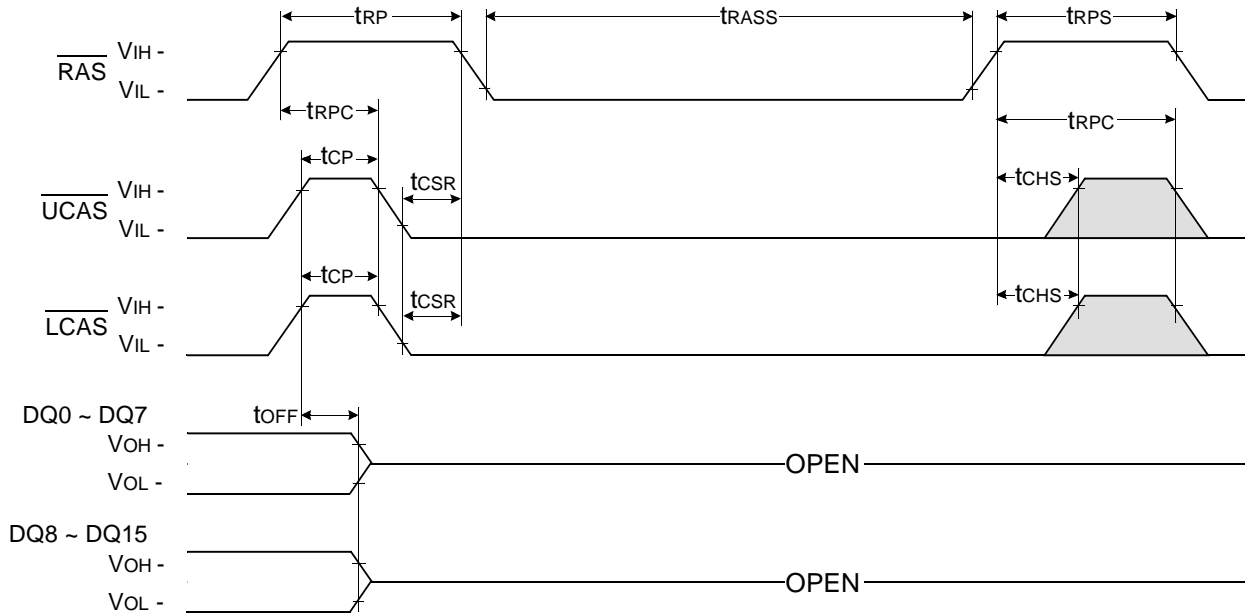
NOTE : DOUT = OPEN



□ Don't care
 ■ Undefined

$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ SELF REFRESH CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



KM416C1000C, KM416C1200C
KM416V1000C, KM416V1200C

CMOS DRAM

PACKAGE DIMENSION

