National Semiconductor Corporation

DM9310/DM8310 Synchronous 4-Bit Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The DM9310/DM8310 are decade counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operating eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable input. Low-to-high transitions at the load input are perfectly acceptable regardless of the logic levels on the clock or enable inputs. The clear function is asynchronous and a low level at the clear input sets of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs.

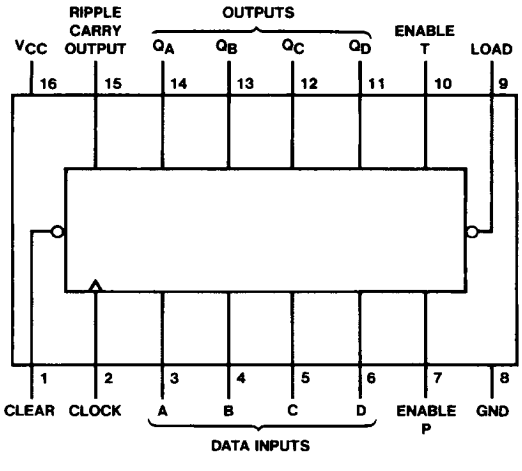
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed-forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low level transitions at the enable P or T inputs may occur regardless of the logic level in the clock.

FEATURES

- Direct replacement for Fairchild 9310
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs
- Typical clock frequency 35 MHz
- Pin-for-pin replacements popular 54/74 counters 9310—54160A/74160A (decade)

Connection Diagram

Dual-In-Line Package



TL/F/6603–1

Order Number DM9310J or DM8310N
See NS Package Number J16A or N16A

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM93	−55°C to +125°C
DM83	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM9310			DM8310			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 5)		0		25	0		25	MHz
t_W	Pulse Width (Note 5)	Clock	25			25			ns
		Clear	20			20			
t_{SU}	Setup Time (Note 5)	Data	20			20			ns
		Enable P	20			20			
		Load	25			25			
		Clear	20			20			
t_H	Any Hold Time (Notes 1 & 5)		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The minimum HOLD time is as specified or as long as the CLOCK input takes to rise from 0.8V to 2V, whichever is longer.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	CLK, EN T			80	μA
			Other			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	CLK, EN T			−3.2	mA
			Other			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM93	−20		−57	mA
			DM83	−18		−57	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)	DM93		59	85	mA
			DM83		59	94	
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 4)	DM93		63	91	mA
			DM83		63	101	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CCH} is measured with the LOAD input high, then again with the LOAD input low, with all other inputs high and all outputs open.

Note 4: I_{CCL} is measured with the CLOCK input high, then again with the CLOCK input low, with all other inputs low and all outputs open.

Note 5: T_A = 25°C and V_{CC} = 5V.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

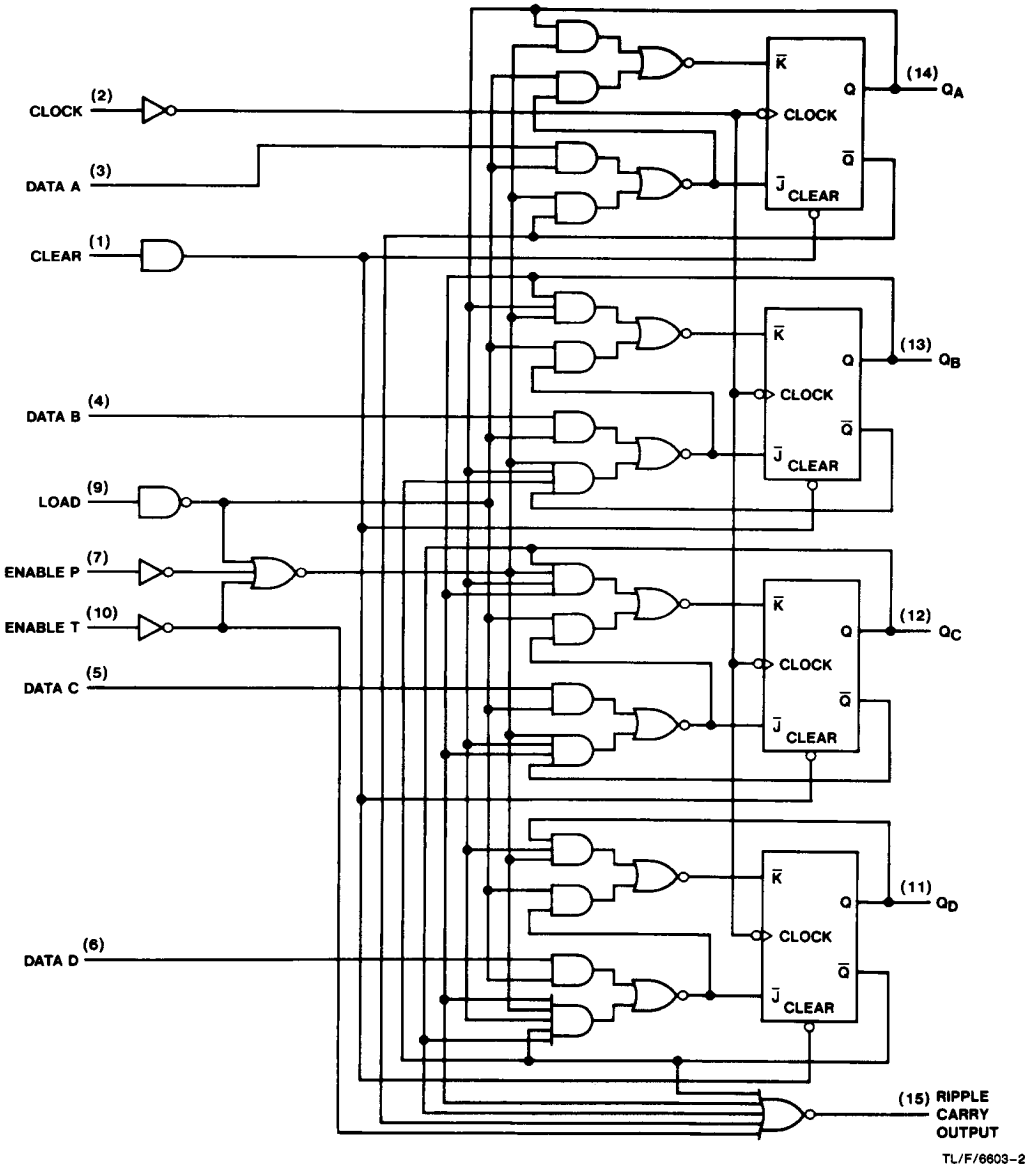
Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q		23	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable T to Ripple Carry		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable T to Ripple Carry		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		36	ns

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Logic Diagram

DM93/8310

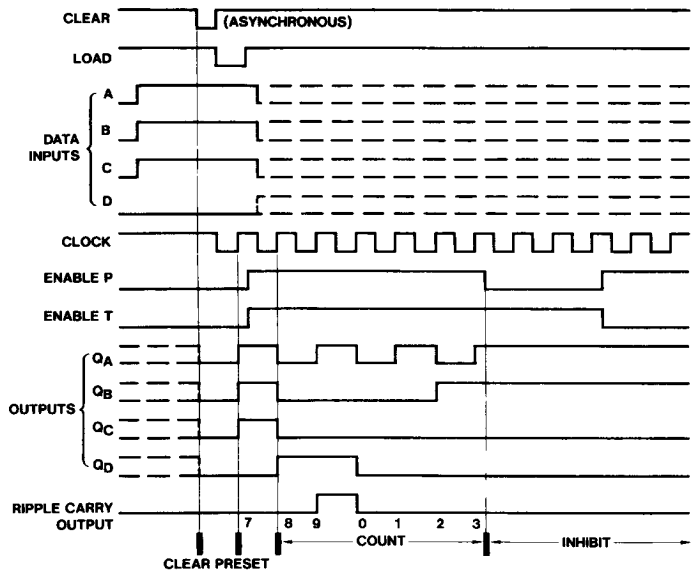


TL/F/6603–2

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Timing Diagram

9310/8310 Synchronous Decade Counters
Typical Clear, Preset, Count and Inhibit Sequence



TL/F/6603–3

Sequence:

(1) Clear outputs to zero.

(2) Preset to BCD seven.

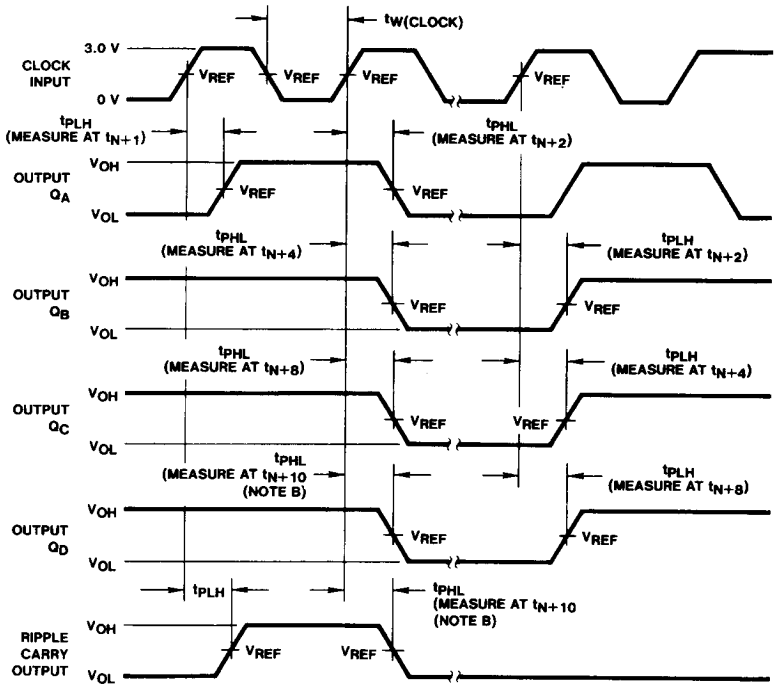
(3) Count to eight, nine, zero, one, two, and three.

(4) Inhibit

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Parameter Measurement Information

Switching Time Waveforms



TL/F/6603–4

Note A: The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$, $t_r \leq 10$ ns, $t_f \leq 10$ ns. Vary PRR to measure f_{MAX}.

Note B: Outputs Q_D and carry are tested at t_{n+10} for 9310/8310, where t_n is the bit time when all outputs are low.

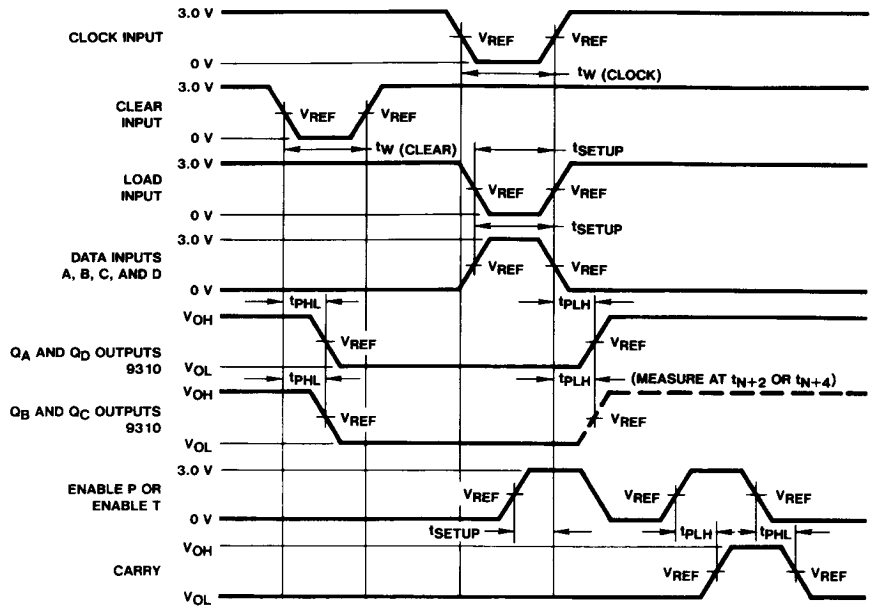
Note C: $V_{REF} = 1.5V$.

4

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Parameter Measurement Information (Continued)

Switching Time Waveforms



TL/F/6603–5

Note A: The input pulses are supplied by generators having the following characteristics: PRR ≤ MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Note B: Enable P and enable T setup times are measured at t_{n+10} for 8310/9310.

Note C: $V_{REF} = 1.5V$.

Powered by ICminer.com Electronic-Library Service CopyRight 2003