QUADRUPLE 2-INPUT NAND SCHMITT TRIGGER

The HEF4093B consists of four Schmitt-trigger circuits. Each circuit functions as a two-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive and negative-going signals. The difference between the positive voltage (V_P) and the negative voltage (V_N) is defined as hysteresis voltage (V_H).

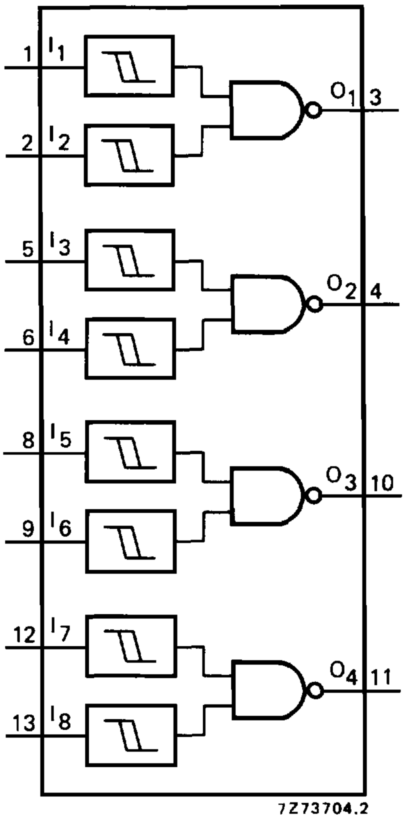

Fig. 1 Functional diagram.

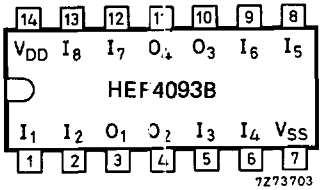

Fig. 2 Pinning diagram.

HEF4093BP(N): 14-lead DIL; plastic (SOT27-1)
HEF4093BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
HEF4093BT(D): 14-lead SO; plastic (SOT108-1)
( ): Package Designator North America

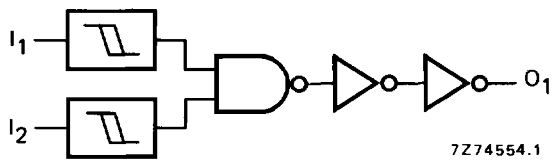

Fig. 3 Logic diagram (one gate).

FAMILY DATA
I_{DD} LIMITS category GATES } see Family Specifications

D.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C

	V_{DD} V	symbol	min.	typ.	max.	
Hysteresis voltage	5	V_H	0,4	0,7	–	V
	10		0,6	1,0	–	V
	15		0,7	1,3	–	V
Switching levels positive-going input voltage	5	V_P	1,9	2,9	3,5	V
	10		3,6	5,2	7	V
	15		4,7	7,3	11	V
negative-going input voltage	5	V_N	1,5	2,2	3,1	V
	10		3	4,2	6,4	V
	15		4	6,0	10,3	V

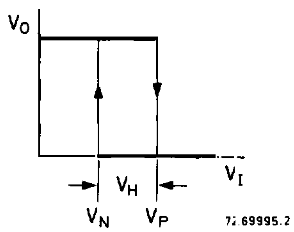

Fig. 4 Transfer characteristic.

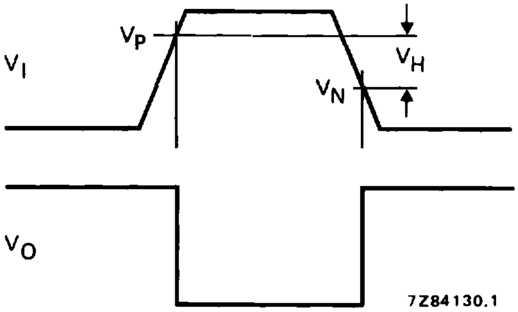

Fig. 5 Waveforms showing definition of V_P, V_N and V_H; where V_N and V_P are between limits of 30% and 70%.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays	5		90	185	ns	63 ns + (0,55 ns/pF) C_L
I_n → O_n	10	t_{PHL}	40	80	ns	29 ns + (0,23 ns/pF) C_L
HIGH to LOW	15		30	60	ns	22 ns + (0,16 ns/pF) C_L
	5		85	170	ns	58 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	40	80	ns	29 ns + (0,23 ns/pF) C_L
	15		30	60	ns	22 ns + (0,16 ns/pF) C_L
Output transition						
times	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	
			where
			f_i = input freq. (MHz)
			f_o = output freq. (MHz)
Dynamic power	5	$1300\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	C_L = load capacitance (pF)
dissipation per	10	$6400\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	$\Sigma(f_oC_L)$ = sum of outputs
package (P)	15	$18\,700\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	V_{DD} = supply voltage (V)

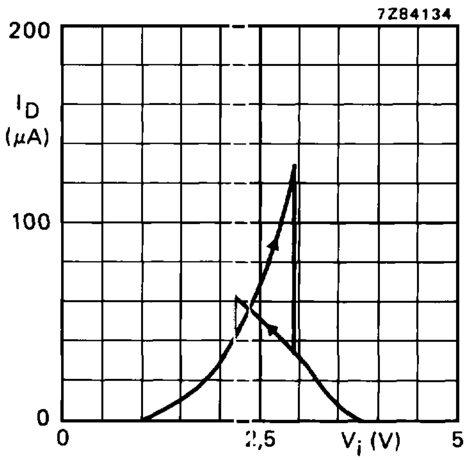

Fig. 6 Typical drain current as a function of input voltage; V_{DD} = 5 V; T_{amb} = 25 °C.

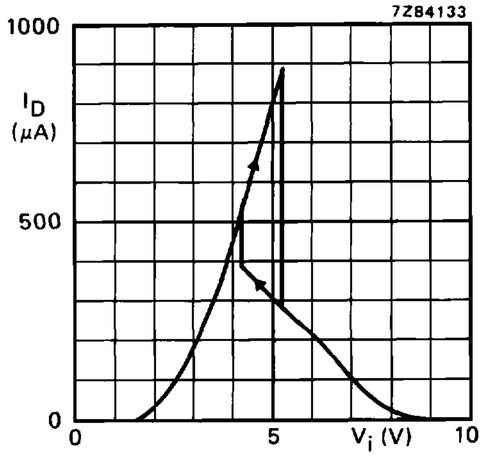

Fig. 7 Typical drain current as a function of input voltage; V_{DD} = 10 V; T_{amb} = 25 °C.

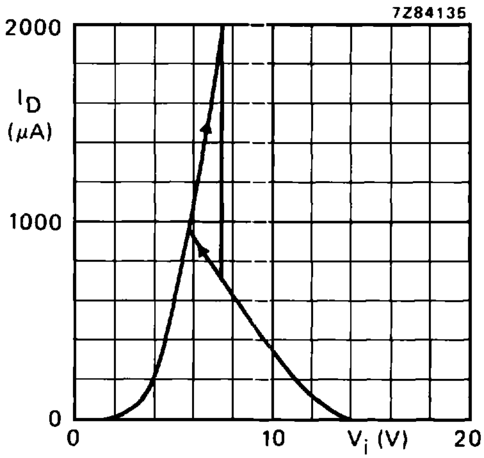

Fig. 8 Typical drain current as a function of input voltage; V_{DD} = 15 V; T_{amb} = 25 °C.

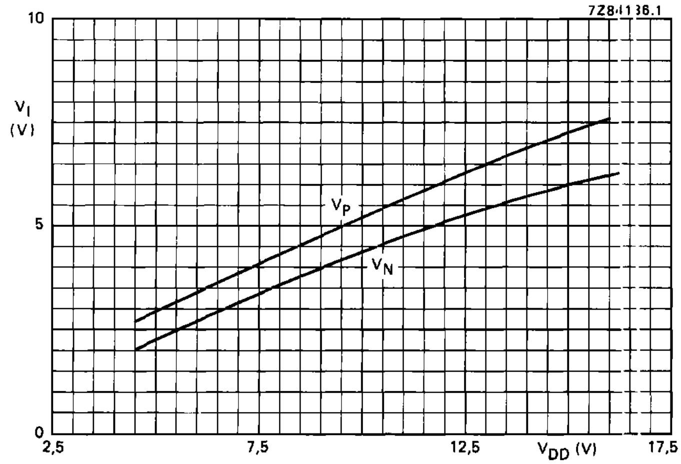

Fig. 9 Typical switching levels as a function of supply voltage V_{DD}; T_{amb} = 25 °C.

APPLICATION INFORMATION

Some examples of applications for the HEF4093B are:

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators.

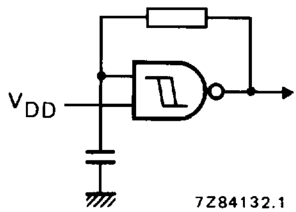

Fig. 10 The HEF4093B used as a astable multivibrator.

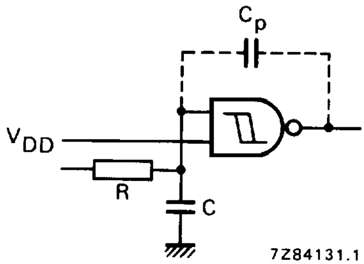

Fig. 11 Schmitt trigger driven via a high impedance ($R > 1\ k\Omega$).

If a Schmitt trigger is driven via a high impedance ($R > 1\ k\Omega$) then it is necessary to incorporate a capacitor C of such value that: $\frac{C}{C_p} > \frac{V_{DD}-V_{SS}}{V_H}$, otherwise oscillation can occur on the edges of a pulse.

C_p is the external parasitic capacitance between inputs and output; the value depends on the circuit board layout.

Note

The two inputs may be connected together, but this will result in a larger through-current at the moment of switching.