

# CAT93C46A/56A/66A/86A

1K/2K/4K/16K-Bit Serial E<sup>2</sup>PROM

## FEATURES

- High Speed Operation: 1MHz
- Low Power CMOS Technology
- Wide Operating Voltage Range
  - $V_{cc} = 4.5V$  to  $5.5V$
  - $V_{cc} = 2.7V$  to  $6.0V$
  - $V_{cc} = 2.5V$  to  $6.0V$
  - $V_{cc} = 1.8V$  to  $6.0V$
- Self-Timed Write Cycle with Auto-Clear
- Hardware and Software Write Protection
- Power-Up Inadvertant Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Commercial and Industrial Temperature Ranges
- x16 Serial Memory

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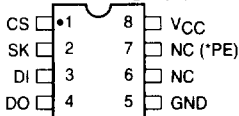
## DESCRIPTION

The CAT93C46A/56A/66A/86A is a 1K/2K/4K/16K-bit Serial E<sup>2</sup>PROM memory devices which are configured as registers of 16-bits. Each register can be written (or read) serially by using the DI (or DO) pin. The CAT93C46A/56A/66A/86A are manufactured using

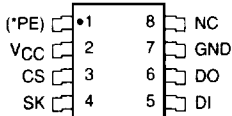
Catalyst's advanced CMOS E<sup>2</sup>PROM floating gate technology. The devices are designed to endure 100,000 program/erase cycles and have a data retention of 100 years. The devices are available in 8-pin DIP or SOIC packages.

## PIN CONFIGURATION

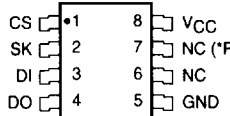
### DIP Package (P)



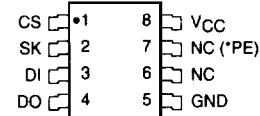
### SOIC Package (J)



### SOIC Package (S)



### SOIC Package (K)



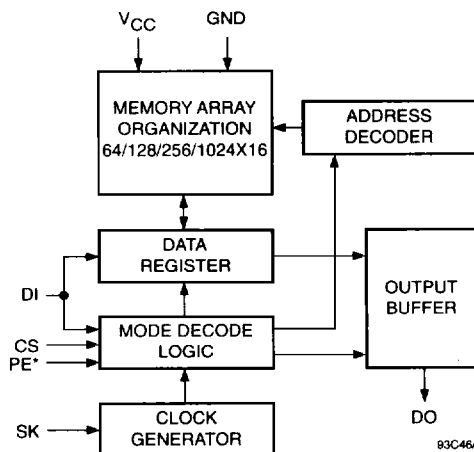
\*PE (only for 93C86A)

93CXXA F01

## PIN FUNCTIONS

| Pin Name        | Function                   |
|-----------------|----------------------------|
| CS              | Chip Select                |
| SK              | Clock Input                |
| DI              | Serial Data Input          |
| DO              | Serial Data Output         |
| V <sub>cc</sub> | +1.8V to 6.0V Power Supply |
| GND             | Ground                     |
| PE*             | Program Enable             |
| NC              | No Connect                 |

## BLOCK DIAGRAM



93C46/56/66 F02

**ABSOLUTE MAXIMUM RATINGS\***

Temperature Under Bias ..... -55°C to +125°C  
 Storage Temperature ..... -65°C to +150°C  
 Voltage on any Pin with  
     Respect to Ground<sup>(1)</sup> ..... -2.0V to +V<sub>CC</sub> +2.0V  
 V<sub>CC</sub> with Respect to Ground ..... -2.0V to +7.0V  
 Package Power Dissipation  
     Capability (Ta = 25°C) ..... 1.0W  
 Lead Soldering Temperature (10 secs) ..... 300°C  
 Output Short Circuit Current<sup>(2)</sup> ..... 100 mA

**\*COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

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**RELIABILITY CHARACTERISTICS**

| Symbol                             | Parameter          | Min.    | Max. | Units       | Reference Test Method         |
|------------------------------------|--------------------|---------|------|-------------|-------------------------------|
| N <sub>END</sub> <sup>(3)</sup>    | Endurance          | 100,000 |      | Cycles/Byte | MIL-STD-883, Test Method 1033 |
| T <sub>DR</sub> <sup>(3)</sup>     | Data Retention     | 100     |      | Years       | MIL-STD-883, Test Method 1008 |
| V <sub>ZAP</sub> <sup>(3)</sup>    | ESD Susceptibility | 2000    |      | Volts       | MIL-STD-883, Test Method 3015 |
| I <sub>LTH</sub> <sup>(3)(4)</sup> | Latch-Up           | 100     |      | mA          | JEDEC Standard 17             |

**D.C. OPERATING CHARACTERISTICS**

V<sub>CC</sub> = +1.8V to +6.0V, unless otherwise specified.

| Symbol                               | Parameter                                 | Limits                    |      |  | Units  | Test Conditions  |
|--------------------------------------|---|---------------------------|------|--|--------|--|
|                                      |   | Min.                      | Typ. | Max.                                       |        |  |
| I <sub>CC</sub>                      | Power Supply Current (Operating)          |                           |      | 3  | mA     | DI = 0.0V, f <sub>SK</sub> = 1MHz<br>V <sub>CC</sub> = 5.0V, CS = 5.0V,<br>Output Open |
| I <sub>SB</sub>                      | Power Supply Current (Standby)            |                           |      | 50   | µA     | CS = 0V  |
| I <sub>LI</sub>                      | Input Leakage Current                     |                           |      | 2  | µA     |  |
| I <sub>LO</sub>                      | Output Leakage Current                    |                           |      | 10   | µA     | V <sub>OUT</sub> = 0V to V <sub>CC</sub> ,<br>CS = 0V                                  |
| V <sub>IL1</sub><br>V <sub>IH1</sub> | Input Low Voltage<br>Input High Voltage   | -0.1<br>2                 |      | 0.8<br>V <sub>CC</sub> +1                  | V<br>V | 4.5V ≤ V <sub>CC</sub> < 5.5V  |
| V <sub>IL2</sub><br>V <sub>IH2</sub> | Input Low Voltage<br>Input High Voltage   | 0<br>V <sub>CC</sub> X0.7 |      | V <sub>CC</sub> X0.2<br>V <sub>CC</sub> +1 | V<br>V | 1.8V ≤ V <sub>CC</sub> < 2.7V  |
| V <sub>OL1</sub><br>V <sub>OH1</sub> | Output Low Voltage<br>Output High Voltage | 2.4                       |      | 0.4  | V<br>V | 4.5V ≤ V <sub>CC</sub> < 5.5V<br>I <sub>OL</sub> = 2.1mA<br>I <sub>OH</sub> = -400µA   |
| V <sub>OL2</sub><br>V <sub>OH2</sub> | Output Low Voltage<br>Output High Voltage | V <sub>CC</sub> -0.2      |      | 0.2  | V<br>V | 1.8V ≤ V <sub>CC</sub> < 2.7V<br>I <sub>OL</sub> = 1mA<br>I <sub>OH</sub> = -100µA     |

**Note:**

- (1) The minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V<sub>CC</sub> +0.5V, which may overshoot to V<sub>CC</sub> +2.0V for periods of less than 20 ns.
- (2) Output shorted for no more than one second. No more than one output shorted at a time.
- (3) This parameter is tested initially and after a design or process change that affects the parameter.
- (4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1V to V<sub>CC</sub> +1V.

**PIN CAPACITANCE**

| Symbol                          | Test                           | Max. | Units | Conditions           |
|---------------------------------|--------------------------------|------|-------|----------------------|
| C <sub>OUT</sub> <sup>(1)</sup> | OUTPUT CAPACITANCE (DO)        | 5    | pF    | V <sub>OUT</sub> =OV |
| C <sub>IN</sub> <sup>(1)</sup>  | INPUT CAPACITANCE (CS, SK, DI) | 5    | pF    | V <sub>IN</sub> =OV  |

Note:

(1) This parameter is tested initially and after a design or process change that affects the parameter.

**INSTRUCTION SET**

| Instruction | Device Type           | Start Bit | Opcode | Address x16 | Data x16 | PE <sup>(1)</sup> | Comments            |
|-------------|-----------------------|-----------|--------|-------------|----------|-------------------|---------------------|
| READ        | 93C46A                | 1         | 10     | A5-A0       |          |                   | Read Address AN-A0  |
|             | 93C56A <sup>(2)</sup> | 1         | 10     | A7-A0       |          |                   |                     |
|             | 93C66A                | 1         | 10     | A7-A0       |          |                   |                     |
|             | 93C86A                | 1         | 10     | A9-A0       |          | X                 |                     |
| ERASE       | 93C46A                | 1         | 11     | A5-A0       |          |                   | Clear Address AN-A0 |
|             | 93C56A <sup>(2)</sup> | 1         | 11     | A7-A0       |          |                   |                     |
|             | 93C66A                | 1         | 11     | A7-A0       |          |                   |                     |
|             | 93C86A                | 1         | 11     | A9-A0       |          | 1                 |                     |
| WRITE       | 93C46A                | 1         | 01     | A5-A0       | D15-D0   |                   | Write Address AN-A0 |
|             | 93C56A <sup>(2)</sup> | 1         | 01     | A7-A0       | D15-D0   |                   |                     |
|             | 93C66A                | 1         | 01     | A7-A0       | D15-D0   |                   |                     |
|             | 93C86A                | 1         | 01     | A9-A0       | D15-D0   | 1                 |                     |
| EWEN        | 93C46A                | 1         | 00     | 11XXXX      |          |                   | Write Enable        |
|             | 93C56A                | 1         | 00     | 11XXXXXX    |          |                   |                     |
|             | 93C66A                | 1         | 00     | 11XXXXXX    |          |                   |                     |
|             | 93C86A                | 1         | 00     | 11XXXXXXXX  |          | X                 |                     |
| EWDS        | 93C46A                | 1         | 00     | 00XXXX      |          |                   | Write Disable       |
|             | 93C56A                | 1         | 00     | 00XXXXXX    |          |                   |                     |
|             | 93C66A                | 1         | 00     | 00XXXXXX    |          |                   |                     |
|             | 93C86A                | 1         | 00     | 00XXXXXXXX  |          | X                 |                     |
| ERAL        | 93C46A                | 1         | 00     | 10XXXX      |          |                   | Clear All Addresses |
|             | 93C56A                | 1         | 00     | 10XXXXXX    |          |                   |                     |
|             | 93C66A                | 1         | 00     | 10XXXXXX    |          |                   |                     |
|             | 93C86A                | 1         | 00     | 10XXXXXXXX  |          | 1                 |                     |
| WRAL        | 93C46A                | 1         | 00     | 01XXXX      | D15-D0   |                   | Write All Addresses |
|             | 93C56A                | 1         | 00     | 01XXXXXX    | D15-D0   |                   |                     |
|             | 93C66A                | 1         | 00     | 01XXXXXX    | D15-D0   |                   |                     |
|             | 93C86A                | 1         | 00     | 01XXXXXXXX  | D15-D0   | 1                 |                     |

Note:

(1) Only applicable to 93C86A

(2) Address bit A7 is "Don't Care" bit, but must be kept at either a "1" or "0" for Read, Write and Erase Commands.

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A.C. CHARACTERISTICS

| SYMBOL                         | PARAMETER                    | Limits                     |      |   |      |                             |      | UNITS | Test Conditions        |
|--------------------------------|------------------------------|----------------------------|------|---|------|-----------------------------|------|-------|------------------------|
|                                |                              | V <sub>CC</sub> = 1.8V-6V* |      | V <sub>CC</sub> = 2.7V -6V<br>V <sub>CC</sub> = 2.5V-6V |      | V <sub>CC</sub> = 4.5V-5.5V |      |       |                        |
|                                |                              | Min.                       | Max. | Min.  | Max. | Min.                        | Max. |       |                        |
| t <sub>CSS</sub>               | CS Setup Time                | 200                        |      | 100   |      | 50                          |      | ns    | C <sub>L</sub> = 100pF |
| t <sub>CSH</sub>               | CS Hold Time                 | 0                          |      | 0   |      | 0                           |      | ns    |                        |
| t <sub>DIS</sub>               | DI Setup Time                | 400                        |      | 200   |      | 100                         |      | ns    |                        |
| t <sub>DIH</sub>               | DI Hold Time                 | 400                        |      | 200   |      | 100                         |      | ns    |                        |
| t <sub>PD1</sub>               | Output Delay to 1            |                            | 1    |   | 0.5  |                             | 0.25 | μs    |                        |
| t <sub>PD0</sub>               | Output Delay to 0            |                            | 1    |   | 0.5  |                             | 0.25 | μs    |                        |
| t <sub>HZ</sub> <sup>(1)</sup> | Output Delay to High-Z       |                            | 400  |   | 200  |                             | 100  | ns    |                        |
| t <sub>EW</sub>                | Program/Erase Pulse Width    |                            | 10   |   | 10   |                             | 10   | ms    |                        |
| t <sub>CSMIN</sub>             | Minimum CS Low Time          | 1                          |      | 0.5   |      | 0.25                        |      | μs    |                        |
| t <sub>SKHI</sub>              | Minimum SK High Time         | 1                          |      | 0.5   |      | 0.25                        |      | μs    |                        |
| t <sub>SKLOW</sub>             | Minimum SK Low Time          | 1                          |      | 0.5   |      | 0.25                        |      | μs    |                        |
| t <sub>SV</sub>                | Output Delay to Status Valid |                            | 1    |   | 0.5  |                             | 0.25 | μs    |                        |
| SK <sub>MAX</sub>              | Maximum Clock Frequency      | DC                         | 250  | DC  | 500  | DC                          | 1000 | KHZ   |                        |

\* Preliminary data for 93C56A/66A/86A.

NOTE:

(1) This parameter is tested initially and after a design or process change that affects the parameter.

**DEVICE OPERATION**

The CAT93C46A/56A/66A/86A is a 1024/2048/4096/16384-bit nonvolatile memory intended for use with industry standard microprocessors. The CAT93C46A/56A/66A/86A is organized as registers of 16-bits. Therefore, seven 9-bit instructions for 93C46A; seven 11-bit instructions for 93C56A and 93C66A; seven 13-bit instructions for 93C86A, control the reading, writing and erase operations of the device. The CAT93C46A/56A/66A/86A operates on a single supply and will generate on chip, the high voltage required during any write operation.

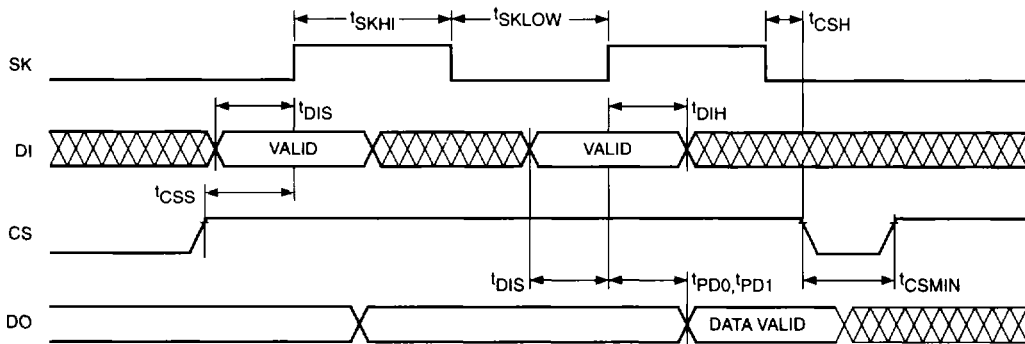
Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after the start of a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

The format for all instructions sent to the device is a logical "1" start bit, a 2-bit (or 4-bit) opcode, 6-bit (93C46A)/ 8-bit (93C56A or 93C66A)/10-bit (93C86A) and for write operations a 16-bit data field.

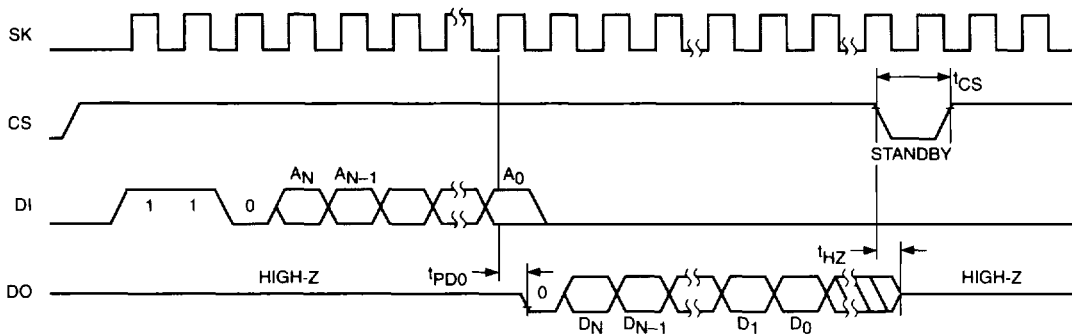
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**Figure 1. Synchronous Data Timing**



5040 FHD F03

**Figure 2. Read Instruction Timing**



5040 FHD F04

**Read**

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93C46A/56A/66A/86A will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay ( $t_{PD0}$  or  $t_{PD1}$ ).

**Write**

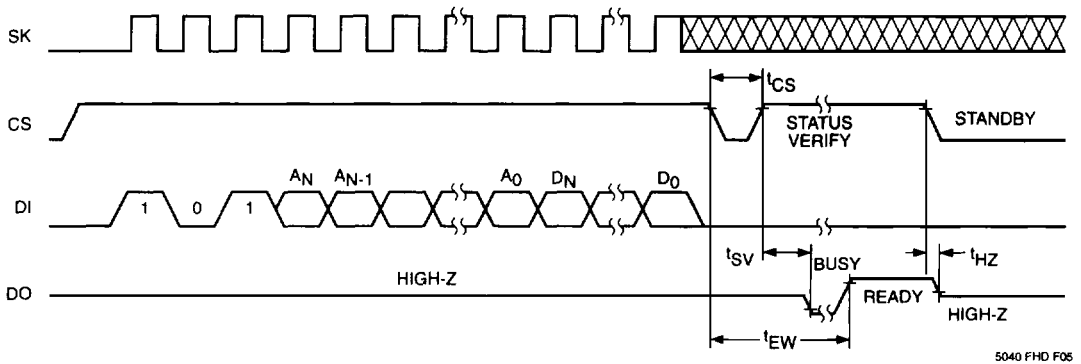
After receiving a WRITE command, address and the data, the CS (Chip Select) pin must be deselected for a minimum of 250ns ( $t_{CSMIN}$ ). The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of

the CAT93C46A/56A/66A/86A can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before it is written into.

**Erase**

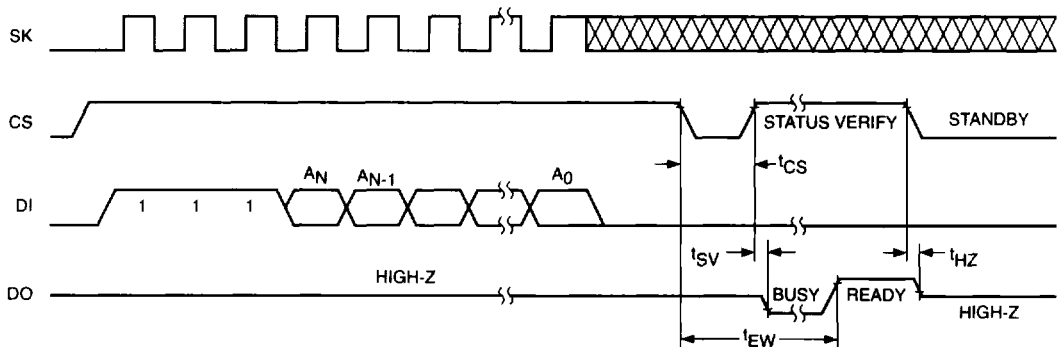
Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deasserted for a minimum of 250ns ( $t_{CSMIN}$ ). The falling edge of CS will start the self clocking clear cycle of the selected memory location. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46A/56A/66A/86A can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

**Figure 3. Write Instruction Timing**



5040 FHD F05

**Figure 4. Erase Instruction Timing**



5040 FHD F07

**Erase/Write Enable and Disable**

The CAT93C46A/56A/66A/86A powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

**Erase All**

Upon receiving an ERAL command, the CS (Chip Select) pin must be deselected for a minimum of 250ns ( $t_{CSMIN}$ ). The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46A/56A/66A/86A can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

status of the CAT93C46A/56A/66A/86A can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

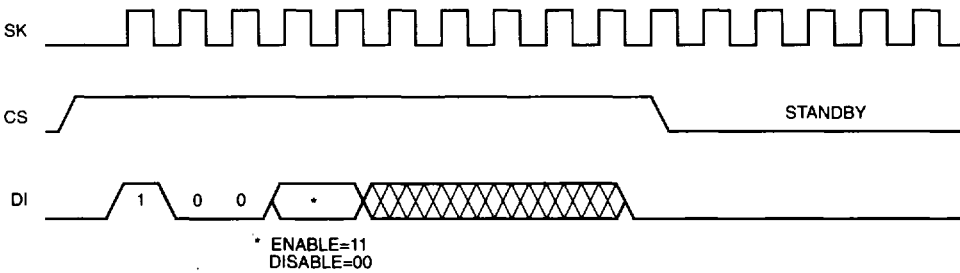
**Write All**

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of 250ns ( $t_{CSMIN}$ ). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46A/56A/66A/86A can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

Note: This note is applicable only to 93C86A. The write, erase, write all and erase all instruction requires PE=1 for 93C86A. If PE is left floating, 93C86A is in program enabled mode.

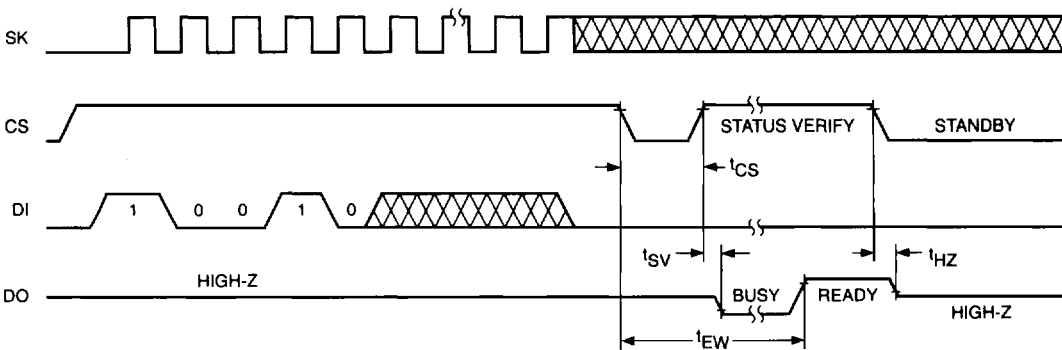
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**Figure 5. EWEN/EWDS Instruction Timing**



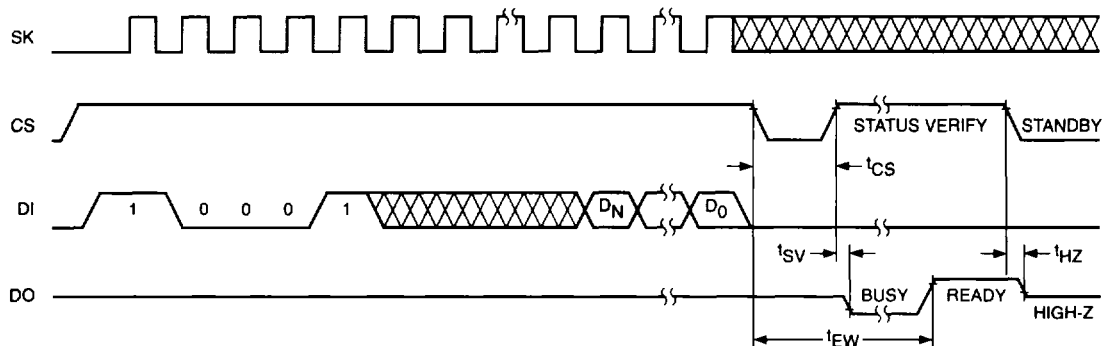
93C46/56/66 F07

**Figure 6. ERAL Instruction Timing**



5040 FHD F08

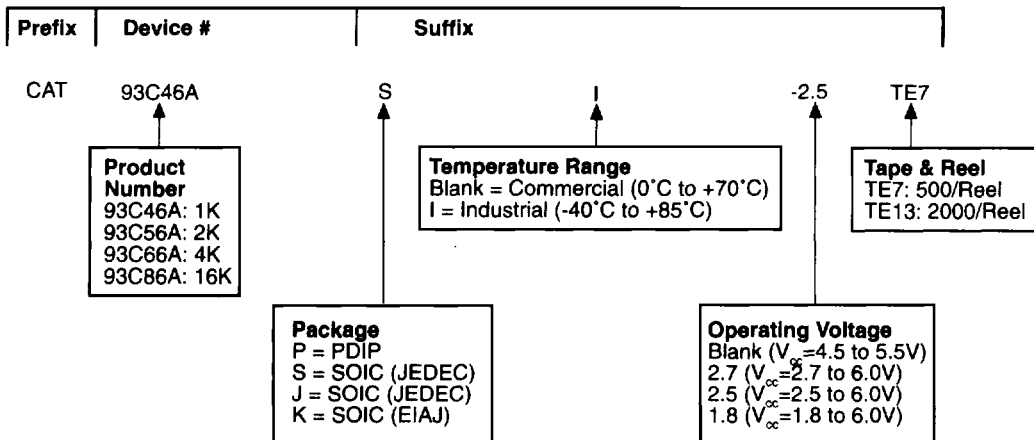
Figure 7. WRAL Instruction Timing



93C46/56/66 F09

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ORDERING INFORMATION



93C46/56/66 F10

Notes:

(1) The device used in the above example is a 93C46ASI-2.5TE7 (SOIC, Industrial Temperature, 2.5 Volt to 6 Volt Operating Voltage, Tape & Reel)