PRELIMINARY DATA SHEET

MOS INTEGRATED CIRCUIT

μPD4811650 for Rev.E

16 M-BIT SYNCHRONOUS GRAM
256K-WORD BY 32-BIT BY 2-BANK

Description

The μPD4811650 is a synchronous graphics memory (SGRAM) organized as 262,144 words × 32 bits × 2 banks random access port.

This device can operate up to 143 MHz by using synchronous interface. Also, it has 8-column Block Write function to improve capability in graphics system.

This product is packaged in 100-pin plastic TQFP (14 × 20 mm).

Features

- 262,144 words × 32 bits × 2 banks memory
- Synchronous interface (Fully synchronous DRAM with all input signals are latched at rising edge of clock)
  : Pulsed interface
  : Automatic precharge and controlled precharge commands
  : Ping-pong operation between the two internal memory banks
  : Up to 143 MHz operation frequency
- Possible to assert random column address in every cycle
- Dual internal banks controlled by A10 (Bank Address: BA)
- Byte control using DQM0 to DQM3 signals both in read and write cycle
- 8-column Block Write (BW) function
- Persistent write per bit (WPB) function
- Wrap sequence : Sequential / Interleave
- Programmable burst length (1, 2, 4, 8 and full page)
- Programmable /CAS latency (-A70R: 3, -A80, -A10, -A12: 2 and 3)
- Power Down operation and Clock Suspend operation
- Auto refresh (CBR refresh) or self refresh capability
- Single 3.3 V ± 0.3 V power supply
- LVTTL compatible inputs and outputs
- 100-pin Plastic TQFP (14 × 20 mm)
- 2,048 refresh cycles/32 ms
- Burst termination by Precharge command
- ★ Burst termination by Burst stop command

Ordering Information

Part number	Cycle time ns (MIN.)	Clock frequency MHz (MAX.)	Package
μPD4811650GF-A70R-9BT	7	143	100-pin Plastic TQFP (14 × 20 mm)
μPD4811650GF-A80-9BT	8	125	
μPD4811650GF-A10-9BT	10	100	
μPD4811650GF-A12-9BT	12	83	

The information in this document is subject to change without notice.

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The mark ★ shows major revised points.

Part Number

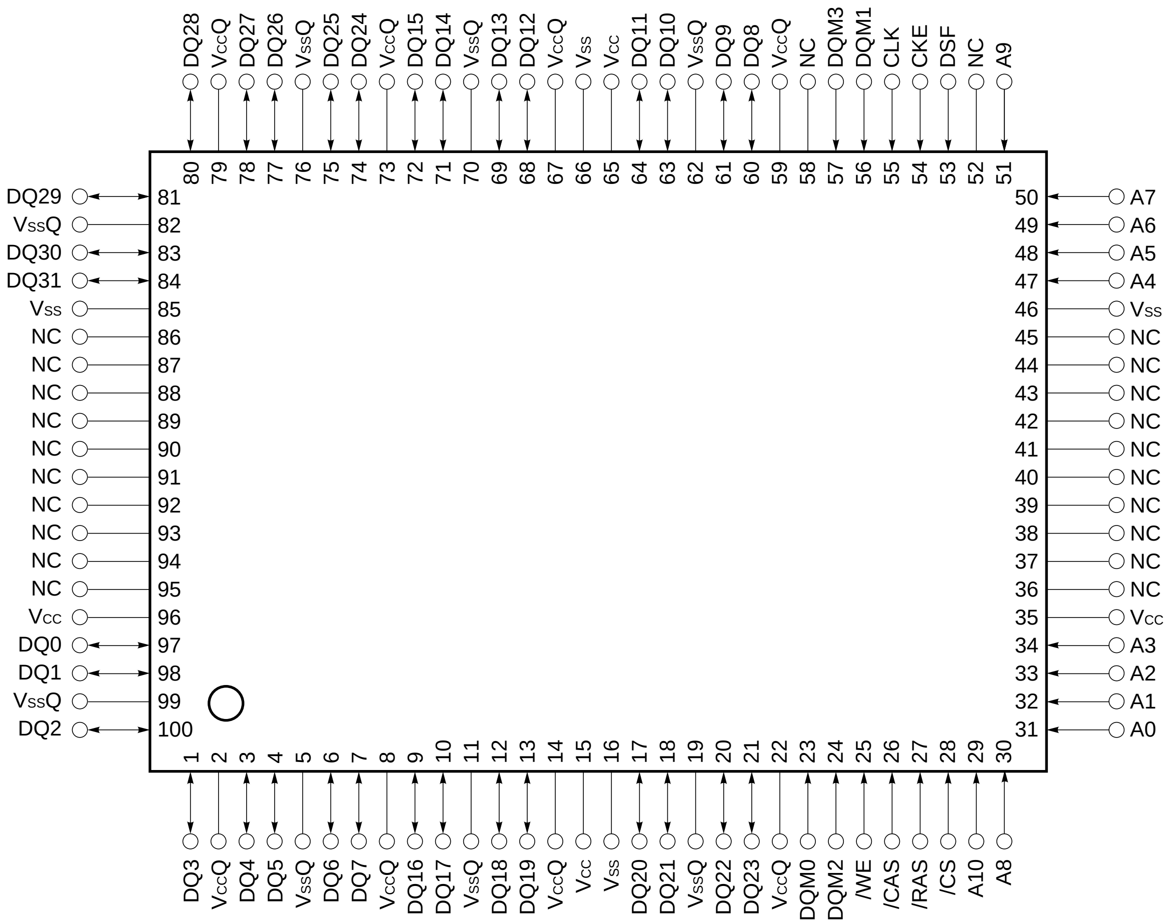
μPD48 1 16 5 0 GF - A 80

- μPD48 — NEC CMOS Application Specific Memory
- 1 — Device code
  - 1: Graphics RAM
- 16 — Capacity
  - 16: 16M bits
- 5 — Words organization
  - 5: x32
- 0 — Function
- GF — Package
  - GF: TQFP
- A — V_{CC}
  - A: 3.3 V ± 0.3 V
- 80 — Cycle time
  - 70R: 7 ns
  - 80: 8 ns
  - 10: 10 ns
  - 12: 12 ns

Pin Configuration (Marking Side)

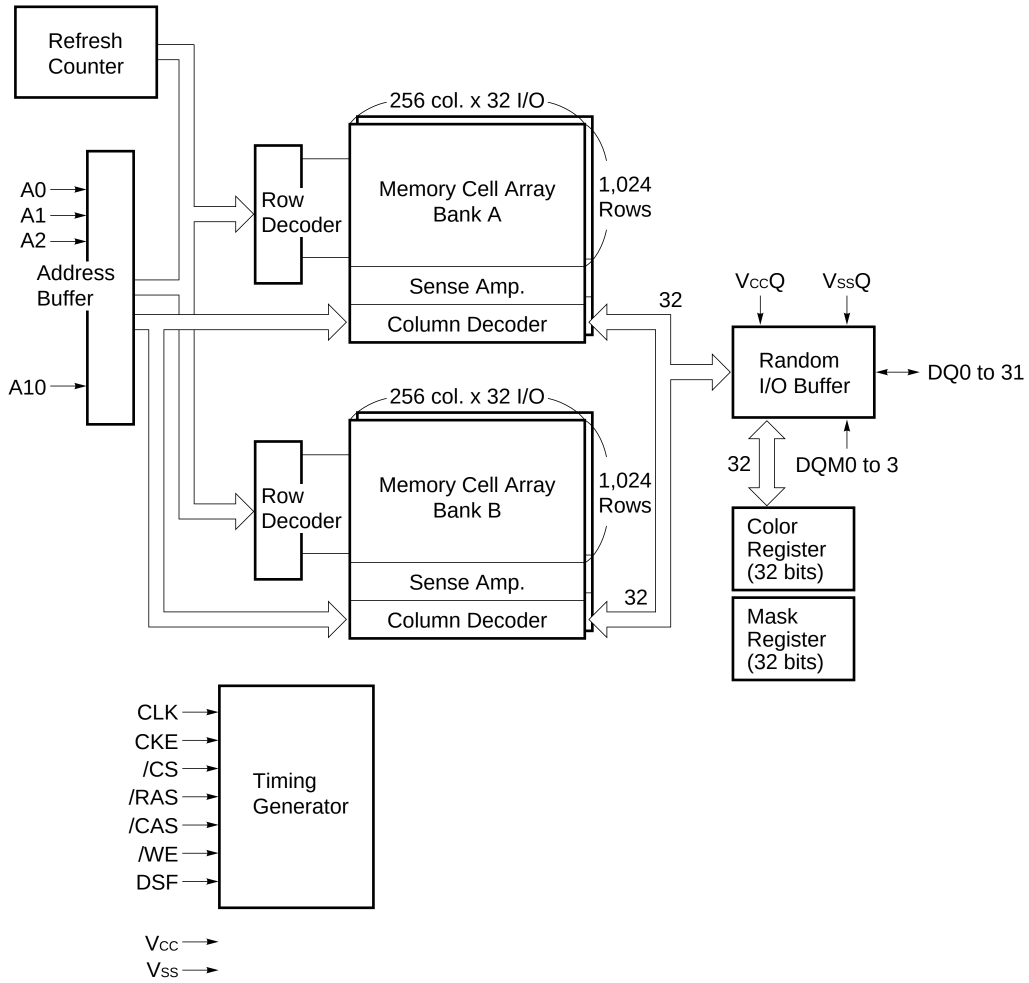
100-pin Plastic TQFP (14 × 20 mm)

μPD4811650GF-Axx-9BT



A0 - A10	:	Address inputs
A0 - A9	:	Row address inputs
A0 - A7	:	Column address inputs
A10	:	Bank address
DQ0 - DQ31	:	Data inputs/outputs
/CS	:	Chip select
/RAS	:	Row address strobe
/CAS	:	Column address strobe
/WE	:	Write enable
DQM0 - DQM3	:	DQ mask enable
DSF	:	Special function enable
CKE	:	Clock enable
CLK	:	System clock input
V_{CC}	:	Supply voltage
V_{SS}	:	Ground
$V_{CC}Q$	:	Supply voltage for DQ
$V_{SS}Q$	:	Ground for DQ
NC	:	No connection

Block Diagram



CONTENTS

1. Input/Output Pin Function

Pin name	Input/Output	Function
CLK	Input	CLK is the master clock input. Other inputs signals are referenced to the CLK rising edge.
CKE	Input	CKE determine validity of the next CLK (clock). If CKE is high, the next CLK rising edge is valid; otherwise it is invalid. If the CLK rising edge is invalid, the internal clock is not asserted and the μPD4811650 suspends operation. When the μPD4811650 is not in burst mode and CKE is negated, the device enters power down mode. During power down mode, CKE must remain low. In Self refresh mode, low level on this pin is also used as part of the input command to specify Self refresh.
/CS	Input	/CS low starts the command input cycle. When /CS is high, commands are ignored but operations continue.
/RAS, /CAS, /WE	Input	/RAS, /CAS and /WE have the same symbols on conventional DRAM but different functions. For details, refer to the command table.
DSF	Input	DSF is part of the inputs of graphics command of the μPD4811650. If DSF is inactive (Low level), μPD4811650 operates as same as SDRAM.
A0 - A9	Input	Row Address is determined by A0 - A9 at the CLK (clock) rising edge in the activate command cycle. Column Address is determined by A0 - A7 at the CLK rising edge in the read or write command cycle. A9 defines the precharge mode. When A9 is high in the precharge command cycle, both banks are precharged; when A9 is low, only the bank selected by A10 is precharged. When A9 is high in read or write command cycle, the precharge starts automatically after the burst access.
A10		A10 is the bank address signal (BA). In command cycle, A10 low selects bank A and A10 high selects bank B.
DQM0 - DQM3	Input	DQM controls I/O buffers. DQM0 corresponds to the lowest byte (DQ0 to DQ7), DQM1 corresponds to DQ8 to DQ15, DQM2 corresponds to DQ16 to DQ23. DQM3 corresponds to DQ24 to DQ31. In read mode, DQM controls the output buffers like a conventional /OE pin. DQM high and DQM low turn the output buffers off and on, respectively. The DQM latency for the read is two clocks. In write mode, DQM controls the word mask. Input data is written to the memory cell if DQM is low but not if DQM is high. The DQM latency for the write is zero.
DQ0 - DQ31	Input/Output	DQ pins have the same function as I/O pins on a conventional DRAM. These are normally 32-bit data bus and are used for inputting and outputting data. • Function as the mask data input pins in the special register set command. Write operations can be performed after Active command with WPB (old mask data). • Functions as the column selection data input pin in the block write cycle.
V_{CC}, V_{SS}, $V_{CC}Q$, $V_{SS}Q$	(Power supply)	V_{CC} and V_{SS} are power supply pins for internal circuits. $V_{CC}Q$ and $V_{SS}Q$ are power supply pins for the output buffers.

2. Commands

Mode register set command

(/CS, /RAS, /CAS, /WE, DSF = Low)

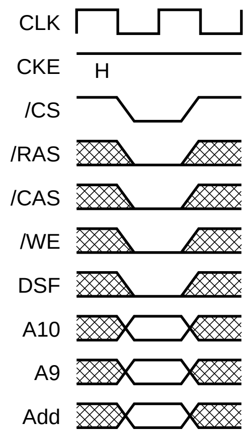
The μPD4811650 has a mode register that defines how the device operates. In this command, A0 through A10 are the data input pins. After power on, the mode register set command must be executed to initialize the device.

The mode register can be set only when both banks are in idle state.

During 2 CLK (t_{RSC}) following this command, the μPD4811650 cannot accept any other commands.

Refer to **6. Programming the Mode Register**.

Fig.1 Mode register set command



Bank activate command

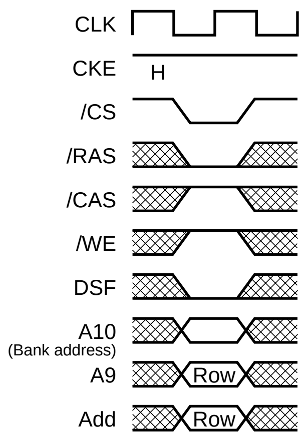
(/CS, /RAS, /DSF = Low, /CAS, /WE = High)

The μPD4811650 has two banks, each with 1,024 rows.

This command activates the bank selected by A10 (BA) and a row address selected by A0 through A9.

This command corresponds to a conventional DRAM's /RAS falling.

Fig.2 Row address strobe and bank activate command



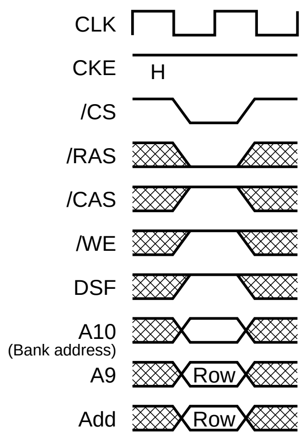
Bank activate command with WPB enable

(/CS, /RAS = Low, /CAS, /WE, /DSF = High)

This command is same as Bank activate command. After this command, write per bit function is available. Mask register's data is used as write mask data.

Refer to **12. Write/Block Write with Write Per Bit**.

Fig.3 Row address strobe and bank activate command with WPB enable



Precharge command

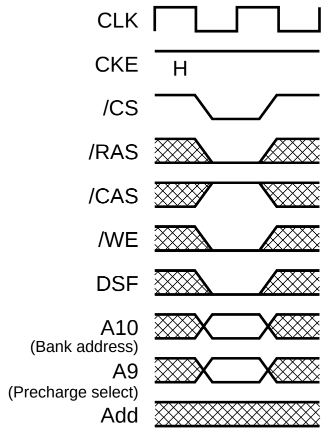
(/CS, /RAS, /WE, DSF = Low, /CAS = High)

This command begins precharge operation of the bank selected by A10 (BA) and A9. When A9 is High, both banks are precharged, regardless of A10. When A9 is Low, only the bank selected by A10 is precharged. A10 low selects bank A and A10 high selects bank B.

After this command, the μPD4811650 can't accept the activate command to the precharging bank during t_{RP} (precharge to activate command period). This command can terminate the current burst operation (2, 4, 8, full page burst length).

This command corresponds to a conventional DRAM's /RAS rising.
Refer to **10. Precharge** and **11. Auto Precharge**.

Fig.4 Precharge command

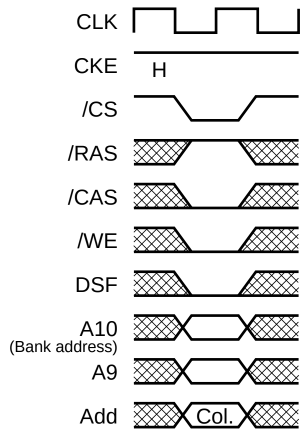


Write command

(/CS, /CAS, /WE, DSF = Low, /RAS = High)

If the mode register is in the burst write mode, this command sets the burst start address given by the column address to begin the burst write operation. The first write data must be input with this write operation. The first write data in burst mode can input with this command with subsequent data on following clocks.

Fig.5 Column address and write command

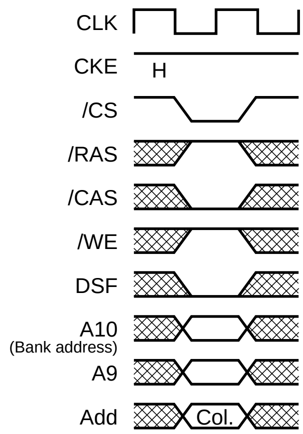


Read command

(/CS, /CAS, DSF = Low, /RAS, /WE = High)

This command sets the burst start address given by the column address.
Read data is available after /CAS latency requirements have been met.

Fig.6 Column address and read command



CBR (auto) refresh command

(/CS, /RAS, /CAS, DSF = Low, /WE, CKE = High)

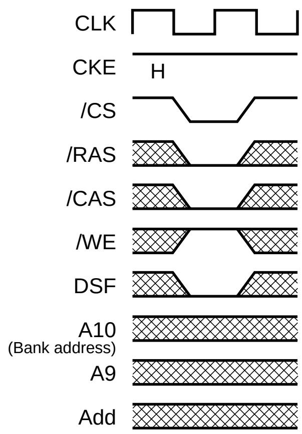
This command is a request to begin the CBR refresh operation. The refresh address is generated internally.

Before executing CBR refresh, both banks must be precharged.

After this cycle, both banks will be in the idle (precharged) state and ready for a bank activate command.

During t_{RC} period (from refresh command to refresh or activate command), the μPD4811650 cannot accept any other command.

Fig.7 CBR (auto) refresh command



Self refresh entry command

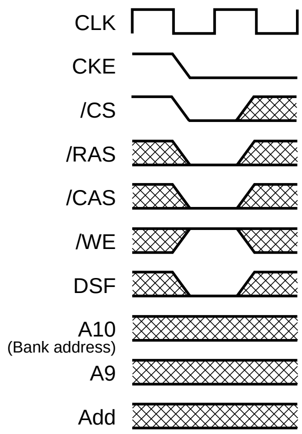
(/CS, /RAS, /CAS, DSF, CKE = Low, /WE = High)

After the command execution, self refresh operation continues while CKE remains low. When CKE goes high, the μPD4811650 exits the self refresh mode.

During self refresh mode, refresh interval and refresh operation are performed internally, so there is no need for external control.

Before executing self refresh, both banks must be precharged.

Fig.8 Self refresh entry command



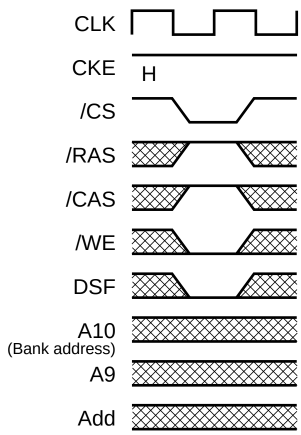
★ **Burst stop command in full page**

(/CS, /WE, DSF = Low, /RAS, /CAS = High)

This command can stop the current burst operation.

Refer to **14. Read/Write Command Interval** and **15. Burst Termination**.

Fig.9 Burst stop command in Full Page Mode

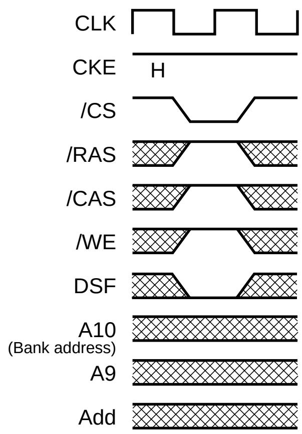


No operation

(/CS, DSF = Low, /RAS, /CAS, /WE = High)

This command is not a execution command. No operations begin or terminate by this command.

Fig.10 No operation



Special register set command

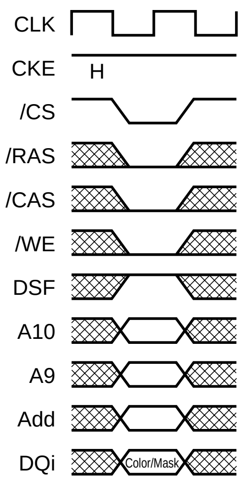
(/CS, /RAS, /CAS, /WE = Low, DSF = High)

The μPD4811650 has two special registers for graphics commands. One is color register and the other is mask register. In this command, A0 through A10 are the data input pins for the register select (color or mask register). DQ0 through DQ31 are the data input pins for the Color data or the WPB data.

During 2 CLK (t_{RSC}) following this command, the μPD4811650 can not accept any other commands.

Refer to **8. Programming the Special Register**.

Fig.11 Special register set command



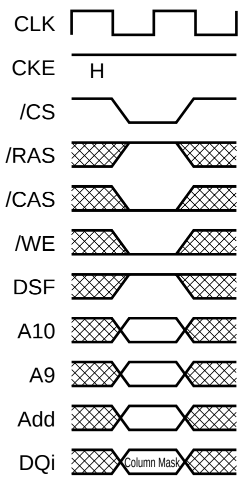
Masked block write command

(/CS, /CAS, /WE = Low, /RAS, DSF = High)

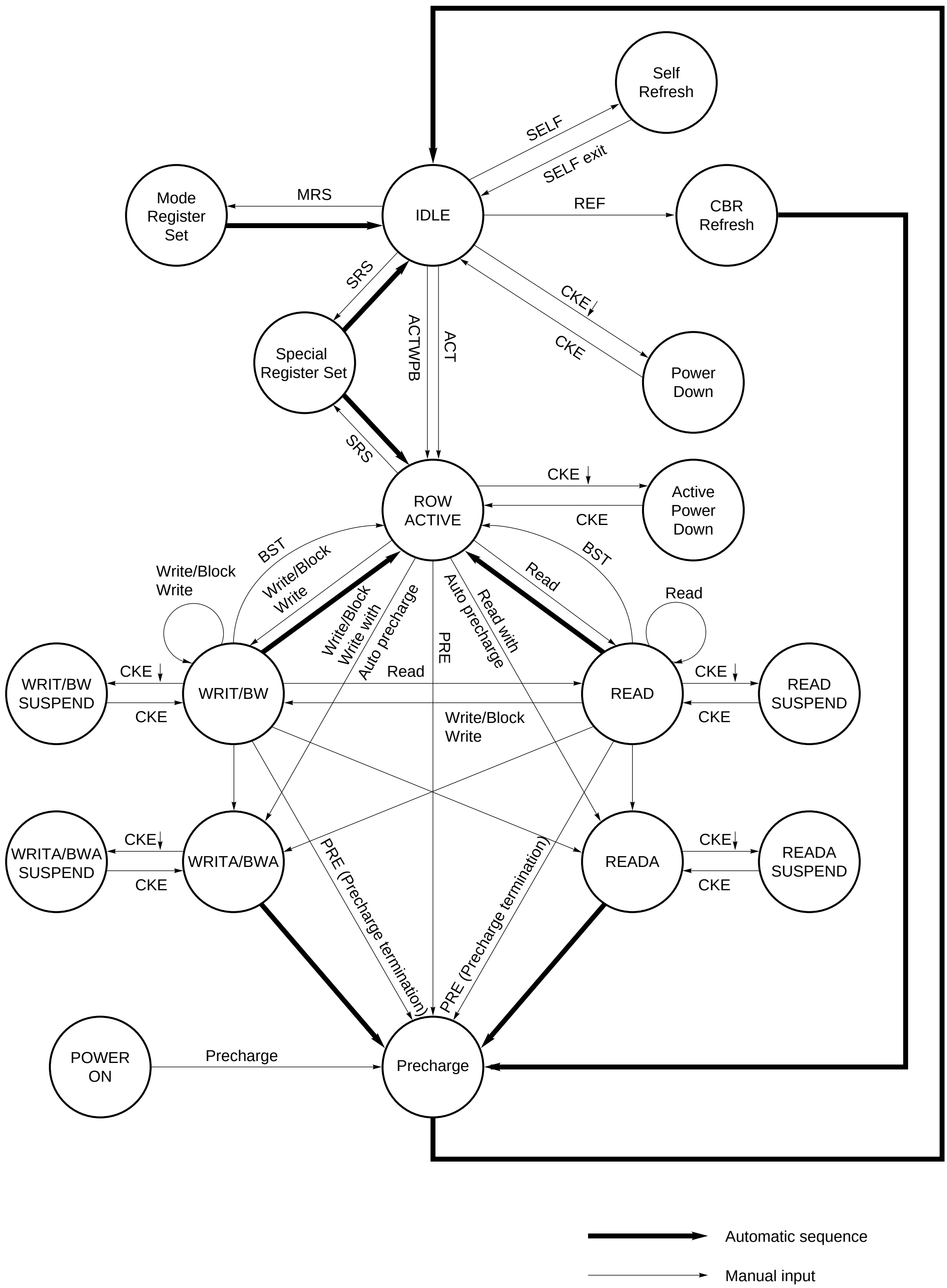
This command activates 8-column block write function. In this command, the burst length = 1. Write data comes from color register, column address mask data is input from DQi in this command.

Refer to **13. Block Write**.

Fig.12 Masked block write command



3. Simplified State Diagram



4. Truth Table

4.1 Command Truth Table

Function	Symbol	CKE		/CS	/RAS	/CAS	/WE	DSF	Address			
		n - 1	n						A10	A9	A8	A7-A0
Device deselect	DESL	H	x	H	x	x	x	x	x	x	x	x
No operation	NOP	H	x	L	H	H	H	L	x	x	x	x
Burst stop in full page	BST	H	x	L	H	H	L	L	x	x	x	x
Read	READ	H	x	L	H	L	H	L	BA	L	x	CA
Read with auto precharge	READA	H	x	L	H	L	H	L	BA	H	x	CA
Write	WRIT	H	x	L	H	L	L	L	BA	L	x	CA
Write with auto precharge	WRITA	H	x	L	H	L	L	L	BA	H	x	CA
Masked block write	BW	H	x	L	H	L	L	H	BA	L	x	CA
Masked block write with auto precharge	BWA	H	x	L	H	L	L	H	BA	H	x	CA
Bank activate	ACT	H	x	L	L	H	H	L	BA	RA		
Bank activate with WPB enable	ACTWPB	H	x	L	L	H	H	H	BA	RA		
Precharge select bank	PRE	H	x	L	L	H	L	L	BA	L	x	x
Precharge all banks	PALL	H	x	L	L	H	L	L	x	H	x	x
Mode register set	MRS	H	x	L	L	L	L	L	OP.CODE			
Special register set	SRS	H	x	L	L	L	L	H	OP.CODE			

Remark H = High level, L = Low level, x = High or Low level (Don' t care), BA = Bank address (A10), RA = Row address, CA = Column address

4.2 DQM Truth Table

Function	Symbol	CKE		DQMi
		n - 1	n	
Data write/output enable	ENBi	H	x	L
Data mask/output disable	MASKi	H	x	H

Remark H = High level, L = Low level, x = High or Low level (Don' t care), i = 0, 1, 2, 3

4.3 CKE Truth Table

Current state	Function	Symbol	CKE		/CS	/RAS	/CAS	/WE	DSF	Address
			n – 1	n						
Activating	Clock suspend mode entry		H	L	x	x	x	x	x	x
Any	Clock suspend		L	L	x	x	x	x	x	x
Clock suspend	Clock suspend mode exit		L	H	x	x	x	x	x	x
Idle	CBR refresh command	REF	H	H	L	L	L	H	L	x
Idle	Self refresh entry	SELF	H	L	L	L	L	H	L	x
Self refresh	Self refresh exit		L	H	L	H	H	H	x	x
			L	H	H	x	x	x	x	x
Idle	Power down entry		H	L	x	x	x	x	x	x
Power down	Power down exit		L	H	x	x	x	x	x	x

Remark H = High level, L = Low level, x = High or Low level (Don' t care)

4.4 Operative Command Table Note 1

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Current state	/CS	/RAS	/CAS	/WE	DSF	Address	Command	Action	Notes
Idle	H	x	x	x	x	x	DESL	Nop or Power down	2
	L	H	H	H	x	x	NOP	Nop or Power down	2
	L	H	H	L	H	x	Undefined	ILLEGAL	
	L	H	H	L	L	x	BST	ILLEGAL	3
	L	H	L	H	H	x	Undefined	ILLEGAL	
	L	H	L	H	L	BA, CA, A9	READ/READA	ILLEGAL	3
	L	H	L	L	H	BA, CA, A9	BW/BWA	ILLEGAL	3
	L	H	L	L	L	BA, CA, A9	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	H	BA, RA	ACTWPB	Bank active with WPB: Latch RA	
	L	L	H	H	L	BA, RA	ACT	Bank active: Latch RA	
	L	L	H	L	H	x	Undefined	ILLEGAL	
	L	L	H	L	L	BA, A9	PRE/PALL	Nop	11
	L	L	L	H	H	x	Undefined	ILLEGAL	
	L	L	L	H	L	x	REF/SELF	CBR refresh/Self refresh	4,12
	L	L	L	L	H	Op-Code	SRS	Special register access	
	L	L	L	L	L	Op-Code	MRS	Mode register access	12
Bank active	H	x	x	x	x	x	DESL	Nop	
	L	H	H	H	x	x	NOP	Nop	
	L	H	H	L	H	x	Undefined	ILLEGAL	
	L	H	H	L	L	x	BST	ILLEGAL	3
	L	H	L	H	H	x	Undefined	ILLEGAL	
	L	H	L	H	L	BA, CA, A9	READ/READA	Begin read; Latch CA: Determine AP	5
	L	H	L	L	H	BA, CA, A9	BW/BWA	Begin block write; Latch CA: Determine AP	5
	L	H	L	L	L	BA, CA, A9	WRIT/WRITA	Begin write; Latch CA: Determine AP	5
	L	L	H	H	H	BA, RA	ACTWPB	ILLEGAL	3
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	H	x	Undefined	ILLEGAL	
	L	L	H	L	L	BA, A9	PRE/PALL	Precharge	6
	L	L	L	H	H	x	Undefined	ILLEGAL	
	L	L	L	H	L	x	REF/SELF	ILLEGAL	
	L	L	L	L	H	Op-Code	SRS	Special register access	
	L	L	L	L	L	Op-Code	MRS	ILLEGAL	

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Current state	/CS	/RAS	/CAS	/WE	DSF	Address	Command	Action	Notes
Read	H	x	x	x	x	x	DESL	Continue burst to end → Bank active	
	L	H	H	H	x	x	NOP	Continue burst to end → Bank active	
	L	H	H	L	H	x	Undefined	ILLEGAL	
★	L	H	H	L	L	x	BST	Burst stop→Bank active	
	L	H	L	H	H	x	Undefined	ILLEGAL	
	L	H	L	H	L	BA, CA, A9	READ/READA	Term burst, new read: Determine AP	7
	L	H	L	L	H	BA, CA, A9	BW/BWA	Term burst, Start block write: Determine AP	7, 8
	L	H	L	L	L	BA, CA, A9	WRIT/WRITA	Term burst, Start write: Determine AP	7, 8
	L	L	H	H	H	BA, RA	ACTWPB	ILLEGAL	3
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	H	x	Undefined	ILLEGAL	
	L	L	H	L	L	BA, A9	PRE/PALL	Term burst, precharge timing for reads	
	L	L	L	H	H	x	Undefined	ILLEGAL	
	L	L	L	H	L	x	REF/SELF	ILLEGAL	
	L	L	L	L	H	Op-Code	SRS	ILLEGAL	
	L	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write/Block write	H	x	x	x	x	x	DESL	Continue burst to end→Write recovering	
	L	H	H	H	x	x	NOP	Continue burst to end→Write recovering	
	L	H	H	L	H	x	Undefined	ILLEGAL	
★	L	H	H	L	L	x	BST	Burst stop→Bank active	
	L	H	L	H	H	x	Undefined	ILLEGAL	
	L	H	L	H	L	BA, CA, A9	READ/READA	Term burst, start read: Determine AP	7, 8
	L	H	L	L	H	BA, CA, A9	BW/BWA	Term burst, new block write: Determine AP	7
	L	H	L	L	L	BA, CA, A9	WRIT/WRITA	Term burst, new write: Determine AP	7
	L	L	H	H	H	BA, RA	ACTWPB	ILLEGAL	3
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	H	x	Undefined	ILLEGAL	
	L	L	H	L	L	BA, A9	PRE/PALL	Term burst, precharge timing for writes	3, 9
	L	L	L	H	H	x	Undefined	ILLEGAL	
	L	L	L	H	L	x	REF/SELF	ILLEGAL	
	L	L	L	L	H	Op-Code	SRS	ILLEGAL	
	L	L	L	L	L	Op-Code	MRS	ILLEGAL	

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Current state	/CS	/RAS	/CAS	/WE	DSF	Address	Command	Action	Notes
Read with auto precharge	H	x	x	x	x	x	DESL	Continue burst to end → precharging	
	L	H	H	H	x	x	NOP	Continue burst to end → precharging	
	L	H	H	L	H	x	Undefined	ILLEGAL	
	L	H	H	L	L	x	BST	ILLEGAL	
	L	H	L	H	H	x	Undefined	ILLEGAL	
	L	H	L	H	L	BA, CA, A9	READ/READA	ILLEGAL	
	L	H	L	L	H	BA, CA, A9	BW/BWA	ILLEGAL	
	L	H	L	L	L	BA, CA, A9	WRIT/WRITA	ILLEGAL	
	L	L	H	H	H	BA, RA	ACTWPB	ILLEGAL	3
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	H	x	Undefined	ILLEGAL	
	L	L	H	L	L	BA, A9	PRE/PALL	ILLEGAL	3
	L	L	L	H	H	x	Undefined	ILLEGAL	
	L	L	L	H	L	x	REF/SELF	ILLEGAL	
	L	L	L	L	H	Op-Code	SRS	ILLEGAL	
	L	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write/Block write with auto precharge	H	x	x	x	x	x	DESL	Continue burst to end → Write recovering with auto precharge	
	L	H	H	H	x	x	NOP	Continue burst to end → Write recovering with auto precharge	
	L	H	H	L	H	x	Undefined	ILLEGAL	
	L	H	H	L	L	x	BST	ILLEGAL	
	L	H	L	H	H	x	Undefined	ILLEGAL	
	L	H	L	H	L	BA, CA, A9	READ/READA	ILLEGAL	
	L	H	L	L	H	BA, CA, A9	BW/BWA	ILLEGAL	
	L	H	L	L	L	BA, CA, A9	WRIT/WRITA	ILLEGAL	
	L	L	H	H	H	BA, RA	ACTWPB	ILLEGAL	3
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	H	x	Undefined	ILLEGAL	
	L	L	H	L	L	BA, A9	PRE/PALL	ILLEGAL	3
	L	L	L	H	H	x	Undefined	ILLEGAL	
	L	L	L	H	L	x	REF/SELF	ILLEGAL	
	L	L	L	L	H	Op-Code	SRS	ILLEGAL	
	L	L	L	L	L	Op-Code	MRS	ILLEGAL	

(4/7)

Current state	/CS	/RAS	/CAS	/WE	DSF	Address	Command	Action	Notes
Precharging	H	x	x	x	x	x	DESL	Nop → Enter idle after t_{RP}	
	L	H	H	H	x	x	NOP	Nop → Enter idle after t_{RP}	
	L	H	H	L	H	x	Undefined	ILLEGAL	
	L	H	H	L	L	x	BST	ILLEGAL	3
	L	H	L	H	H	x	Undefined	ILLEGAL	
	L	H	L	H	L	BA, CA, A9	READ/READA	ILLEGAL	3
	L	H	L	L	H	BA, CA, A9	BW/BWA	ILLEGAL	3
	L	H	L	L	L	BA, CA, A9	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	H	BA, RA	ACTWPB	ILLEGAL	3
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	H	x	Undefined	ILLEGAL	
	L	L	H	L	L	BA, A9	PRE/PALL	Nop → Enter idle after t_{RP}	11
	L	L	L	H	H	x	Undefined	ILLEGAL	
	L	L	L	H	L	x	REF/SELF	ILLEGAL	
	L	L	L	L	H	Op-Code	SRS	Special register access	
	L	L	L	L	L	Op-Code	MRS	ILLEGAL	
Bank activating	H	x	x	x	x	x	DESL	Nop → Enter bank active after t_{RCD}	
(t_{RCD})	L	H	H	H	x	x	NOP	Nop → Enter bank active after t_{RCD}	
	L	H	H	L	H	x	Undefined	ILLEGAL	
	L	H	H	L	L	x	BST	ILLEGAL	3
	L	H	L	H	H	x	Undefined	ILLEGAL	
	L	H	L	H	L	BA, CA, A9	READ/READA	ILLEGAL	3
	L	H	L	L	H	BA, CA, A9	BW/BWA	ILLEGAL	3
	L	H	L	L	L	BA, CA, A9	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	H	BA, RA	ACTWPB	ILLEGAL	3, 10
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	3, 10
	L	L	H	L	H	x	Undefined	ILLEGAL	
	L	L	H	L	L	BA, A9	PRE/PALL	ILLEGAL	3
	L	L	L	H	H	x	Undefined	ILLEGAL	
	L	L	L	H	L	x	REF/SELF	ILLEGAL	
	L	L	L	L	H	Op-Code	SRS	Special register access	
	L	L	L	L	L	Op-Code	MRS	ILLEGAL	

(5/7)

Current state	/CS	/RAS	/CAS	/WE	DSF	Address	Command	Action	Notes
Write recovering	H	x	x	x	x	x	DESL	Nop → Enter bank active after t_{DPL}	
(t_{DPL})	L	H	H	H	x	x	NOP	Nop → Enter bank active after t_{DPL}	
	L	H	H	L	H	x	Undefined	ILLEGAL	
	L	H	H	L	L	x	BST	ILLEGAL	3
	L	H	L	H	H	x	Undefined	ILLEGAL	
	L	H	L	H	L	BA, CA, A9	READ/READA	Begin read; Latch CA: Determine AP	8
	L	H	L	L	H	BA, CA, A9	BW/BWA	Begin block write; Latch CA: Determine AP	
	L	H	L	L	L	BA, CA, A9	WRIT/WRITA	Begin write; Latch CA: Determine AP	
	L	L	H	H	H	BA, RA	ACTWPB	ILLEGAL	3
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	H	x	Undefined	ILLEGAL	
	L	L	H	L	L	BA, A9	PRE/PALL	ILLEGAL	3
	L	L	L	H	H	x	Undefined	ILLEGAL	
	L	L	L	H	L	x	REF/SELF	ILLEGAL	
	L	L	L	L	H	Op-Code	SRS	Special register access	
	L	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write recovering	H	x	x	x	x	x	DESL	Nop → Enter precharge after t_{DPL}	
with auto	L	H	H	H	x	x	NOP	Nop → Enter precharge after t_{DPL}	
precharge	L	H	H	L	H	x	Undefined	ILLEGAL	
	L	H	H	L	L	x	BST	ILLEGAL	
	L	H	L	H	H	x	Undefined	ILLEGAL	
	L	H	L	H	L	BA, CA, A9	READ/READA	ILLEGAL	3, 8
	L	H	L	L	H	BA, CA, A9	BW/BWA	ILLEGAL	3
	L	H	L	L	L	BA, CA, A9	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	H	BA, RA	ACTWPB	ILLEGAL	3
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	H	x	Undefined	ILLEGAL	
	L	L	H	L	L	BA, A9	PRE/PALL	ILLEGAL	3
	L	L	L	H	H	x	Undefined	ILLEGAL	
	L	L	L	H	L	x	REF/SELF	ILLEGAL	
	L	L	L	L	H	Op-Code	SRS	Special register access	
	L	L	L	L	L	Op-Code	MRS	ILLEGAL	

(6/7)

Current state	/CS	/RAS	/CAS	/WE	DSF	Address	Command	Action	Notes
Refreshing	H	x	x	x	x	x	DESL	Nop → Enter idle after tRC	
	L	H	H	H	x	x	NOP	Nop → Enter idle after tRC	
	L	H	H	L	H	x	Undefined	ILLEGAL	
	L	H	H	L	L	x	BST	ILLEGAL	
	L	H	L	H	H	x	Undefined	ILLEGAL	
	L	H	L	H	L	BA, CA, A9	READ/READA	ILLEGAL	
	L	H	L	L	H	BA, CA, A9	BW/BWA	ILLEGAL	
	L	H	L	L	L	BA, CA, A9	WRIT/WRITA	ILLEGAL	
	L	L	H	H	H	BA, RA	ACTWPB	ILLEGAL	
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	
	L	L	H	L	H	x	Undefined	ILLEGAL	
	L	L	H	L	L	BA, A9	PRE/PALL	ILLEGAL	
	L	L	L	H	H	x	Undefined	ILLEGAL	
	L	L	L	H	L	x	REF/SELF	ILLEGAL	
	L	L	L	L	H	Op-Code	SRS	ILLEGAL	
	L	L	L	L	L	Op-Code	MRS	ILLEGAL	
Mode register accessing	H	x	x	x	x	x	DESL	Nop → Enter idle after tRSC	
	L	H	H	H	x	x	NOP	Nop → Enter idle after tRSC	
	L	H	H	L	H	x	Undefined	ILLEGAL	
	L	H	H	L	L	x	BST	ILLEGAL	
	L	H	L	H	H	x	Undefined	ILLEGAL	
	L	H	L	H	L	BA, CA, A9	READ/READA	ILLEGAL	
	L	H	L	L	H	BA, CA, A9	BW/BWA	ILLEGAL	
	L	H	L	L	L	BA, CA, A9	WRIT/WRITA	ILLEGAL	
	L	L	H	H	H	BA, RA	ACTWPB	ILLEGAL	
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	
	L	L	H	L	H	x	Undefined	ILLEGAL	
	L	L	H	L	L	BA, A9	PRE/PALL	ILLEGAL	
	L	L	L	H	H	x	Undefined	ILLEGAL	
	L	L	L	H	L	x	REF/SELF	ILLEGAL	
	L	L	L	L	H	Op-Code	SRS	ILLEGAL	
	L	L	L	L	L	Op-Code	MRS	ILLEGAL	

(7/7)

Current state	/CS	/RAS	/CAS	/WE	DSF	Address	Command	Action	Notes
Special mode register accessing	H	x	x	x	x	x	DESL	Nop → Enter previous state after t_{RSC}	
	L	H	H	H	x	x	NOP	Nop → Enter previous state after t_{RSC}	
	L	H	H	L	H	x	Undefined	ILLEGAL	
	L	H	H	L	L	x	BST	ILLEGAL	
	L	H	L	H	H	x	Undefined	ILLEGAL	
	L	H	L	H	L	BA, CA, A9	READ/READA	ILLEGAL	
	L	H	L	L	H	BA, CA, A9	BW/BWA	ILLEGAL	
	L	H	L	L	L	BA, CA, A9	WRIT/WRITA	ILLEGAL	
	L	L	H	H	H	BA, RA	ACTWPB	ILLEGAL	
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	
	L	L	H	L	H	x	Undefined	ILLEGAL	
	L	L	H	L	L	BA, A9	PRE/PALL	ILLEGAL	
	L	L	L	H	H	x	Undefined	ILLEGAL	
	L	L	L	H	L	x	REF/SELF	ILLEGAL	
	L	L	L	L	H	Op-Code	SRS	ILLEGAL	
	L	L	L	L	L	Op-Code	MRS	ILLEGAL	

Notes 1. All entries assume that CKE was active (High level) during the preceding clock cycle.

2. If both banks are idle, and CKE is inactive (Low level), μPD4811650 will enter Power down mode. All input buffers except CKE will be disabled.

3. Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.

4. If both banks are idle, and CKE is inactive (Low level), μPD4811650 will enter Self refresh. All input buffers except CKE will be disabled.

5. Illegal if t_{RCD} is not satisfied.

6. Illegal if t_{RAS} is not satisfied.

7. Must satisfy burst interrupt condition.

8. Must satisfy bus contention, bus turn around, and/or write recovery requirements.

9. Must mask preceding data which don't satisfy t_{DPL}.

10. Illegal if t_{RRD} is not satisfied.

11. Nop to bank precharging or in idle state. May precharge bank(s) indicated by BA (and A9).

12. Illegal if any bank is not idle.

Remark H = High level, L = Low level, x = High or Low level (Don't care), V = Valid Data input,
BA = Bank address (A10), A9 = Precharge select, RA = Row address, CA = Column address,
Term = Terminate, AP = Auto precharge, NOP = No operation,
ILLEGAL = Device operation and/or data-integrity are not guaranteed

4.5 Command Truth Table for CKE

Current state	CKE n-1	CKE n	/CS	/RAS	/CAS	/WE	DSF	Address	Action	Notes
Self refresh (S.R.)	H	x	x	x	x	x	x	x	INVALID, CLK(n–1) would exit S.R.	
	L	H	H	x	x	x	x	x	S.R. Recovery	
	L	H	L	H	H	x	x	x	S.R. Recovery	
	L	H	L	H	L	x	x	x	ILLEGAL	
	L	H	L	L	x	x	x	x	ILLEGAL	
	L	L	x	x	x	x	x	x	Maintain S.R.	
Self refresh recovery	H	H	H	x	x	x	x	x	Idle after t_{RC}	
	H	H	L	H	H	x	x	x	Idle after t_{RC}	
	H	H	L	H	L	x	x	x	ILLEGAL	
	H	H	L	L	x	x	x	x	ILLEGAL	
	H	L	H	x	x	x	x	x	ILLEGAL	
	H	L	L	H	H	x	x	x	ILLEGAL	
	H	L	L	H	L	x	x	x	ILLEGAL	
	H	L	L	L	x	x	x	x	ILLEGAL	
Power down (P.D.)	H	x	x	x	x	x	x	x	INVALID, CLK(n–1) would exit P.D.	
	L	H	x	x	x	x	x	x	EXIT P.D. → Idle	
	L	L	x	x	x	x	x	x	Maintain power down mode	
Both banks idle	H	H	H	x	x	x	x	x	Refer to operations in Operative Command Table	
	H	H	L	H	x	x	x	x	Refer to operations in Operative Command Table	
	H	H	L	L	H	x	x	x	Refer to operations in Operative Command Table	
	H	H	L	L	L	H	L	x	Refresh	
	H	H	L	L	L	L	x	Op-Code	Refer to operations in Operative Command Table	
	H	L	H	x	x	x	x	x	Refer to operations in Operative Command Table	
	H	L	L	H	x	x	x	x	Refer to operations in Operative Command Table	
	H	L	L	L	H	x	x	x	Refer to operations in Operative Command Table	
	H	L	L	L	L	H	L	x	Self refresh	1
	H	L	L	L	L	L	x	Op-Code	Refer to operations in Operative Command Table	
	L	x	x	x	x	x	x	x	Power down	1
Row active	H	x	x	x	x	x	x	x	Refer to operations in Operative Command Table	
	L	x	x	x	x	x	x	x	Power down	2
Any state other than listed above	H	H	x	x	x	x	x	x	Refer to operations in Operative Command Table	
	H	L	x	x	x	x	x	x	Begin clock suspend next cycle	2
	L	H	x	x	x	x	x	x	Exit clock suspend next cycle	
	L	L	x	x	x	x	x	x	Maintain clock suspend	

Notes 1. Self refresh can be entered only from the both banks idle state. Power down can be entered from the both banks idle state or row active state.

2. Must be legal command as defined in Operative Command Table.

Remark H = High level, L = Low level, x = High or Low level (Don't care)

4.6 Command Truth Table for Two Banks Operation

/CS	/RAS	/CAS	/WE	DSF	A10(BA)	A9	A8 - A0	Action	"FROM"State[Note1]	"TO"State[Note2]
H	x	x	x	x	x	x	x	NOP	Any	Any
L	H	H	H	L	x	x	x	NOP	Any	Any
L	H	H	L	L	x	x	x	BST	(R/W/A)0(I/A)1	A0(I/A)1
									I0(I/A)1	I0(I/A)1
									(R/W/A)1(I/A)0	A1(I/A)0
									I1(I/A)0	I1(I/A)0
L	H	L	H	L	H	H	CA	Read	(R/W/A)1(I/A)0	RP1(I/A)0
					H	H	CA		A1(R/W)0	RP1A0
					H	L	CA		(R/W/A)1(I/A)0	R1(I/A)0
					H	L	CA		A1(R/W)0	R1A0
					L	H	CA		(R/W/A)0(I/A)1	RP0(I/A)1
					L	H	CA		A0(R/W)1	RP0A1
					L	L	CA		(R/W/A)0(I/A)1	R0(I/A)1
					L	L	CA		A0(R/W)1	R0A1
L	H	L	L	L/H	H	H	CA	Write/Block Write	(R/W/A)1(I/A)0	WP1(I/A)0
					H	H	CA		A1(R/W)0	WP1A0
					H	L	CA		(R/W/A)1(I/A)0	W1(I/A)0
					H	L	CA		A1(R/W)0	W1A0
					L	H	CA		(R/W/A)0(I/A)1	WP0(I/A)1
					L	H	CA		A0(R/W)1	WP0A1
					L	L	CA		(R/W/A)0(I/A)1	W0(I/A)1
					L	L	CA		A0(R/W)1	W0A1
L	L	H	H	L/H	H	RA		Active Row	I1Any0	A1Any0
					L	RA			I0Any1	A0Any1
L	L	H	L	L	x	H	x	Precharge	(R/W/A/I)0(I/A)1	I0I1
					x	H	x		(R/W/A/I)1(I/A)0	I1I0
					H	L	x		(R/W/A/I)1(I/A)0	I1(I/A)0
					H	L	x		(I/A)(R/W/A/I)0	I1(R/W/A/I)0
					L	L	x		(R/W/A/I)0(I/A)1	I0(I/A)1
					L	L	x		(I/A)0(R/W/A/I)1	I0(R/W/A/I)1
L	L	L	H	L	x	x	x	Refresh	I0I1	I0I1
L	L	L	L	L	Op-Code			Mode Register Access	I0I1	I0I1
L	L	L	L	H	Op-Code			Special Register Access	(I/A)0(I/A)1	(I/A)0(I/A)1

Notes **1.** If the μPD4811650 is in a state other than above listed in the "FROM" State column, the command is illegal.

2. The states listed under "TO" might not be entered on the next clock cycle.
Timing restrictions apply.

Remark H = High level, L = Low level, x = High or Low level (Don't care),
BA = Bank address (A10)
State abbreviations
I = Idle
A = Bank active
R = Read with No precharge (No precharge is posted)
W = Write with No precharge (No precharge is posted)
RP = Read with auto precharge (Precharge is posted)
WP = Write with auto precharge (Precharge is posted)
Any = Any State
X0Y1 = Bank0 is in state “X”, Bank1 = in state “Y”
(X/Y)0Z1 = Z1(X/Y)0 = Bank0 is in state “X” or “Y”, Bank1 is in state “Z”

5. Initialization

The synchronous GRAM is initialized in the power-on sequence according to the following.

(1) Apply power and start clock. Attempt to maintain CKE = “H”, DQM = “H”, and NOP or DESL condition at the inputs.

(2) Maintain stable power, stable clock, CKE = “H”, DQM = “H”, and NOP or DESL condition for a minimum of 100 μs.

(3) Issue precharge commands for all banks of the device.

(4) Issue a mode register set command to initialize the mode register.

(5) Issue two or more auto refresh commands.

The device is now in the IDLE state and is ready for normal operation.

Remarks **1.** The sequence of Mode register programming and Refresh above may be transposed.
2. The data bus is guaranteed to be high impedance after waiting a minimum of 100 μs (Refer to step (2) above). It is recommended to maintain CKE and DQM high until the Precharge command is issued.

6. Programming the Mode Register

The mode register is programmed by the Mode register set command using address bits A10 through A0 as data inputs. The register retains data until it is reprogrammed or the device loses power.

The mode register has four fields;

Options	: A10 through A7
/CAS latency	: A6 through A4
Wrap type	: A3
Burst length	: A2 through A0

Following mode register programming, no command can be asserted before at least 2 CLK (t_{RSC}) have elapsed.

/CAS Latency

/CAS latency is the most critical of the parameters being set. It tells the device how many clocks must elapse before the data will be available.

The value is determined by the frequency of the clock and the speed grade of the device. The table in **16.2 Relationship between Frequency and Latency** shows the relationship of /CAS latency to the clock period and the speed grade of the device.

Burst Length

Burst Length is the number of words that will be output or input in a read or write cycle. After a read burst is completed, the output bus will become Hi-Z.

The burst length is programmable as 1, 2, 4, 8 or full page (256 columns).

Wrap Type (Burst Sequence)

The wrap type specifies the order in which the burst data will be addressed. The μPD4811650 supports “Sequential mode” and “Interleave mode”.

The table in **7.1 Burst Length and Sequence** shows the addressing sequence for each burst length.

7. Mode Register

10	9	8	7	6	5	4	3	2	1	0	
0	0	0	1								JEDEC Standard Test Set (refresh counter test)

10	9	8	7	6	5	4	3	2	1	0	
0	1	0	0	LTMODE			WT	BL			Burst Read and Single Write (for Write Through Cache)

10	9	8	7	6	5	4	3	2	1	0	
		1	0								Use in future

10	9	8	7	6	5	4	3	2	1	0	
x	x	1	1	V	V	V	V	V	V	V	Vender Specific

V = Valid
x = Don't care

10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	LTMODE			WT	BL			Mode Register Set

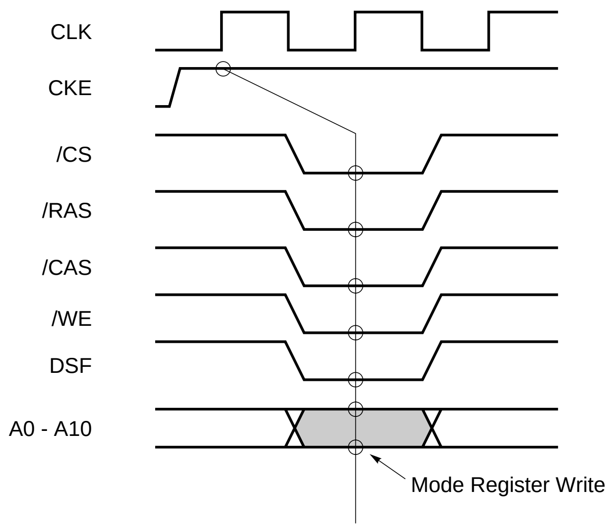
Burst length	A2-0	WT = 0	WT = 1
	000	1	1
	001	2	2
	010	4	4
	011	8	8
	100	R	R
	101	R	R
	110	R	R
	111	Full page	R

Wrap type		
	0	Sequential
	1	Interleave

Latency mode	A6-4	/CAS latency
	000	R
	001	R
	010	2
	011	3
	100	R
	101	R
	110	R
	111	R

Remark R : Reserved

Mode Register Write Timing



7.1 Burst Length and Sequence

[Burst of Two]

Starting Address (column address A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
0	0, 1	0, 1
1	1, 0	1, 0

[Burst of Four]

Starting Address (column address A1 - A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
00	0, 1, 2, 3	0, 1, 2, 3
01	1, 2, 3, 0	1, 0, 3, 2
10	2, 3, 0, 1	2, 3, 0, 1
11	3, 0, 1, 2	3, 2, 1, 0

[Burst of Eight]

Starting Address (column address A2 - A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

Full page burst is an extension of the above tables of Sequential Addressing with the length being 256.

8. Programming the Special Register

The special register is programming by the Special register set command using address bits A10 through A0 and data bits DQ0 through DQ31. The color and mask register retain data until it is reprogrammed or the device losed power.

The special register has four fields;

Reserved : A10 through A7
Color register : A6
Mask register : A5
Reserved : A4 through A0

Following special register programming, no command can be asserted before at least 2 CLK (t_{RSC}) have elapsed.

8.1 Color Register

Color register is used as write data in Block Write cycle. In Special Register set command, if A5 is "0" and A6 is "1", the color register is selected. And the data of DQ0 through DQ31 is stored to color register as color data (write data).

8.2 Mask Register

Mask register is used as write mask data in Write and Block Write cycle. In Special Register set command, if A5 is "1" and A6 is "0", the mask register is selected. And the data of DQ0 through DQ31 is stored to mask register as write mask data.

8.3 Special Register

10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	LC	LM	0	0	0	0	0

	Bits 5	Function
Mask Register	0	Not Load
	1	Load

	Bits 6	Function
Color Register	0	Not Load
	1	Load

Remark If LC and LM are both high (1), data of Mask and Color register will be unknown.

9. Address Bits of Bank Address and Precharge

Row (Activate command)

A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10

A10	
0	**Select Bank A "Activate" command**
1	**Select Bank B "Activate" command**

(Precharge command)

A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10

A9	A10	**Result**
0	0	**Precharge Bank A**
0	1	**Precharge Bank B**
1	x	**Precharge All Banks**

x : Don't care

Col. (/CAS strobes)

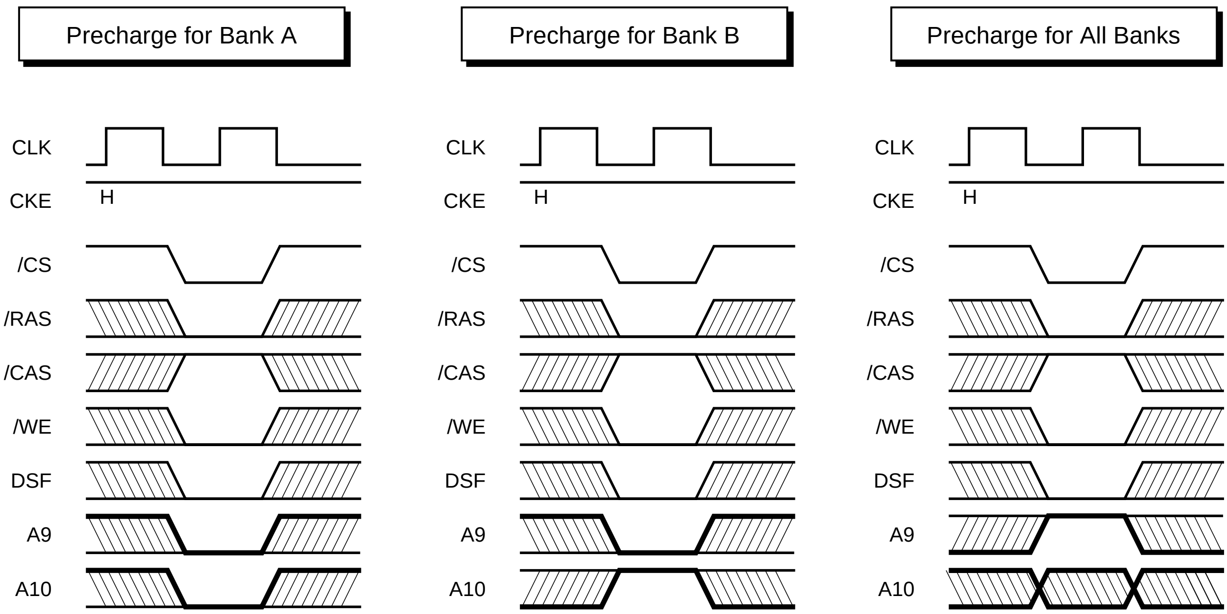
A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10

A9:

A9	
0	**disables Auto-Precharge (End of Burst)**
1	**enables Auto-Precharge (End of Burst)**

A10:

A10	
0	**enables Read/Write commands for Bank A**
1	**enables Read/Write commands for Bank B**



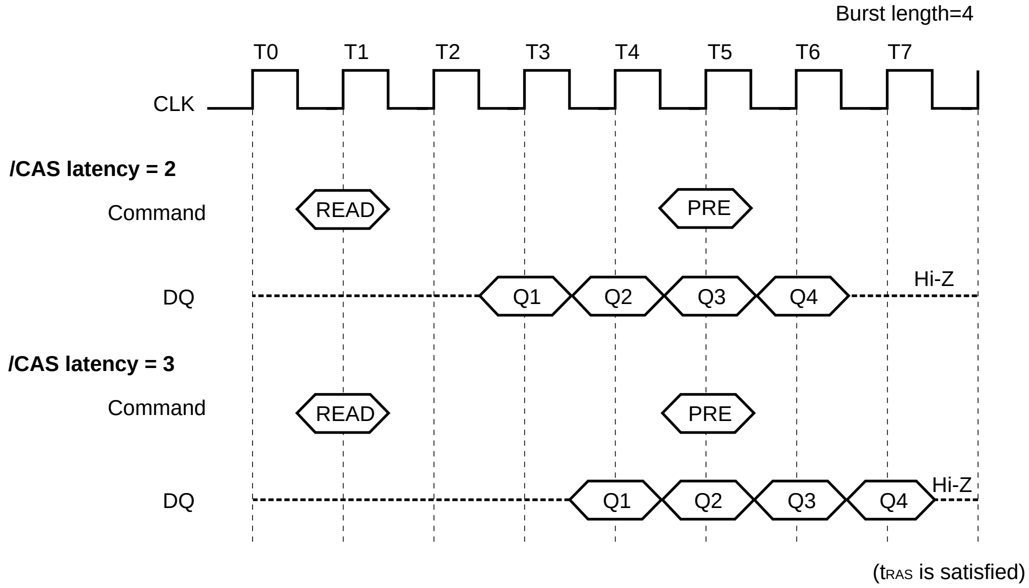
10. Precharge

The precharge command can be asserted anytime after $t_{RAS(MIN.)}$ is satisfied.

Soon after the precharge command is asserted, precharge operation performed and the synchronous GRAM enters the idle state after t_{RP} is satisfied. The parameter t_{RP} is the time required to perform the precharge.

The earliest timing in a read cycle that a precharge command can be asserted without losing any data in the burst is as follows.

/CAS latency = 2 : One clock earlier than the last read data.
/CAS latency = 3 : Two clocks earlier than the last read data.



In order to write all data to the memory cell correctly, the asynchronous parameter "t_{DPL}", "t_{BPL}" must be satisfied. The $t_{DPL(MIN.)}$, $t_{BPL(MIN.)}$ specification define the earliest time that a precharge command can be asserted. Minimum number of clocks are calculated by dividing $t_{DPL\ (MIN.)}$, $t_{BPL(MIN.)}$ with clock cycle time.

In summary, the precharge command can be asserted relative to reference clock that indicates the last data word is valid. In the following table, minus means clocks before the reference; plus means time after the reference.

/CAS latency	Read	Write	Block Write
2	–1	$+t_{DPL(MIN.)}$	$+t_{BPL(MIN.)}$
3	–2	$+t_{DPL(MIN.)}$	$+t_{BPL(MIN.)}$

11. Auto Precharge

During a read or write/block write command cycle, A9 controls whether auto precharge is selected. A9 high in the read or write/block write command (Read with Auto precharge command or Write with Auto precharge command/Block Write with Auto precharge command), auto precharge is selected and begins after the burst access automatically.

The t_{RAS} must be satisfied with a read with auto precharge or a write/ block write with auto precharge operation. In addition, the next activate command to the bank being precharged cannot be executed until the precharge cycle ends.

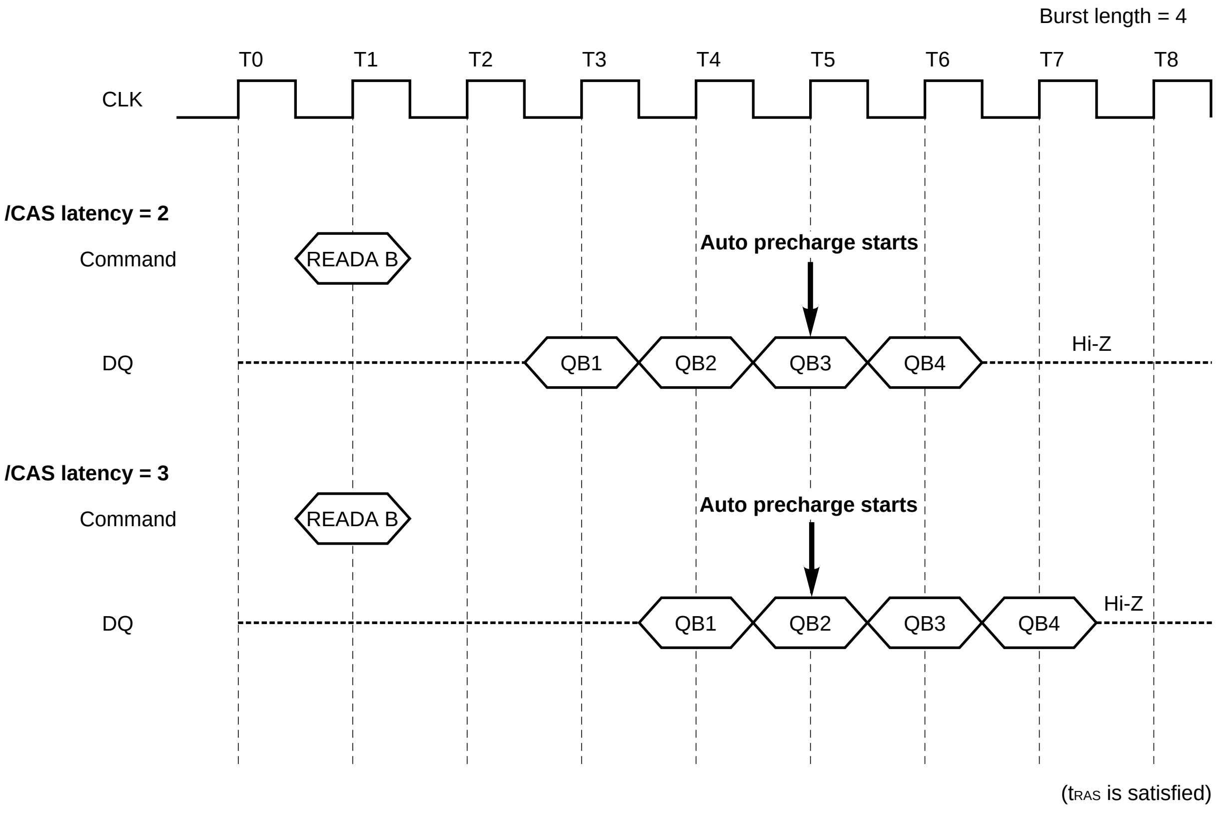
In read cycle, once auto precharge has started, an activate command to the bank can be issued after t_{RP} has been satisfied.

In write cycle, the t_{DAL}, t_{BAL} must be satisfied to issue the next activate command to the bank being precharged.

The timing that begins the auto precharge cycle depends on both the /CAS latency programmed into the mode register and whether read or write/block write cycle.

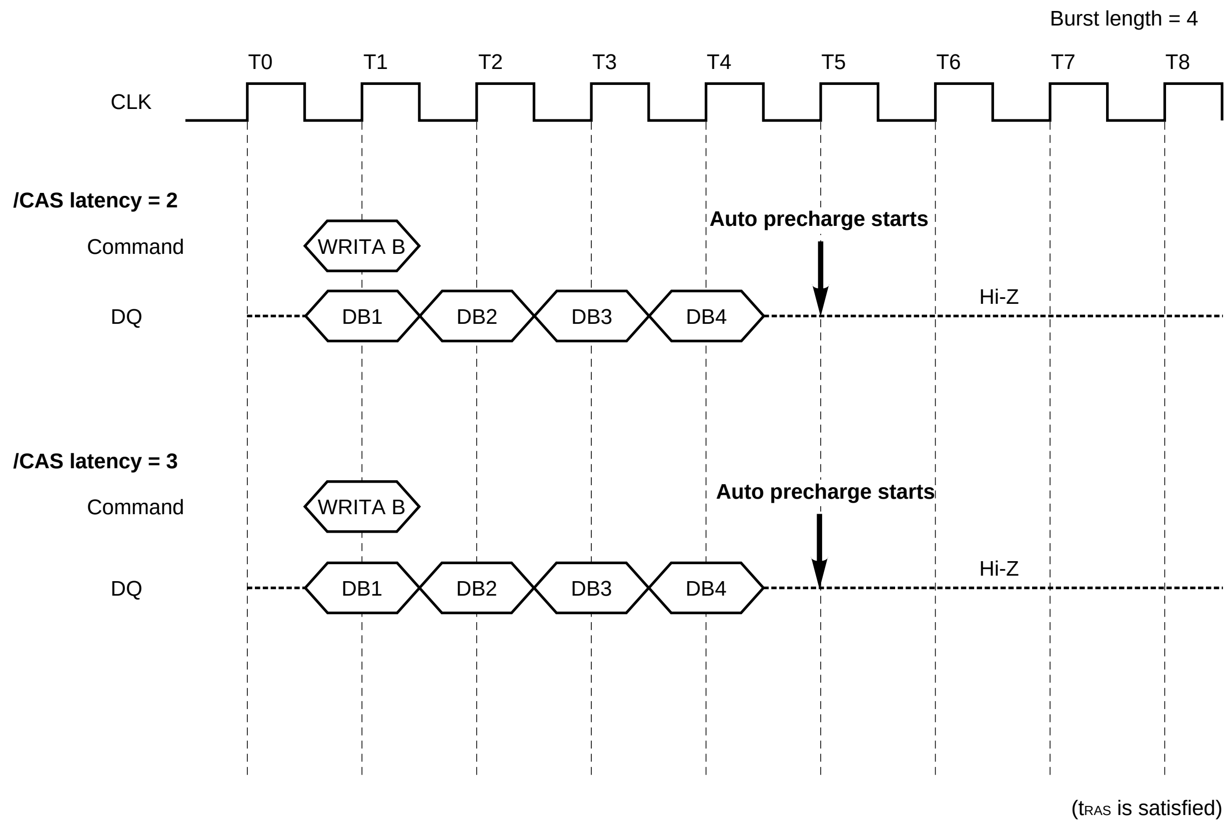
11.1 Read with Auto Precharge

During a read cycle, the auto precharge begins one clock earlier (/CAS latency of 2) or two clocks earlier (/CAS latency of 3) the last data word output.



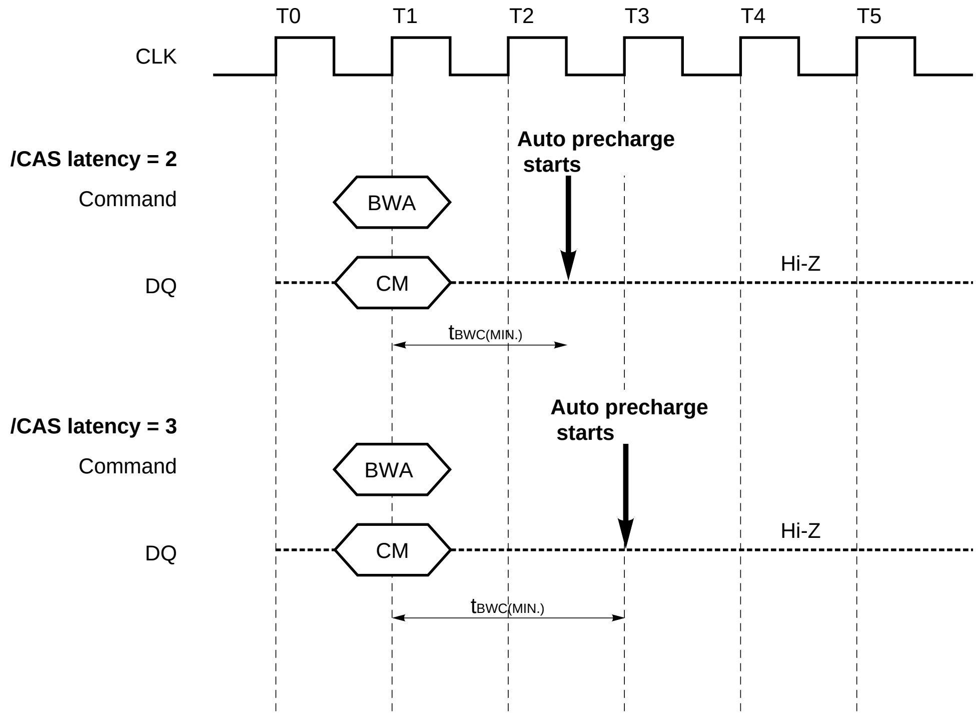
11.2 Write with Auto Precharge

During a write cycle, the auto precharge begins one clock after the last data word input to the device (/CAS latency of 2 or 3).



11.3 Block Write with Auto Precharge

During a block write cycle, the auto precharge begins after t_{BWC} of the last data word input to the device (/CAS latency of 2 or 3).



(t_{RAS} is satisfied)

Remark CM : Column Mask

In summary, the auto precharge cycle begins relative to a reference clock that indicates the last data word is valid. In the table below, minus means clocks before the reference; plus means clocks after the reference.

/CAS latency	Read	Write	Block Write
2	–1	+1	$+t_{BWC(MIN.)}$
3	–2	+1	$+t_{BWC(MIN.)}$

12. Write/Block Write with Write Per Bit

12.1 Write Per Bit

The write per bit function writes data using the write mask data only in the required DQi pins. It writes when the write mask data is “1” and prohibits writing when the data is “0” (Refer to **8.2 Mask Register**).

To use WPB operation

(1) Execute Special register set command and set WPB data (32 bits) to mask register.

(2) Execute Bank Activate with WPB enable command (ACTWPB) after t_{RSC} (2 CLK) period from Special register set command (SRS).

(3) Execute Write/Block write command after t_{RCD} period from ACTWPB.

In case SRS command is executed in activate state to set new WPB data, it is necessary to take t_{RSC} (2 CLK) interval between SRS and Write/Block write command.

Remark Mask data = Mask register’s data (WPB) + DQMi
DQMi is prior to Mask register’s data (WPB)

13. Block Write

13.1 Block Write

This cycle writes the color register data in 256 bits (8 columns x 32 I/Os) memory cell in one cycle. The memory cell range in which data can be written in one block write cycle is eight continuous columns on one row address.
This cycle controls writing in 8 columns x 8 DQ = 64 bits by DQM0 to DQM3 input. Color register data is written to the memory cell if DQM is low but not if DQM is high. DQM0 corresponds to the lowest byte (DQ0 to DQ7), DQM1 corresponds to DQ8 to DQ15, DQM2 corresponds to DQ16 to DQ23, DQM3 corresponds to DQ24 to DQ31.
Any column of the eight columns can be selected and writing prohibited. Determine whether to write or prohibit writing according to the data selected for column (Refer to **13.2 Column Mask**).

To use Block write operation

(1) Execute Special register set command and set color data (32 bits) to color register.

(2) Execute Bank Activate (ACT) or Bank Activate with WPB enable command (ACTWPB) after t_{RSC} (2 CLK) period from SRS.

(3) Execute Block write command after t_{RCD} period from ACT or ACTWPB.

In case new Write/Block write is executed or, it is necessary to take t_{BWC} interval from Block Write command to new Write/Block write command.

13.2 Column Mask

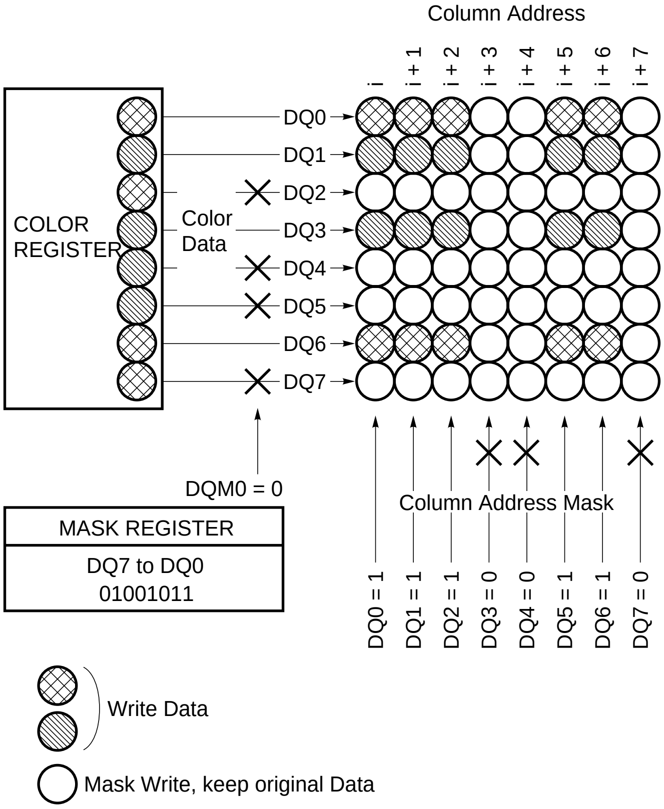
In block write cycle any column of the eight columns can be selected and writing prohibited. Determine which column to select according to the DQi pin to which the data selected for the column is to be input. Refer to the table below.

Column address Note	Column address and corresponding DQ pin				Column select data	Writing
	A2	A1	A0	DQi	(DQi)	
i (1st column)	0	0	0	DQ0/DQ8/ DQ16/DQ24	1	Yes
					0	No
i+1 (2nd column)	0	0	1	DQ1/DQ9/ DQ17/DQ25	1	Yes
					0	No
i+2 (3rd column)	0	1	0	DQ2/DQ10/ DQ18/DQ26	1	Yes
					0	No
i+3 (4th column)	0	1	1	DQ3/DQ11/ DQ19/DQ27	1	Yes
					0	No
i+4 (5th column)	1	0	0	DQ4/DQ12/ DQ20/DQ28	1	Yes
					0	No
i+5 (6th column)	1	0	1	DQ5/DQ13/ DQ21/DQ29	1	Yes
					0	No
i+6 (7th column)	1	1	0	DQ6/DQ14/ DQ22/DQ30	1	Yes
					0	No
i+7 (8th column)	1	1	1	DQ7/DQ15/ DQ23/DQ31	1	Yes
					0	No

Note Refer to **13.3 Block Write Function**.

Remark i is times of 8 numeric.

13.3 Block Write Function



Remarks **1.** i is times of 8 numeric.

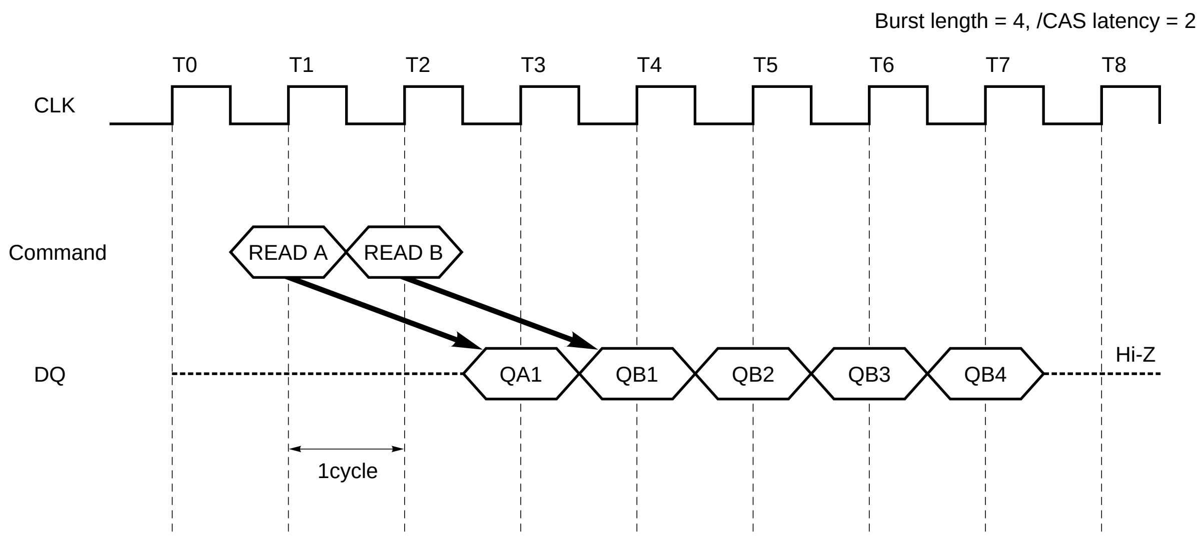
2. This diagram shows only for DQ0 - DQ7. The other DQ is similar as this.

14. Read/Write Command Interval

14.1 Read to Read Command Interval

During a read cycle, when new Read command is asserted, it will be effective after /CAS latency, even if the previous Read operation does not completed. Read command will be interrupted by another Read command.

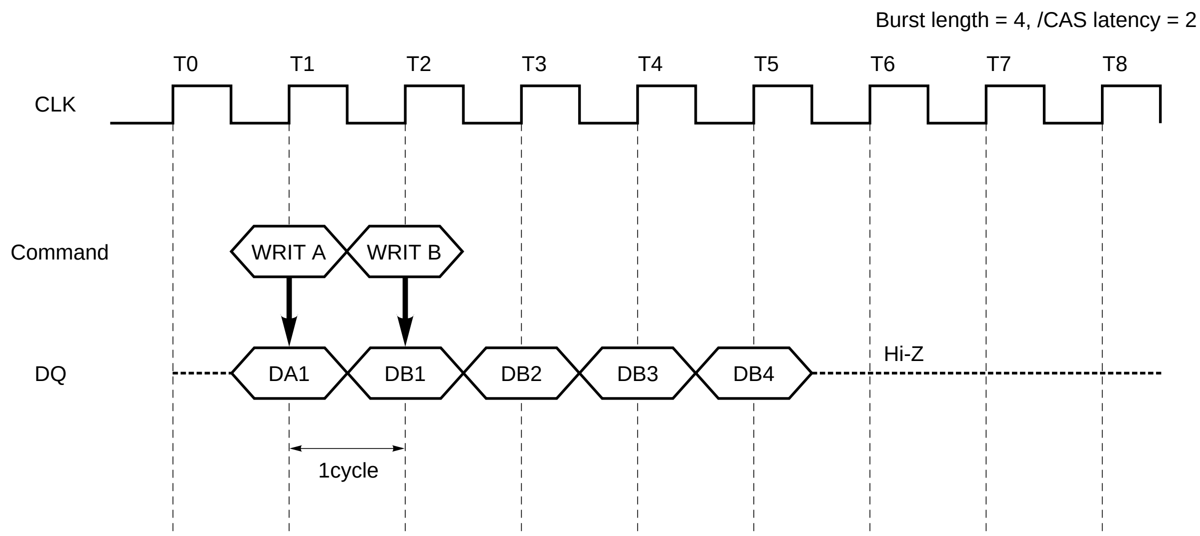
The interval between the commands is minimum 1 cycle. Each Read command can be asserted in every clock without any restriction.



14.2 Write to Write Command Interval

During a write cycle, when new Write command is asserted, the previous burst will terminate and the new burst will begin with a new Write command. Write command will be interrupted by another Write command.

The interval between the commands is minimum 1 cycle. Each Write command can be asserted in every clock without any restriction.

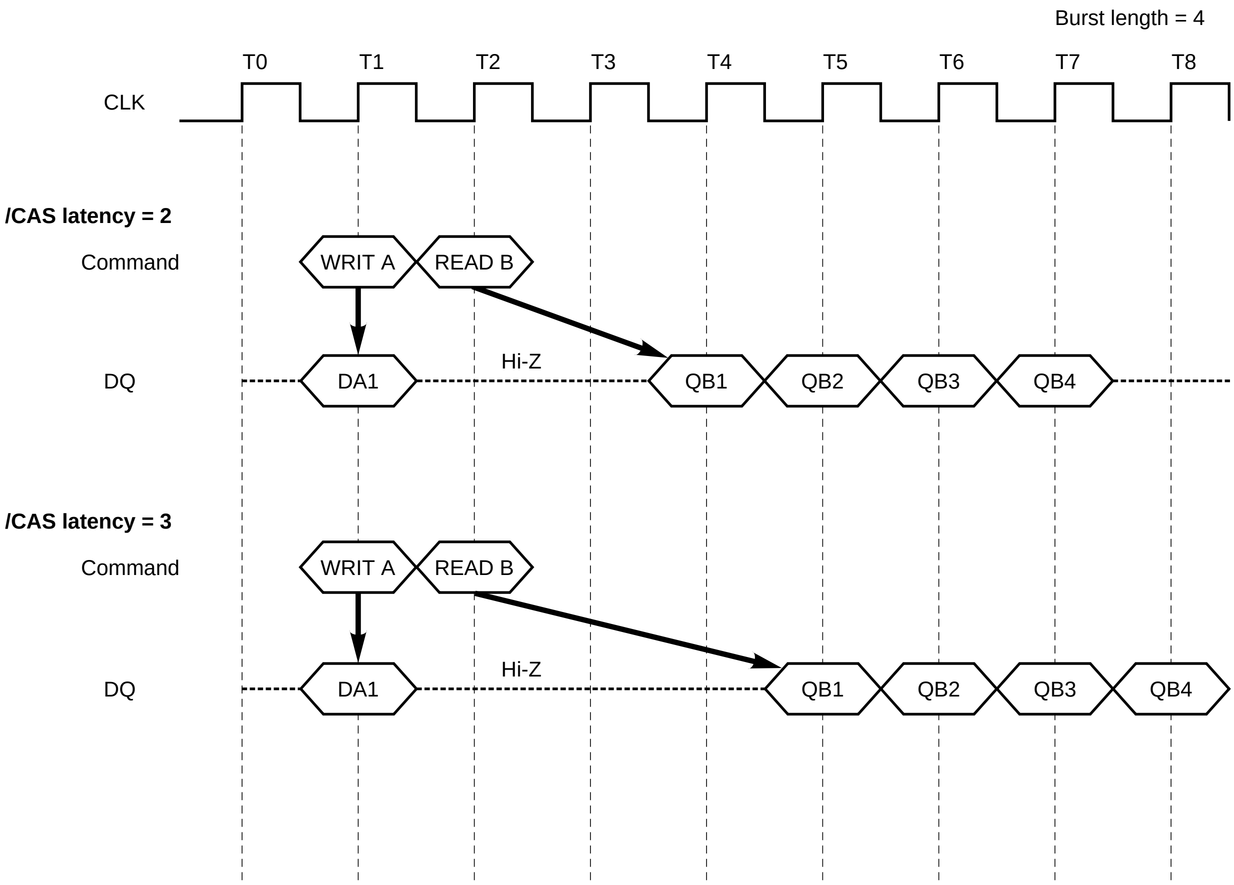


14.3 Write to Read Command Interval

Write command and Read command interval is also 1 cycle.

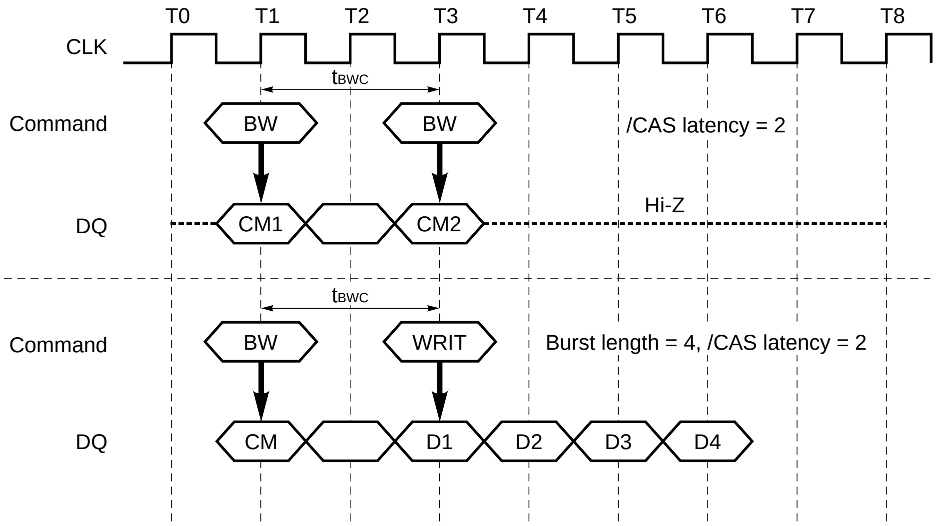
Only the write data before Read command will be written.

The data bus must be Hi-Z at least one cycle prior to the first DOUT.



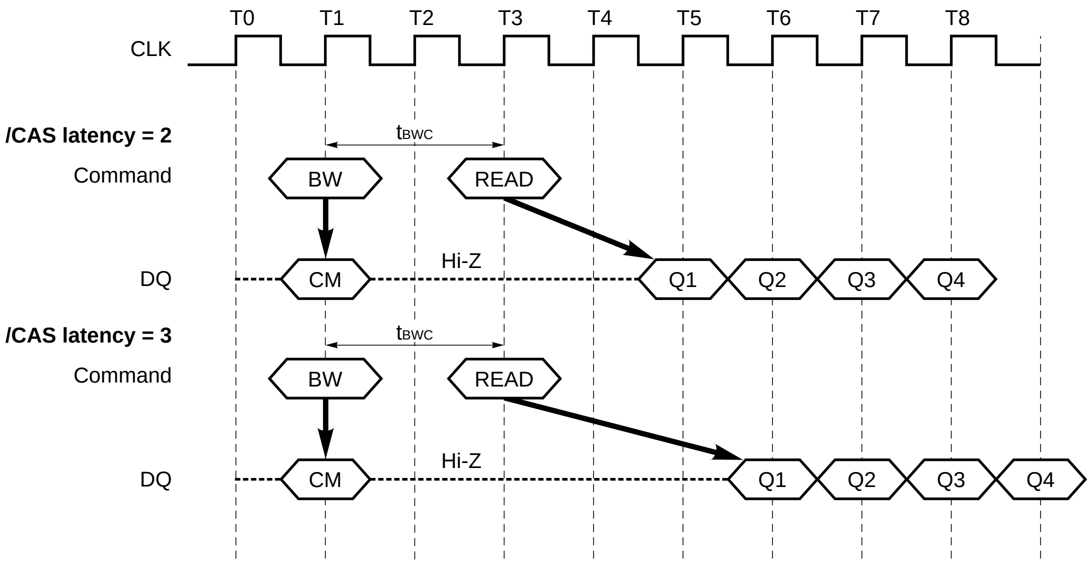
14.4 Block Write to Write or Write/Block Write Command Interval

The interval between Block write command and new Block write command or Write command is t_{BWC} or minimum 1 cycle. If t_{CK} is less than t_{BWC}, NOP command should be issued for the cycle between Block write command and the following Write command or new Block write command.



14.5 Block Write to Read Command Interval

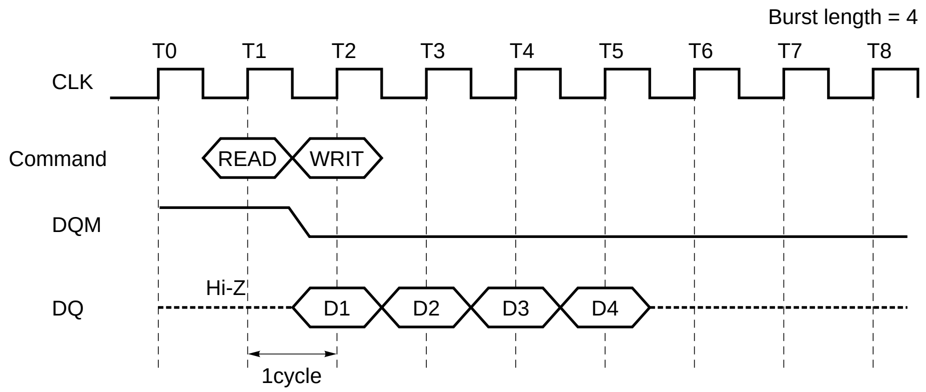
Block write command and Read command is also t_{BWC} or minimum 1 cycle. The data bus must be Hi-Z at least one cycle prior to the first D_{OUT}.



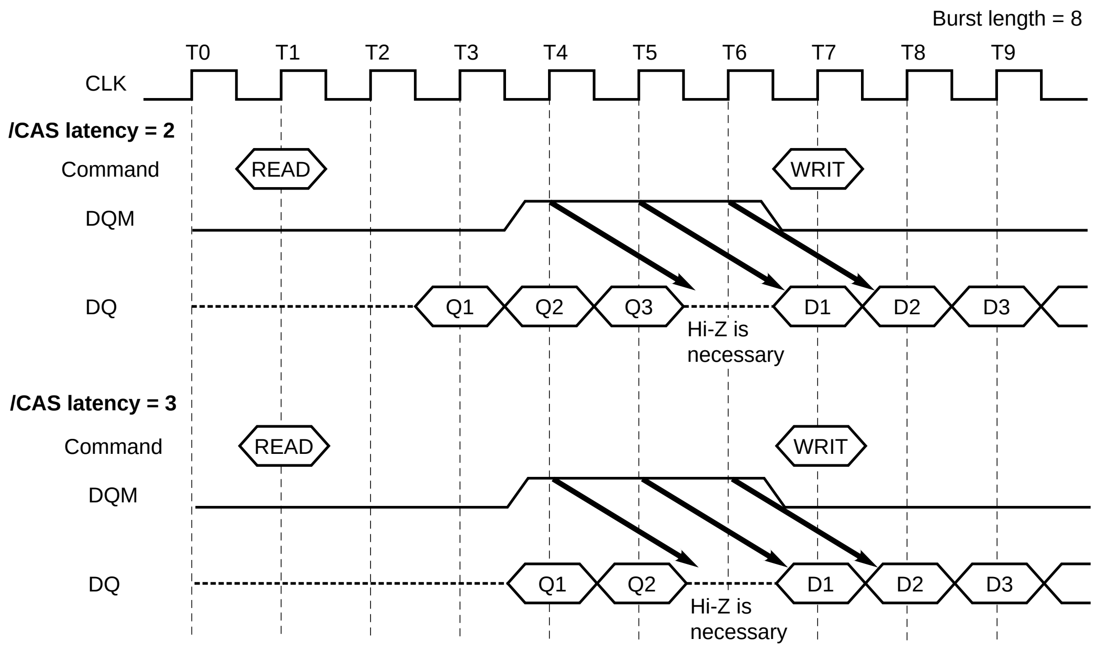
14.6 Read to Write/Block Write Command Interval

During a read cycle, Read command can be interrupted by Write/Block write command.

The Read and Write/Block write command interval is minimum 1 cycle. There is a restriction to avoid data conflict. The data bus must be Hi-Z using DQM before Write/Block write command.



Read command can be interrupted by Write/Block write command. DQM must be High at least 3 clocks prior to the Write command.

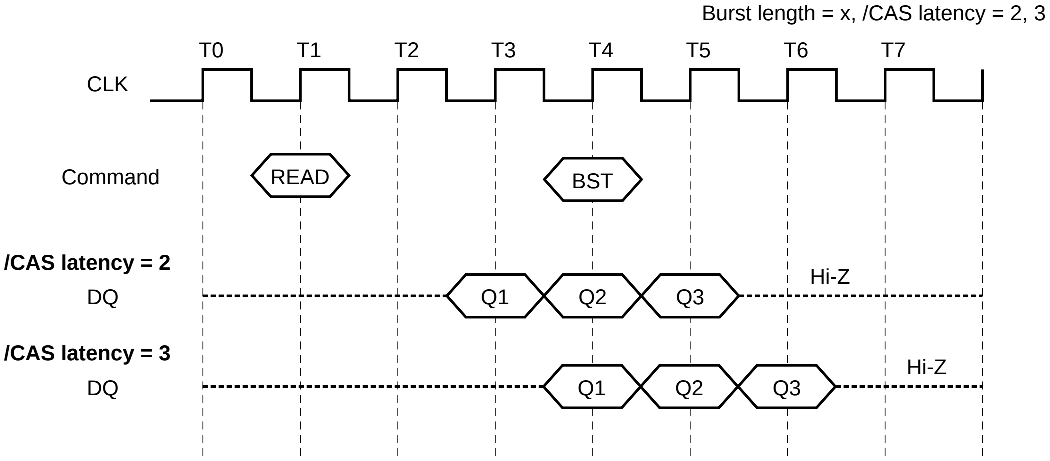


15. Burst Termination

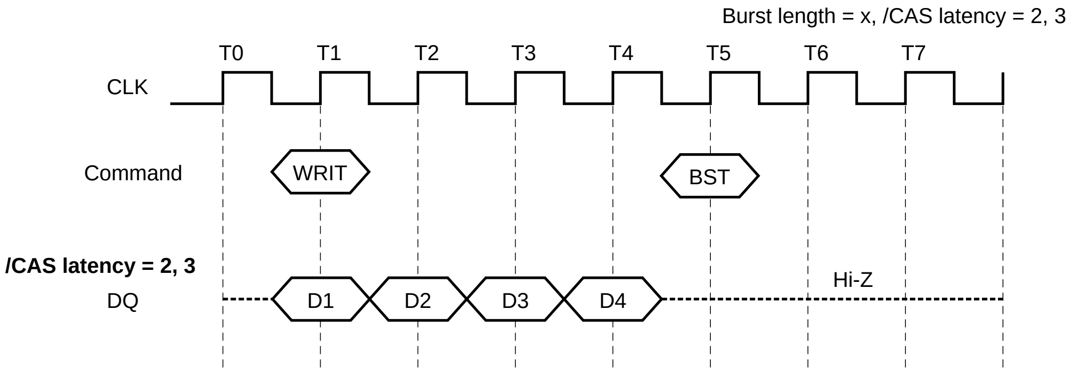
Burst termination is to terminate a burst operation other than using a read or write command.

★ 15.1 Burst Stop Command

During a read cycle, when the burst stop command is asserted, the burst read data are terminated and the data bus goes to high-impedance after the /CAS latency from the burst stop command.



During a write cycle, when the burst stop command is asserted, the burst read data are terminated and data bus goes to high-impedance at the same clock with the burst stop command.

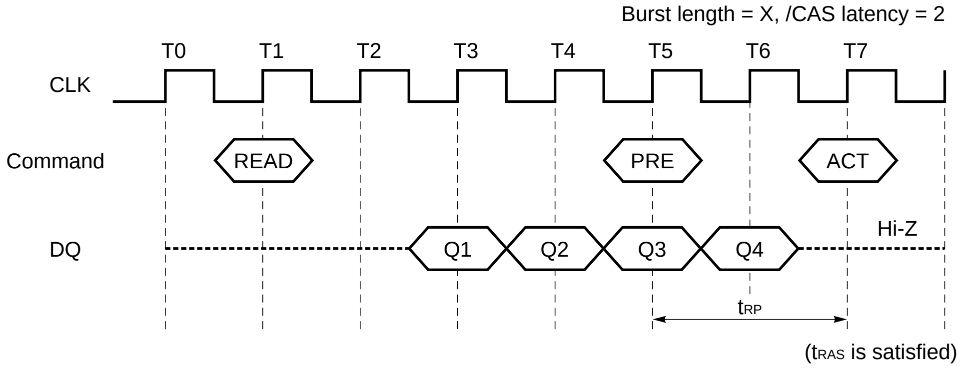


15.2 Precharge Termination

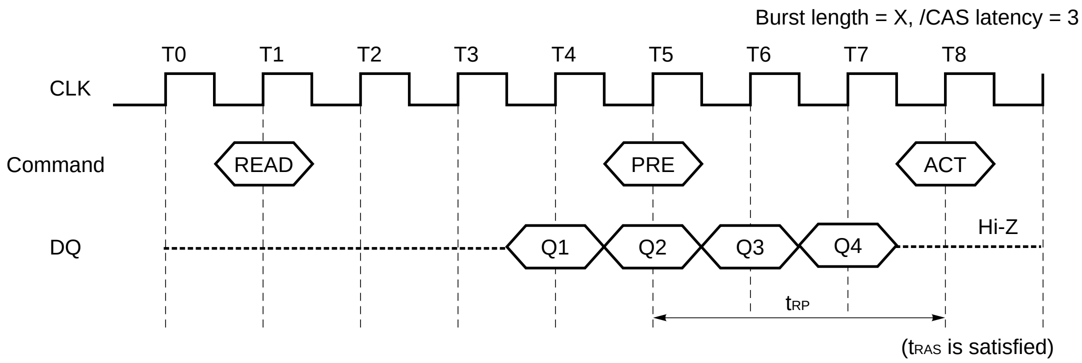
15.2.1 Precharge Termination in Read Cycle

During a read cycle, the burst read operation is terminated by a precharge command.
When the precharge command is asserted, the burst read operation is terminated and precharge starts.
The same bank can be activated again after t_{RP} from the precharge command.
To issue a precharge command, t_{RAS} must be satisfied.

When /CAS latency is 2, the read data will remain valid until one clock after the precharge command.



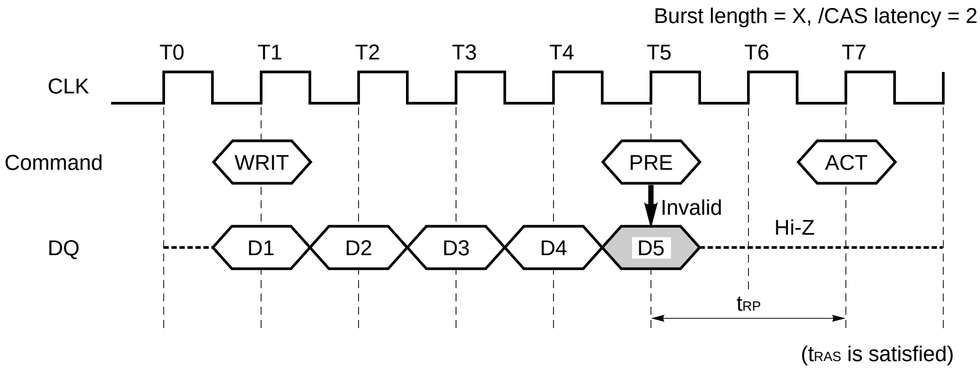
When /CAS latency is 3, the read data will remain valid until two clocks after the precharge command.



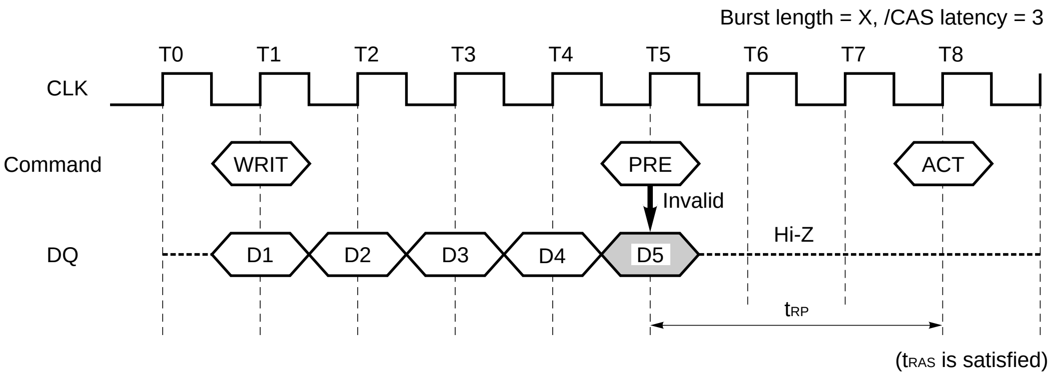
15.2.2 Precharge Termination in Write cycle

During a write cycle, the burst write operation is terminated by a precharge command.
When the precharge command is asserted, the burst write operation is terminated and precharge starts.
The same bank can be activated again after t_{RP} from the precharge command.
To issue a precharge command, t_{RAS} must be satisfied.

When /CAS latency is 2, the write data written prior to the precharge command will be correctly stored. However, the data written at the same clock as the precharge command will not be stored.



When /CAS latency is 3, the write data written prior to the precharge command will be correctly stored. However, the data written at the same clock as the precharge command will not be stored.



16. Electrical Specifications

- All voltages are referenced to V_{SS} (GND).
- After power up, wait more than 100 μs and then, execute **Power on sequence and Auto Refresh** before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V_{CC}, $V_{CC}Q$		–1.0 to +4.6	V
Voltage on input pin relative to GND	V_T		–1.0 to +4.6	V
Short circuit output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		–55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage (-A70R)	V_{CC}, $V_{CC}Q$		3.4	3.5	3.6	V
Supply voltage (-A80, -A10, -A12)	V_{CC}, $V_{CC}Q$		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		–0.3		+ 0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10	2		6	pF
	C_{I2}	CLK, CKE, /CS, /RAS, /CAS, /WE, DSF, DQM0 - DQM3	2		6	
Data input/output capacitance	$C_{I/O}$	DQ0 - DQ31	2		7	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition			MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	Burst length = 1 $t_{RAS} \geq t_{RAS(MIN.)}$, $t_{RP} \geq t_{RP(MIN.)}$, I_O = 0 mA		-A70R		230	mA	1
				-A80		220		
				-A10		205		
				-A12		180		
Precharge standby current in power down mode	$I_{CC2}P$	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = 15 ns				4	mA	
	$I_{CC2}PS$	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = ∞				3		
Precharge standby current in non power down mode	$I_{CC2}N$	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = 15 ns, /CS ≥ $V_{IH(MIN.)}$, Input signals are changed one time during 30 ns.				36	mA	
	$I_{CC2}NS$	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = ∞ Input signals are stable.				22		
Active standby current in power down mode	$I_{CC3}P$	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = 15 ns				5	mA	
	$I_{CC3}PS$	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = ∞				4		
Active standby current in non power down mode	$I_{CC3}N$	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = 15 ns, /CS ≥ $V_{IH(MIN.)}$, Input signals are changed one time during 30 ns.				50	mA	
	$I_{CC3}NS$	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = ∞ Input signals are stable.				25		
Operating current (Burst mode)	I_{CC4}	$t_{CK} \geq t_{CK(MIN.)}$, I_O = 0 mA	/CAS latency = 2	-A80		220	mA	2
				-A10		200		
				-A12		170		
			/CAS latency = 3	-A70R		345		
				-A80		300		
				-A10		250		
				-A12		210		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC(MIN.)}$		-A70R		190	mA	3
				-A80		180		
				-A10		170		
				-A12		150		
Self refresh current	I_{CC6}	CKE ≤ 0.2 V				2	mA	
Operating current (Block Write Mode)	I_{CC7}	$t_{CK} \geq t_{CK(MIN.)}$, I_O = 0 mA, $t_{BWC} \geq t_{BWC(MIN.)}$		-A70R		290	mA	
				-A80		250		
				-A10		210		
				-A12		180		
Input leakage current	$I_{I(L)}$	V_I = 0 to 3.6 V, all other pins not under test = 0 V			–5.0	+5.0	μA	
Output leakage current	$I_{O(L)}$	D_{OUT} is disabled, V_O = 0 to 3.6 V			–5.0	+5.0	μA	
High level output voltage	V_{OH}	I_O = – 2.0 mA			2.4		V	
Low level output voltage	V_{OL}	I_O = + 2.0 mA				0.4	V	

Notes 1. I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

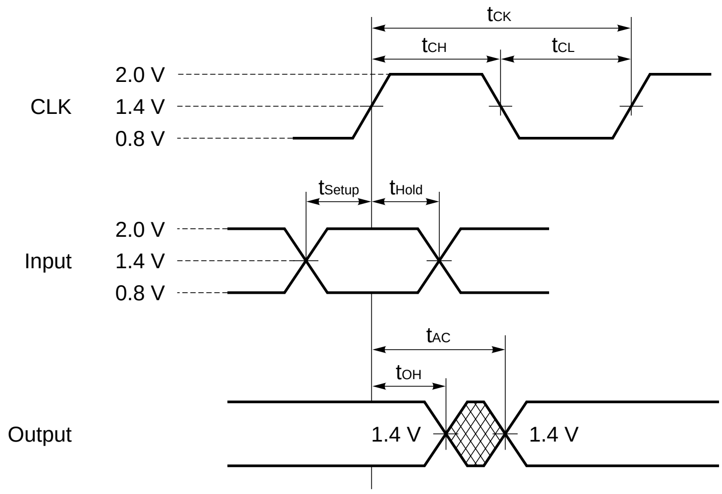
2. I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

3. I_{CC5} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

- AC measurements assume $t_T = 1$ ns.
- Reference level for measuring timing of input signals is 1.4 V. Transition times are measured between V_{IH} and V_{IL}.
- If t_T is longer than 1 ns, reference level for measuring timing of input signals is $V_{IH(MIN.)}$ and $V_{IL(MAX.)}$.
- An access time is measured at 1.4 V.



Synchronous Characteristics

Parameter		Symbol	-A70R		-A80		-A10		-A12		Unit	Note
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Clock cycle time	/CAS latency = 3	t_{CK3}	7	(143 MHz)	8	(125 MHz)	10	(100 MHz)	12	(83 MHz)	ns	
	/CAS latency = 2	t_{CK2}	—	—	12	(83 MHz)	13	(77 MHz)	15	(67 MHz)	ns	
Access time from CLK	/CAS latency = 3	t_{AC3}		6.0		6.5		7.5		8	ns	1
	/CAS latency = 2	t_{AC2}	—	—		9		10		11	ns	1
CLK high level width		t_{CH}	3		3		3.5		4		ns	
CLK low level width		t_{CL}	3		3		3.5		4		ns	
Data-out hold time		t_{OH}	2.5		2.5		3		3		ns	1
Data-out low-impedance time		t_{LZ}	0		0		0		0		ns	
Data-out high-impedance time	/CAS latency = 3	t_{HZ3}	2.5	6.0	2.5	6.5	3	7.5	3	8	ns	
	/CAS latency = 2	t_{HZ2}	—	—	2.5	9	3	10	3	11	ns	
Data-in setup time		t_{DS}	2.5		2.5		2.5		3		ns	
Data-in hold time		t_{DH}	1		1		1		1.5		ns	
Address setup time		t_{AS}	2.5		2.5		2.5		3		ns	
Address hold time		t_{AH}	1		1		1		1.5		ns	
CKE setup time		t_{CKS}	2.5		2.5		2.5		3		ns	
CKE hold time		t_{CKH}	1		1		1		1.5		ns	
CKE setup time (Power down exit)		t_{CKSP}	2.5		2.5		2.5		3		ns	
Command (/CS, /RAS, /CAS, /WE, DSF, DQM) setup time		t_{CMS}	2.5		2.5		2.5		3		ns	
Command (/CS, /RAS, /CAS, /WE, DSF, DQM) hold time		t_{CMH}	1		1		1		1.5		ns	

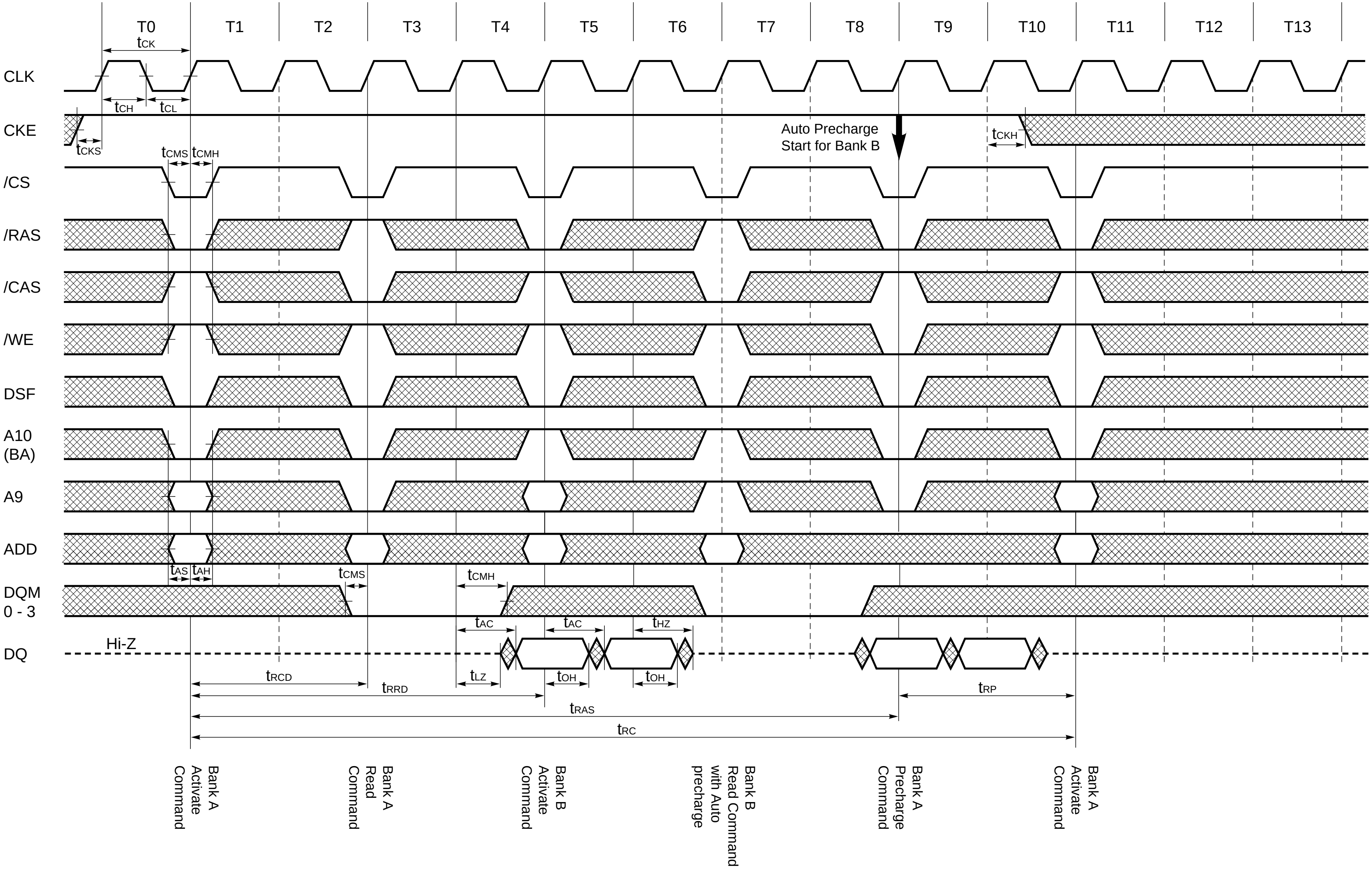
Note 1. Loading capacitance is 30 pF.

Asynchronous Characteristics

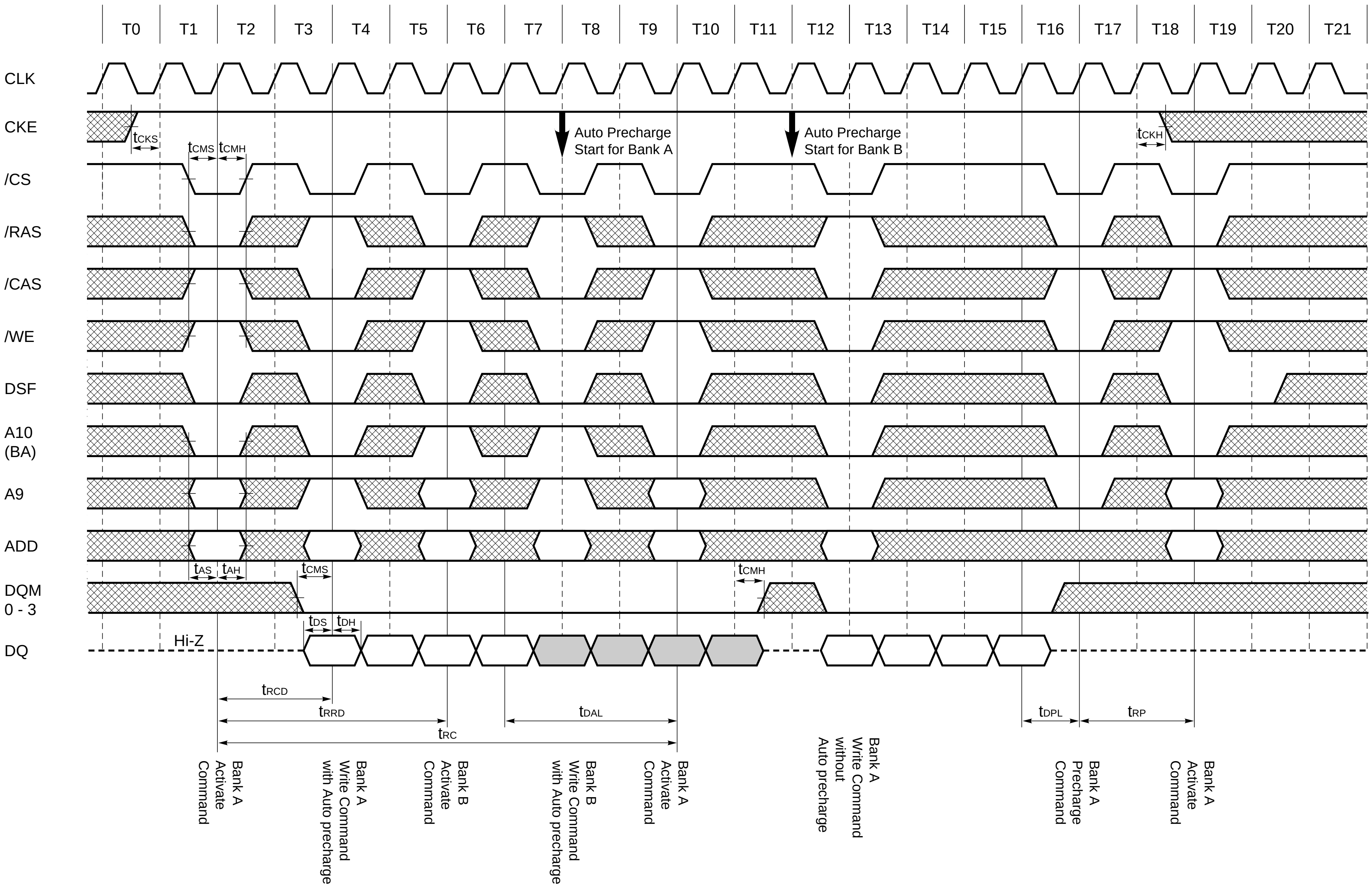
Parameter		Symbol	-A70R		-A80		-A10		-A12		Unit	Note
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
REF to REF/ACT command period		t_{RC}	70		72		78		90		ns	
ACT to PRE command period		t_{RAS}	48	120,000	48	120,000	50	120,000	60	120,000	ns	
PRE to ACT command period		t_{RP}	21		24		26		30		ns	
Delay time ACT to READ/WRITE command		t_{RCD}	21		24		24		30		ns	
ACT(0) to ACT(1) command period		t_{RRD}	21		24		30		36		ns	
Data-in to PRE command period	/CAS latency = 3	t_{DPL3}	7		8		10		12		ns	
	/CAS latency = 2	t_{DPL2}	—	—	12		13		15		ns	
Data-in to ACT(REF) command period (Auto precharge)	/CAS latency = 3	t_{DAL3}	1CLK+21		1CLK+24		1CLK+26		1CLK+30		ns	
	/CAS latency = 2	t_{DAL2}	—	—	1CLK+24		1CLK+26		1CLK+30		ns	
Block write cycle time		t_{BWC}	14		16		20		24		ns	
Block write data-in to PRE command period		t_{BPL}	14		16		20		24		ns	
Block write data-in Active (REF) command period (Auto precharge)		t_{BAL}	35		40		46		54		ns	
Mode register set cycle time		t_{RSC}	2		2		2		2		CLK	
Transition time		t_T	0.5	30	0.5	30	1	30	1	30	ns	
Refresh time (2,048 refresh cycles)		t_{REF}		32		32		32		32	ms	

16.1 AC Parameters for Read/Write Cycles

AC Parameters for Read Timing (Burst length = 2, /CAS latency = 2)



AC Parameters for Write Timing (Burst length = 4, /CAS latency = 2)

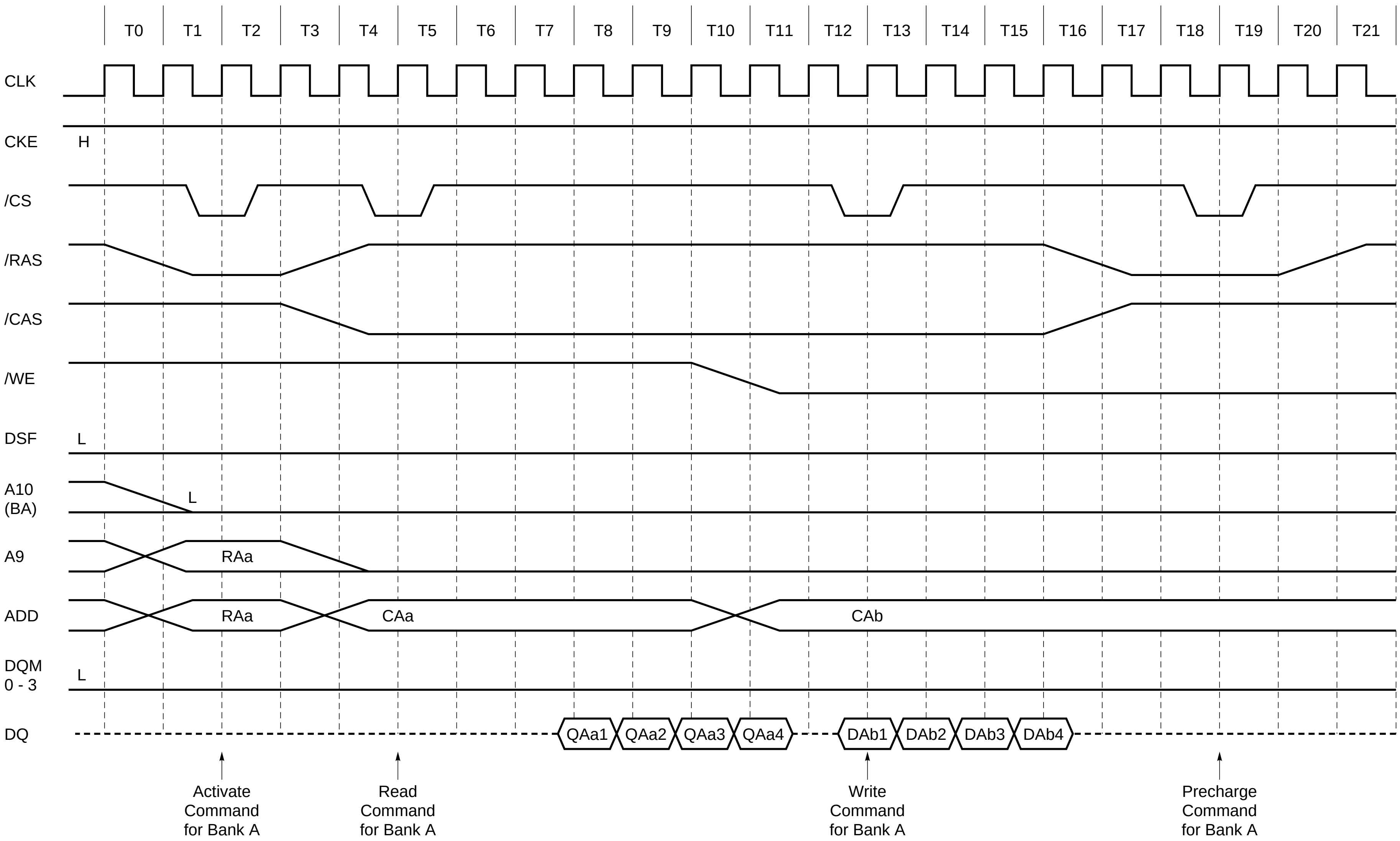


16.2 Relationship between Frequency and Latency

Speed version	-A70R		-A80		-A10		-A12	
Clock cycle time [ns]	7	—	8	12	10	13	12	15
Frequency [MHz]	143	—	125	83	100	77	83	67
/CAS latency	3	—	3	2	3	2	3	2
[t_{RCD}]	3	—	3	2	3	2	3	2
/RAS latency (/CAS latency + [t_{RCD}])	6	—	6	4	6	4	6	4
[t_{RC}]	10	—	9	6	8	6	8	6
[t_{RAS}]	7	—	6	4	5	4	5	4
[t_{RRD}]	3	—	3	2	3	3	3	3
[t_{RP}]	3	—	3	2	3	2	3	2
[t_{DPL}]	1	—	1	1	1	1	1	1
[t_{DAL}]	4	—	4	3	4	3	4	3

16.3 /CS Function

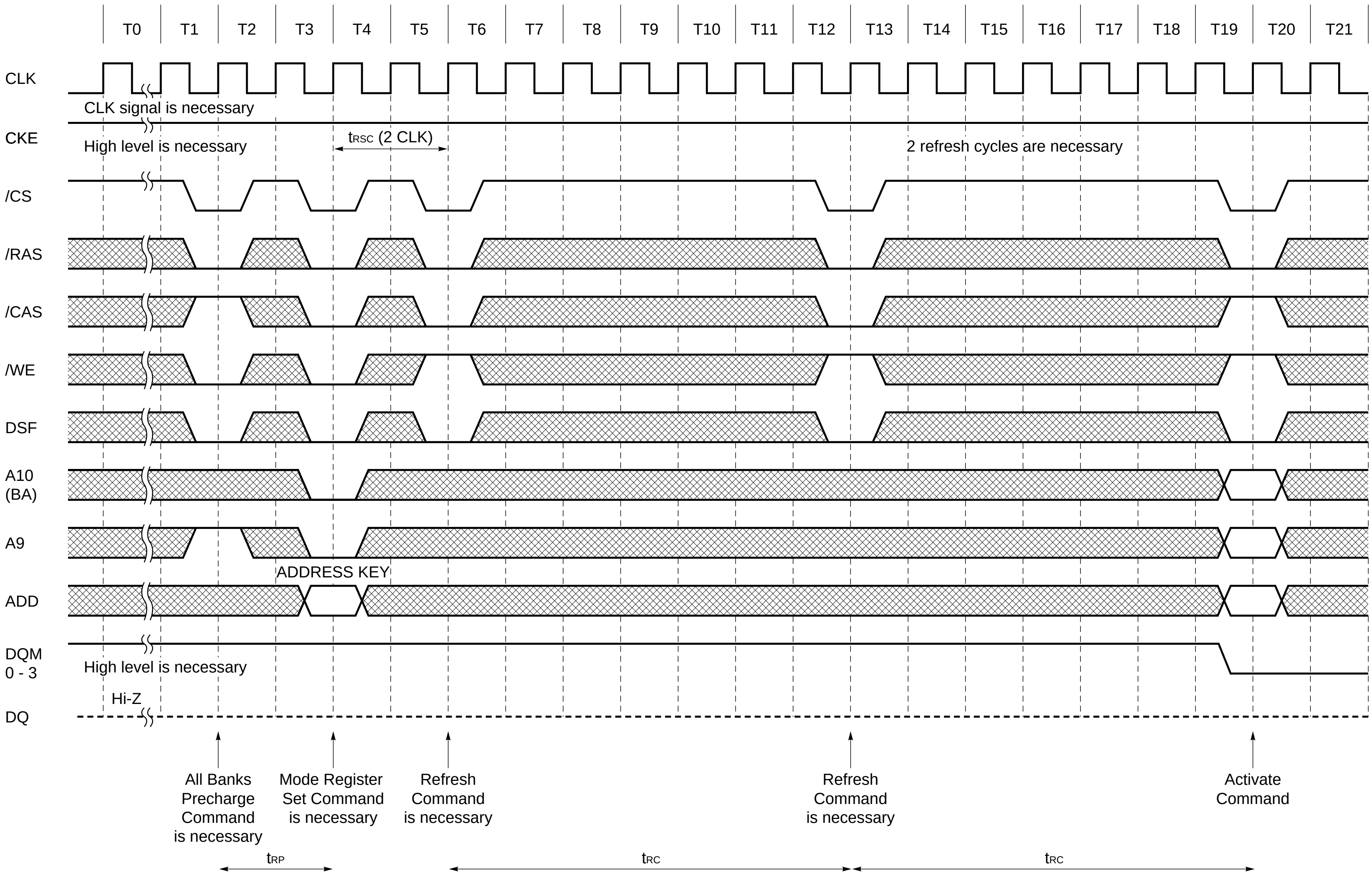
/CS function (Only /CS signal needs to be asserted at minimum rate) (at 100 MHz Burst length = 4, /CAS latency = 3)



16.4 Basic Cycles

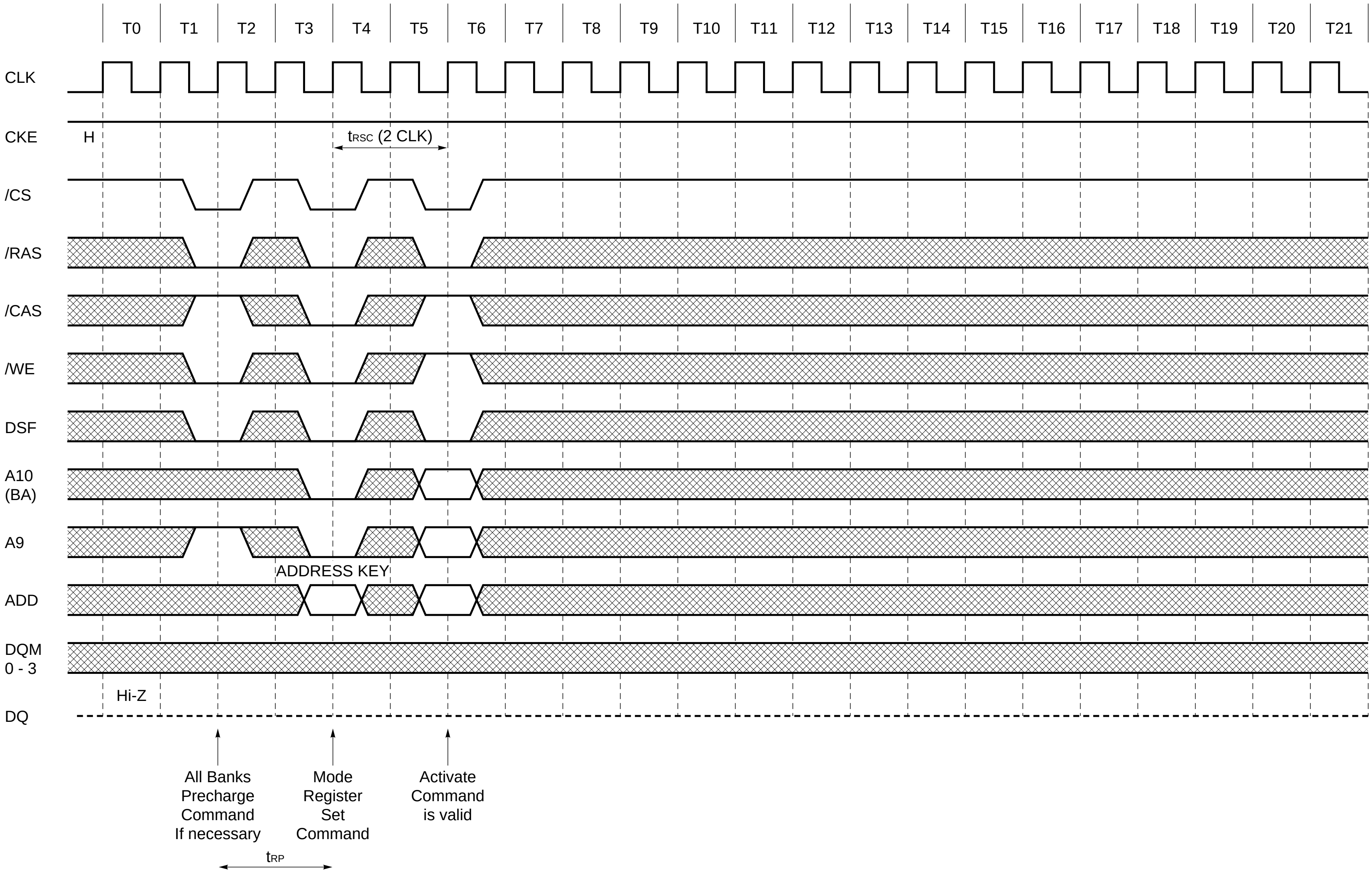
16.4.1 Initialization

Power on Sequence and Auto Refresh



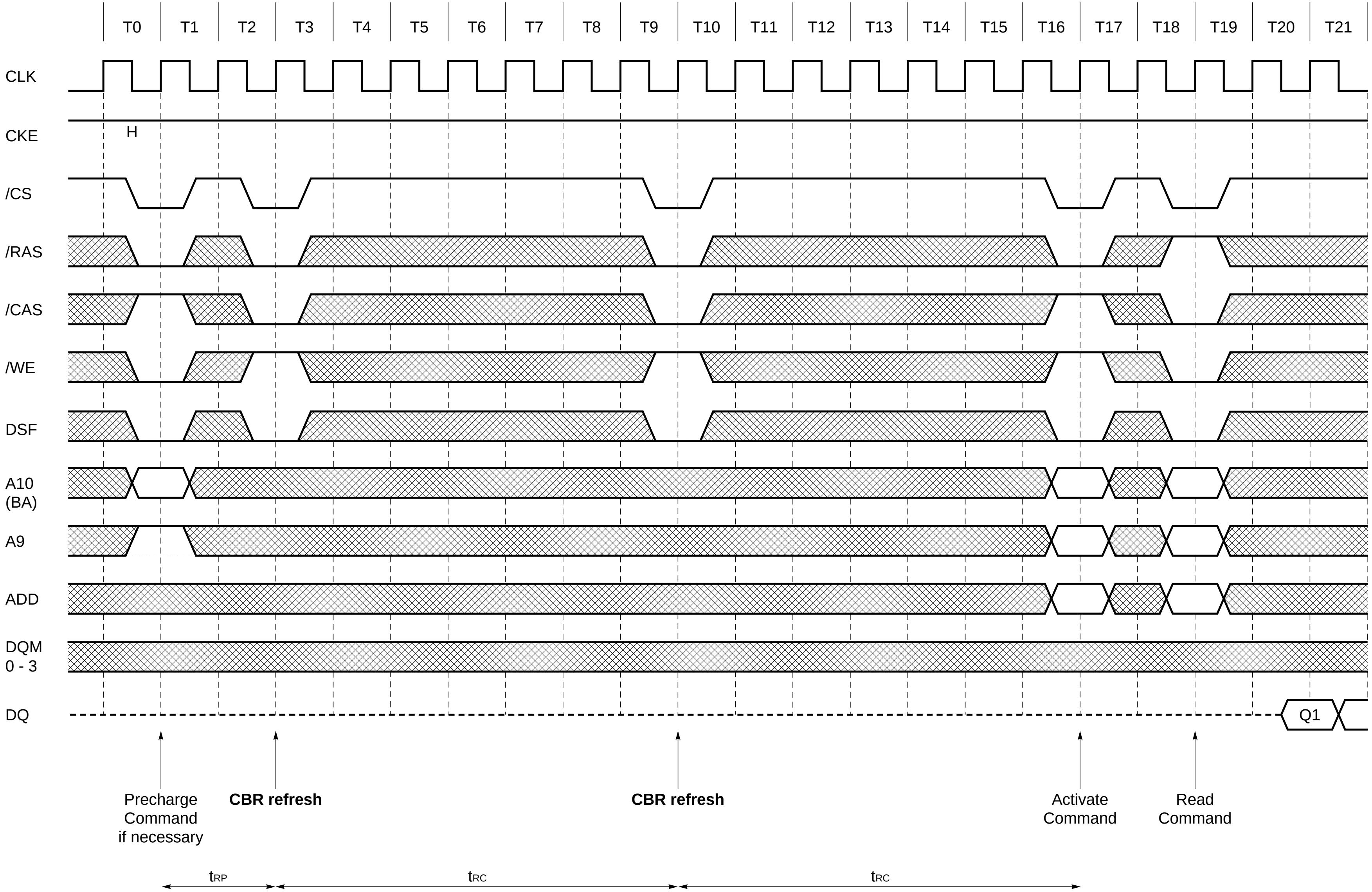
16.4.2 Mode Register Set

Mode Register (Burst length = 4, /CAS latency = 2)

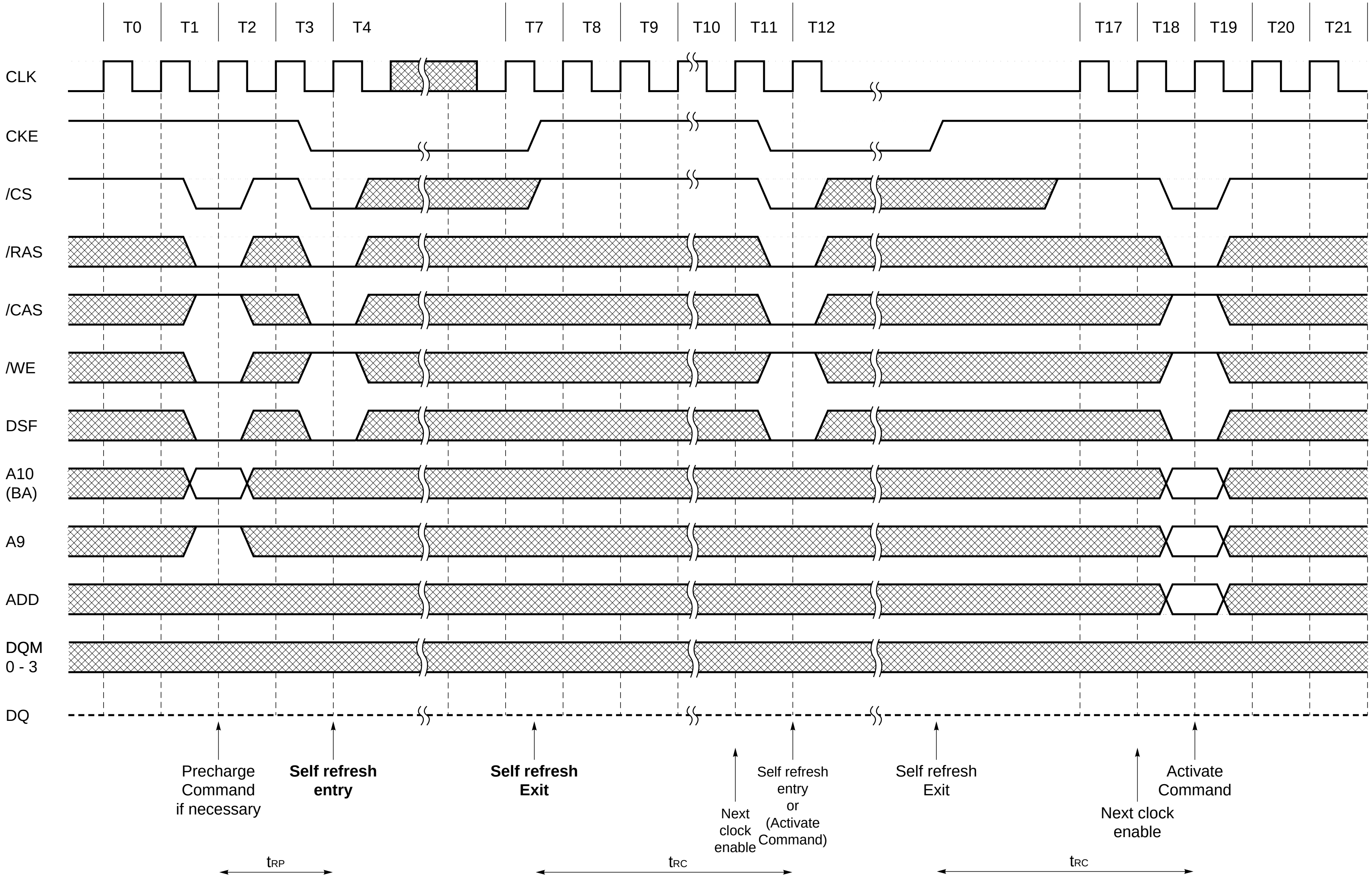


16.4.3 Refresh Cycle

CBR Refresh (/CAS latency = 2)

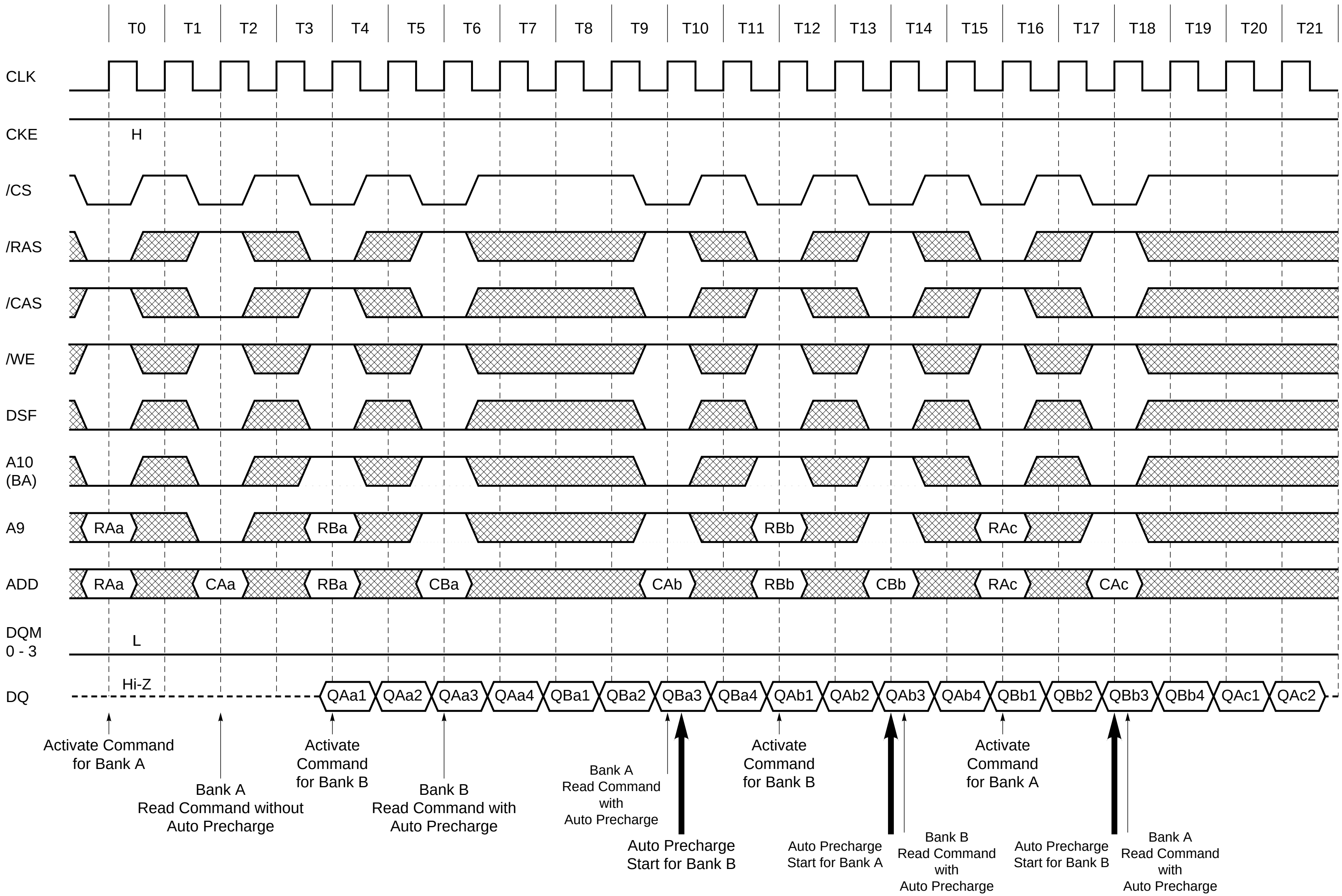


Self Refresh (entry and exit)

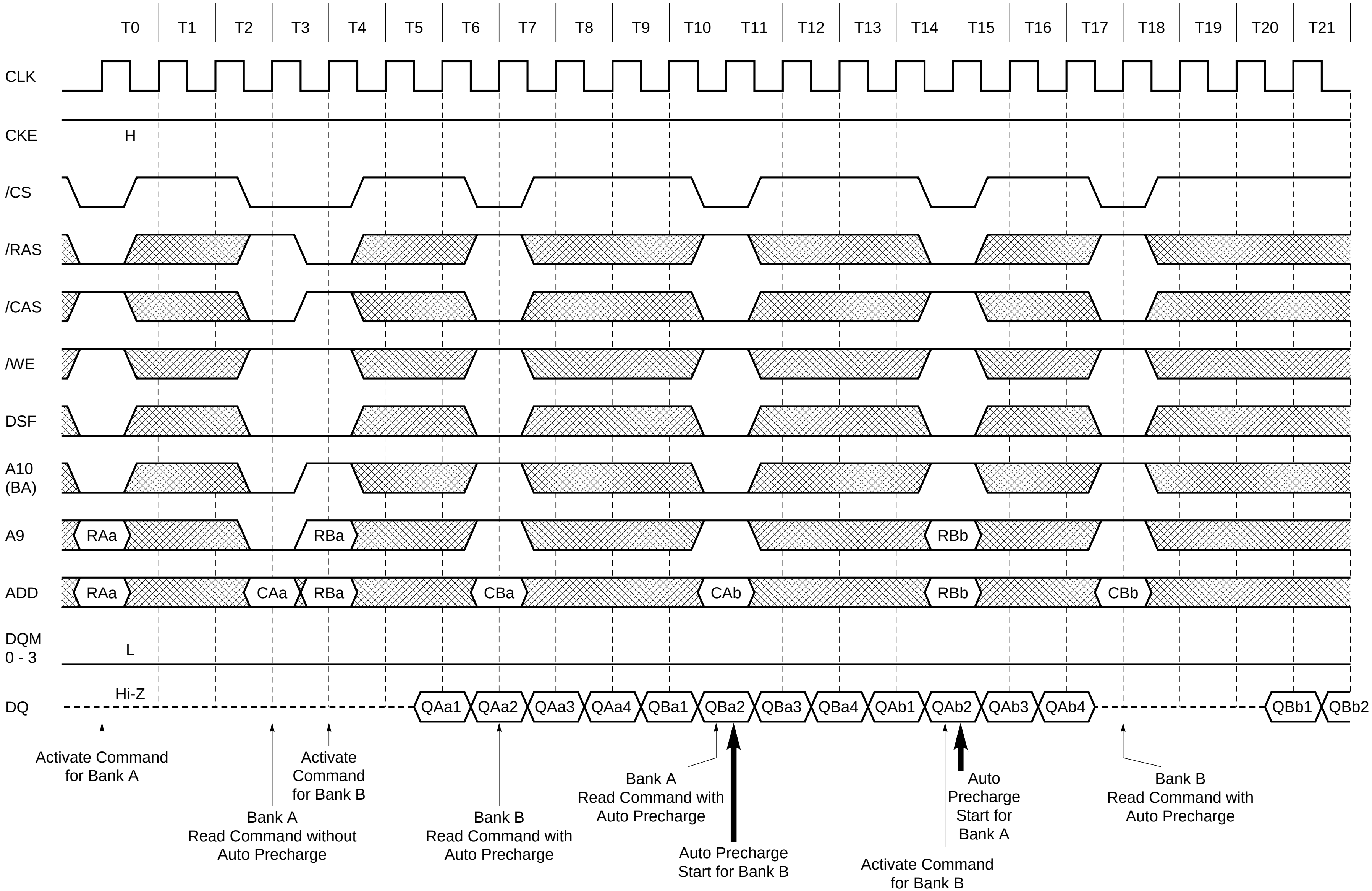


16.4.4 Cycle with Auto Precharge

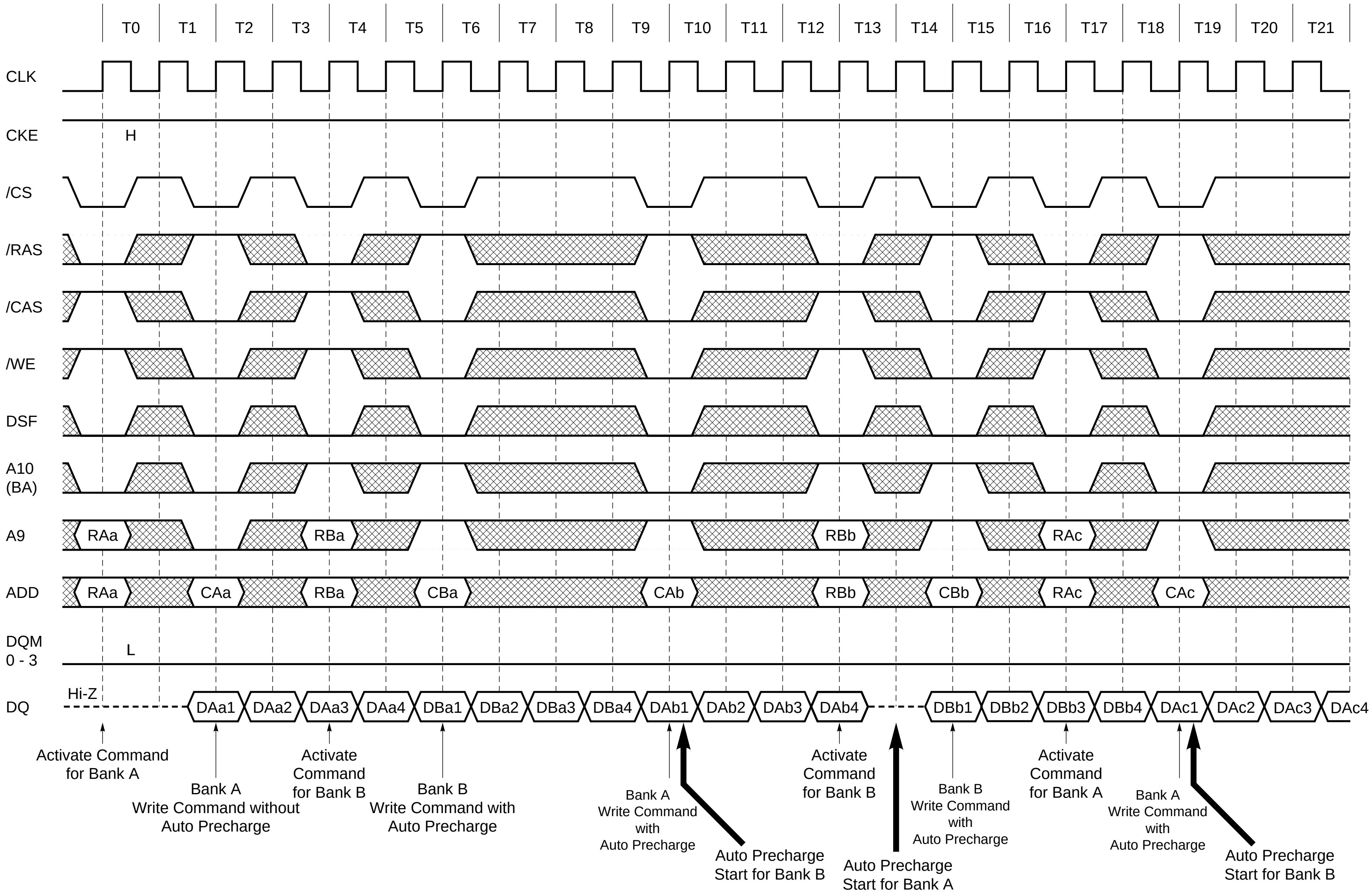
Auto Precharge after Read Burst (1/2) (Burst length = 4, /CAS latency = 2)



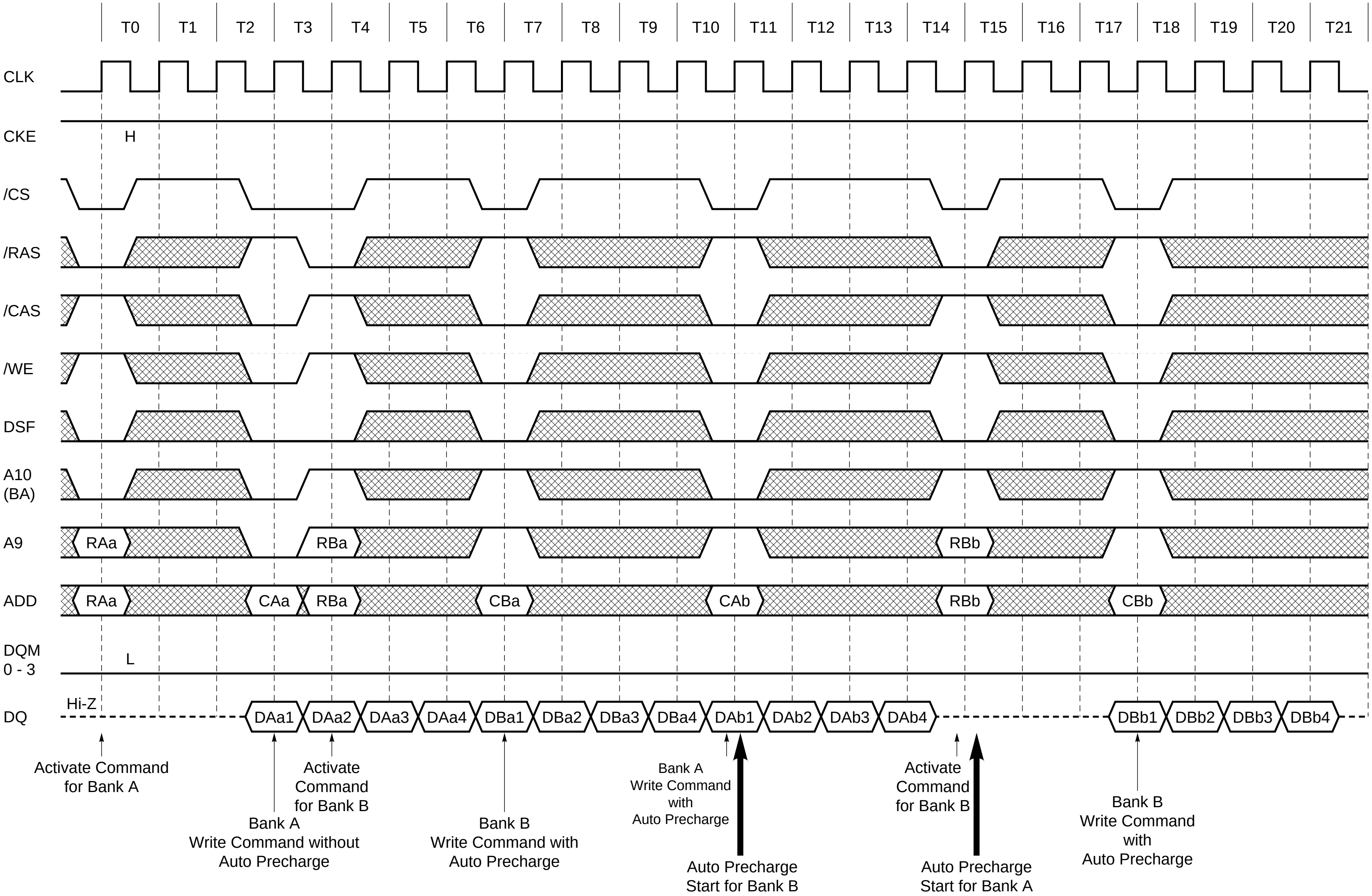
Auto Precharge after Read Burst (2/2) (Burst length = 4, /CAS latency = 3)



Auto Precharge after Write Burst (1/2) (Burst length = 4, /CAS latency = 2)

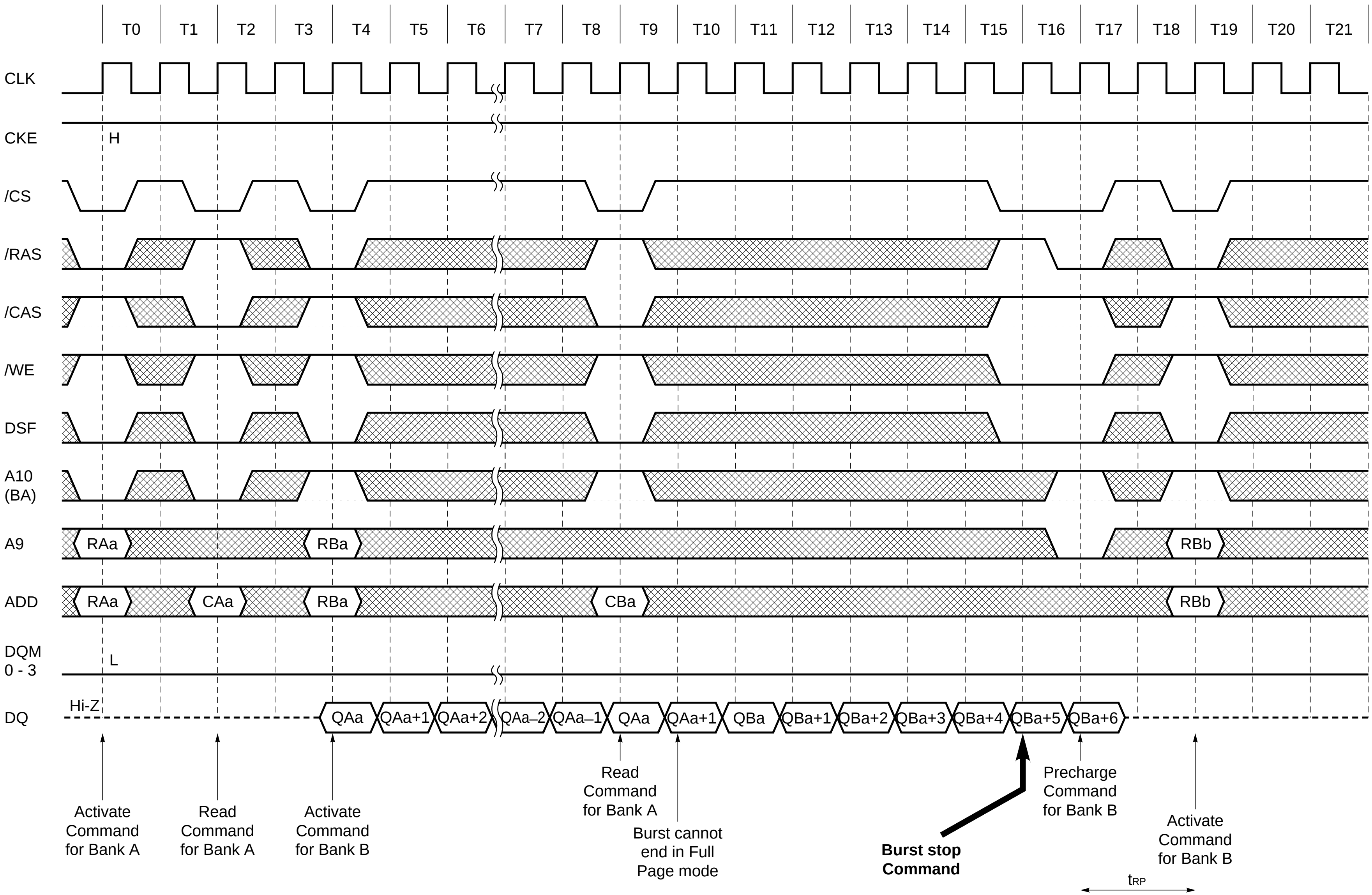


Auto Precharge after Write Burst (2/2) (Burst length = 4, /CAS latency = 3)

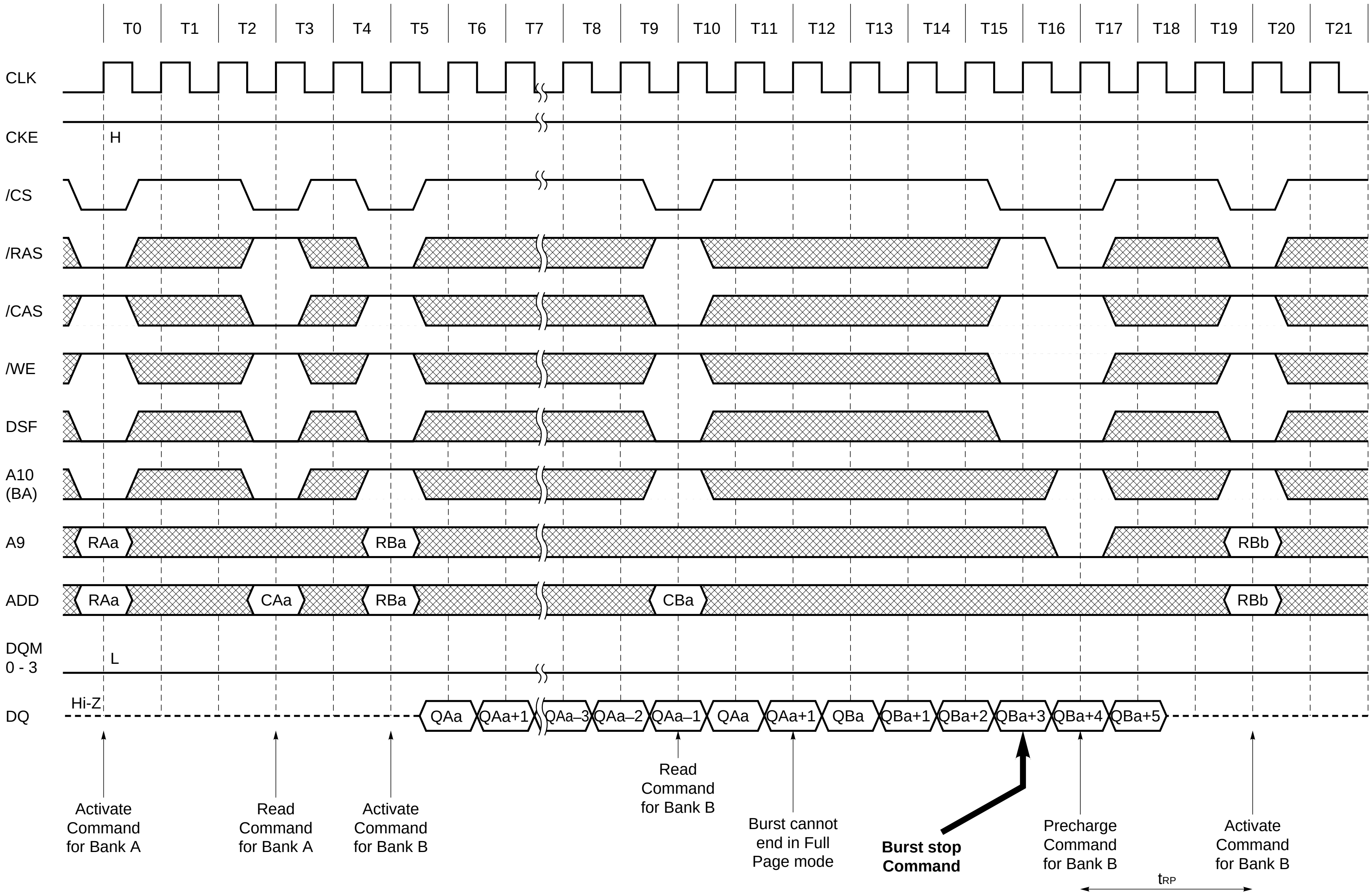


16.4.5 Full Page Mode Cycle

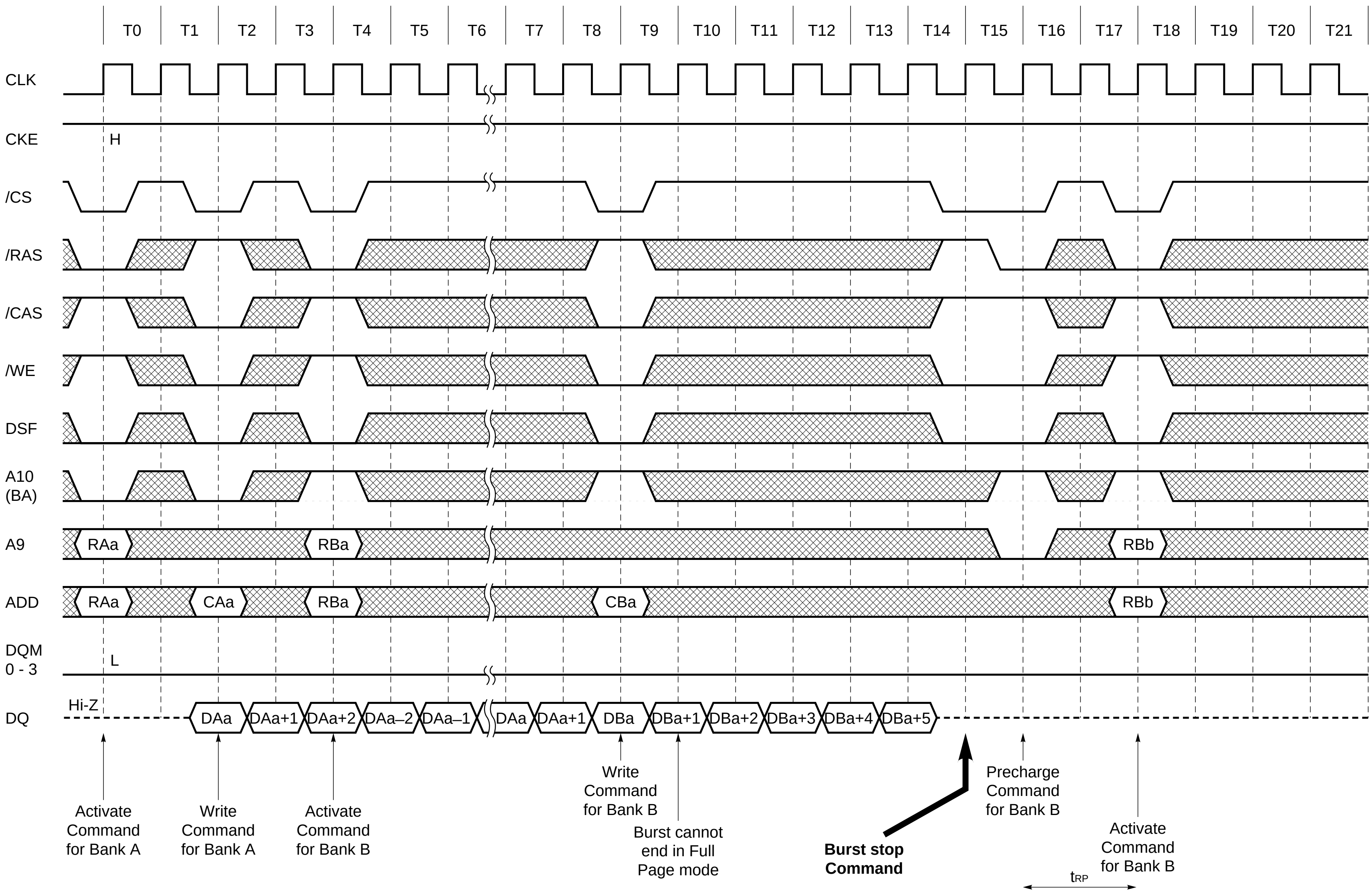
Full Page READ Cycle (1/2) (/CAS latency = 2)



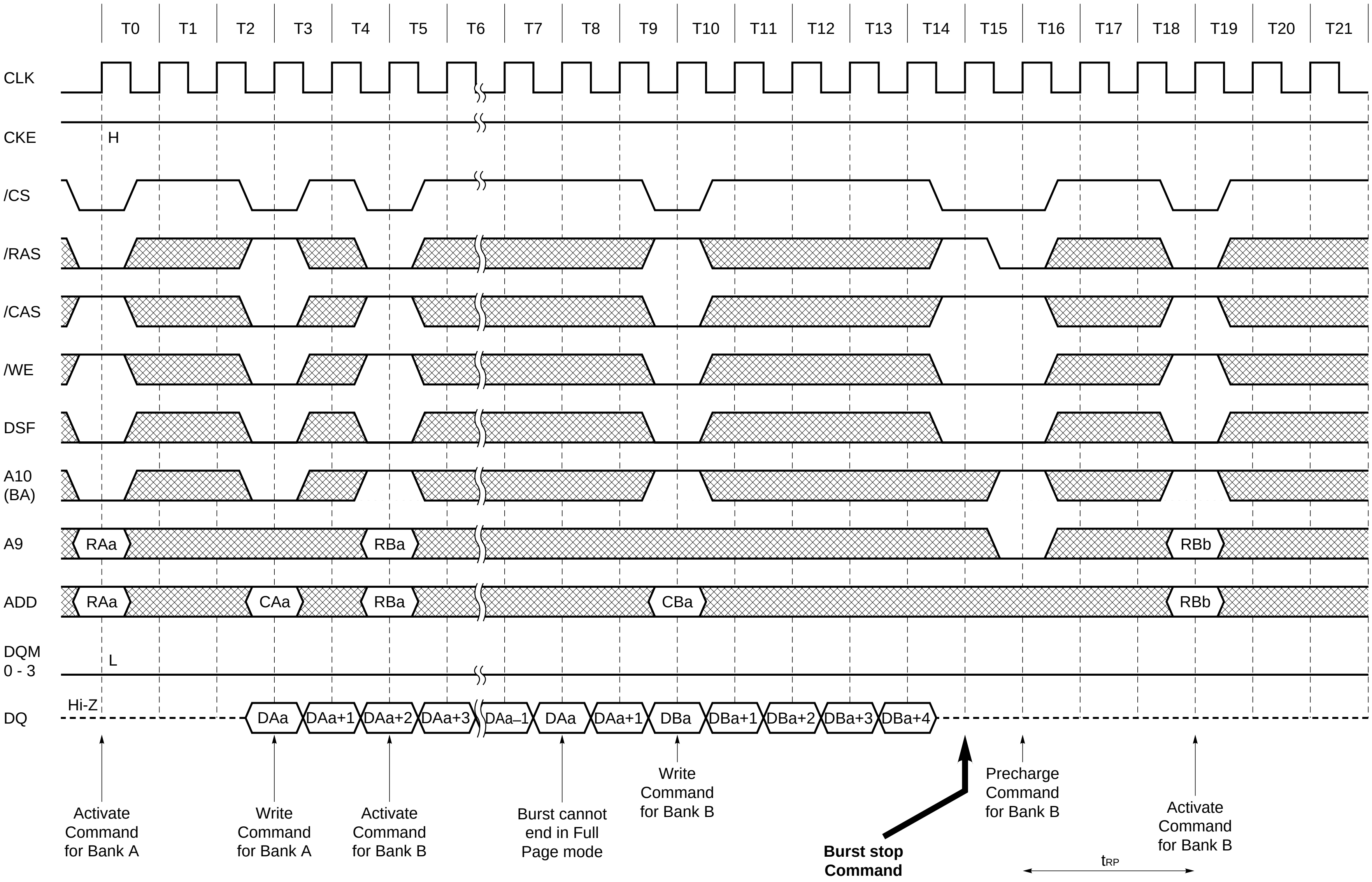
Full Page READ Cycle (2/2) (/CAS latency = 3)



Full Page WRITE Cycle (1/2) (/CAS latency = 2)

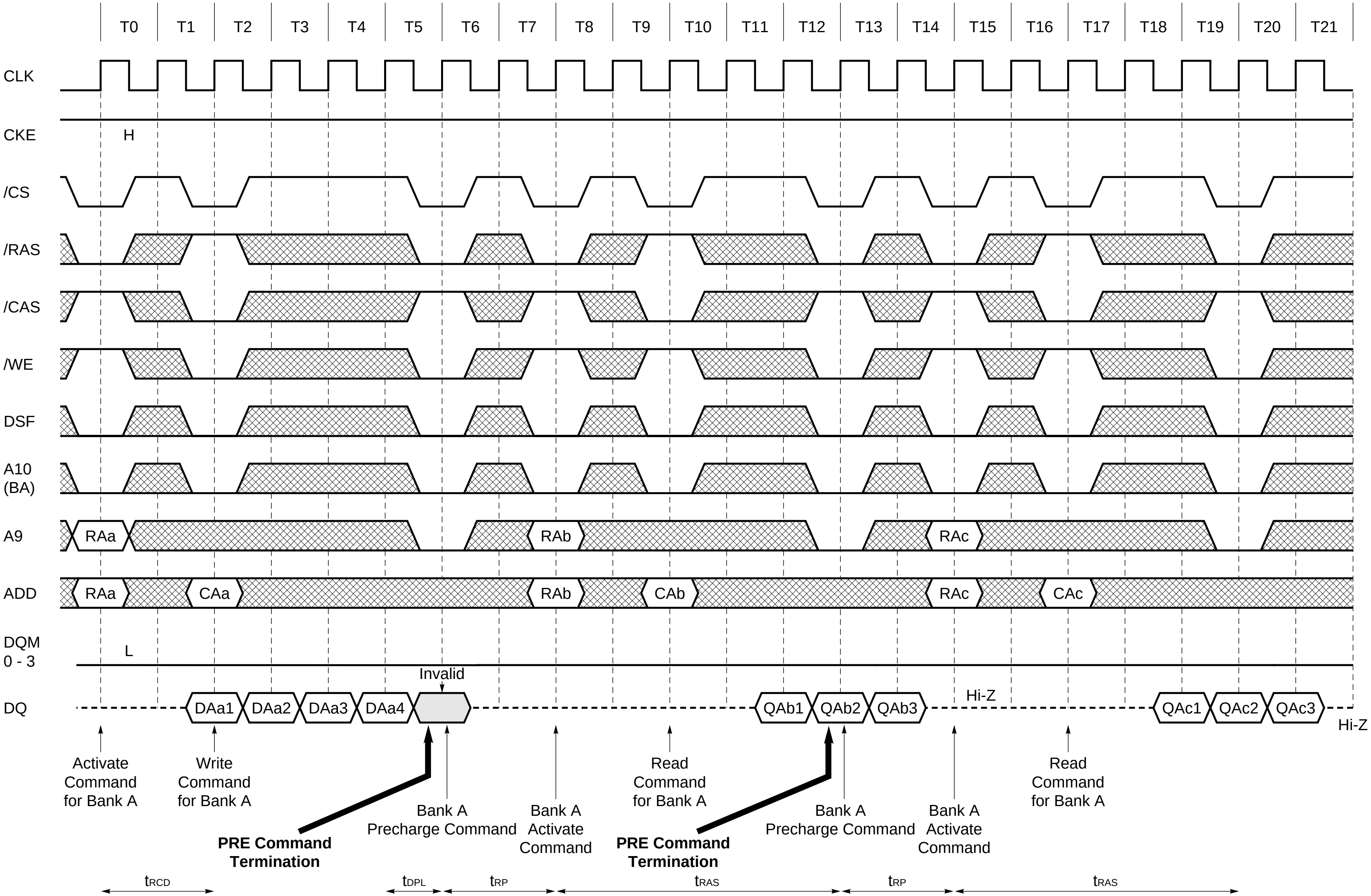


Full Page WRITE Cycle (2/2) (/CAS latency = 3)

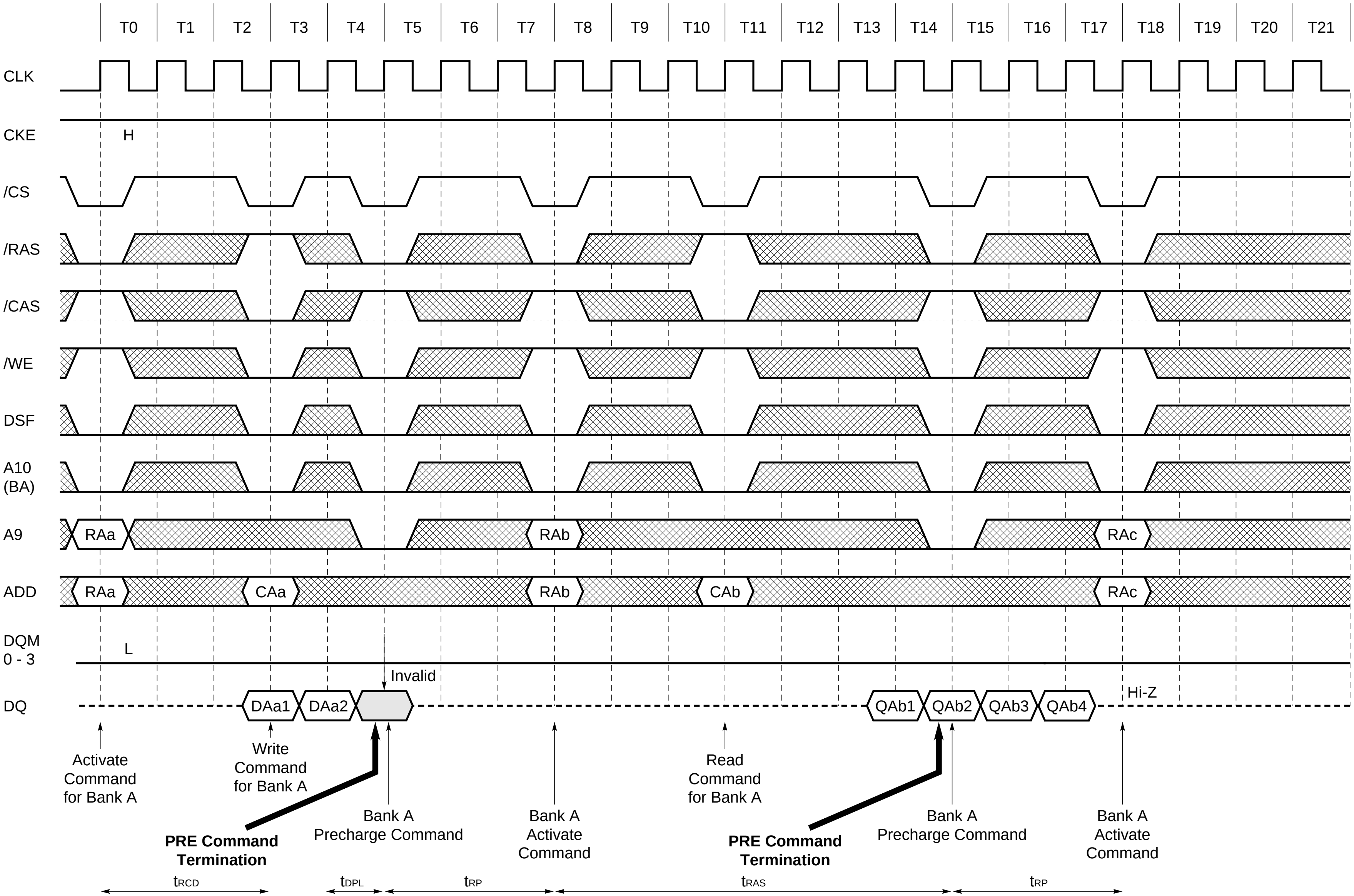


16.4.6 Precharge Termination Cycle

PRE (Precharge) Termination of Burst (1/2) (Burst length = 2, 4, 8, Full, /CAS latency = 2)

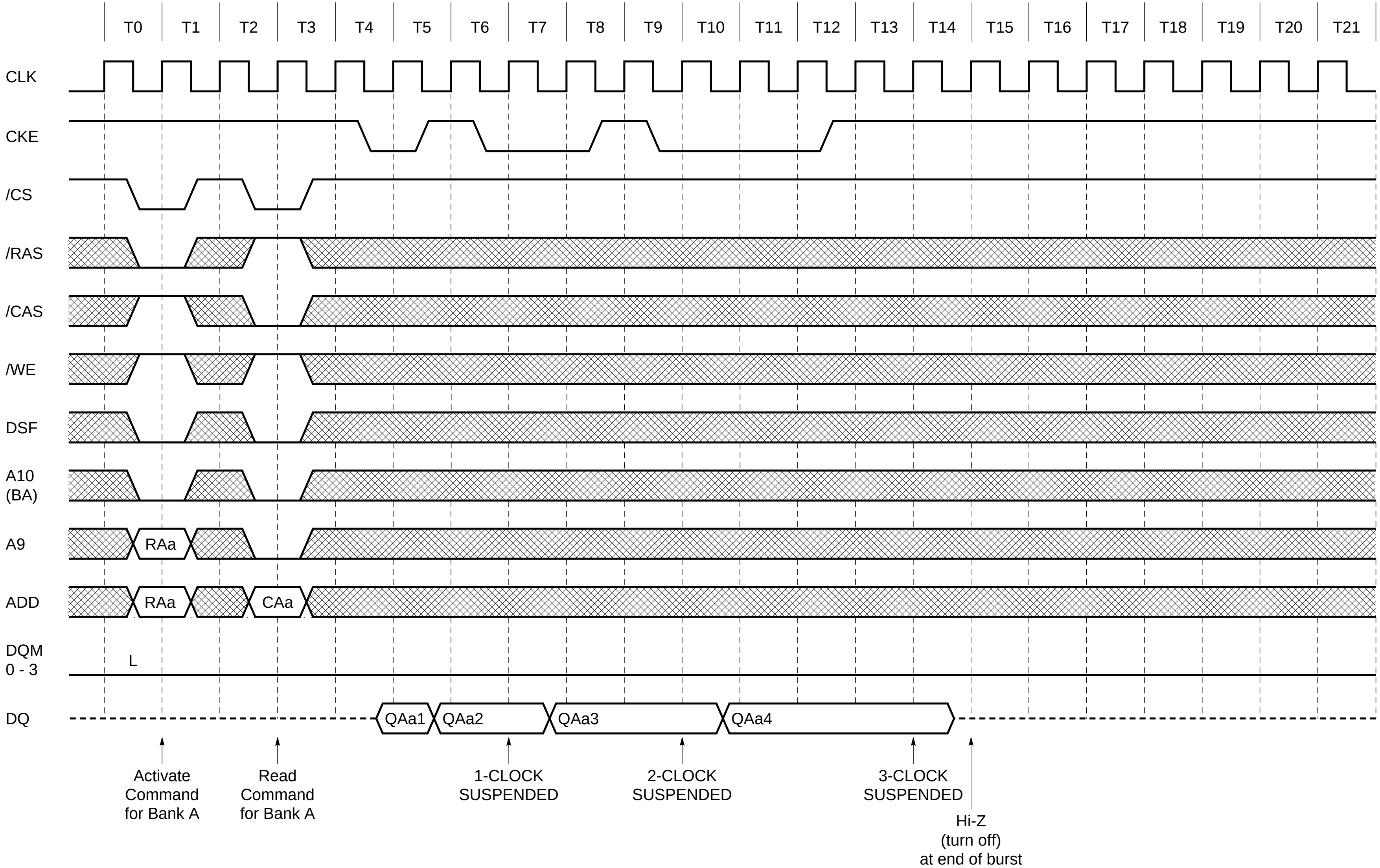


PRE (Precharge) Termination of Burst (2/2) (Burst length = 2, 4, 8, Full, /CAS latency = 3)

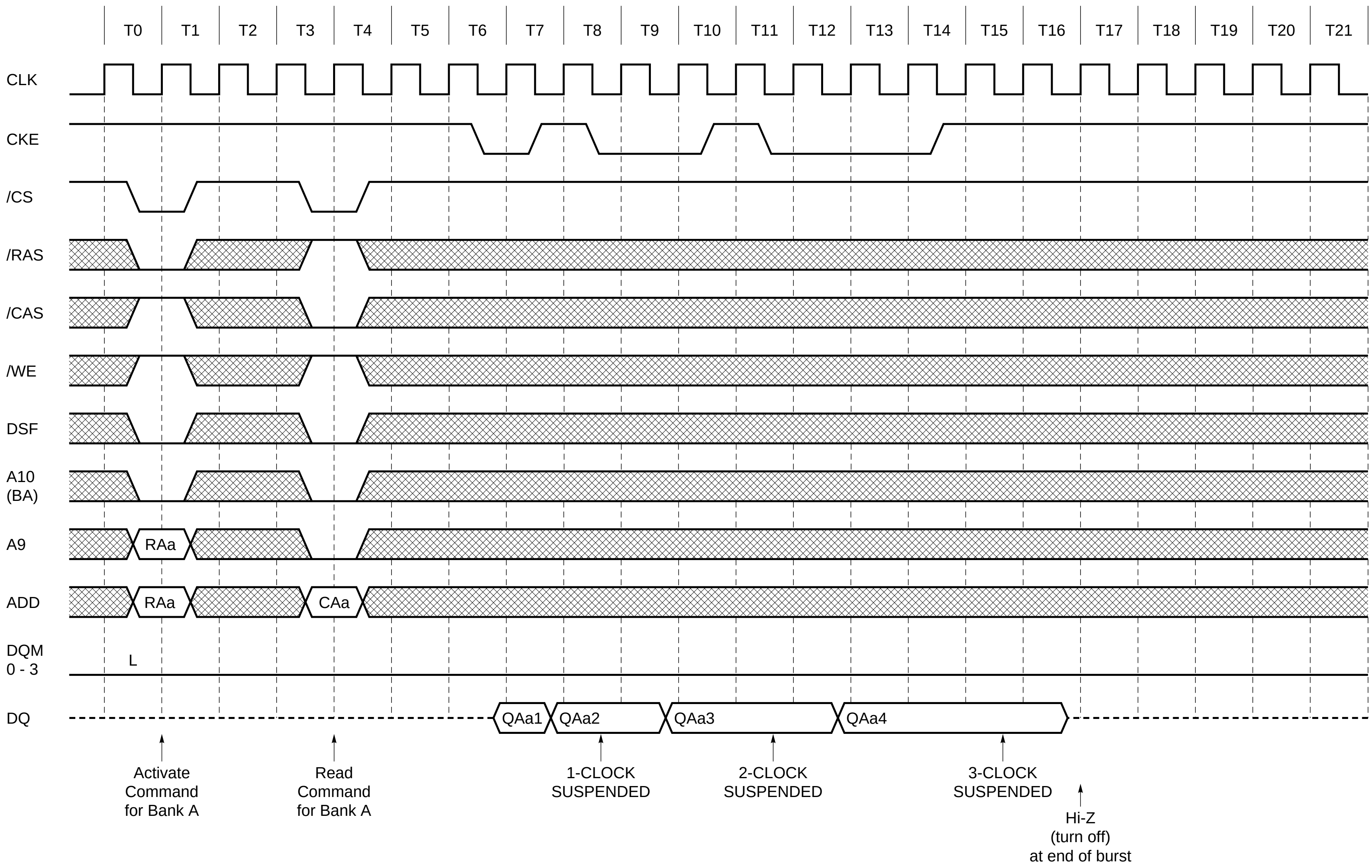


16.4.7 Clock Suspension

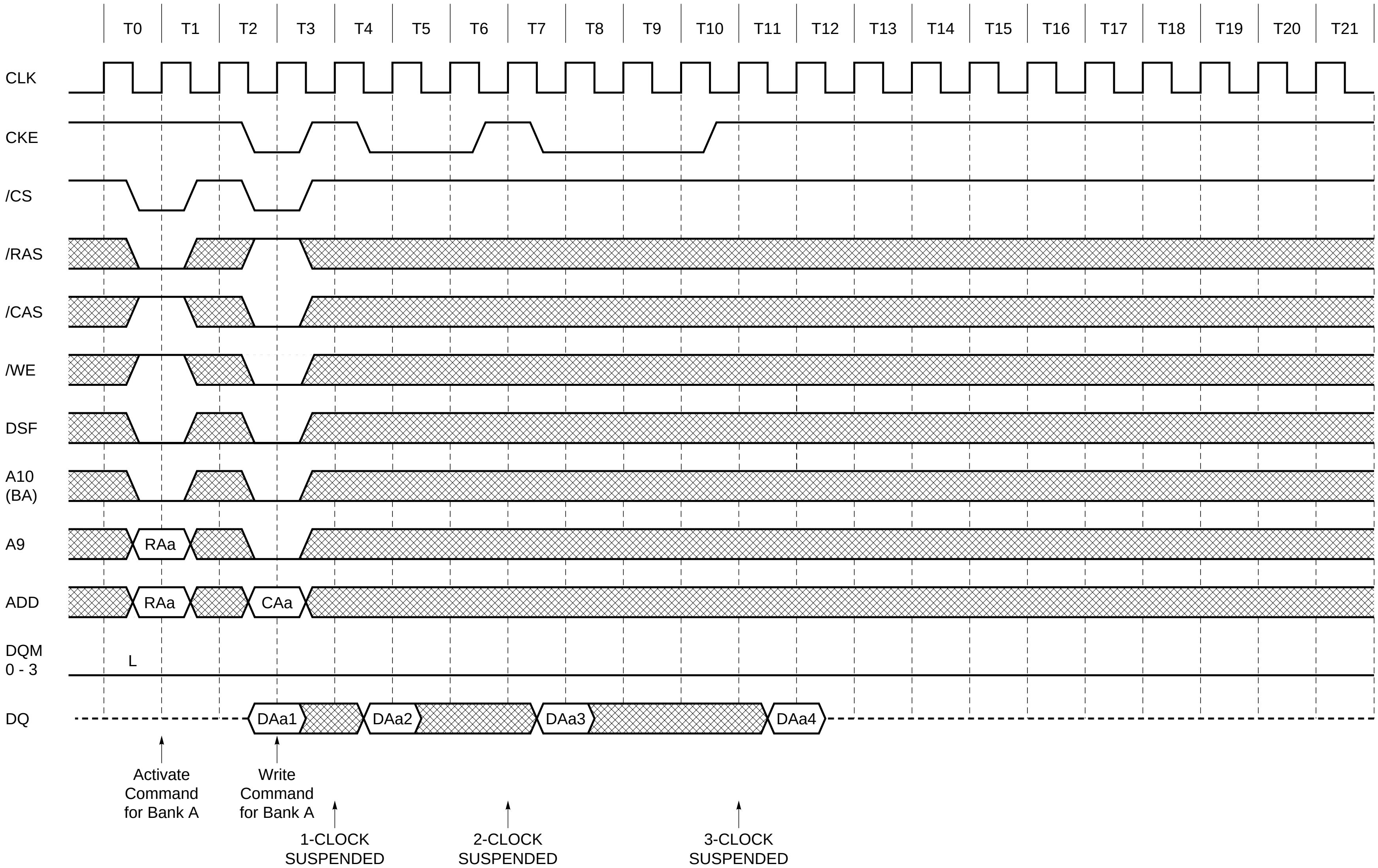
Clock Suspension during Burst Read (using CKE Function) (1/2) (Burst length = 4, /CAS latency = 2)



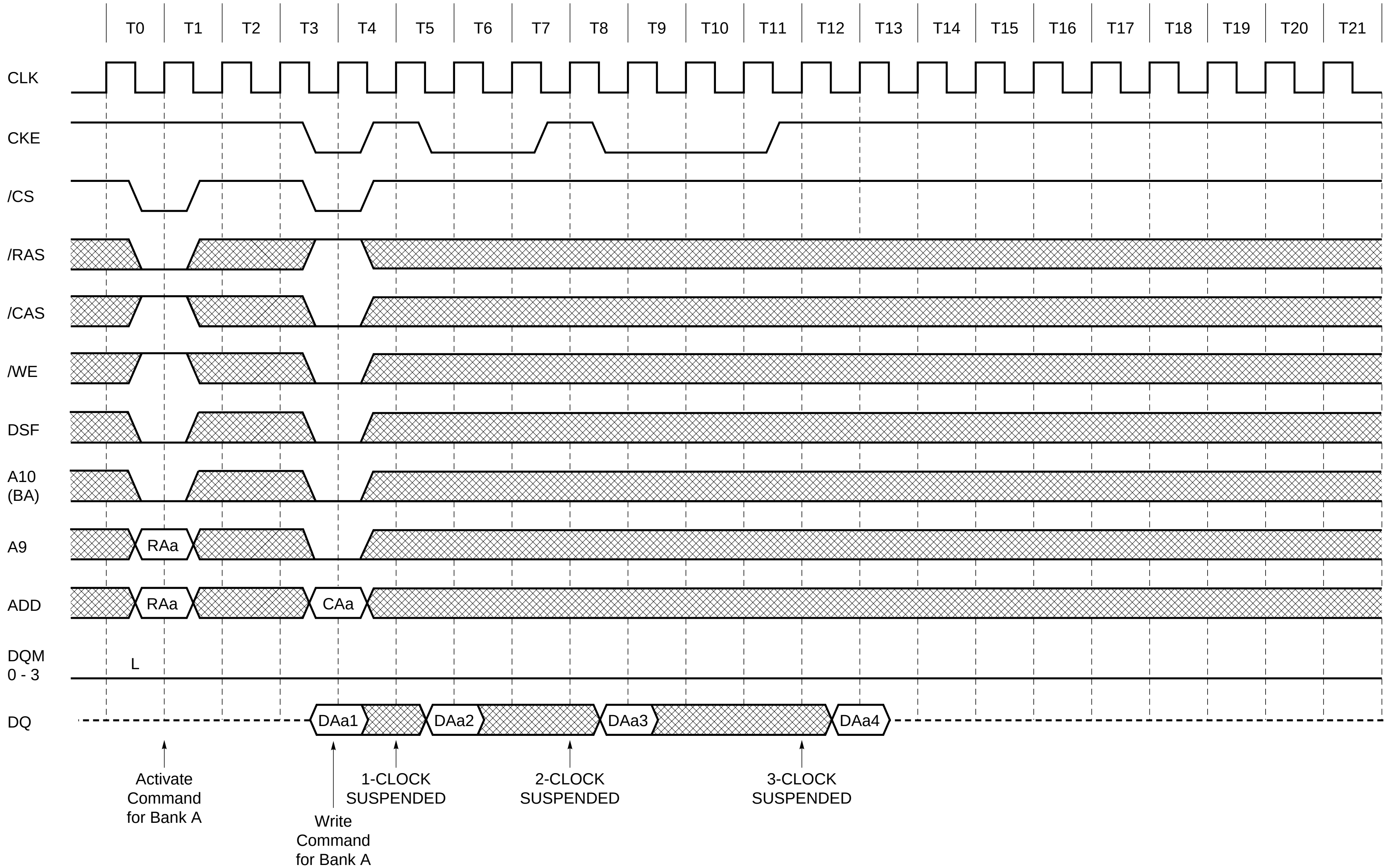
Clock Suspension during Burst Read (using CKE Function) (2/2) (Burst length = 4, /CAS latency = 3)



Clock Suspension during Burst Write (using CKE Function) (1/2) (Burst length = 4, /CAS latency = 2)

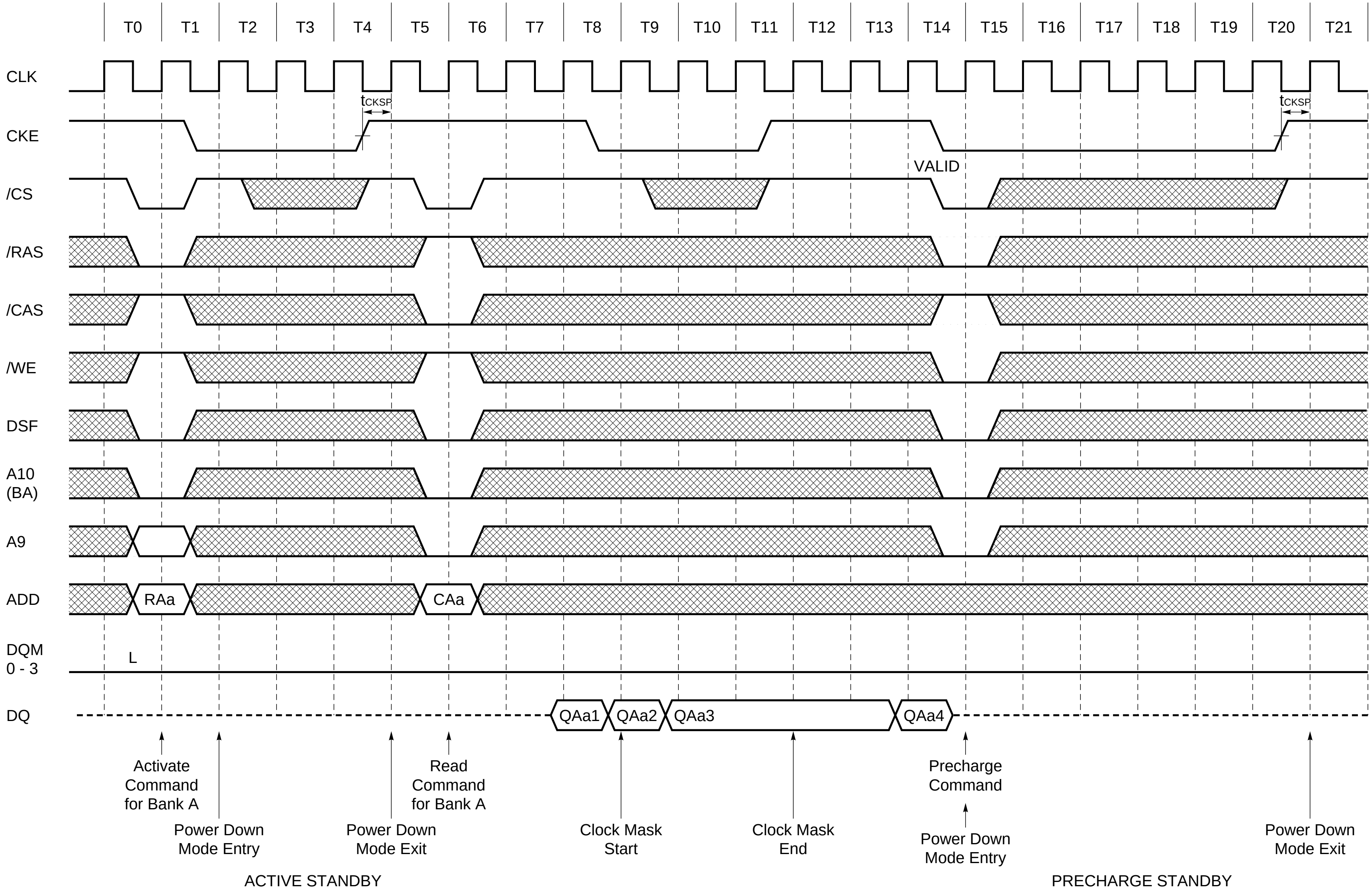


Clock Suspension during Burst Write (using CKE Function) (2/2) (Burst length = 4, /CAS latency = 3)



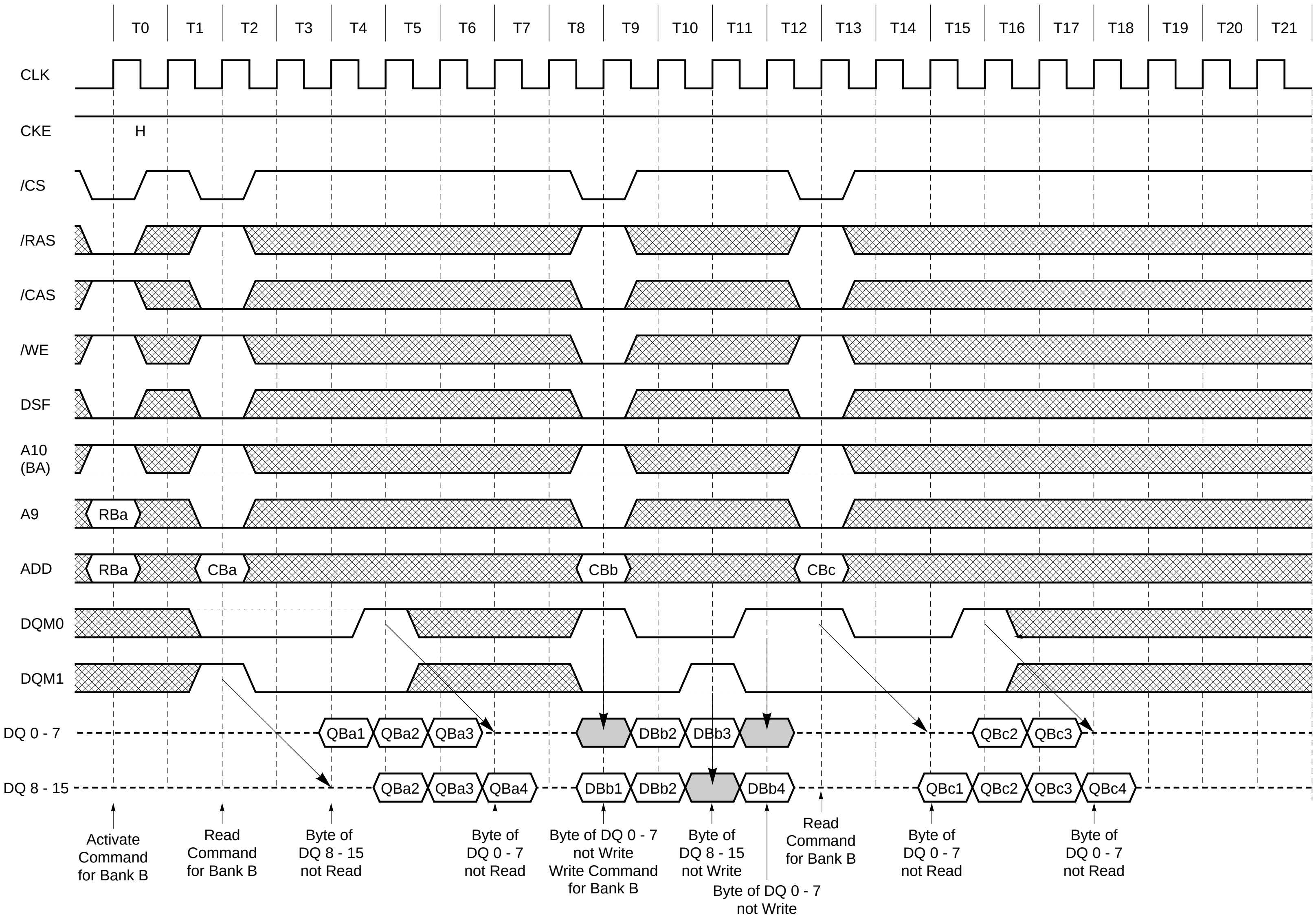
16.4.8 Power Down Mode

Power Down Mode and Clock Suspension (Burst length = 4, /CAS latency = 2)



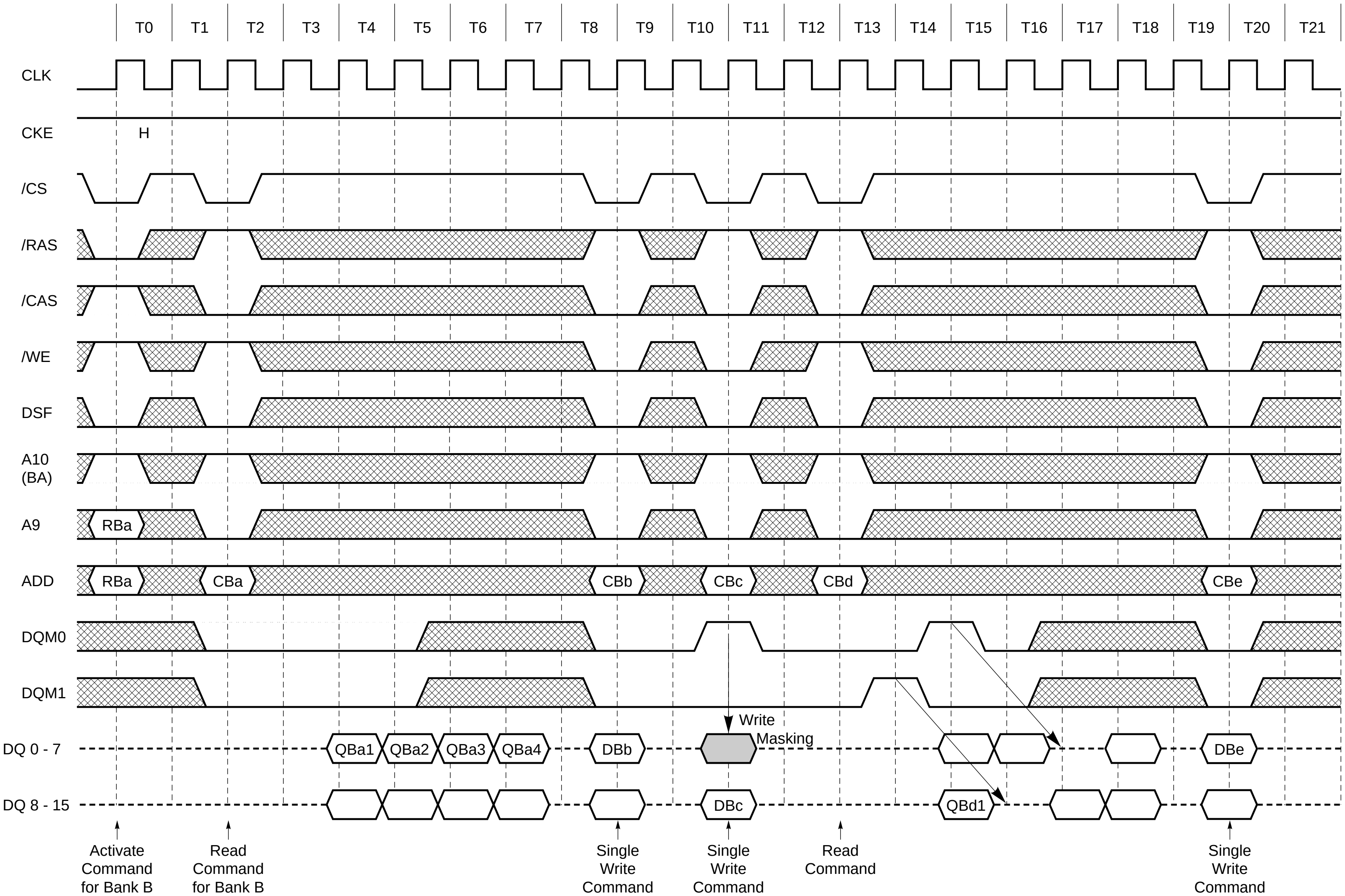
16.4.9 Other Cycles

Byte Read/Write Operation (By DQM) (Burst length = 4, /CAS latency = 2)



Remark The timings of DQM2, DQM3, and the corresponding DQ16 - 23, DQ24 - 31 are omitted.

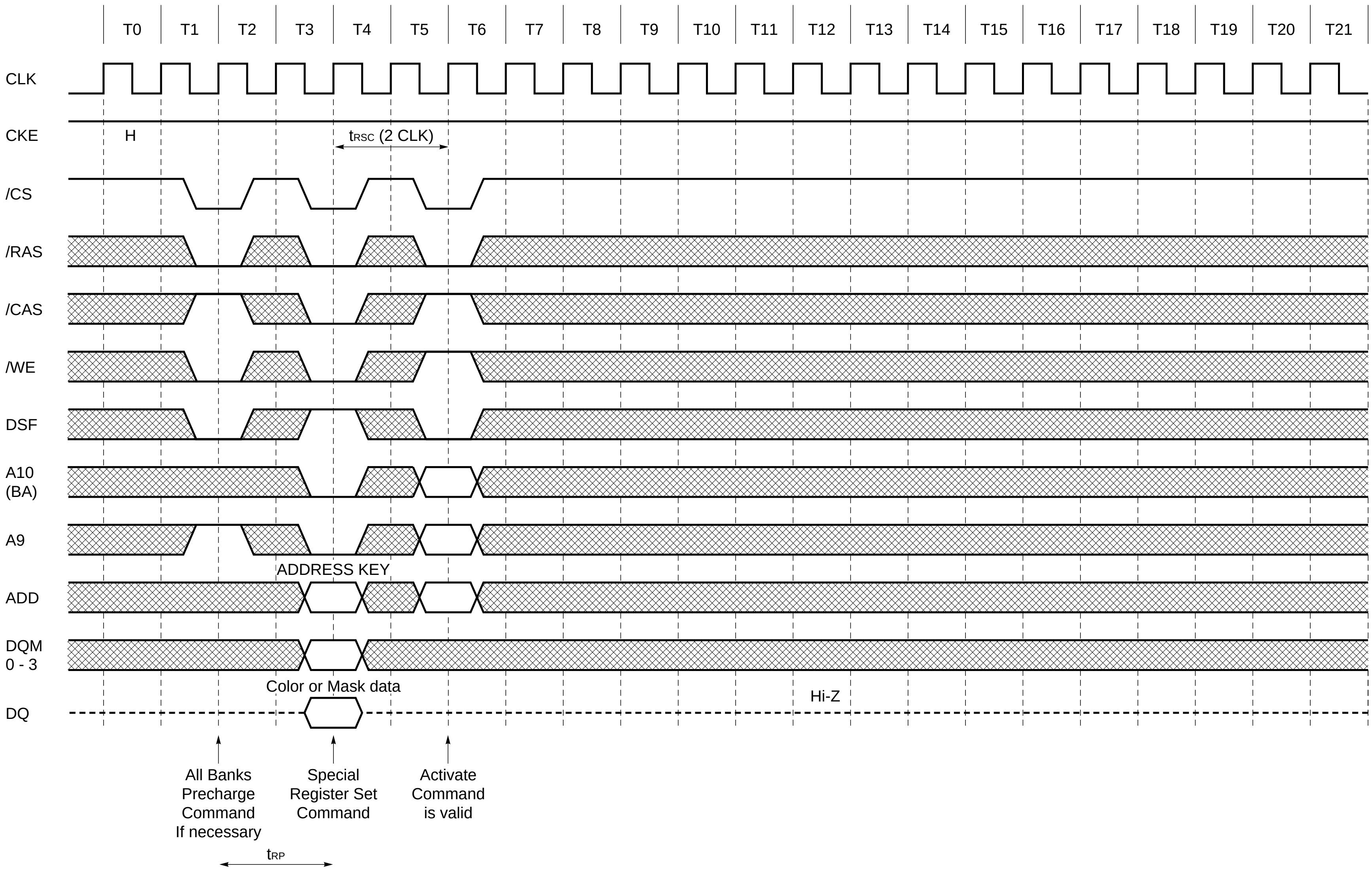
Burst Read and Single Write (Burst length = 4, /CAS latency = 2)



Remark The timings of DQM2, DQM3, and the corresponding DQ16 - 23, DQ24 - 31 are omitted.

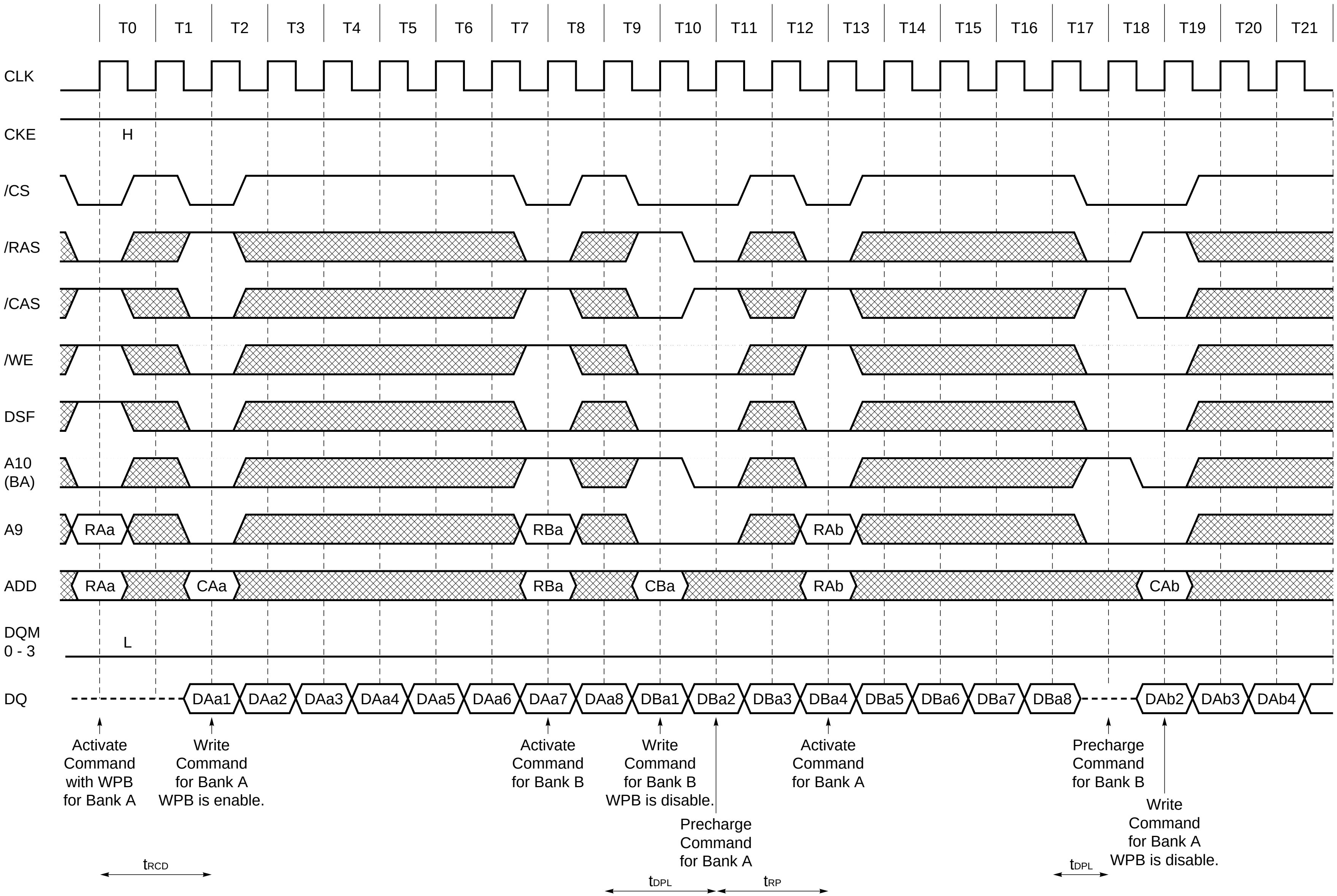
16.5 Graphics Cycles

Special Register Set (Burst length = 4, /CAS latency = 2)

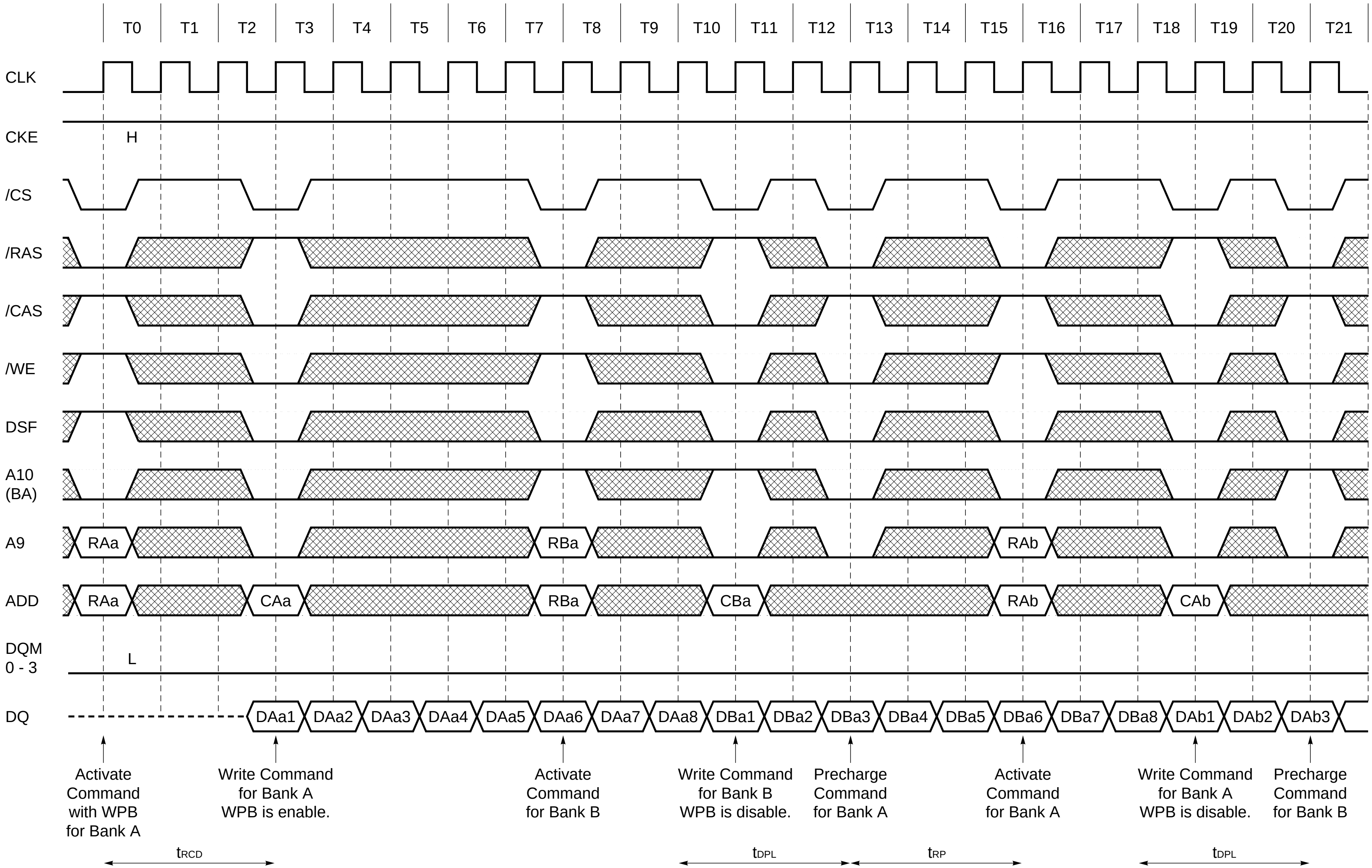


Remark Special Register Set command is able to input at idle state or row active state.

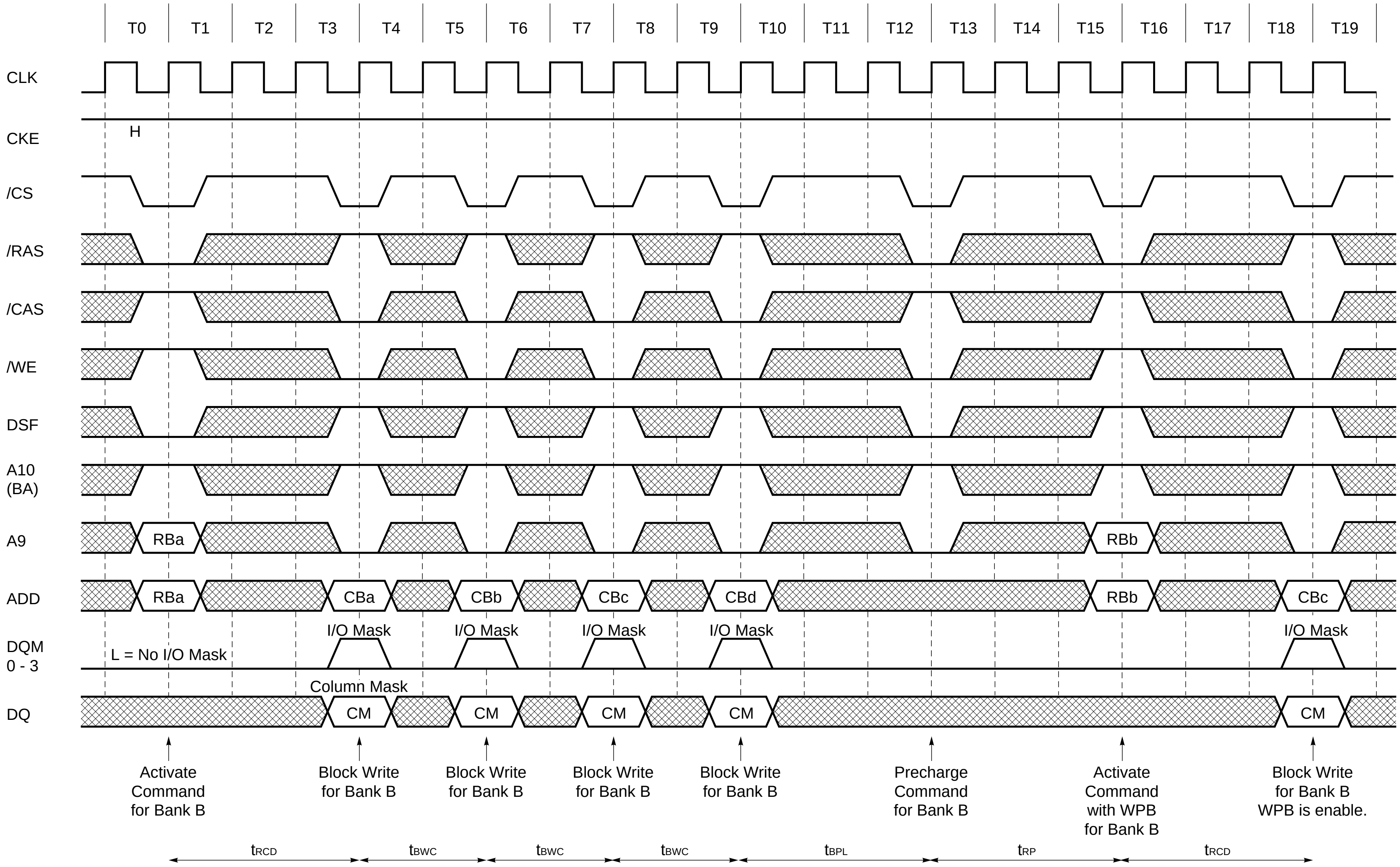
Random Row Write with WPB (Ping-pong banks) (1/2) (Burst length = 8, /CAS latency = 2)



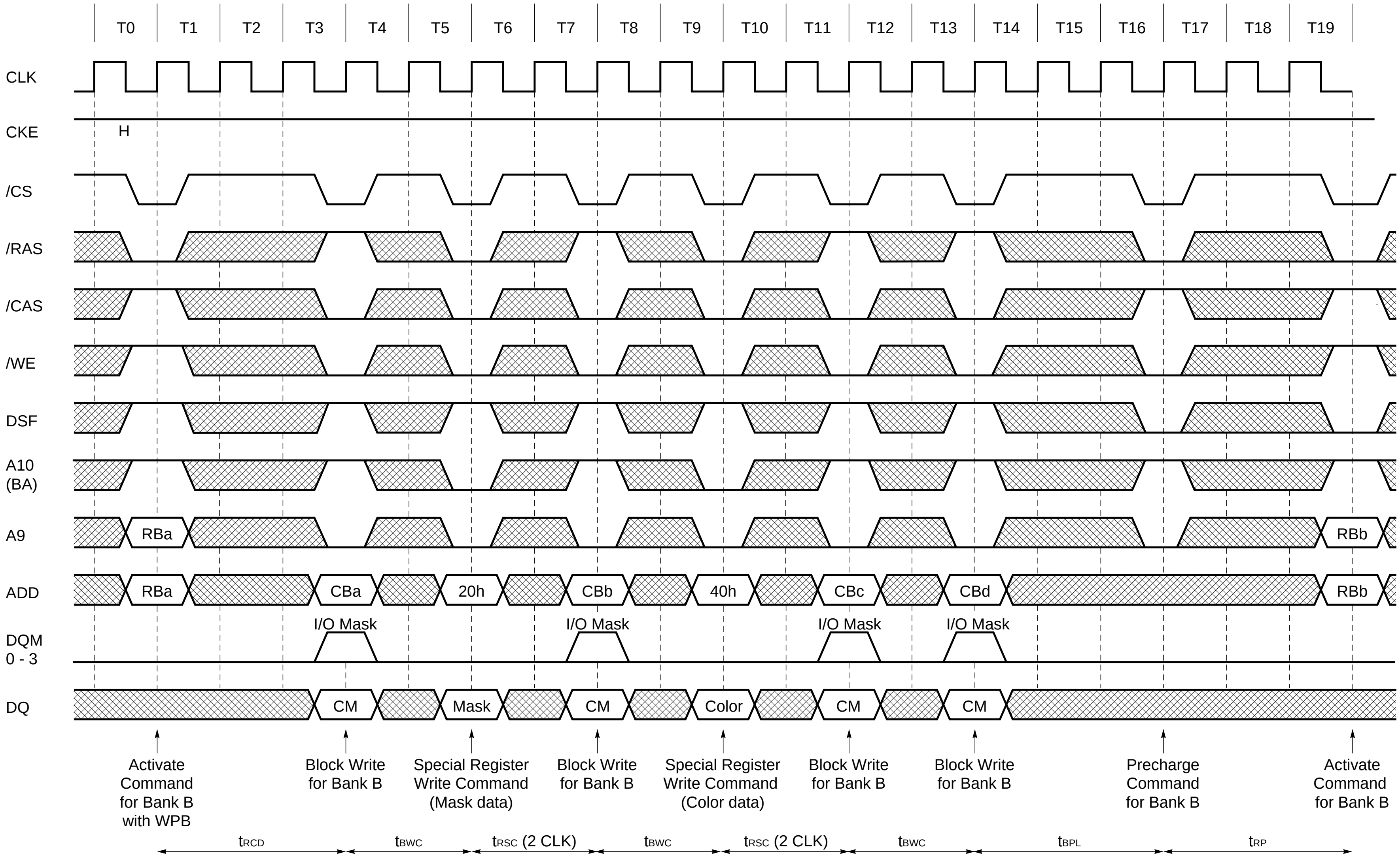
Random Row Write with WPB (Ping-pong banks) (2/2) (Burst length = 8, /CAS latency = 3)



Block Write (page at same bank) (/CAS latency = 3)



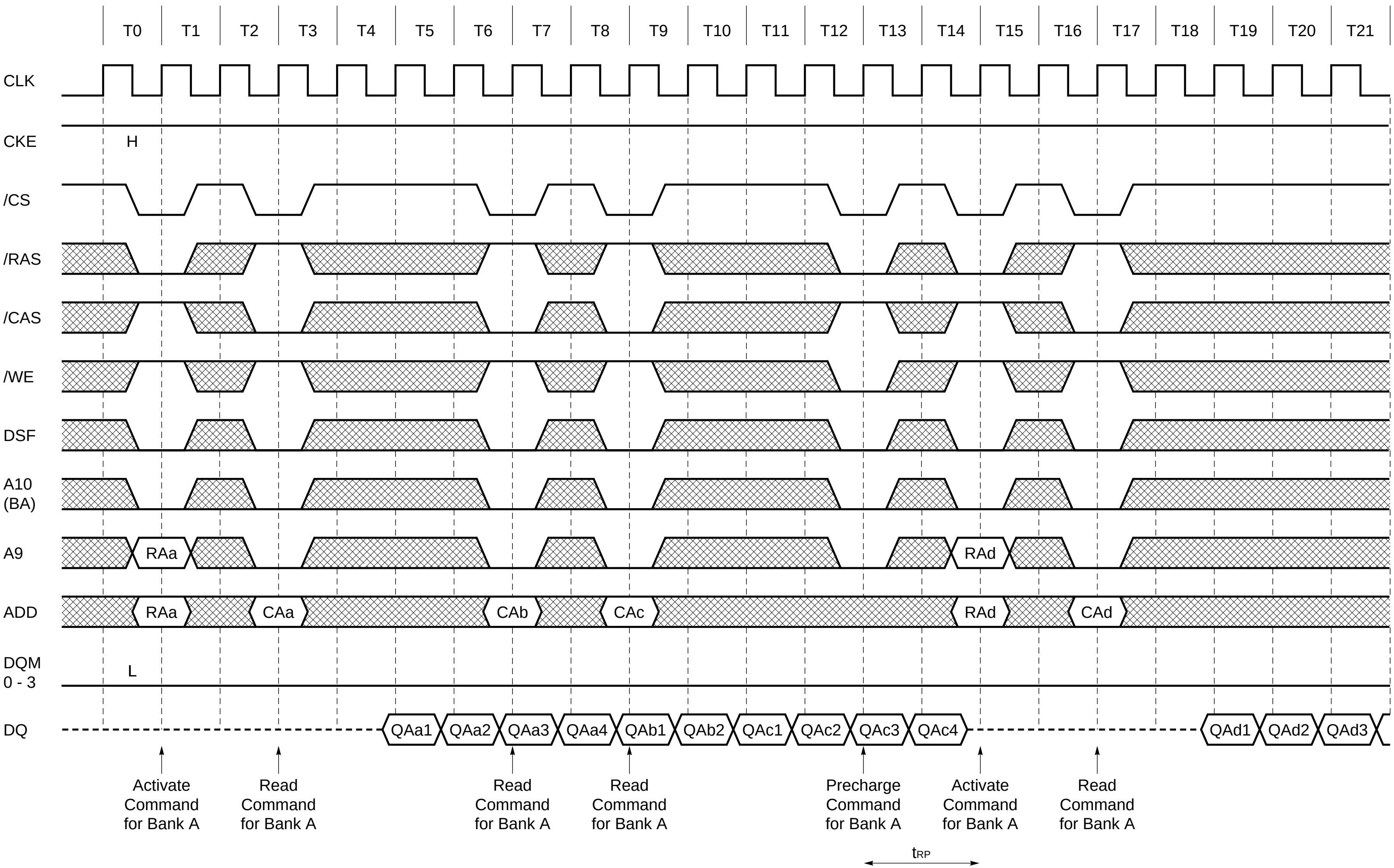
Block Write (page at same bank) changing color and mask data (/CAS latency = 3)



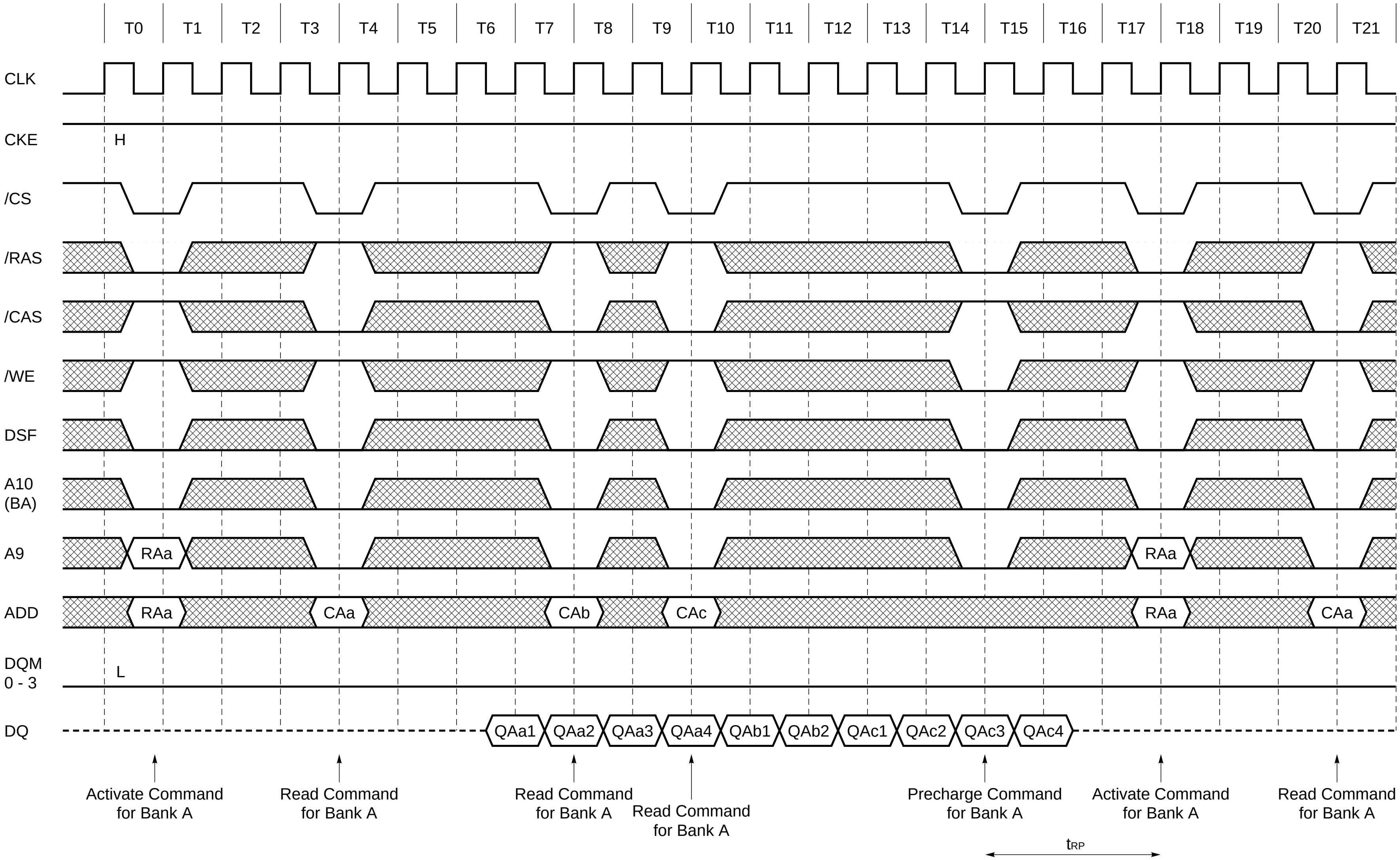
16.6 Application Cycles

16.6.1 Page Cycles with Same Bank

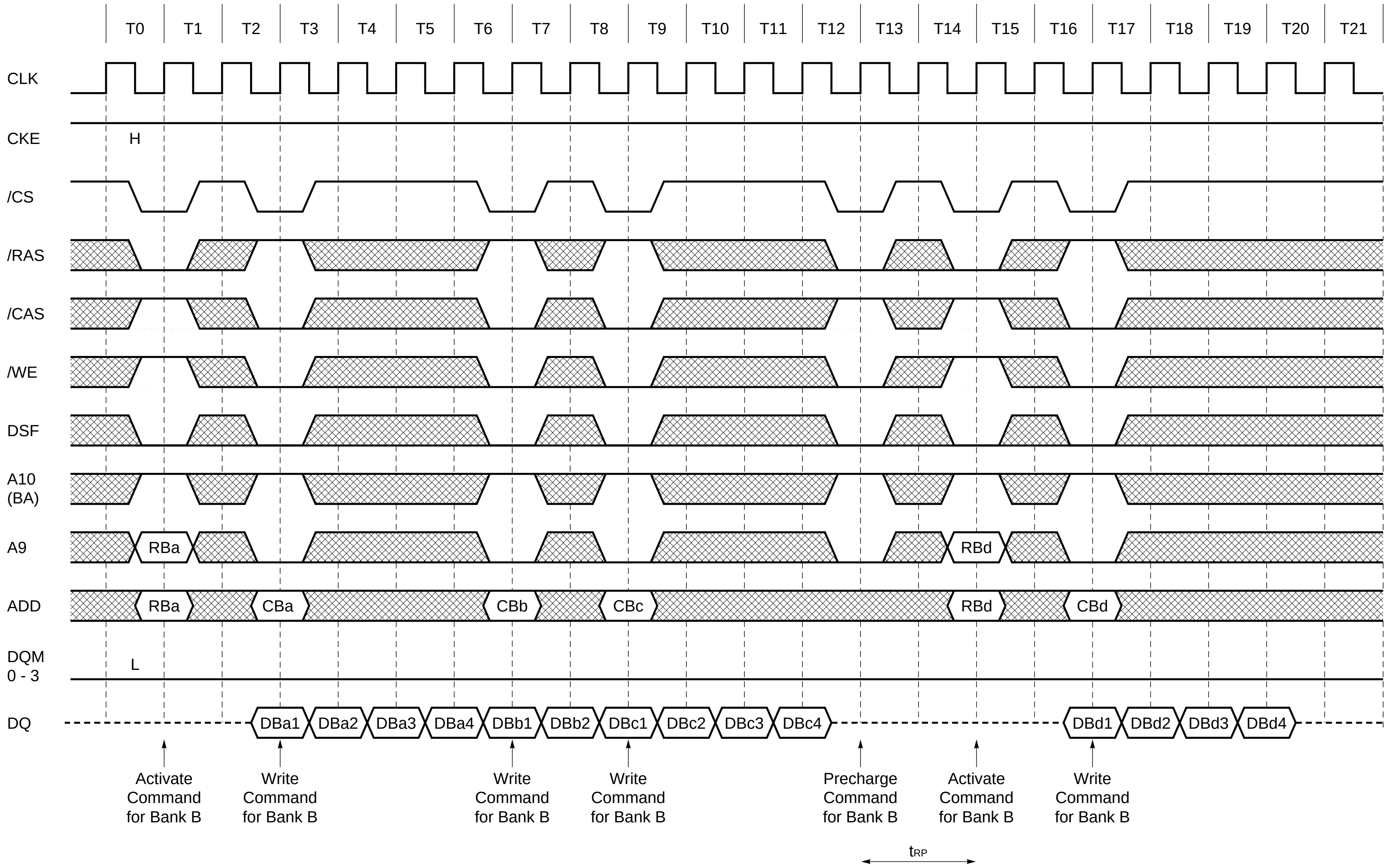
Random Column Read (page with same bank) (1/2) (Burst length = 4, /CAS latency = 2)



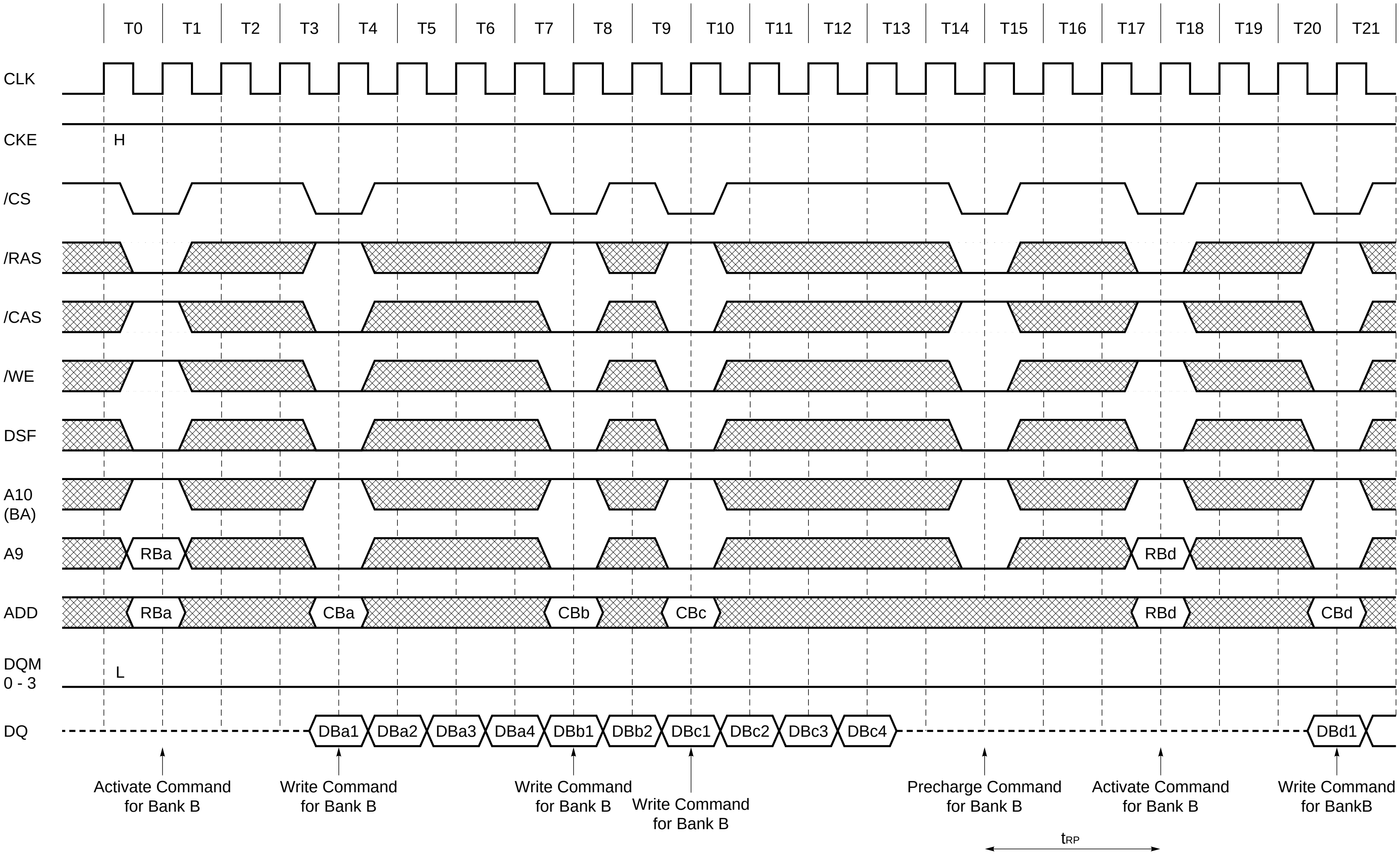
Random Column Read (page with same bank) (2/2) (Burst length = 4, /CAS latency = 3)



Random Column Write (page with same bank) (1/2) (Burst length = 4, /CAS latency = 2)

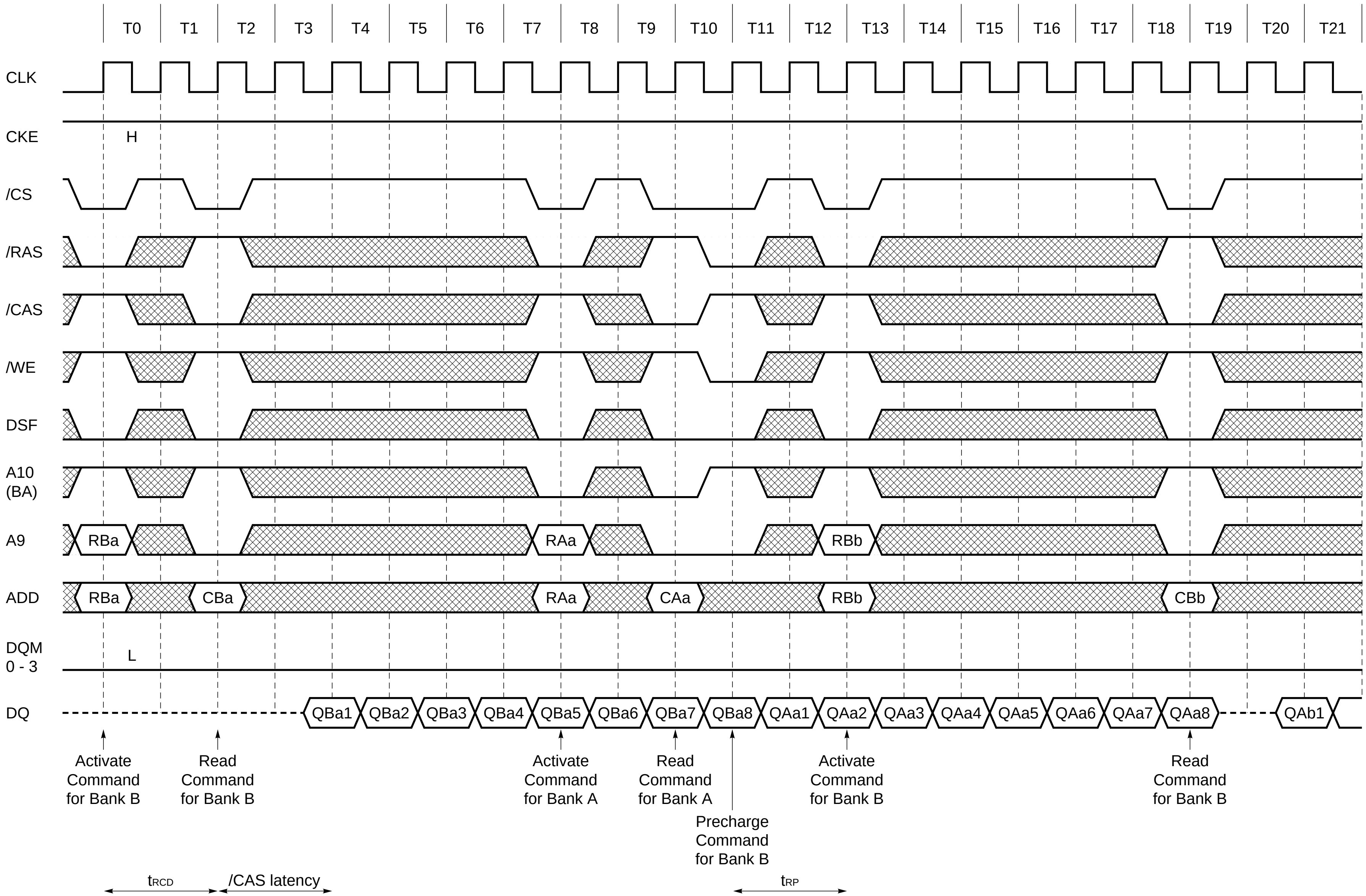


Random Column Write (page with same bank) (2/2) (Burst length = 4, /CAS latency = 3)

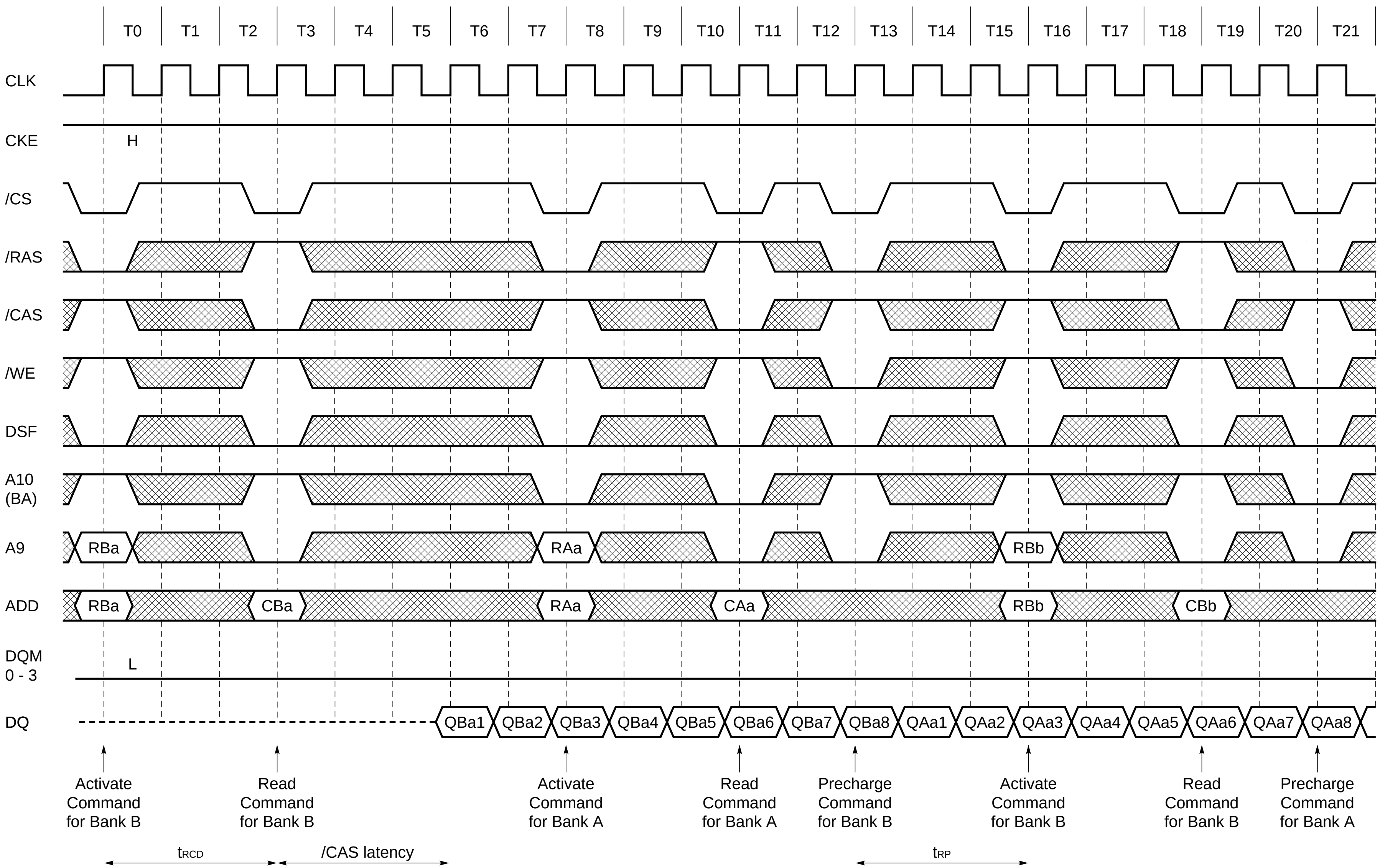


16.6.2 Cycles with Ping-pong Banks

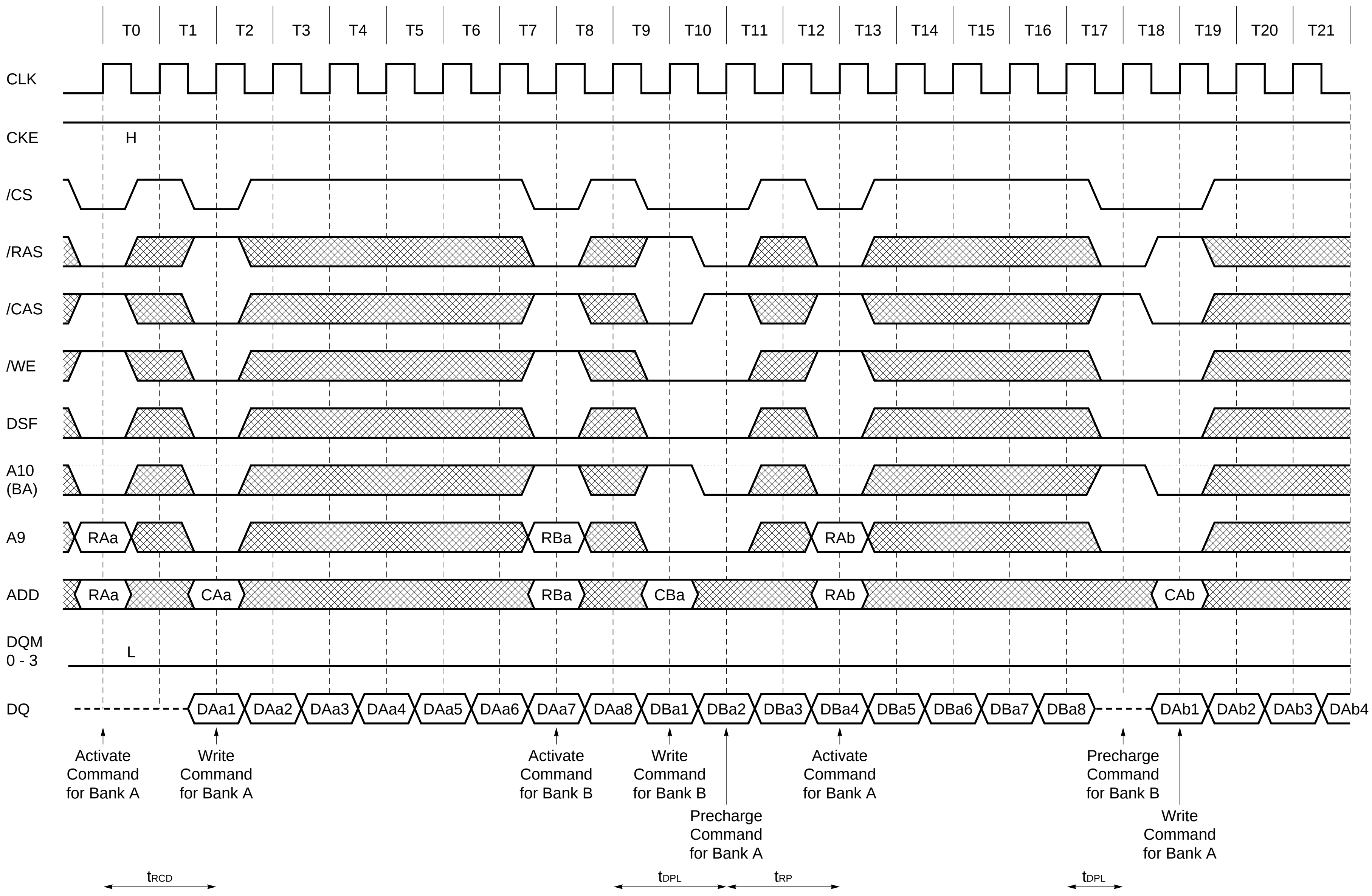
Random Row Read (Ping-pong banks) (1/2) (Burst length = 8, /CAS latency = 2)



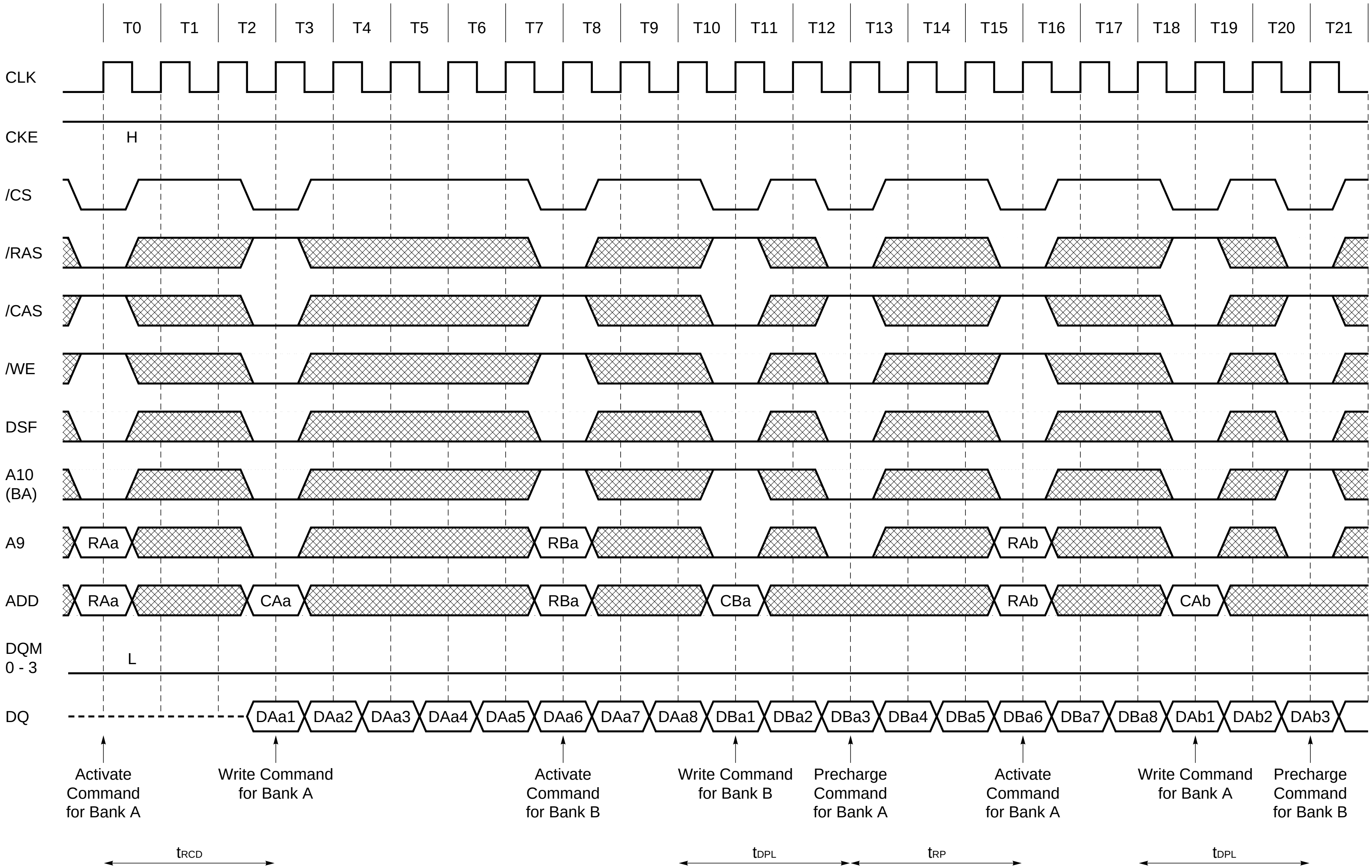
Random Row Read (Ping-pong banks) (2/2) (Burst length = 8, /CAS latency = 3)



Random Row Write (Ping-pong banks) (1/2) (Burst length = 8, /CAS latency = 2)

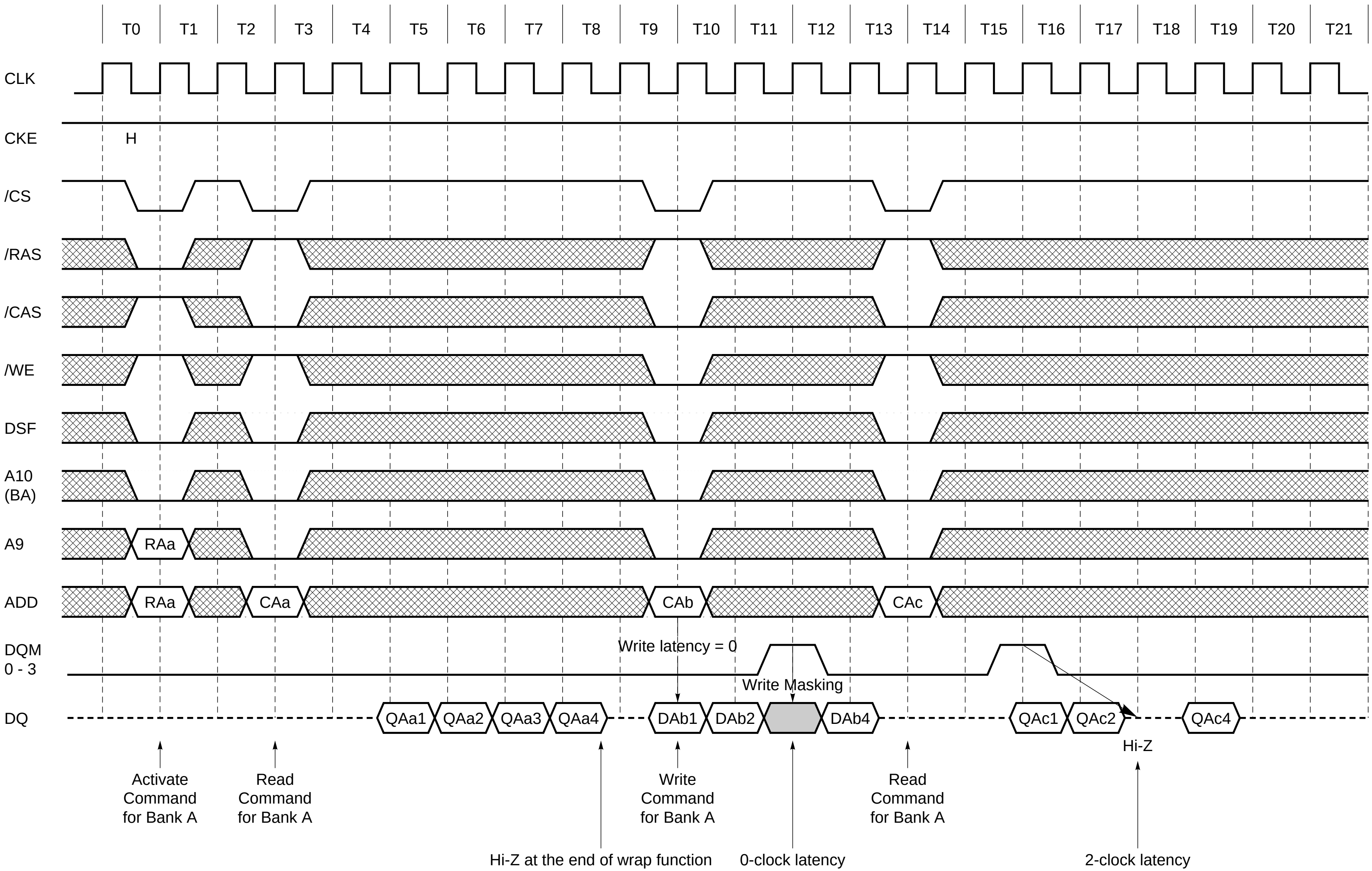


Random Row Write (Ping-pong banks) (2/2) (Burst length = 8, /CAS latency = 3)

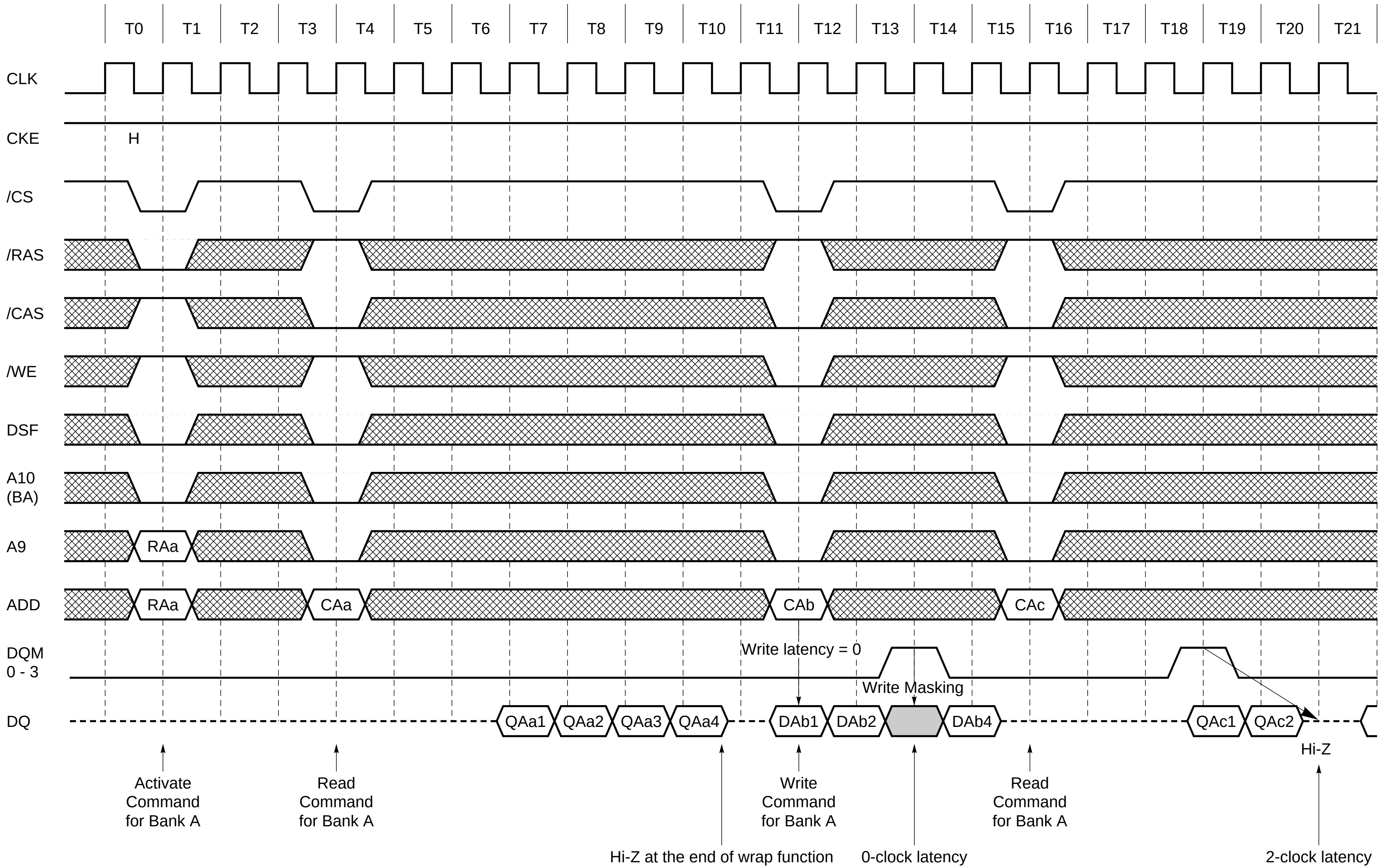


16.6.3 READ and WRITE Cycles

READ and WRITE (1/2) (Burst length = 4, /CAS latency = 2)

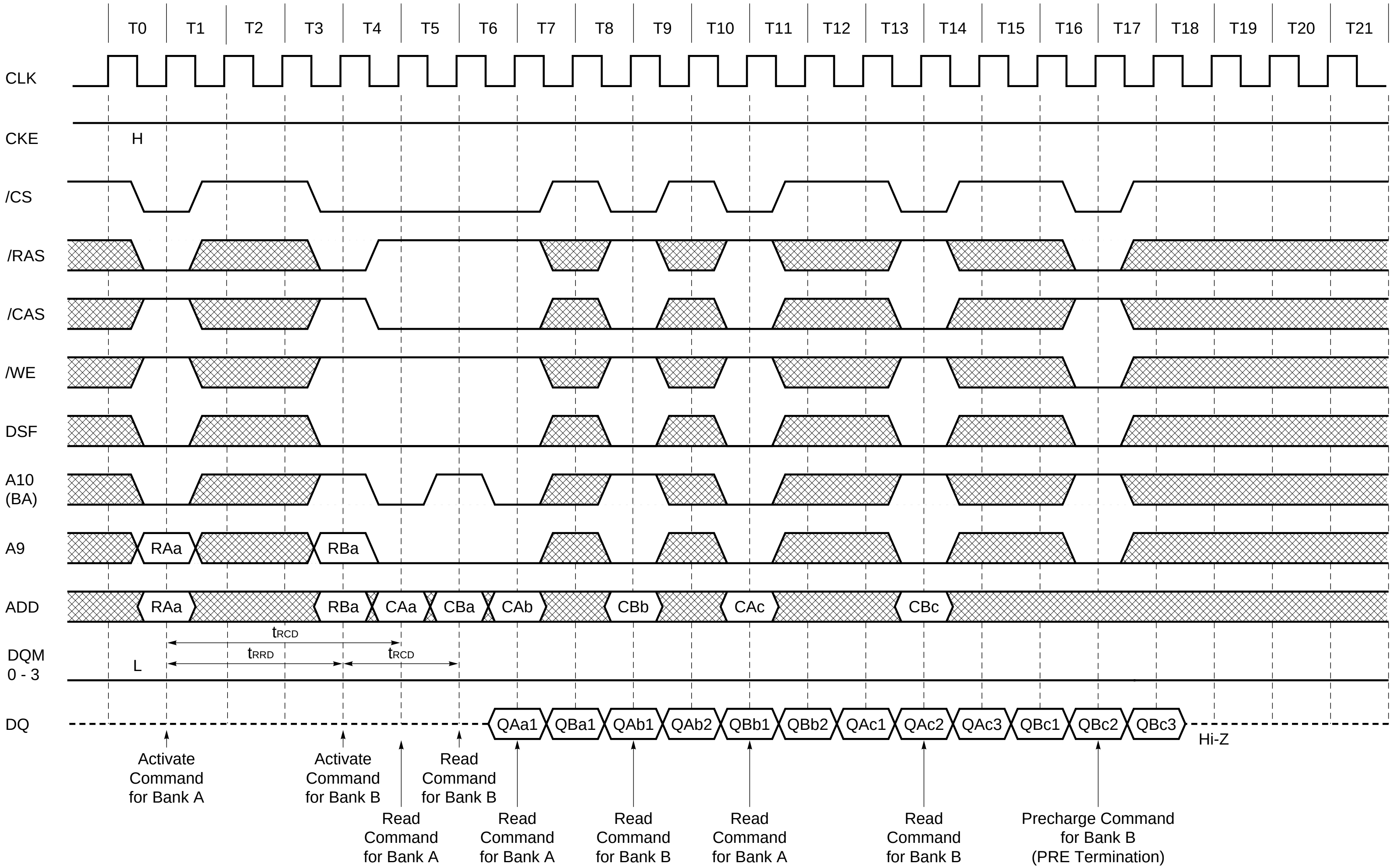


READ and WRITE (2/2) (Burst length = 4, /CAS latency = 3)

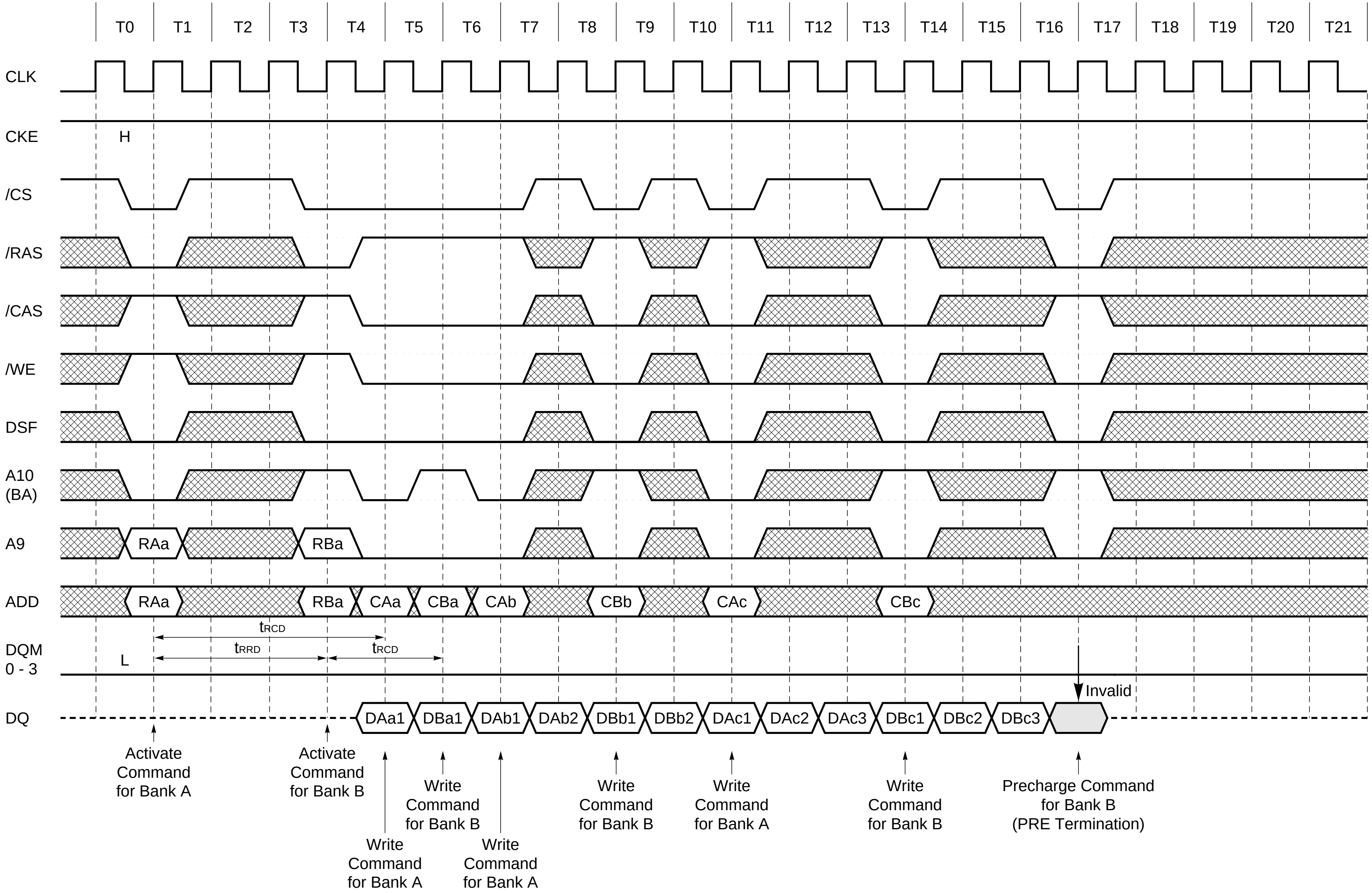


16.6.4 Full Page Random Cycles

Full Page Random Column Read (Burst length = Full Page, /CAS latency = 2)

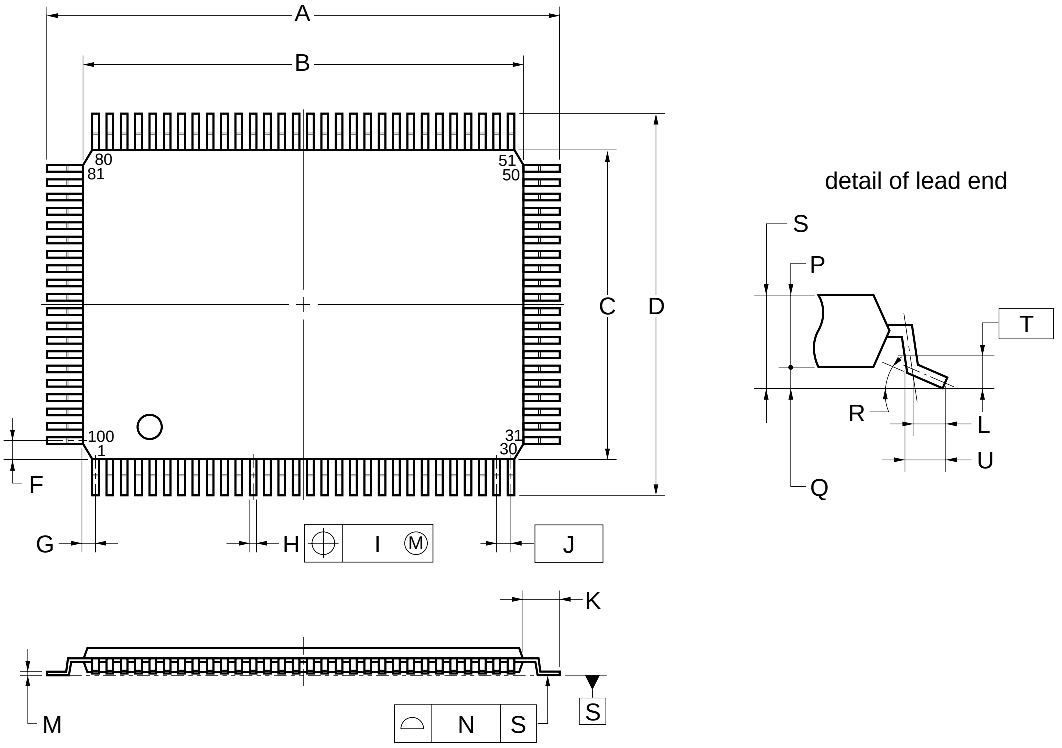


Full Page Random Column Write (Burst length = Full Page, /CAS latency = 2)



17. Package Drawing

100 PIN PLASTIC TQFP (14×20)



NOTES

1. Controlling dimension —— millimeter.
2. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.2±0.2	$0.913^{+0.009}_{-0.008}$
B	20.0±0.2	$0.787^{+0.009}_{-0.008}$
C	14.0±0.2	0.551±0.008
D	17.2±0.2	0.677±0.008
F	0.825	0.032
G	0.575	0.023
H	0.32±0.06	$0.013^{+0.002}_{-0.003}$
I	0.10	0.004
J	0.65(T.P.)	0.026
K	1.6±0.15	0.063±0.006
L	0.8	0.031
M	0.17±0.05	$0.007^{+0.002}_{-0.003}$
N	0.10	0.004
P	1.0	0.039
Q	0.1±0.05	0.004±0.002
R	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
S	$1.10^{+0.30}_{-0.05}$	$0.043^{+0.013}_{-0.002}$
T	0.25	0.010
U	0.88±0.15	$0.035^{+0.007}_{-0.006}$

S100GF-65-9BT

18. Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD4811650.

Type of Surface Mount Device

μPD4811650GF-9BT : 100-pin Plastic TQFP (14 x 20 mm)

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]