

TC55464P/J-17, TC55464P/J-20 TC55464P/J-25, TC55464P/J-35

65,536 WORD × 4 BIT CMOS STATIC RAM

DESCRIPTION

The TC55464P/J is a 262,144 bits high speed static random access memory organized as 65,536 words by 4 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's CMOS technology and advanced circuit form provide high speed feature.

The TC55464P/J has low power feature with device control using Chip Enable ($\overline{CE}$). Also the device power at memory access is reduced by automatic power down circuit form.

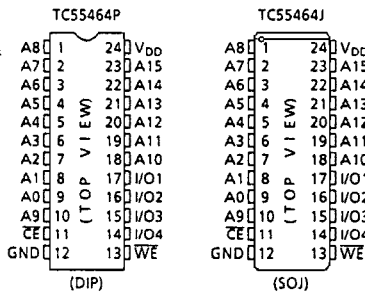
The TC55464P/J is suitable for use in cache memory where high speed is required. All Inputs and Outputs are directly TTL compatible.

The TC55464P/J is packaged in a 24 pin standard DIP and SOJ with 300 mil width for high density surface assembly.

FEATURES

- Fast access time :
 - TC55464P/J-17 17ns(MAX.)
 - TC55464P/J-20 20ns(MAX.)
 - TC55464P/J-25 25ns(MAX.)
 - TC55464P/J-35 35ns(MAX.)
- Low power dissipation
 - Operation : TC55464P/J-17 120mA(MAX.)
 - TC55464P/J-20 120mA(MAX.)
 - TC55464P/J-25 120mA(MAX.)
 - TC55464P/J-35 100mA(MAX.)
 - Standby : 1mA(MAX.)
- 5V single power supply :
 - 17 : 5V±5%
 - 20/25/35 : 5V±10%
- Fully static operation
- All Inputs and Outputs : TTL compatible
- Package
 - TC55464P : DIP24-P-300B
 - TC55464J : SOJ24-P-300A

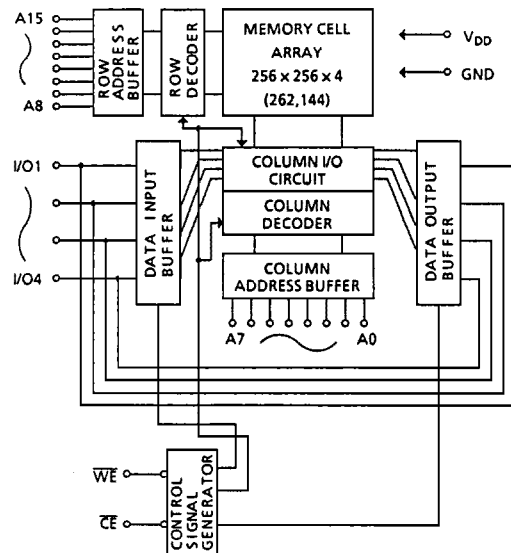
PIN CONNECTION



PIN NAMES

A0~A15	Address Inputs
I/O1~I/O4	Data Inputs / Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
V _{DD}	Power(+ 5V)
GND	Ground

BLOCK DIAGRAM



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MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	- 0.5~7.0	V
V_{IN}	Input Voltage	- 2.0~7.0	V
V_{IO}	Input/Output Voltage	- 0.5~ $V_{DD} + 0.5$	V
P_D	Power Dissipation	1.0	W
T_{solder}	Soldering Temperature - Time	260-10	°C-sec
T_{strg}	Storage Temperature	- 65~150	°C
T_{opr}	Operating Temperature	- 10~85	°C

DC RECOMMENDED OPERATING CONDITIONS ($T_a = 0\sim 70^\circ\text{C}$)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V _{DD}	Power Supply Voltage	- 17	4.75	5.0	5.25	V
		- 20/25/35	4.5	5.0	5.5	
V _{IH}	Input High Voltage		2.2	-	V _{DD} + 0.5	V
V _{IL}	Input Low Voltage		- 0.5 *	-	0.8	V

* - 3V Pulse Width : 10ns

DC and OPERATING CHARACTERISTICS ($T_a = 0\sim 70^\circ\text{C}$, - 17 : $V_{DD} = 5V \pm 5\%$, - 20/25/35 : $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I _{IL}	Input Leakage Current	V _{IN} = 0~V _{DD}			-	-	± 1	μA
I _{OH}	Output High Current	V _{OH} = 2.4V			- 4	-	-	mA
I _{OL}	Output Low Current	V _{OL} = 0.4V			8	-	-	mA
I _{LO}	Output Leakage Current	CE = V _{IH} or WE = V _{IL} , V _{OUT} = 0~V _{DD}			-	-	± 1	μA
I _{DDO}	Operating Current	tcycle = Min cycle CE = V _{IL} Other Input = V _{IH} /V _{IL}	V _{DD} = 5.25V	- 17	-	-	120	mA
				- 20	-	-	120	
			V _{DD} = 5.5V	- 25	-	-	120	
				- 35	-	-	100	
I _{DDs1}	Standby Current	tcycle = Min cycle CE = V _{IH} Other Input = V _{IH} /V _{IL}	V _{DD} = 5.25V	- 17	-	-	20	mA
				- 20				
			V _{DD} = 5.5V	- 25				
				- 35				
I _{DDs2}		CE = V _{DD} - 0.2V Other Input = V _{DD} - 0.2V or 0.2V			-	-	1	

CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = GND$	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = GND$	8	pF

Note : This parameter is periodically sampled and is not 100% tested.

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AC CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$ (1), -17 : $V_{DD} = 5V \pm 5\%$, -20/25/35 : $V_{DD} = 5V \pm 10\%$)

READ CYCLE

SYMBOL	PARAMETER	TC55464P/J-17		TC55464P/J-20		TC55464P/J-25		TC55464P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	17	-	20	-	25	-	35	-	ns
t_{ACC}	Address Access Time	-	17	-	20	-	25	-	35	ns
t_{CO}	$\overline{CE}$ Access Time	-	17	-	20	-	25	-	35	ns
t_{OH}	Output Data Hold Time from Address Change	5	-	5	-	5	-	5	-	ns
t_{COE}	Output Enable Time from $\overline{CE}$	5	-	5	-	5	-	5	-	ns
t_{COD}	Output Disable Time from $\overline{CE}$	-	10	-	10	-	10	-	15	ns
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	0	-	0	-	ns
t_{PD}	Chip Deselection to Power Down Time	-	17	-	20	-	25	-	35	ns

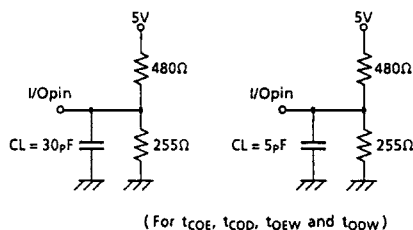
WRITE CYCLE

SYMBOL	PARAMETER	TC55464P/J-17		TC55464P/J-20		TC55464P/J-25		TC55464P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	17	-	20	-	25	-	35	-	ns
t_{CW}	Chip Enable to End of Write	13	-	13	-	15	-	20	-	ns
t_{AS}	Address Set Up Time	0	-	0	-	0	-	0	-	ns
t_{WP}	Write Pulse Width	13	-	13	-	15	-	20	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	0	-	0	-	ns
t_{DS}	Data Set Up Time	10	-	10	-	12	-	15	-	ns
t_{DH}	Data Hold Time	0	-	0	-	0	-	0	-	ns
t_{OEw}	Output Enable Time from $\overline{WE}$	0	-	0	-	0	-	0	-	ns
t_{ODw}	Output Disable Time from $\overline{WE}$	-	8	-	8	-	10	-	15	ns

AC TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	Fig. 1

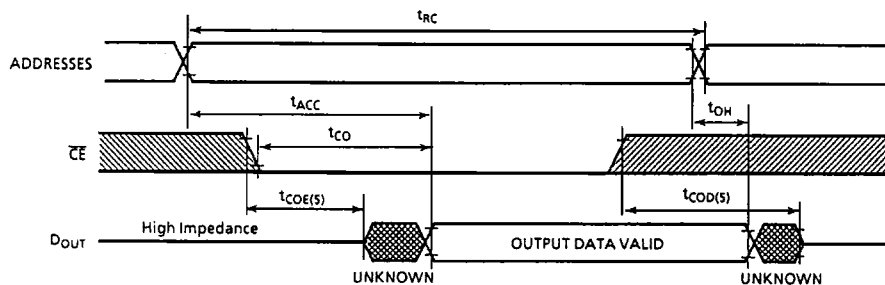
Fig. 1



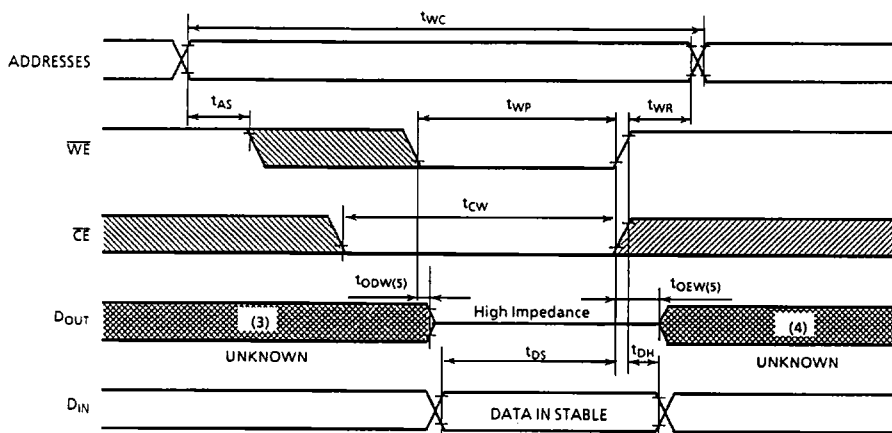
TC55464P/J—17, TC55464P/J—20 TC55464P/J—25, TC55464P/J—35

TIMING WAVEFORMS

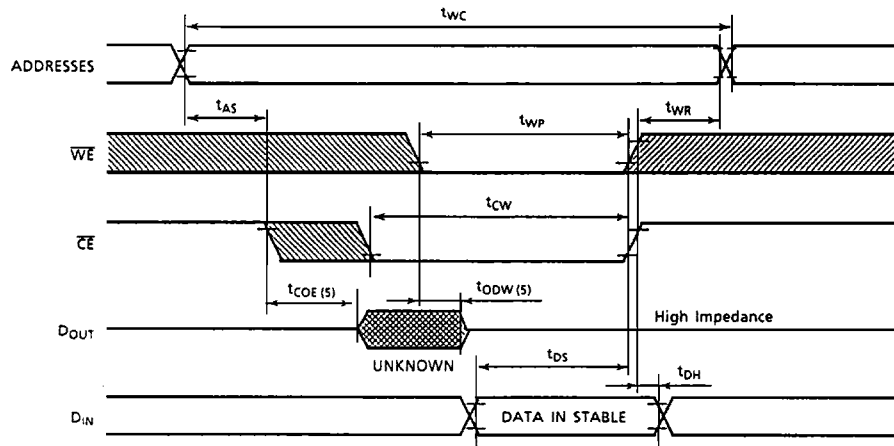
READ CYCLE (2)



WRITE CYCLE 1 ($\overline{WE}$ Controlled Write)



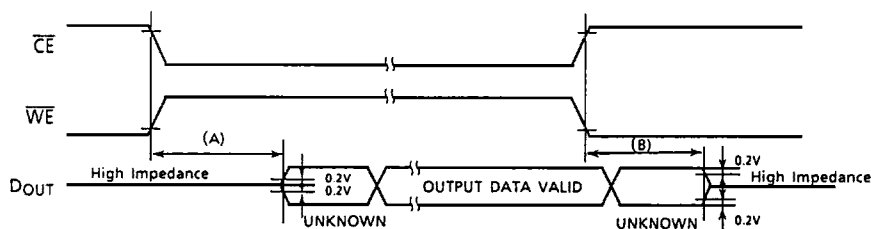
WRITE CYCLE 2 ($\overline{CE}$ Controlled Write)



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Note: 1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. $\overline{WE}$ is High for Read Cycle.
3. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.
5. These parameters are specified as follows and measured by using the load shown in Fig. 1.
 - (A) $t_{COE}, t_{OE\overline{W}}$ Output Enable Time
 - (B) $t_{COD}, t_{OD\overline{W}}$ Output Disable Time

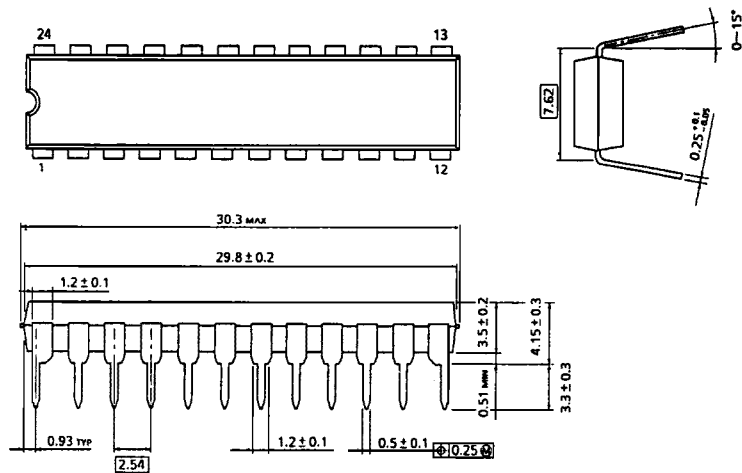


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OUTLINE DRAWINGS

Plastic DIP (DIP24 – P – 300B)

Unit : mm



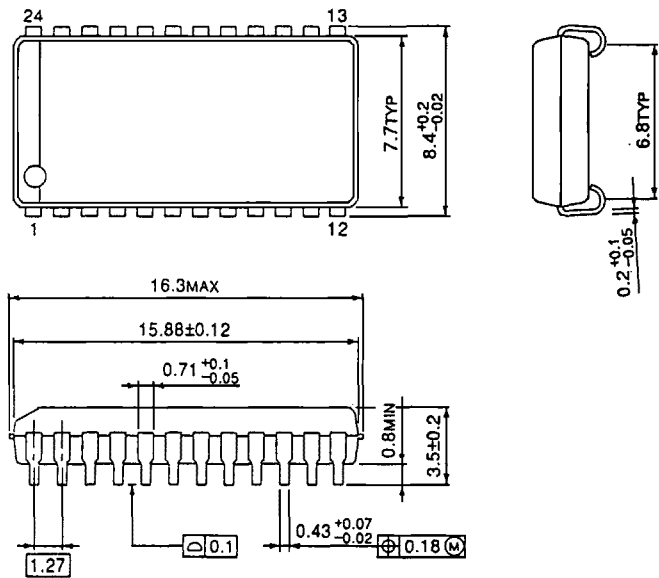
Weight : 1.72g (Typ.)

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OUTLINE DRAWINGS

Plastic SOJ (SOJ24—P—300A)

Unit : mm



Weight : 0.72g (Typ.)