Data Sheet
June 1995

AT&T Microelectronics

T7250C Enhanced User-Network Interface for ISDN and Proprietary Endpoints

Standard Features

- Powerdown mode of operation (less than 15 mW)
- Automatic activation/deactivation
- 1.536 MHz/2.048 MHz clock for codec
- Programmable system clock output
- Grouped (2B+D) serial data transfer option
- D-channel address recognition
- Parallel readout of selected B-channel via microprocessor bus interface
- Two register banks:
  — 16 foreground registers (same as T7250A/B)
  — 9 background registers (same as T7250B)
- Runs all existing T7250A software via foreground registers
- Background registers provide enhanced functionality
- Supports ITU-T I.430/ANSI T1.605/ETSI 300 012 Standard for ISDN 2B+D Basic Access at the S/T reference point
- 16-byte FIFO buffers for HDLC processing of D channel
- Interchangeable B channels
- Optional B- and D-channel inversion
- Powerup reset
- Programmable sanity (watchdog) timer:
  — Multiple modes of operation
- Local and remote loopback test modes
- Crystal or clock input acceptable
- All digital outputs can be tristated for board-level testing
- Parallel microprocessor interface with separate address and data leads, programmable interrupt polarity, and maskable interrupts
- Programmable clock and synchronization signals for direct connection to codecs, HDLC framers, and rate adapters
- TTL/CMOS-compatible I/O

Enhanced Features

- Improved S/T interface framing algorithm that meets CTS2 requirements
- Analog interface connects to the AT&T 2768A dual, low-capacitance transformer (2.5 to 1 turns ratio), providing an increased margin to ITU-T I.430 impedance templates
- Analog interface also compatible with AT&T 2776A single, low-capacitance transformer for applications requiring reinforced insulation
- Improved HDLC formatter
- Improved timing specifications allow interfacing to higher-performance microprocessors

Description

The T7250C is an enhanced version of the field-proven T7250A/B integrated services digital network (ISDN) basic rate line transceivers for 4-wire S/T interface to terminal endpoints. It provides the line interface in terminal equipment used for basic access service to an ISDN. Features include a powered down mode of operation (<15 mW), D-channel address recognition, parallel readout of B channels, automatic activation/deactivation, and flexible clocking options. An optional serial data transfer mode provides contiguous access to 18-bit (2B+D) information groups. The T7250C is software compatible with the T7250A/B (register set). The device conforms to all ITU-T I.430/ANSI T1.605/ETSI 300 012 specifications for point-to-point and point-to-multipoint (passive bus) configurations.

Table of Contents

Contents

Page

Description (continued)

The T7250C fully supports priority, contention resolution, multiframing, and activation/deactivation processes. Additionally, an HDLC formatter and a sophisticated queue manager have been integrated into the T7250C to simplify the D-channel interface.

The T7250C connects to the 4-wire I.430 subscriber loop via the AT&T 2768A dual transformer (2.5 to 1 turns ratio), or two AT&T 2776A single transformers when reinforced insulation is required.

The T7250C is manufactured by using CMOS technology and is available in a 44-pin PLCC or a 48-pin TQFP. The device uses a 5 V supply and has a nominal power consumption of 45 mW. In the deeply powered down state, the power consumption may be reduced to less than 15 mW. A $\overline{\text{PWRDN}}$ output signal is available for system use. Figure 1 shows a high-level block diagram.

Applications

- Video conferencing
- LAN/WAN interconnection
- ISDN terminals
- Featurephones
- PCs
- Workstations
- Digital modems

There are several application notes available for the T7250C listed in the reference section of the document [1], [2], [3].

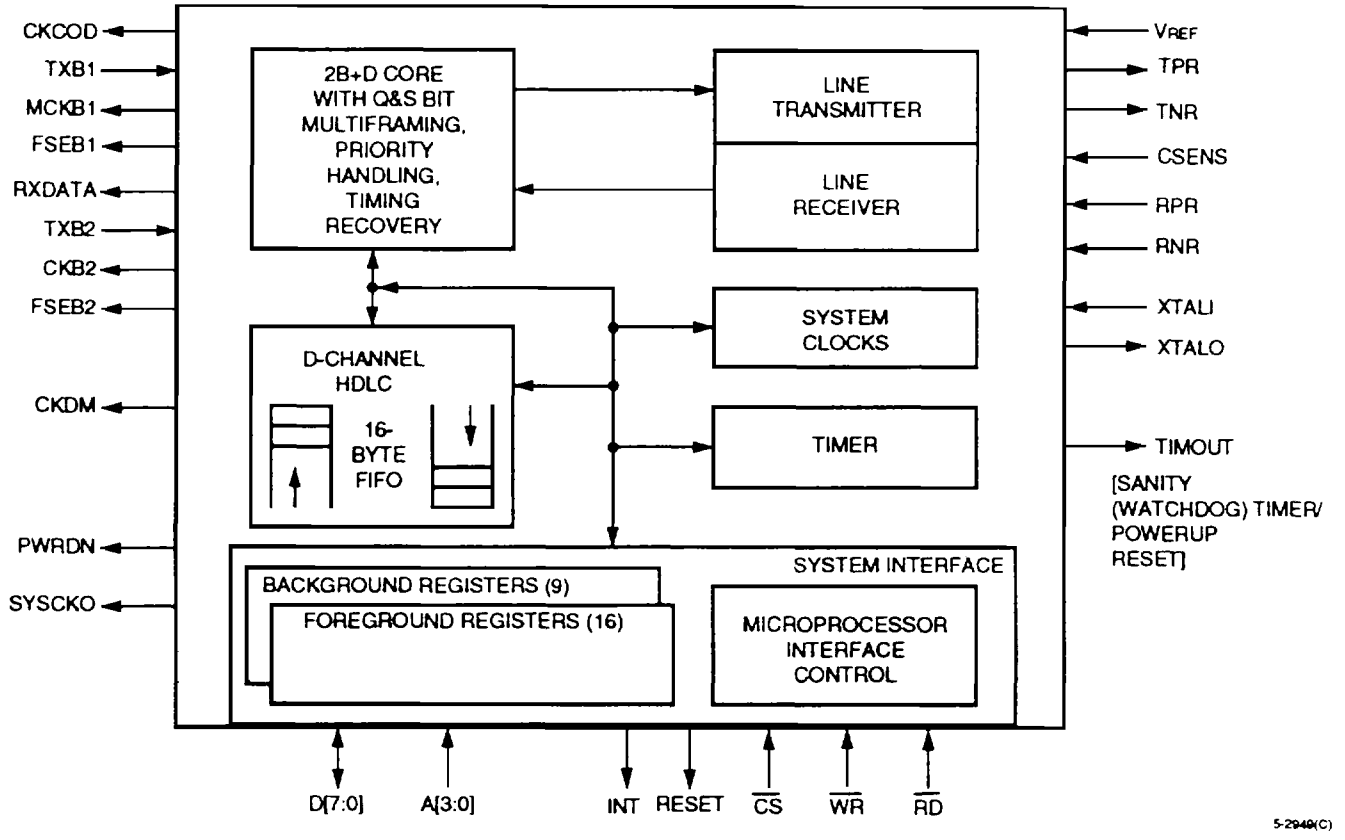


Figure 1. Block Diagram

Pin Information

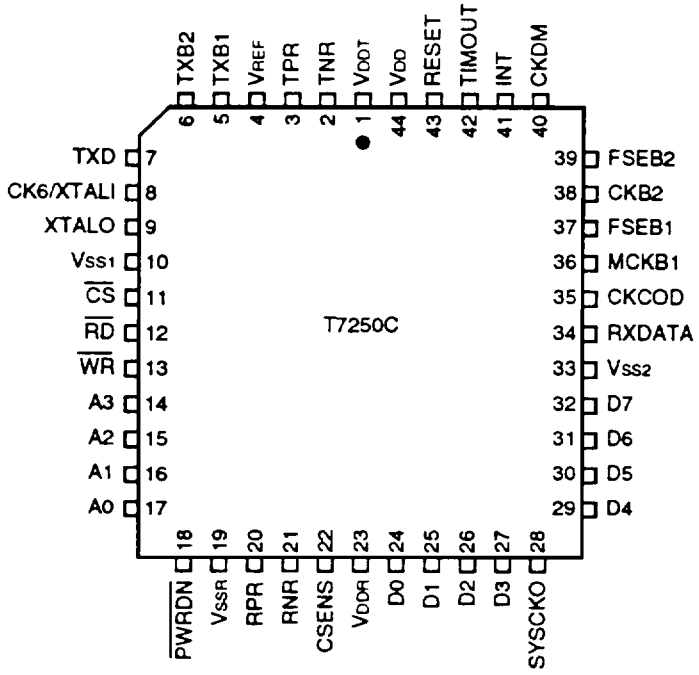


Figure 2. Pin Assignments, 44-Pin PLCC

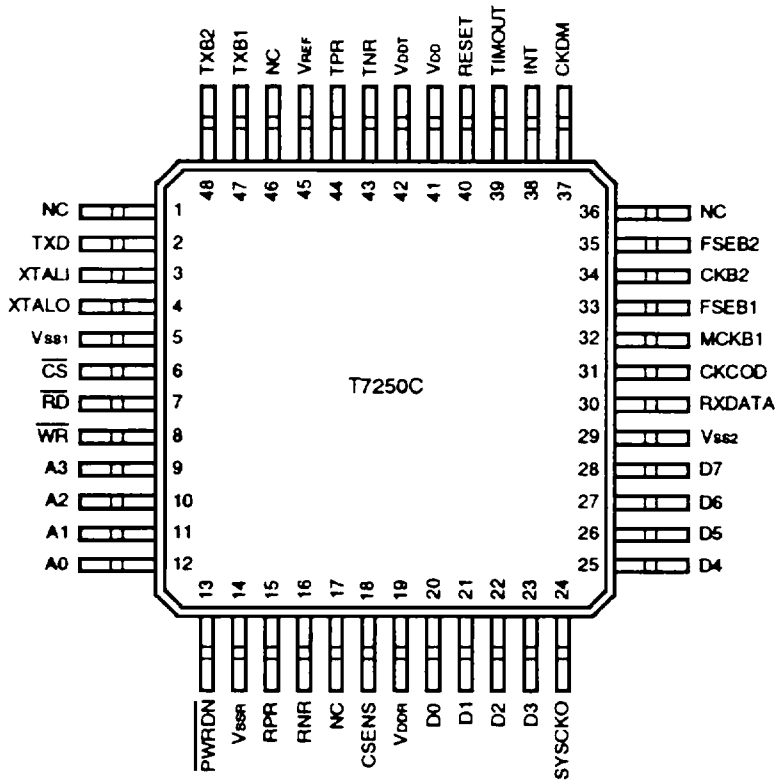


Figure 3. Pin Assignments, 48-Pin TQFP

Pin Information (continued)

Table 1. Pin Descriptions

PLCC Pin	TQFP Pin	Symbol	Type	Name/Function
1	42	V_{DDT}	P	**5 V Supply (Transmitter).** Power supply for the subscriber line transmitter. It is recommended that this be connected to the digital supply. 1.0 µF and 0.1 µF decoupling capacitors should be tied from V_{DDT} to digital ground.
2	43	TNR	O	**Transmit Negative Rail.** Transmitter negative output in alternate bipolar code.
3	44	TPR	O	**Transmit Positive Rail.** Transmitter positive output in alternate bipolar code.
4	45	V_{REF}	I	**Voltage Sense.** Connect to V_{DDT} through a 29.4 kΩ (±1.0%) resistor. Connect to ground if all digital outputs are to be tristated for board-level testing.
5	47	TXB1	I	**Transmit B1.** B1 data that is to be transmitted to the network. Input data is sampled on the falling edge of the noninverted 192 kHz clock relative to FSEB1. **Note:** For an optional grouped (2B+D) serial data transfer mode in 18-bit groups, see Appendix A.
6	48	TXB2	I	**Transmit B2.** B2 data that is to be transmitted to the network. Input data is sampled on the falling edge of the 192 kHz clock relative to FSEB2. **Note:** The TXB2 pin is not used in the optional grouped (2B+D) data transfer mode. See Appendix A.
7	2	TXD	O	**Internal Transmit D-Channel Serial Data.** This signal is provided for test visibility only. The data that appears on this pin is the data that passes from the internal HDLC transmitter to the internal S/T transmitter. TXD is tristated when V_{REF} is low.
8	3	CK6/ XTALI	I	**6 MHz Clock/Crystal In.** This is the 6.144 MHz reference clock input used for the phase-locked loop and other internal device logic. If an external clock oscillator is used, it is connected to this pin and must be 6.144 MHz ± 100 ppm to meet I.430 free-running frequency requirements. The input level of this pin (TTL or CMOS) is programmed via the EDR (external drive) bit in register BR7. The default input levels are CMOS. If a crystal is used, it is connected between this pin and XTALO (pin 9). In this case, a 39 pF (±5%) capacitor must be connected from this pin to V_{SS1}. Crystal requirements are given in Table 15.
9	4	XTALO	O	**Crystal Out.** If a crystal is used, it is connected between this pin and CK6/XTALI, and a 39 pF (±5%) capacitor is connected from this pin to V_{SS1}. Crystal requirements are given in Table 15. If an external clock oscillator is used, this pin is left unconnected.
10	5	V_{SS1}	G	**Digital Ground 1.** Logic and input buffer ground.
11	6	$\overline{CS}$	I	**Chip Select.** $\overline{CS}$ is driven low by the microprocessor to select the T7250C device for reading or writing. When $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ are low, the S/T receiver is looped back to the transmitter.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

PLCC Pin	TQFP Pin	Symbol	Type	Name/Function
12	7	$\overline{RD}$	I	**Read.** A low on this pin when $\overline{CS}$ is low enables the T7250C device to drive the data bus. This signal is used to read data from the registers. The device drives the data bus with data from the register that is addressed by A[3:0]. When $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ are low, the S/T receiver is looped back to the transmitter.
13	8	$\overline{WR}$	I	**Write.** A low on this pin when $\overline{CS}$ is low enables the T7250C device to accept data from the microprocessor. Data on D[7:0] is latched into the register addressed by A[3:0] on the rising edge of $\overline{WR}$. When $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ are low, the S/T receiver is looped back to the transmitter.
14—17	9—12	A[3:0]	I	**Address Bus.** These four address pins are used to select the internal registers. See Table 5 and Table 8 for register definitions.
18	13	$\overline{PWRDN}$	O	**Powerdown.** This signal (low/true) indicates when the chip has entered the powered down mode of operation. It may be used to gracefully shut down different circuits in the system. $\overline{PWRDN}$ is asserted when (a) the powerdown (PD) status is indicated via the line interface as part of an automatic deactivation sequence, or (b) when the Pwrdn bit in register R0 is set to 1 under program control. $\overline{PWRDN}$ is tristated when V_{REF} is low.
19	14	V_{SSR}	G	**Analog Ground (Receiver).** Analog ground for the subscriber line receiver.
20	15	RPR	I	**Receive Positive Rail.** Receiver positive input in alternate bipolar code.
21	16	RNR	I	**Receive Negative Rail.** Receiver negative input in alternate bipolar code.
22	18	CSENS	I	**Current Sense.** Connect this pin to V_{SSR} via a 11.5 kΩ ± 1.0% resistor.
23	19	V_{DDR}	P	**5 V Analog Supply (Receiver).** Analog power supply for the subscriber line receiver. 1.0 µF and 0.1 µF decoupling capacitor should be tied from V_{DDR} to V_{SSR}.
24—27 29—32	20—23 25—28	D[0:3] D[4:7]	I/O I/O	**Data Bus.** These eight bidirectional data lines are used to read or write on-chip registers by using the $\overline{RD}$ or $\overline{WR}$ strobes. On a read cycle, data is read from the device on these lines. On a write cycle, data is transmitted to the device on these lines. When V_{REF} is low, or when $\overline{CS}$ or $\overline{RD}$ is not active, the D[7:0] pins are tristated. The D[7:0] pins are also tristated when $\overline{RD}$ and $\overline{WR}$ are both active.
28	24	SYSCKO	O	**System Clock Output.** This signal is programmable via R4, bit 5 (Syscko) to be either a 6.144 MHz clock (Syscko = 0, default) or a 192 kHz clock (Syscko = 1). Both clocks are free-running. Additional options (1.536 MHz and dc levels) are available to keep the power consumption to a minimum during normal operation and during the powered down mode of operation. For programming details, see Table 8, register BR8. For programmable options in the powered down mode, see register BR7. SYSCKO is tristated when V_{REF} is low.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

PLCC Pin	TQFP Pin	Symbol	Type	Name/Function
33	29	V_{SS2}	G	**Digital Ground 2.** Output buffer ground.
34	30	RXDATA	O	**Receive Data.** Data received from the network side at 192 kbits/s. B1 (64 kbits/s) and B2 (64 kbits/s) channel data are separated by using the individual frame strobe/enable B signals (FSEB1 or FSEB2) and/or the clocks (MCKB1 or CKB2). MCKB1, CKB2, FSEB1, and FSEB2 are all synchronized to the codec clock CKCOD. The D bits also appear on this lead. RXDATA is tristated when V_{REF} is low. **Note:** An optional grouped (2B+D) serial data access mode is available on RXDATA. See Appendix A for programming details.
35	31	CKCOD	O	**Clock for Codec.** The clock frequency on this pin is either 2.048 MHz or 1.536 MHz. The default value is 2.048 MHz. The 1.536 MHz output is available when the CKCOD bit in the background register BR8 is programmed to a 1. All B-channel clocks and strobes are synchronized to this clock. CKCOD is tristated when V_{REF} is low.
36	32	MCKB1	O	**Master Clock or B1 Clock.** The signal on this pin can be programmed to be either CK192 (192 kHz clock) or CKB1 (192 kHz clock enabled only for the B1 channel), depending on the value of the software bit Clkmux (R4, bit 2). When Clkmux is 1 (default), MCKB1 is CK192. MCKB1 is synchronized to the codec clock CKCOD. The MCKB1 clock can be inverted by setting R0, bit 3 (C1pol = 1). MCKB1 is tristated when V_{REF} is low. **Note:** In the optional grouped (2B+D) data transfer mode, 18 clock pulses occur in a window defined by the 18-bit 2B+D envelope signal on FSEB1. See Appendix A and Figure 21.
37	33	FSEB1	O	**Frame Strobe or Enable B1.** This pin is programmable via the B1f bit in the control register R4. The signal can be either the 8 kHz frame strobe signal for a codec device used on the B1 channel or an enable B1 gating signal, which indicates the active period for B1-channel data when it is high during the 8 bits of B1. Timing of the enable signal is programmable via the control signal R4, bit 7 (codec1). Available options are shown in Figure 20. FSEB1 is activated only when INFO 2 or INFO 4 is being received, or when local loopback is activated. Otherwise, FSEB1 is inactive but not tristated. FSEB1 is tristated when V_{REF} is low. **Notes:** The FSEB1 signal may also be used as a DMA request signal to transfer B1-channel data available in background register BR9 and controlled by BR8. See Table 8 for more details. In an optional grouped (2B+D) serial data transfer mode, FSEB1 may be programmed to be an 18-bit envelope signal defining the transfer window. FSEB1 may also be programmed to be a strobe signal identifying the (2B+D) information groups. See Appendix A and Figure 21.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

PLCC Pin	TQFP Pin	Symbol	Type	Name/Function
38	34	CKB2	O	**Clock for B2 Channel.** This is a 192 kHz output clock signal that is enabled only in the B2 time slot of RXDATA. CKB2 is synchronized to CKCOD (either 2.048 MHz or 1.536 MHz depending on the value of the CKCOD bit in register BR8). The CKB2 clock can be inverted by setting R0, bit 3 (C2pol = 1). CKB2 is tristated when VREF is low. **Note:** In the optional grouped (2B+D) serial data transfer mode, CKB2 is enabled only in the B2 time slot of the 18-bit (2B+D) group. See Figure 21.
39	35	FSEB2	O	**Frame Strobe or Enable B2.** The output on this pin is programmable via the B2f bit in the control register (R4, bit 3). The signal can be either the 8 kHz frame strobe signal for a codec device used on the B2 channel, or an enable B2 gating signal, which indicates the active period for B2-channel data when it is high during the 8 bits of B2. Timing of the enable signal is programmable via the control signal R4, bit 6 (codec2). Available options are shown in Figure 20. FSEB2 is activated only when INFO 2 or INFO 4 is being received, or when local loopback is activated. Otherwise, FSEB2 is inactive but not tristated. FSEB2 is tristated when VREF is low. **Notes:** The FSEB2 signal may also be used as a DMA request signal to transfer B2-channel data available in BR9 and controlled by BR8. See Table 8 for details. In the optional (2B+D) grouped serial data transfer mode, FSEB2 may be programmed to be a gating envelope signal defining the B2-channel time slot of the (2B+D) information groups (see Figure 21). FSEB2 cannot be programmed for a strobe signal in the grouped (2B+D) mode.
40	37	CKDM	O	**D-Channel Clock.** This is programmable to be either an 8 kHz or a 16 kHz clock. When R0, bit 1 (Ckdm) is 0 (default), this is a free-running (synchronous with 6.144 MHz reference clock input), 16 kHz signal that is used internally for clocking the D channel. This clock is a 2.6 µs low-going pulse that occurs at a 16 kHz rate. The pulse corresponds to the location of the D bits. When Ckdm is a 1, CKDM is a free-running, 8 kHz clock. This clock operates with a duty cycle of nearly 50%, with D bit alignment. CKDM is tristated when VREF is low.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

PLCC Pin	TQFP Pin	Symbol	Type	Name/Function
41	38	INT	O	**Interrupt.** Ten conditions can cause an interrupt signal of programmable polarity to be generated. Register pairs R9 and R10 and BR7 and BR8 provide interrupt control and status. R9 and BR7 allow the microprocessor to selectively mask any of the interrupts. R10 and BR8 identify ten interrupt conditions: 1. D-channel access has been lost via mismatch. 2. The received I.430 information state has changed. 3. Q-channel multiframe has been completed. 4. S word available. 5. D-channel transmission has been completed. 6. D-channel transmit queue is at or below a specified level. 7. D-channel receive queue is at or above a specified level. 8. D-channel end-of-frame has been received. 9. Powerdown mode is being entered. 10. B-channel data is available for parallel readout. R4, bit 1 controls the interrupt polarity. Default is active-high. See Table 5, register R9 and Table 8, register BR7 for interrupt mask details. INT is tristated when V_{REF} is low.
42	39	TIMOUT	O	**Timer Time-Out.** This signal occurs when a programmable timer times out and on powerup. The powerup pulse goes high with powerup and stays on until the system power supply reaches a nominal value of 3.8 V. The pulse continues to stay high for 1.5 ms—7.5 ms (typical, 3.5 ms). On a timer time-out, the pulse is of programmed polarity for a minimum of 57 µs. R4, bit 0 controls the polarity of this signal. Default is active-high. Refer to register R13 for details of the various modes of timer operation. TIMOUT is tristated when V_{REF} is low.
43	40	RESET	I	**Reset.** A high on this pin resets the device, provided TIMOUT is not active. The RESET pulse must be active for at least 175 ns. If TIMOUT is active when RESET goes high, device reset occurs after the TIMOUT pulse.
44	41	V_{DD}	P	**5 V Supply (Digital).** 1.0 µF and 0.1 µF decoupling capacitors should be tied from V_{DD} to digital ground.
—	1, 17, 36, 46	NC	—	**No Connect.**

Architecture

The T7250C provides the user-to-network interface for terminal endpoints connected to an ISDN. It operates from a 6.144 MHz clock, which can be either a crystal input or a clock input. There are six major blocks: the system interface controller, the system clocks, the 2B+D core, the HDLC formatter, the S/T line transceiver, and the timer. Figure 1 shows a high-level block diagram of the T7250C device.

System Interface Controller

The system interface controller conveys status information and provides control for the T7250C via a microprocessor bus interface. The controller maintains two register banks: the foreground bank (R[15:0]) and the background bank (BR[9:1]). The foreground bank has sixteen registers. These are identical to those of the T7250A and are described in Table 5. The background bank has nine additional registers, which are described in Table 8 of this document. The following sections describe the standard features of the chip that are controlled by the foreground register bank, and the enhanced features that are controlled by the background register bank.

The microprocessor interface allows parallel asynchronous access to all control, data, and status registers. Separate address and data lines are available so that most general-purpose microprocessors can be interfaced easily.

All control and status registers are readable. There are two types of reads: latched or dynamic. The default is a latched read, but R0, bit 4 allows the microprocessor to specify when reads should be dynamic. In the latched mode, the read value is frozen within the read cycle. In the dynamic mode, changes in status are reflected on the data bus while $\overline{RD}$ is activated. Wait-states should not be required. Latched reads are recommended for normal operation. Internally, 425 ns (worst case) are required for a write cycle, but the external interface requires a write pulse of only 50 ns. Reads of 175 ns are possible (see timing diagram in Figure 16).

The T7250C has an interrupt output, INT, to alert the microprocessor if it needs to be serviced. The polarity of INT is programmable, and all interrupts are maskable. Interrupt status bits in registers R10 and BR8 reveal the source of the interrupt even if the interrupt is masked (in R9 and BR7). Reading the status register resets the interrupts automatically. Once an interrupt is cleared, it is not regenerated until the condition that caused it goes away, and then the condition reoccurs. If a new interrupt occurs while reading the interrupt status registers R10 or BR8, the INT signal will go inactive for a minimum of 80 ns after a read, and then reassert itself. This ensures accurate interrupt reporting in edge-triggered host systems.

System Clocks

The system clocks block provides three system-level clocks—SYSCKO, CKCOD, and CKDM. To maintain compatibility with the T7250A, SYSCKO is programmable via R4, bit 5 (Syscko) to be either a 6.144 MHz clock (Syscko = 0) or a 192 kHz clock (Syscko = 1). In the T7250C, additional outputs (1.536 MHz and dc level) are available on SYSCKO. The desired frequencies may be programmed for the fully powered and the powered down modes. Bit pairs (SC[1:0]) and (PDSC[1:0]) in BR8 and BR7 control the system clock output frequency. Programming details are given in Tables 7 and 8. The lower the frequency output on SYSCKO, the lower the power consumption and electromagnetic interference (EMI).

CKCOD is a 2.048 MHz or a 1.536 MHz clock that is an ideal master clock for codecs. The 1.536 MHz option is selected via BR8, bit 7. All B-channel clocks and frame timing signals are internally synchronized to CKCOD to reduce noise to peripheral devices. CKDM is programmable via R0, bit 1 (Ckdm) to be either the 16 kHz D-channel clock (Ckdm = 0) or an 8 kHz clock (Ckdm = 1).

2B+D Core

The 2B+D core is responsible for timing recovery, framing, transmit formatting, contention resolution, priority handling, and S- and Q-channel multiframing. Figure 7 shows the bit positions in a 48-bit frame structure. Figure 8 shows the multiframe structure of 20 frames. The 2B+D core also supports activation/deactivation procedures, parallel readout of B channels, and loopback.

Timing Recovery

A digital phase-locked loop extracts timing from a transformer-coupled signal received from the network termination (NT). It derives a 192 kHz clock that is used for sampling all data, both transmit and receive.

Architecture (continued)

Framing

The 2B+D core also derives framing from received data. It creates separate clocks for B1 data, B2 data, Q data, S data, and D data. The B- and D-channel clocks are accessible for system use. The exact operation is programmable for maximum flexibility and ease of interface to peripheral devices. A B2-channel clock is always provided (CKB2). The user can specify via R0, bit 2 (C2pol = 1) that the clock be inverted. This allows for interfacing with peripheral devices that transmit data on the falling edge of the clock and sample data on the rising edge of the clock (most HDLC framers). The powerup initialization default value of this bit is C2pol = 0.

Another clock can be programmed to be either a B1 clock or a continuous 192 kHz clock (MCKB1). As with the B2 clock, the user can specify that MCKB1 be inverted (R0, bit 3).

Programmable frame timing signals (FSEB2 and FSEB1) provide the 8 kHz synchronization signal required by codecs. FSEB2 and FSEB1 are programmable via R4, bits 3 and 4 (B2f and B1f) to be either a frame strobe (Bxf = 1) or an enable signal (Bxf = 0). The timing of the enable signal is programmable via R4, bits 6 and 7. These 8 kHz frame timing signals are present only when INFO 2 or INFO 4 is being received. In effect, they automatically disable codecs when framing is lost. The only exception is that the framing signals are enabled when either B-channel local loopback is enabled. Figure 20 shows the timing relationships between the clocks and the frame strobe signals.

Data received from the NT is provided on a single lead, RXDATA. The clocks and frame timing signals allow peripheral devices to extract the appropriate data. D-channel data provided on RXDATA contains the HDLC-formatted bit sequence. Normally, processed D-channel bytes are accessed directly through register R3. Figure 19 shows the bit alignment timing on the RXDATA pin relative to the 48-bit frame received at the line interface.

An optional serial data transfer mode, called the grouped (2B+D) serial data transfer mode is available in the T7250C. In this mode, user (2B+D) data is transferred in groups of 18 bits as shown in Figure 21 and described in Appendix A. This mode is useful in system applications requiring access to 2B+D information in contiguous time slots. The grouped mode is programmed via the G2BD bit (bit 3) in register BR8.

Transmit Formatting

The transmit formatter combines data and control as specified by Recommendation I.430 and forms the 48-bit frame. Q- and D-channel data to be transmitted to the NT are entered through the microprocessor interface. Dedicated leads, TXB1 and TXB2, are provided for inserting B-channel data that is to be transmitted to the NT. The multiplexed stream is sent to the S/T transceiver for transmission. Figure 19 shows the bit transport timing on the dual rail line interface, relative to the TXB1 and TXB2 inputs.

Contention Resolution

The 2B+D core supports contention resolution that is required for passive bus operations. It continuously monitors the received D-echo bit and compares it to the previously transmitted D bit. If they match, the terminal is allowed to continue its transmission. If they do not match, the terminal is not allowed to transmit on the D channel. When the mismatch occurs, R10, bit 0 is set. The microprocessor can specify that it should be interrupted when this condition occurs. The S/T interface controller returns to the D-channel monitoring state after reporting a mismatched echo bit.

Priority Handling

The 2B+D core supports the ITU-T I.430 priority mechanism. There are two classes of priority, high (signaling) and low (data). Signaling information is given priority over other types of information (data) by selecting the high-priority class. R8, bit 2 (pry) controls this function. The priority within a class also varies. Within the signaling and data class, there are two priorities: high and low. In the signaling class, a high priority on the D channel is indicated by eight successive 1s on the E (D-bit echo) channel, and a low priority on the D channel is indicated by nine successive 1s on the E channel. In the data class, a high priority on the D channel is indicated by ten successive 1s on the E channel. The number of 1s is eleven for the lower level of priority in the data class. The priority level is automatically toggled within a priority class following a successful transmission. This gives all competing terminals fair access in a passive bus arrangement. R8, bit 4 (lpry) contains status information that indicates the current priority within a class.

Architecture (continued)

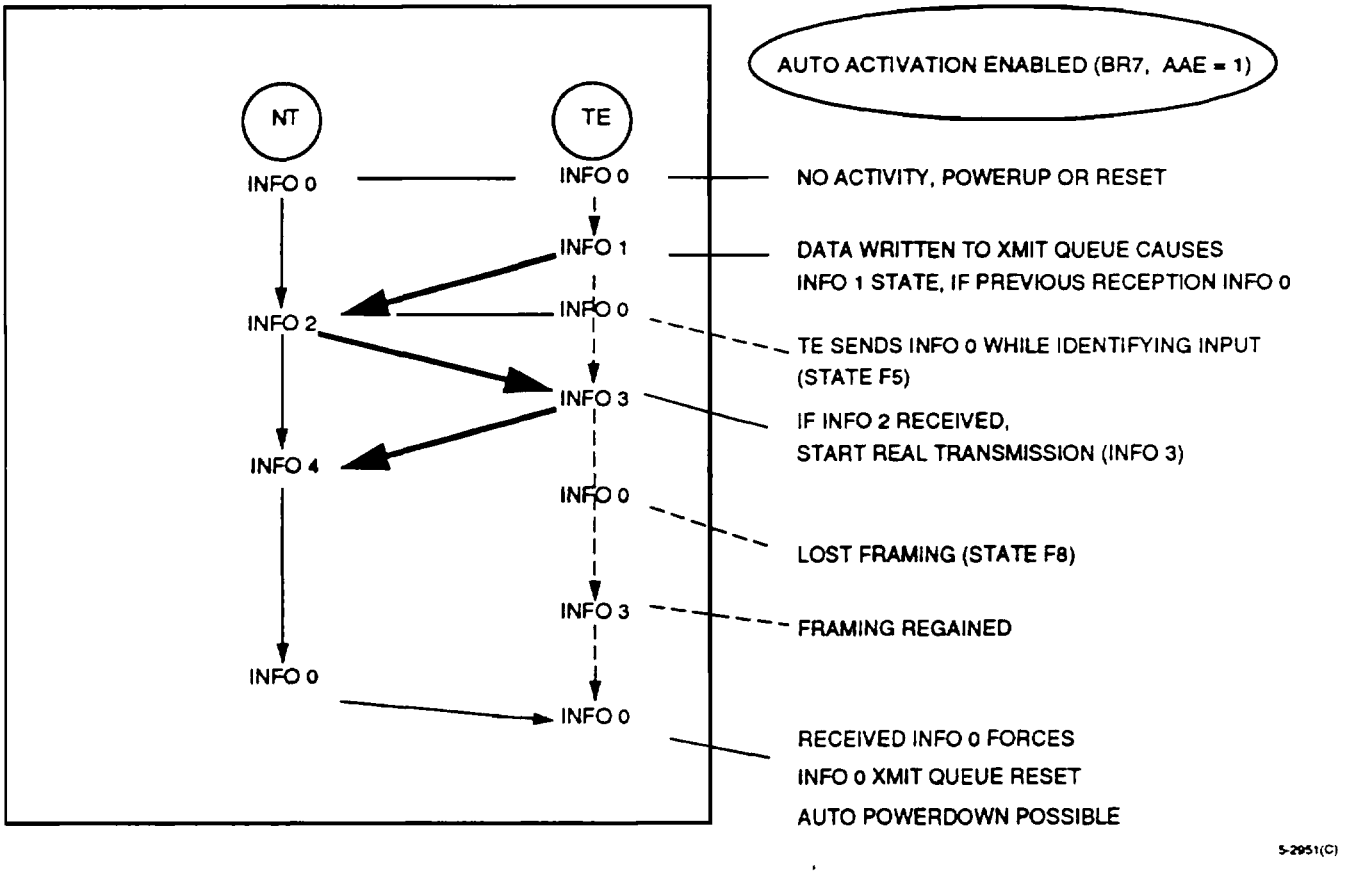
Activation/Deactivation Procedures

ITU-T I.430 link activation and deactivation procedures are also supported. The T7250C device continuously monitors and reports the receive information state through R1, bits 0—3. The microprocessor can specify that it be interrupted when the receive information state changes (richgie bit in R10). The T7250C also allows the microprocessor to control the transmitted information state through R2, bits 0 and 1. When AAE = 0 in BR7, the microprocessor can manually control the link activation and deactivation procedures.

The T7250B device requires incoming framing from the NT to meet the I.430 bipolar violation requirements (14-bit criteria) for frame alignment to occur. Once frame alignment is gained, however, only the F-bit bipolar violation is required to maintain alignment. The T7250B does not lose framing if the second bipolar violation violates the 14-bit criteria. The framing algorithm used in the T7250C requires that both the F-bit and the second bipolar violations occur in the proper locations and that there are no more than two per frame. After frame alignment is established, three bad frames are required to report lost framing in R1, bits 2 and 3.

Auto Activation

Auto activation allows powering up the device from its powered down mode to establish synchronization between the TE and NT. Auto activation is enabled by setting AAE = 1 in BR7. Specific types of signals (INFO patterns) are sent and monitored across the line interface during the auto activation sequence. Refer to Section 6.2 of the I.430 specification for general information. Figure 4 shows the automatic activation process as implemented in the T7250C.



Notes:
As in the T7250A, activation/deactivation can also be done under microprocessor control; received INFO change (richg) alerts microprocessor, and then transmit stream is controlled via R2 (tss[1:0]).

Refer to I.430 document for the TE states.

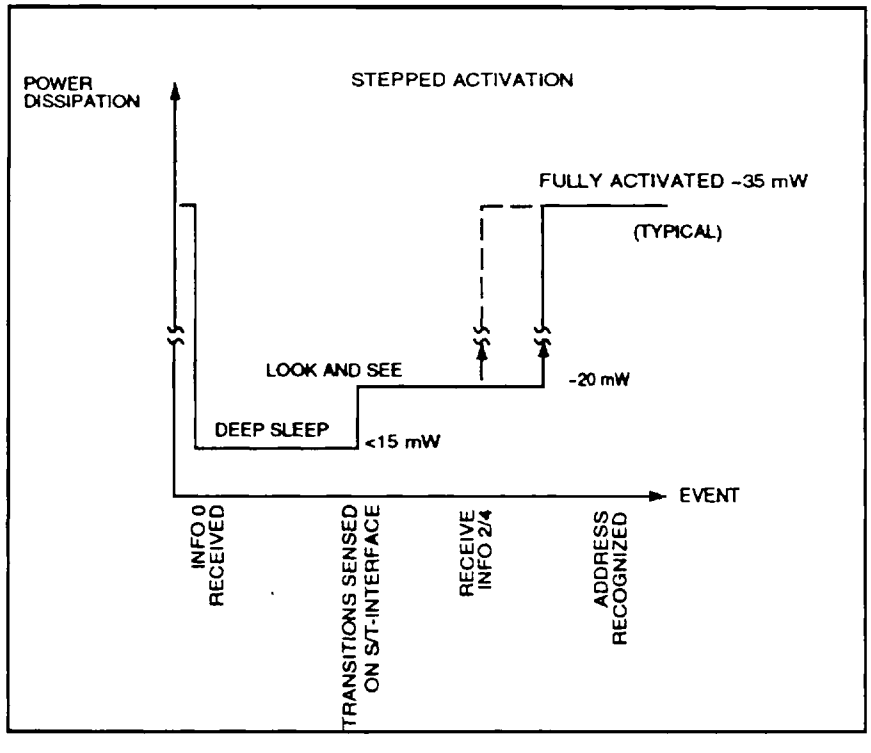
Figure 4. Flow Graph of the Automatic Activation Process in the T7250C

Architecture (continued)

Either the TE or the NT can initiate communication across the line interface. When reset or when power is applied, the T7250C transmits INFO 0 (no signal). If INFO 0 is received, the T7250C continues transmitting INFO 0. If INFO 2 or INFO 4 is received, the T7250C acquires framing and then transmits INFO 3. Auto activation is initiated by the TE when the T7250C initially sends and receives INFO 0, and then sends an INFO 1 signal. INFO 1 is a repeating pattern of positive zero, negative 0 and six 1s. INFO 1 is initiated when data is written to the D-channel transmit queue, provided INFO 0 is received.

When the NT connected to the T7250C (TE) senses the INFO 1 sequence received from the TE, or when the NT wants to activate the TE, it sends an INFO 2 pattern. INFO 2 is a frame received by the TE with all bits of the B, D, and E (echo D) channels set to binary 0. The N and L bits of the 48-bit INFO 2 frame follow the standard I.430 encoding conventions with the activation bit A set to 0. In the T7250C, INFO 2 is identified by verifying proper framing and checking for A = 0. Monitoring the INFO 2 pattern allows the clock recovery logic in the T7250C to adjust and synchronize its transmission to that of the NT. A maximum of 24 INFO 2 frames is required for loop synchronization. INFO 2 is reported after the third synchronized frame. Thus, a maximum of 27 INFO 2 frames may be required for its detection. The T7250C then enters the INFO 3 state so that normal transmission can begin with operational data on the B and D channels. Normal transmission begins when priority requirements for D-channel access are satisfied. When an INFO 4 pattern is received from the NT, the activation sequence is complete. INFO 4 is reported after two frames. The TE and NT can now exchange data back and forth across the line interface. If INFO 0 is received when the TE is sending INFO 3, INFO 0 is transmitted and the transmit queue is cleared. If after synchronization with an NT an unrecognized signal (not INFO 0, 2, or 4) is received by the T7250C, lost framing is reported in R1, bits 2 and 3 (rss[0:1]) after three frames.

When the T7250C is in auto activation mode with the S/T interface inactive and data is written into the D-channel transmit FIFO, INFO 1 is transmitted to the NT. D-channel transmission begins by the T7250C immediately upon reception of INFO 2 from the NT. Since the NT may require a few frames before it recognizes the reception of INFO 3, the first D-channel frame sent by the T7250C can be missed by the network. To prevent this, a dummy D-channel frame can be written to the transmit FIFO to initiate start-up. Actual D-channel messages can commence when INFO 4 is reported in register R1, bits 2 and 3 (current received information pattern).



5-2952(C)

Figure 5. Automatic Powerup Sequence in the T7250C

Architecture (continued)

Auto Powerdown Deactivation

To allow automatic powerdown, using the auto deactivation sequence across the line interface, the APDA bit in register BR7 (bit 6) is set to 1. When the line receiver identifies the arrival of INFO 0 frames (64 successive 1s) instead of INFO 4 or INFO 2 from the NT, the auto deactivation sequence begins. The line transmitter turns off and then starts sending INFO 0 frames (see Section 6.2.7 of I.430). The T7250C then enters the powerdown mode and sets the PD status bit in register BR8 (bit 5). If the powerdown interrupt enable (PDIE) bit is set in BR7 (bit 5), the hardware interrupt signal INT is asserted. The transmit D-channel queue is reset, and automatic powerdown is possible. This PDIE interrupt mechanism of the T7250C is useful for TEs that use the automatic activation/deactivation feature in the background.

Automatic powerdown is controlled by changes on the S interface. Therefore, if BR7, bit 6 = 1 and the loop is then deactivated, the chip will power down. However, if the microprocessor interface is then accessed, the chip will power up, and it will not power down again unless the line activates and deactivates. To avoid this, examine the INFO state. If the loop is activated, operation is as expected; if the loop is deactivated, the last instruction should be set R0, bit 0 = 1 so that the device powers down.

Powerdown and Powerup Options

The T7250C may also be powered down directly under microprocessor control by setting the Pwrdn bit in the foreground register R0. Regardless of how the device enters a powered down state, a hardware signal, $\overline{\text{PWRDN}}$, is activated and made available for system use. The SYSCKO frequency is governed by the value programmed for PDSC[1:0] in register BR7.

In the powered down mode, the lowest power dissipation is achieved by programming the SYSCKO signal to a dc level by setting both the PDSC1 and PDSC0 bits in register BR7. The T7250C comes out of the powered down mode with a read or write access to the device, or with a reset or powerup, or when the NT initiates auto activation.

Figure 5 shows the automatic powerup sequence in the T7250C. The T7250C remains in the deep sleep powerdown state as long as INFO 0 is received. If auto activation has been enabled, the T7250C enters a slightly higher powered look-and-see powerdown state if transitions are sensed on the S/T interface. In this look-and-see state, all outputs, including the SYSCKO and $\overline{\text{PWRDN}}$ outputs remain in the powerdown state.

If address recognition has been disabled, the T7250C is fully activated when INFO 2 or INFO 4 is detected. If address recognition has been enabled, then the T7250C remains in the look-and-see state until an address is matched.

Parallel Readout of B-Channel Data

In the T7250C, the B-channel data presented to the TXB1 or TXB2 pins, or the RXDATA pin are available in register BR9 for parallel access via the microprocessor interface. The choices for B-channel selection are programmed by using 2 bits, PBS and PBTXB in register BR8. The PBS bit is for parallel B-channel selection; if this bit is set, the B2 channel is selected. Otherwise, the B1 channel is selected (default). The PBTXB bit, when set, selects the B-channel data that is transmitted to the network. When PBTXB = 0, received B-channel data is selected.

The selected B-channel byte is held in register BR9 until it is read. Reads should be made within a 115 µs interval to avoid losing any B-channel data. The first received bit is treated as the most significant bit and stored in the bit 7 location of BR9 (refer to B-channel bit order Section 6.4.2.4 of the T1.605 document). To alert the microprocessor of the B available status, the BA bit is set in register BR8 (bit 4). In addition, if the B available interrupt enable (BAIE) control bit is set in BR7 (bit 4), the hardware interrupt signal INT is also asserted. The polarity of the interrupt signal INT is programmable as in the T7250A through the foreground register R4.

For noninterrupt-driven applications, another mechanism is available for parallel readout of B-channel data. The BA bit in register BR8 changes from a 0 to a 1 when new B-channel data is available for reading via BR9. By scanning the BA bit in BR8, one can use the polled mode of operation to access the B-channel data stored in BR9.

Direct Memory Access to Parallel B-Channel Data

Microprocessors that only require a DMA Request Signal (e.g., 80188) for direct memory access could use either the FSEB1 or the FSEB2 signals as a DMA request signal to transfer the selected B-channel byte from register BR9 to system memory. This transfer method may be useful in voice storage applications or in clear channel applications using nonstandard protocols on the B channel.

Architecture (continued)

Loopbacks, 1s Transmission, Data Inversion, and Exchange B1 and B2

The 2B+D core handles remote and local loopback functions, transmit 1s, and data inversion. Remote loopbacks provide a loopback of B1, B2, and/or D channel DSL (digital subscriber loop) data. That is, data received in the specified channel of the DSL from the NT is automatically transmitted in that same channel of the DSL. Remote loopback of the B2 channel is not supported in the grouped (2B+D) serial data transfer mode.

Local loopbacks are provided for local terminal tests. During loopbacks, 1s are automatically transmitted on the specified channel of the DSL. Data that would otherwise be transmitted on the DSL is strobed in the specified time slot of RXDATA. Transmission of 1s on the B1 and B2 channels can be controlled by the t1b1 and t1b2 bits in R12. See Table 2 and Table 5 for details. Data inversion controls (R8, bits 6 and 7, b1i and b2i) allow the data of the specified channel to be inverted. This feature is useful for transmission on restricted channels where inverted HDLC is used. Note that local and remote loopbacks cannot be performed on the same channel simultaneously. Also note that zeros can be transmitted on a specified channel(s) of the DSL by simultaneously activating the transmit 1s and the data invert functions. This is useful for Recommendation I.430 compliance tests.

An additional remote loopback is available when $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ pins are simultaneously held low. This loopback routes the bit stream received from the NT back to the T7250C transmitter. The T7250C framing circuitry is bypassed during this loopback (the NT's framing is transmitted back towards the NT).

The B1 exchange B2 feature (controlled by b1xb2— R8, bit 1) allows the user to specify that B1 and B2 information should be internally exchanged. This permits designers to connect a peripheral device to either channel without limiting its operation to that channel. When b1xb2 is activated, the timing signals, the strobes FSEB1 and FSEB2, and the needed clocks are swapped so that data is presented to the MCKB1 and CKB2 pins in swapped channels. Thus, remote and local loopbacks function properly when b1xb2 is activated. The values transmitted via TPR and TNR at the line interface (DSL) and the values received at RXDATA for several programmable configurations are shown in Table 2. The first example in Table 2 shows that for normal operation, the chip inputs TXB1 and TXB2 are transmitted in the B1 and B2 time slots of the line interface. At the RXDATA output, the B1 time slot receives data from the DSL B1 time slot. Similarly, the B2 data received at RPR and RNR appears in the B2 time slot of RXDATA. The rest of Table 2 shows various conditions and corresponding register settings. Figure 6 shows the data path with respect to loopbacks and transmit 1s controls.

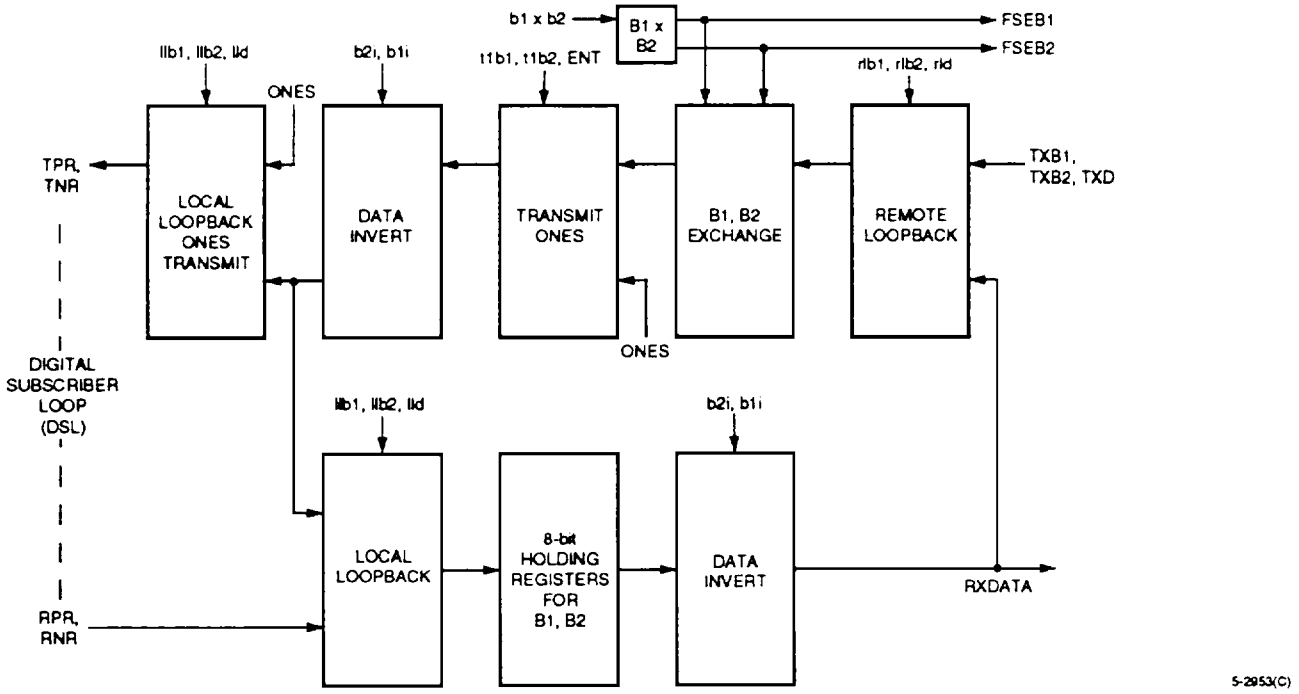


Figure 6. 2B+D Data Paths and Loopback Controls

Architecture (continued)

Table 2. 2B+D Core Programming Examples

Conditions	Transmit		Receive (RXDATA)*	
	DSL Channel Time Slot	Transmitted Value	Time Slot	Received Value
Normal; no loopbacks or exchanges (R8, bits 7, 6, 1 = 0; R12 = 0)	B1 B2	TXB1 TXB2	B1 B2	B1 (DSL) B2 (DSL)
Local loop B1 (R12 = 10 Hex R8, bits 7, 6, 1 = 0)	B1 B2	1s TXB2	B1 B2	TXB1 B2 (DSL)
Remote loop B2 (R12 = 01 Hex)	B1 B2	TXB1 B2 (DSL)	B1 B2	B1 (DSL) B2 (DSL)
B1 exchange B2, B1xB2 (R8, bit 1 = 1)	B1 B2	TXB2 TXB1	B1 B2	B2 (DSL) B1 (DSL)
Local loop B1 and B1xB2 (R12 = 10 Hex, R8, bit 1 = 1)	B1 B2	1s TXB1	B1 B2	B2 (DSL) TXB2
Remote loop B1 and B1xB2 (R12 = 02 Hex, R8, bit 1 = 1)	B1 B2	TXB2 B1 (DSL)	B1 B2	B2 (DSL) B1 (DSL)
Invert B1 channel, b1i (R8, bit 7 = 1)	B1 B2	$\overline{\text{TXB1}}$ TXB2	B1 B2	$\overline{\text{B1}}$ (DSL) B2 (DSL)
Invert B1 and local loop B1 (R8, bit 7 = 1, R12 = 10 Hex)	B1 B2	1s TXB2	B1 B2	TXB1 (double invert) B2 (DSL)

* RXDATA's B1 and B2 time slots are marked by FSEB1 and FSEB2. DSL (digital subscriber loop) refers to the (S/T) 4-wire line interface.

Notes:
Remote loopbacks on B-channels have a one-half frame pipeline delay. Local loopbacks on B-channels have a full frame delay. D-channel loopbacks are immediate (next D).

In the grouped (2B+D) serial data transfer mode, remote loopback on the B1-channel is immediate, B2a octet remote loopback is not supported, and remote loopback on the D-channel is immediate.

Architecture (continued)

S- and Q-Channel Multiframing

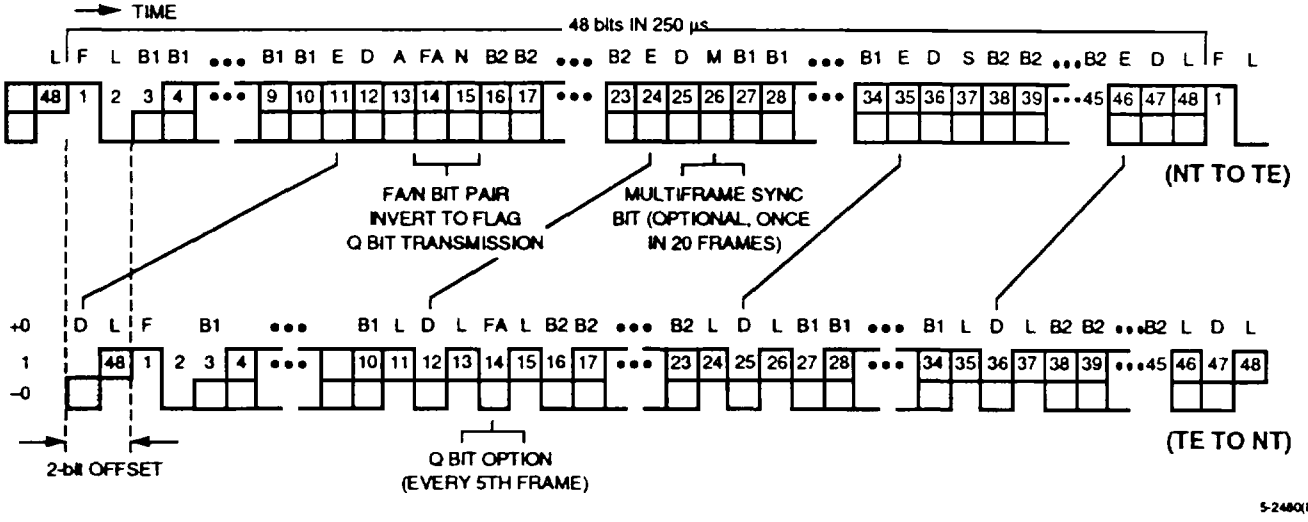
Multiframing, supported by the 2B+D core, provides synchronization for a 4-bit Q channel in the TE-to-NT direction and a 20-bit S channel in the NT-to-TE direction. The S bits are synchronized within a 20-frame multiframe by the M bit (26th bit of the I.430 NT-to-TE frame), which goes true once every 20 frames. Multiframe synchronization requires that either INFO 2 or INFO 4 is being received and that the M bit goes true exactly 20 frames from the previous M bit true. R7, bit 7 (mse) provides status information that indicates whether multiframe synchronization exists. The multiframe also provides Q-channel synchronization. Q bits are identified by appropriately timed inversions of the FA/N pair, as specified in Recommendation I.430. Q-channel synchronization requires that multiframe synchronization is established and that the received FA and N bit inversions (FA = 1, N = 0) occur exactly five frames from the previous FA and N bit inversions. R11, bit 7 (qse) provides status information that indicates whether the FA and N Q-channel synchronization exists. Two status bits (st0 and st1) are available in R7, bits 5 and 6. Bits st0 and st1 indicate how many bits remain to be sent in the current multiframe, provided that Q-channel synchronization is true.

Data nibbles transmitted on the Q channel are written to R11, bits 0—3. When a Q-channel data nibble is written to R11, the enflg (bit 4) must be set. The nibble is later off-loaded internally at the Q-bit time in frame 16 of the multiframe. The enflg bit is then cleared to indicate that a new nibble can be written to R11. A new nibble may also be written after the qdone interrupt flag is set. Use of S-channel interrupts, particularly during frame 16 or frame 1 may also be used for new Q bit writes. Data written to the Q nibble is repeatedly transmitted, if the qloop bit (R11, bit 6) has been set. Repeated transmissions do not regenerate interrupts. The reset default value of each Q bit is a 1. The qdone interrupt does not occur for the all 1s default transmission. If M or Q synchronization is lost, the Q channel automatically transmits 1s, provided that FA = 1 in the received frame. For FA = 0 (normal), 0s are transmitted in the Q position, as required by the ANSI T1.605 standard.

Two modes of operation exist for the S channel. The two modes are controlled by bit 5 in register R5. This control is called the S channel state machine ssm bit. The powerup default value of ssm is 0. With ssm = 0 in R5, register R7 holds the 5-bit S subchannel groups of received S bits (e.g., SC11, SC21, SC31, SC41, SC51; see Section 6.3.4 of the I.430 specification). When new data is available, the ss interrupt (R10, bit 3) can be generated during frames 1, 6, 11, and 16 of the 20-frame multiframe. For example, the S bits displayed by the frame 6 interrupt are from frames 1, 2, 3, 4, 5 (the S bit from frame 5 is SB4—R7, bit 4). S bits in R7 are cleared at system reset.

When ssm = 1 (R8, bit 5), the S subchannel #1 message is assembled during the 20-frame multiframe. At the end of a multiframe, the four S subchannel #1 bits (SC11, SC12, SC13, SC14) are available in SB[0:3] of register R7. The ss interrupt is generated when a 4-bit S word is assembled.

Architecture (continued)



F = Framing bit
L = dc balancing bit
D = D-channel bit
E = Echo D-channel bit
FA = Auxiliary framing bit or Q-channel bit
N = Bit set to binary value N = FA
A = Activation bit
S = S-channel bit
M = Multiframe synchronization bit
B1 = Bit within B-channel 1
B2 = Bit within B-channel 2

Note: The TE-to-NT transmission has a nominal 2-bit delay relative to the NT-to-TE frames.

Figure 7. Frame Structure Including Multiframe Options

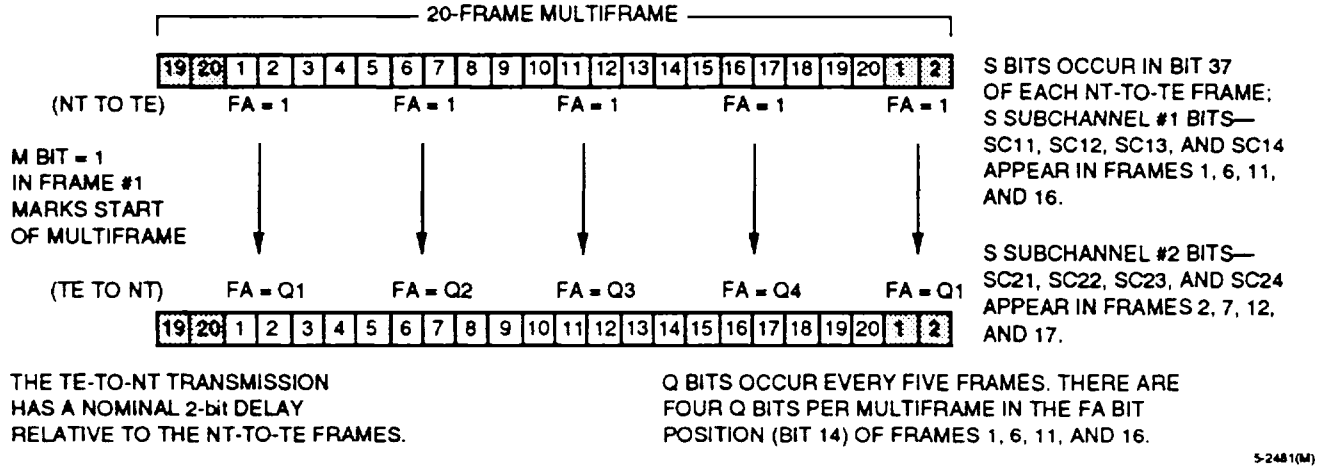


Figure 8. 20-Frame Multiframe

Architecture (continued)

HDLC Formatter

The HDLC formatter supports standard HDLC (high-level data link control) formatting functions that include flag generation and detection, zero-bit insertion/deletion, and error control using the ITU-T-16 polynomial cyclic redundancy check (CRC). D-channel data transfers are made through the microprocessor interface. Sixteen bytes of buffering are provided in both directions of transmission. The HDLC transmitter performs flag generation, performs zero-bit insertion, and calculates the CRC. Whenever five successive 1s occur in the data and CRC to be transmitted, the transmitter automatically inserts a 0 bit after the fifth 1, regardless of the value of the next bit. This prevents the possibility of misinterpreting data or CRC as flags, aborts, or idles.

A D-channel transmission is started by writing data to the 16-byte transmit queue. The HDLC transmitter requests access to the link. The transmission begins after the S/T transceiver acknowledges the request by asserting an internal clear-to-send signal.

Multiple HDLC frames can be written to the queue. All frames must be explicitly tagged with a transmitter frame complete TFC (R2, bit 3). TFC should be set after the last byte of data has been written to the queue. If the last data byte transmitted is not tagged with TFC, an underrun occurs. The transmission ends without a stop flag, which causes an abort (assumes priority is enabled, so underrun aborts do not operate properly during local loopback of the D channel). Transmitter queue status information that indicates whether an underrun occurred is available (UNDABT—R14, bit 5). R14, bits 0—4 provide queue status showing the number of bytes that may be added to the queue.

There are two HDLC transmitter interrupts: TDONE and TE. The TDONE interrupt is set after the transmitter has completed the transmission, including the last bit of the closing flag. The TE interrupt is set when the transmitter queue has reached the programmed level of emptiness (number of bytes available in the queue). Fifteen levels can be specified by TEL[3:0].

The HDLC transmitter can transmit a soft abort via R2, bit 2, in place of the specified data byte in the queue. An immediate abort can be achieved by resetting the transmitter. The HDLC transmitter can also invert all transmitted data.

The HDLC receiver detects flags, does zero-bit deletion, and calculates the CRC. Formatting is done until the HDLC receiver recognizes another flag or an abort sequence. Zero-bit deletion occurs whenever five successive 1s followed by a 0 are received. The 16-bit CRC pattern is computed in parallel with other activities as the serial data for the frame is shifted in and checked against the received CRC pattern. A receive queue manager keeps track of the queue status and updates the receive status register.

On powerup and reset, all data is ignored until a new frame occurs. A frame begins when a flag that is followed by data is detected. The interframe time-fill between HDLC frames may be flags or 1s. Interframe fill of less than 6 bits will be ignored by the HDLC receiver. Interframe fill of more than 5 bits will cause the receiver to idle. Also, two consecutive frames may share a flag. Formatting is done until another flag is detected or until an abort sequence (01111111) is detected. The queue manager keeps track of the queue status and updates the receive status register. The bits in the receive status register (R5) indicate the following:

- Bit 7 indicates end-of-frame (EOF) status. This bit is a 1 if there is an end of frame in the queue.
- Bit 6 provides IDLE status. RIDL is set when 15 consecutive 1s have been received.
- Bit 5 indicates whether an OVERRUN occurred since the last read of the status register. The receive queue should be reset (RRES = 1; R15, bit 1) if bit 5 of the status byte is a 1. Bit 5 of the status byte is cleared when the status register is read.
- Bits 0—4 indicate the number of bytes in the queue, up to and including the first EOF. CRC bytes are not counted.

Binary encoding is used. If no EOF is in the queue, the number tells how many bytes are in the queue.

The queue manager also creates an EOF status byte for each frame and stores it in the queue. The following are included in each EOF status byte:

- Bad CRC (bit 7)—a high (1) indicates that a transmission error occurred.
- Abort (bit 6)—a high indicates the received frame was aborted.
- Bad byte count (bit 4)—a high indicates that the bit count received after zero-bit deletion was not a multiple of eight (i.e., an integer number of bytes).
- Bits 0—3 and bit 5 are 0s.

A frame that is closed normally also causes an EOF. A good frame is implied by an EOF status of all 0s. The receive queue level count in bits 0—4 of register R5 includes the EOF status byte for the frame. The CRC bytes are not included in the queue. The last byte of a frame is always the status word.

Architecture (continued)

On overrun, no EOF status byte is written to the queue. Since the queue is not automatically cleared on an overrun, the receiver should be reset (RRES = 1; R15, bit 1) to avoid reading bad data. After the receiver is reset (by RESET or RRES), data is ignored until the start of a new frame.

Two maskable interrupts, receive full (RF) and receive end of frame (REOF), are generated by the receiver. If the RF interrupt is enabled, an interrupt is generated when the receive queue reaches the programmed level of fullness. Sixteen levels can be specified by RFL[3:0]. If the REOF interrupt is enabled, an interrupt is generated when an REOF occurs. An REOF condition will occur at frame completion or when an abort or overrun is detected.

As stated above, the HDLC controller responds to the reception of 15 consecutive 1s by setting the RIDL bit (R5, bit 6), indicating an idle condition on the D channel. D-channel bits are then ignored until the next flag is received. This all-1s idle pattern (referred to as interframe fill) is typically sent by a switch when there is no valid data to send. However, some switches may send interframe fill of fewer than 15 1s between frames. Interframe fill of less than 6 bits will be ignored by the HDLC receiver. Interframe fill of more than 5 bits will cause the receiver to idle.

Address Recognition

In the T7250C, four address registers, BR[4:1], hold the four byte patterns used to match against the address fields of an incoming LAPD frame. Single-byte address recognition and 2-byte address recognition are possible. The type of address recognition desired is controlled via register BR5. The four choices are the following:

- SAPI (service access point identifier)
- TEI (terminal end point identifier)
- DLCI (data link connection identifier)
- No address recognition

For example, to specify that the byte loaded in BR1 is for a SAPI match, use MAP1S1 = 0 and MAP1S0 = 1 in register BR5. To specify a TEI match, use MAP1S1 = 1 and MAP1S0 = 0. To specify a 2-byte word address recognition, use {MAP1S1 = 1, MAP1S0 = 1} and {MAP2S1 = 1, MAP2S0 = 1} in BR5. If only one of the DLCI pairs is set, 2-byte word address recognition is ignored. For instance, if one of the pairs is programmed to (0, 1) and the other pair is programmed to (1, 1), only a SAPI byte match is made. To disable address recognition on any byte pattern loaded in BR1, use MAP1S1 = 0 and MAP1S0 = 0. To selectively ignore the Command/Response (C/R) bit in a SAPI match, set the SCRM bit in register BR6. When the address recognition feature is enabled, only those LAPD frames whose address patterns match are loaded in the received D-channel queues. Unmatched frames are ignored.

Whether or not the address recognition option is enabled, the T7250C defaults to recognize the broadcast TEI address. To disable broadcast address recognition by a terminal endpoint, reset the BET (broadcast enable TEI) bit to 0 in register BR6 (bit 2).

Regardless of the type of address recognition option used, the entire HDLC frame, except flags and CRC fields, is loaded in the received D-channel FIFO buffers whenever an address match occurs. This ensures full software compatibility with the T7250A.

The T7250C can be programmed to stay in the powered down mode until an address match occurs. To allow D-channel address recognition on powerup, the DARP bit in BR6 (bit 0) should be set to 1. See Figure 8.

Architecture (continued)

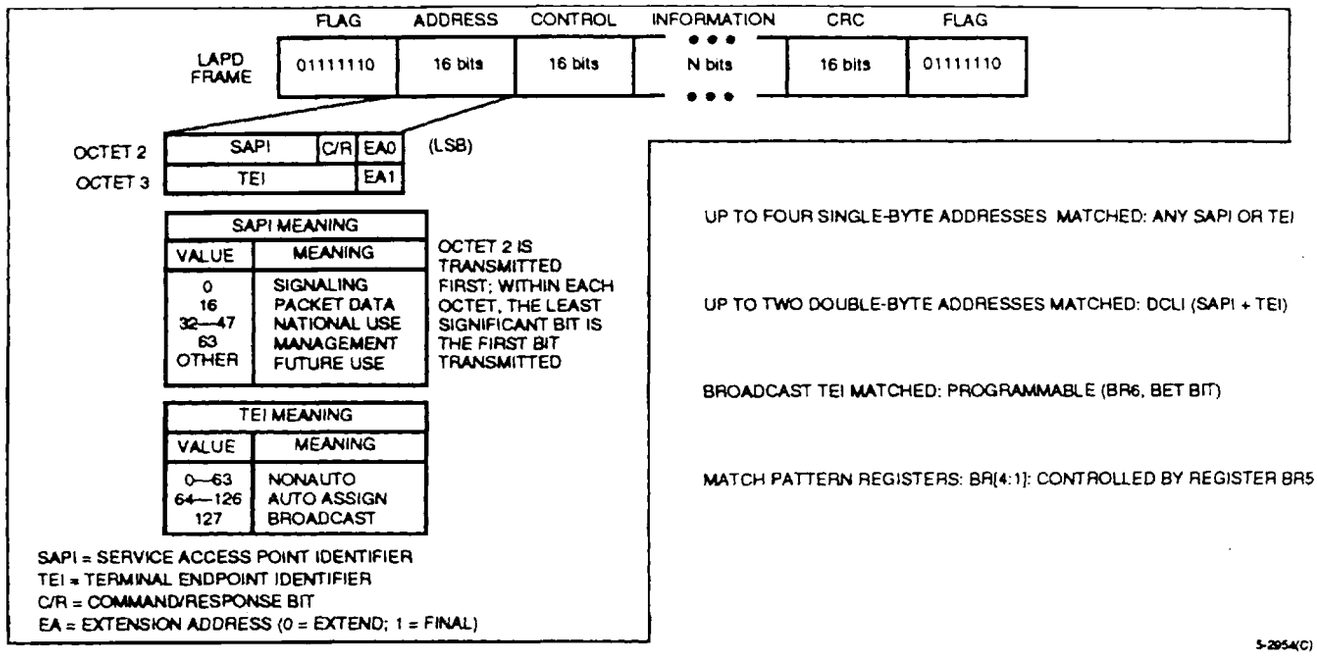


Figure 9. Address Recognition

S/T Transceiver

The S/T transceiver supports encoding and decoding of the 2B+D inverted alternate space inversion (ASI) line code format over four wires. A binary 1 is represented by the absence of a pulse, and a binary 0 is represented by alternate positive or negative pulses. All timing is extracted from the bit and frame timing information that is received from the NT.

The T7250C S/T interface transmitter and receiver meet all Recommendation I.430 specification when configured as shown in Figure 10. Diodes (D1—D8) and zener diodes (ZD1 and ZD2) form one possible example of surge protection circuitry. Low capacitance fast recovery diodes are recommended. The recommended zener voltage for ZD1 and ZD2 is 6.2 V or greater. See Figures 11—13 for S/T interface characteristics. The common-mode suppression blocks shown in Figure 10 are usually common-mode chokes and are used to reduce EMI at the S/T interface.

Transmitter Specifications

When used with the AT&T 2768A or 2776A transformers as shown in Figure 10, the T7250C transmits pulses within the I.430 specified templates for 50 Ω and 400 Ω loads (see Figures 11 and 12). The transmitter requires 112 Ω ± 1.0% external resistance between pins TPR and TNR (excluding transformer resistance). This resistance is usually realized by using 56 Ω ± 1% in each transmitter leg. See Figure 10.

In the inactive and powered down states or when transmitting a binary 1, the following requirements apply:

The output impedance (excluding the 100 Ω line termination), in frequency range of 2 kHz to 1 MHz, should exceed the impedance indicated in Figure 11. This requirement is applicable with an applied sinusoidal voltage of at least 100 mV (rms value).

At a frequency of 96 kHz, the peak current, which results from an applied voltage of up to 1.2 V (peak value), should not exceed 0.6 mA (peak value).

To meet these requirements in the powered-down state, relays should be used to isolate the T7250C transmitter and receiver from the transformer when the device power is off as shown in Figure 10. If the relay contact resistance is more than 4 Ω, its value should be included when calculating resistor values to meet the 112 Ω ± 1.0% requirement between TPR and TNR.

Architecture (continued)

Transmitted Jitter

Transmitted jitter is within ±7% of a bit period as defined by Recommendation I.430 (Section 8.2.2), and phase deviation is within –7% to +15% of a bit period as defined in Recommendation I.430 Section 8.2.3.

Receiver Specifications

The T7250C meets I.430 receiver requirements at the S/T interface when a 2.5:1 transformer is used as shown in Figure 10. More specifically, the transformer-coupled receiver (RPR and RNR inputs) functions with logical 0 voltage level of +1.5 dB to –7.5 dB for point-to-point configurations and +1.5 dB to –3.5 dB for other configurations. The logical 0 voltage level is relative to a 750 mV input and is measured at the S/T interface. Configurations are defined in Recommendation I.430 (Section 8.6.2.1).

Receiver input impedance exceeds 100 kΩ at the RPR and RNR inputs, which is equivalent to an impedance >16 kΩ at the S/T interface. The impedance and peak current requirements for the transmitter also apply to the receiver.

10.0 kΩ ± 10% resistors to RPR and RNR are required to satisfy the I.430 powerdown impedance requirements (see Figure 10).

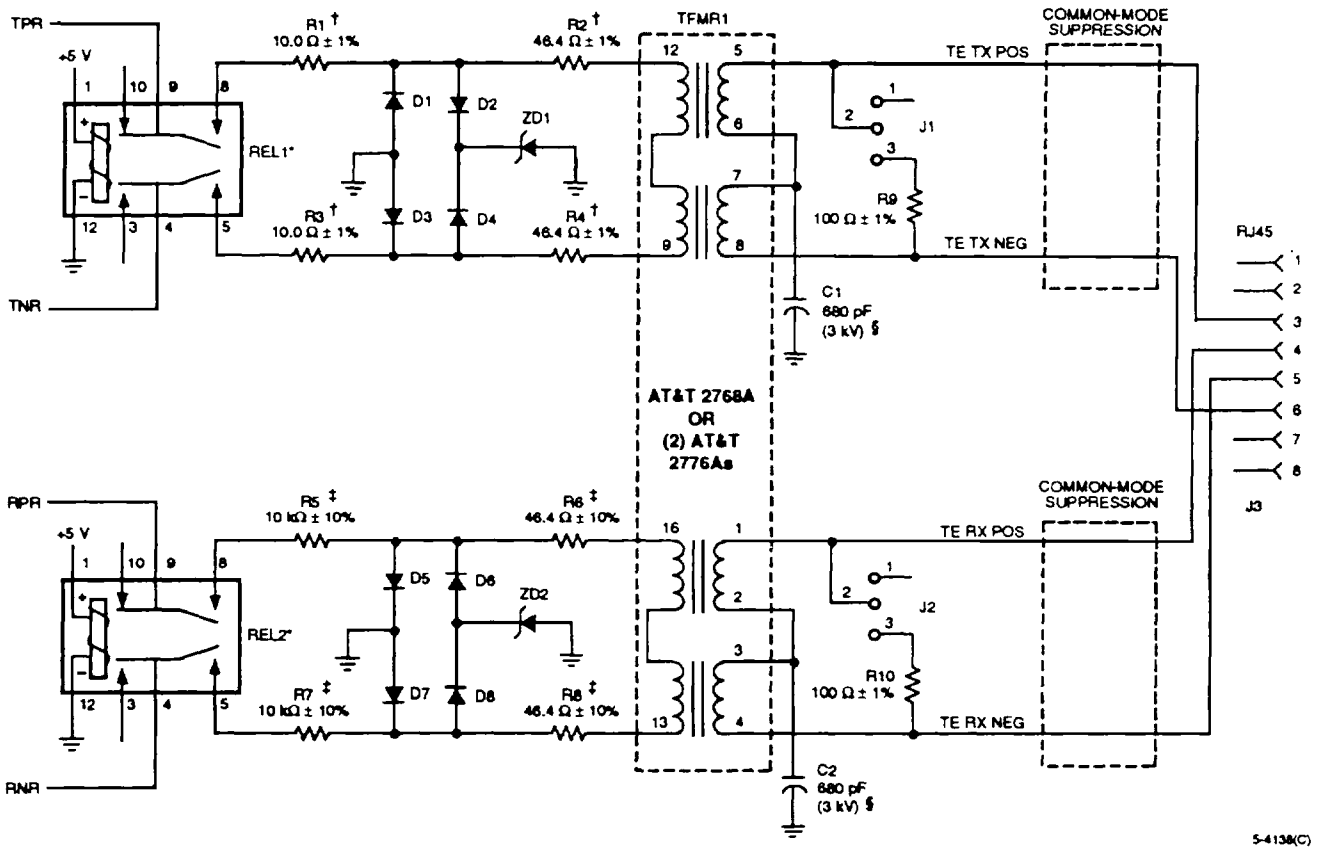
Timer

The T7250C device also has a built-in, general-purpose timer that can be configured for several modes of operation. The time interval is programmable from 0.127 seconds to 2.032 seconds, with a resolution of 0.127 seconds. The output of the timer is available on a pin, TIMOUT, which is asserted for a minimum of 55 µs. Assertion polarity defaults to active-high but can be programmed via a control register (R4, bit 0) to be active-low.

The timer can be configured as a programmable timer, a programmable one-shot or an immediate one-shot, or it can be completely disabled. The programmable timer mode produces a periodic TIMOUT pulse. The immediate one-shot produces an immediate TIMOUT pulse. The programmable one-shot produces a TIMOUT pulse that is delayed by 0.127 seconds multiplied by (1 + programmed offset).

Four timer mode bits (R13, bits 7—4) are used to encode the timer configuration, and four timer offset bits (R13, bits 4—0) are used to determine the cycle time. The cycle time of the timer has a resolution of 0.127 seconds. The timer defaults at powerup to a multivibrator that provides a 57 µs pulse every 2.032 seconds. If the timer register (R13) is accessed with a specific code (0010) in the four most significant bits (R13, bits 7—4 respectively), the timer resets itself to the time-out period specified in the least significant bits (R13, bits 3—0). The timer can also be used as a SANITY timer when TIMOUT is wired to the reset of the T7250C and the resets of other chips in a system. A powerup reset pulse (~4 ms) appears at TIMOUT during powerup providing an integrated solution for powerup reset and sanity.

Architecture (continued)



* These relays (REL1/REL2) isolate the T7250C's transmitter and receiver from the network when the device is powered down (I.430 state F1). This is required to meet peak current specifications for the F1 state.

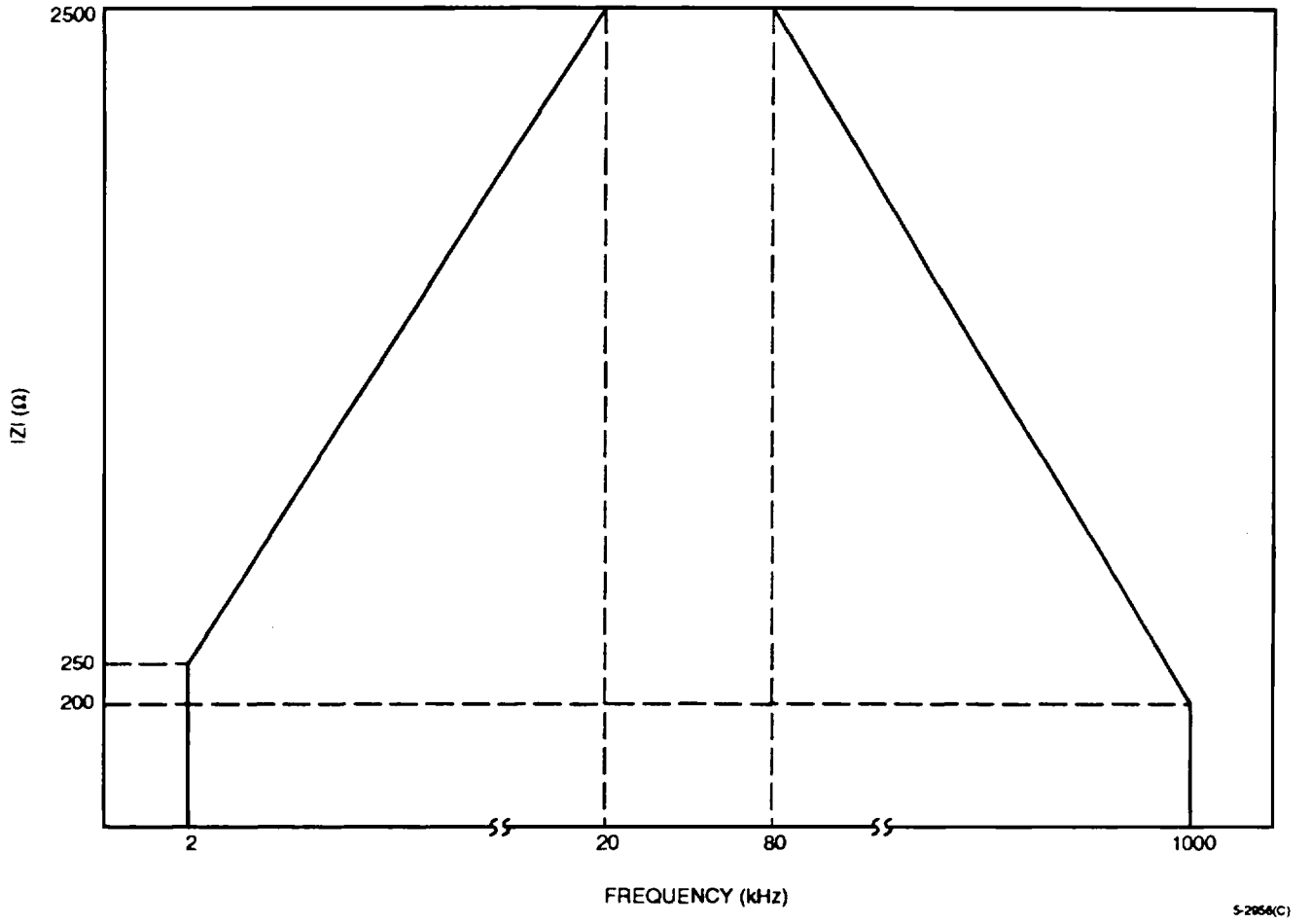
† The actual values for R1—R4 depend on the current handling capacity of the diode bridges (surge protection). The total resistance in each leg of the transmitter (between the chip and the transformer) should be 56 Ω ± 1%.

‡ The actual values for R5—R8 depend on the current handling capacity of the diode bridges (surge protection). The total resistance in each leg of the receiver (between the chip and the transformer) should be 10 kΩ ± 10%.

§ The maximum voltage that the capacitor should be capable of handling is listed in parentheses ().

Figure 10. Line Interface Circuitry

Architecture (continued)



Note: When transmitting a binary 0, the output impedance is ≥20 Ω. The output impedance limit applies for two nominal load impedance (resistive) conditions: 50 Ω and 400 Ω. The output impedance for each nominal load is defined by determining the peak pulse amplitude for loads equal to the nominal value of ±10%. The peak amplitude is defined as the amplitude at the midpoint of the pulse. The limitation applies for pulses of both polarities.

Figure 11. ITU-T I.430 Transmitter Output Impedance Template at the S/T Interface

Architecture (continued)

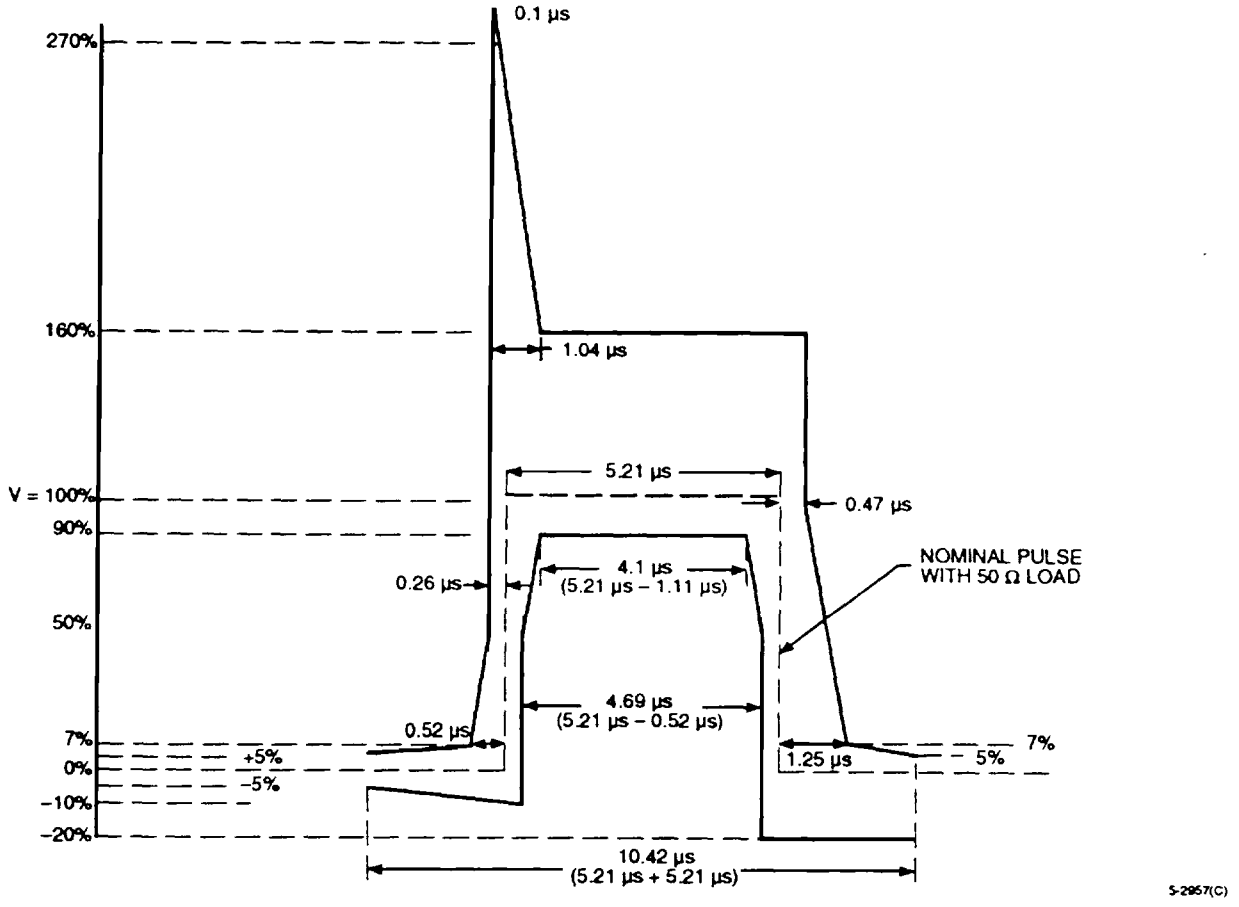


Figure 12. ITU-T I.430 Transmitter Output Pulse Template for 400 Ω Load at the S/T Interface

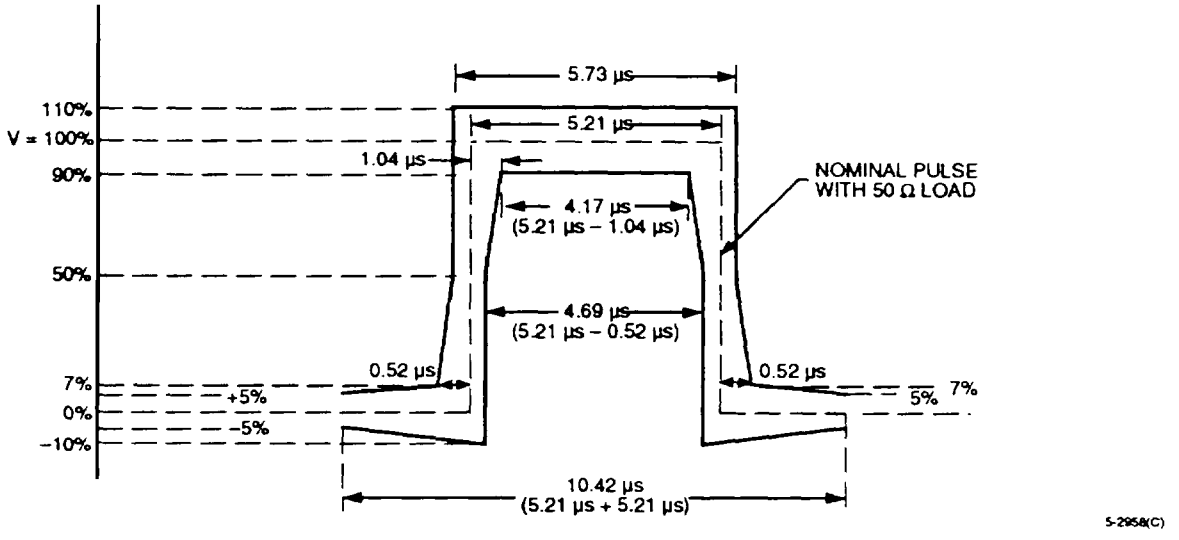


Figure 13. ITU-T I.430 Transmitter Output Pulse Template for 50 Ω Load at the S/T Interface

Register Descriptions

Foreground Registers (R[15:0])

The foreground registers R[15:0] occupy 16 locations in the memory map of the controlling microprocessor system. Separate address and data lines allow virtually any 8-bit or 16-bit microprocessor to be used. The registers are accessed under the control of the following signals: address selects (A[3:0]), chip select ($\overline{CS}$), read ($\overline{RD}$), write ($\overline{WR}$), and the 8-bit bidirectional data bus D[7:0]). Table 3 provides a quick reference summary of the foreground register functions. Table 3 provides a register map showing the layout of all register bits. Table 4 details the functions of register bits. Registers R[9:1] have alternate functions when the background mode of operation is chosen by setting the three most significant bits in R15.

Background Registers (BR[9:1])

The background bank of registers occupies nine locations in the memory map of the controlling microprocessor system. They are addressed the same way as the foreground registers. Functions provided by the background registers are accessed by setting the three most significant bits in register R15 of the foreground bank. Figure 6 gives a quick reference summary of the background register functions. Figure 7 shows the bit map, and Figure 8 contains a detailed description of individual bits. When the background registers BR[9:1] are in use, the two foreground registers R0 and R15 are always accessible. Foreground registers R[14:1] may be accessed by resetting the three most significant bits of R15 to 0s.

Control Registers

Control registers can be written to or read by the microprocessor at any time. The ten control registers in the foreground bank are R0, R2, R4, R6, R8, R9, R11, R12, R13, and R15. Register R0 controls read modes and test modes. R2 controls the transmitter. R4 is a hardware configuration control register that allows the user to specify the desired timing of system interface signals. R6 is the control register used for the buffer full and buffer empty interrupt trigger levels. R8 contains S/T interface controls. R9 contains interrupt mask controls. R11 controls multiframing. R12 controls loopback and transmit 1s functions. R13 provides timer mode control. R15 provides reset control and foreground or background register bank selection. For microprocessor-controlled powerdown option, R0, bit 0 (Pwrdn) should be set to 1.

There are three control registers in the background bank: BR[7:5]. Bit fields in BR5 control the type of address recognition desired in the address pattern registers BR[4:1]. BR6 provides additional control options for address recognition. BR7 provides feature control options like auto activation enable, automatic powerdown, system clock output frequency, and interrupt masks.

Note: Bits 5—7 in R15 must be programmed to 1s for background register selection. The default values (0s) select the foreground registers.

All control registers are automatically initialized on powerup or reset. The HDLC transmitter and receiver and all interrupts are disabled so that the chip is quiet until awakened by the microprocessor. The system interface defaults to a viable configuration. The B channels and codec clock interfaces come up in the mode suitable for the AT&T T7501-Series PCM Codec with Filters. FSEB1 and FSEB2 are the frame strobes but are disabled until INFO 2 or INFO 4 is received. All 1s are transmitted and received on both B channels, which silences the codec. CKCOD is 2.048 MHz. The timer output (TIMOUT) polarity is active-high. The interrupt, INT, is active-high. B1- and B2-channel information are not interchanged. The S/T interface priority mechanism is activated and the priority class is signaling. The clock output on MCKB1 is selected to be the continuous 192 kHz clock. The timer defaults to a 2.048 s period.

Data Registers

Data registers provide read or write access to D-channel transmit/receive data bytes. Data can be written to the 16-byte transmit queue by writing to register R3. Data can be read from the 16-byte receive queue by reading register R3. S-channel data is accessed through register R7. Q-channel data is loaded in register R11.

In the background register bank, there are five data registers: BR[4:1] and BR9. The four registers BR[4:1] store the byte patterns to be used for address recognition in an incoming D-channel frame. BR9 contains the selected B-channel byte for parallel read access by the microprocessor.

Register Descriptions (continued)

Status Registers

Status registers are read-only and allow the microprocessor to inspect the status of various on-chip parameters. The status registers are R1, R5, R10, and R14. R1 provides line interface status information. R5 provides D-channel HDLC receiver status information. R10 indicates the source of an interrupt. R14 provides HDLC transmit queue status information.

Mixed Registers

Registers R8 and R11 provide both status information and control (read and write). R11 provides Q-channel transmission status. The background register BR8 provides feature control options for codec clocks and channel selection (B1 or B2) options for parallel readout of B-channel data. An additional control bit, G2BD in BR8, may be programmed to request a grouped (2B+D) serial data transfer option on the RXDATA and TXB1 pins. Appendix A describes the grouped (2B+D) mode of operation. BR8 also stores two status bits, one for powerdown, and the other for B available. R15 provides control functions including foreground or background register selection. Software resets, priority status, and TCRCB control are provided in the foreground mode of operation.

Note: Upper-case letters in Tables 4 and 5 specify control and status parameters for D-channel HDLC. Lower-case letters specify control and status parameters for the 2B+D core. An upper-case letter followed by lower-case letters specifies system configuration parameters. No such distinctions are made in Tables 7 and 8.

Register Tables

Table 3. Foreground Register Bank Function Summary

Name	Read/Write	Function
R0	R/W	Chip Configuration Register/Powerdown
R1	R	Line Interface Status
R2	R/W	Transmitter Control Register
R3	R/W	D-Channel Data Byte
R4	R/W	Hardware Configuration Register
R5	R	HDLC Receiver Status
R6	R/W	Interrupt Trigger Levels for D-Channel Queues
R7	R	Multiframe Status & S-Channel Bits
R8	R/W	Line Interface Control
R9	R/W	Interrupt Masks
R10	R	Interrupt Status
R11	R/W	Q-Channel Data and Status
R12	R/W	Loopback and Transmit 1s Control
R13	R/W	Timer Configuration Control
R14	R	HDLC Transmitter Queue Status
R15	R/W	Software Resets/Background Register Select

Register Descriptions (continued)

Table 4. Foreground Register Bit Map Summary

Reg	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R0	Chip/Hardware Configuration Control	0	0	0	Dynrd	C1pol	C2pol	Ckdm	Pwrdn
R1	Line Interface Status	—	—	—	—	rss1	rss0	r1	r0
R2	Transmitter Control	ENR	ENT	RINV	TINV	TFC	TABT	tss1	tss0
R3	D-Channel Byte Data	—	—	—	—	—	—	—	—
R4	Hardware Configuration Control	Codec1	Codec2	Syscko	B1f	B2f	Clkmux	Ipol	Tpol
R5	HDLC Receiver Status	EOF	RIDL	OVERRUN	RQS4	RQS3	RQS2	RQS1	RQS0
R6	Interrupt Trigger Level D-Channel Queue Control	RFL3	RFL2	RFL1	RFL0	TEL3	TEL2	TEL1	TEL0
R7	Multiframe and S-Channel Data & Status	mse	st1	st0	SB4	SB3	SB2	SB1	SB0
R8	S/T Line Interface Control and Status	b1i	b2i	ssm	Ipry	prye	pry	b1xb2	clrmm
R9	Interrupt Masks Control	REOFIE	RFIE	TEIE	TDIE	ssie	qdie	richgie	mmie
R10	Interrupt Status	REOF	RF	TE	TDONE	ss	qdone	richg	mm
R11	Q-channel Data and Status	qse	qloop	doneq	enflg	QB4	QB3	QB2	QB1
R12	Loopback and Transmit 1s Control	t1b1	t1b2	lld	llb1	llb2	rld	rlb1	rlb2
R13	Timer Configuration Control	Tm3	Tm2	Tm1	Tm0	Tim3	Tim2	Tim1	Tim0
R14	Transmitter Queue Status and Control	—	—	UNDABT	TQS4	TQS3	TQS2	TQS1	TQS0
R15	Soft Resets/Bank Control Status	Bg —	Bg —	Bg —	TCRCB TCRCB	0 ecd	TRES ecc	RRES ecb	Mres eca

Table 5. Foreground Registers—Bit Definitions

Name	Bit	Symbol	Type	Name/Function
R0	0	Pwrdn	R/W	**Powerdown.** Program to 1 for microprocessor-controlled powerdown. The default value of 0 provides normal operation.
R0	1	Ckdm	R/W	**D-Channel Clock MUX.** This bit controls the frequency of the clock that is output on CKDM (pin 40). When Ckdm = 0 (default), CKDM is the 16 kHz D-channel clock (2.6 µs wide negative pulse train). When Ckdm = 1, CKDM is an 8 kHz, free-running clock.
R0	2	C2pol	R/W	**CKB2 Clock Polarity.** This bit controls the phase of CKB2 (pin 38) relative to the internal clock that is used for sampling and transmitting data. C2pol should be programmed to 0 when the CKB2 is connected to a device that transmits on the rising edge and samples data on the falling edge (most codecs). C2pol should be programmed to 1 when CKB2 is connected to a device that transmits on the falling edge and samples data on the rising edge (most HDLC framers). The powerup initialization default value of C2pol = 0.

Register Descriptions (continued)

Table 5. Foreground Registers—Bit Definitions (continued)

Name	Bit	Symbol	Type	Name/Function
R0	3	C1pol	R/W	**MCKB1 Clock Polarity.** This bit controls the phase of MCKB1 (pin 36) relative to the internal clock that is used for sampling and transmitting data. C1pol should be programmed to 0 when MCKB1 is connected to a device that transmits on the rising edge and sample data on the falling edge (most codecs). C1pol should be programmed to 1 when MCKB1 is connected to a device that transmits on the falling edge and samples data on the rising edge (most HDLC framers). The powerup initialization default value of C1pol = 0.
R0	4	Dynrd	R/W	**Dynamic Read.** When set, this bit specifies that all reads are dynamic. The status bits can be continuously monitored as long as $\overline{RD}$ is low. When 0 (default), all reads are latched. Program to 0 for normal operation.
R0	5—7	—	R/W	**Not Described.** Must be programmed to 0 for normal operation.
R1	0, 1	r[0:1]	R	**Previous Received Information Pattern.** Bits r0 and r1 reflect the received information pattern before the change that caused the richg (R10, bit 1) interrupt. They are encoded the same as rss0 and rss1. When r0 and r1 are different from rss0 and rss1, the received information pattern has changed since the interrupt. Bits r0 and r1 become the current received INFO state when the interrupt status register R10 is read. Then, if INFO states change again before the interrupt routine has read this register R1, the software can detect this change.
R1	2, 3	rss[0:1]	R	**Current Received Information Pattern.** Contains the current information pattern being received from the NT. **rss1 rss0 Definition** 0 0 INFO 0 0 1 INFO 2 1 0 INFO 4 1 1 Lost framing INFO 0 is no signal (64 successive 1s). INFO 2 is normal framing when the A bit is 0. INFO 4 is normal framing with synchronized 2B+D data and D echo; the A is 1. See ITU-T Recommendation I.430 (Section 6.2.2). Three frames are required to establish a change in the INFO state. Lost framing is assumed when a time period equivalent to three 48-bit frames has elapsed without the detection of valid pairs of code violations.
R1	4—7	—	R	**Not Described.**
R2	0, 1	tss[0:1]	R/W	**Transmit Serial Stream (to NT).** These bits control what information pattern is being transmitted to the NT. **tss1 tss0 Definition** 0 0 INFO 0 (default) 0 1 INFO 1 1 x INFO 3 INFO 0 is no signal, INFO 1 is a continuous signal with a pattern of positive 0, negative 0, and six 1s, and INFO 3 is synchronized frames with operational data on B and D channels. See ITU-T Recommendation I.430 (Section 6.2.2).

Register Descriptions (continued)

Table 5. Foreground Registers—Bit Definitions (continued)

Name	Bit	Symbol	Type	Name/Function
R2	2	TABT	R/W	**Transmit Abort (D Channel).** Setting this bit instructs the internal HDLC transmitter to abort the frame. Writing to TABT effectively replaces the last data byte in the queue with an abort sequence. The transmitter finishes shifting out the data in the queue, and then transmits the abort sequence (01111111). TABT is cleared on powerup and reset. TABT and TFC should be set simultaneously to avoid getting an underrun indication.
R2	3	TFC	R/W	**Transmit Frame Complete (D Channel).** Setting this bit instructs the internal HDLC transmitter to close the frame normally after the last data byte. The 16-bit CRC and the closing flag are appended. This bit should be set within 500 µs of writing the last data byte of the frame to the queue. The default value is 0.
R2	4	TINV	R/W	**Transmit Inverted Data (D Channel).** If this bit is set, transmitted D-bit data streams are inverted. The default value is 0. When using D-inversion (RINV = TINV = 1 [R2, bits 4 and 5 = 1]), programming clrmm = prye = 0 (R8, bit 0 = R8, bit 3 = 0) is recommended.
R2	5	RINV	R/W	**Invert Received Data (D Channel).** If this bit is set, received D-bit data streams are inverted. The default value is 0. When using D-inversion (RINV = TINV = 1 [R2, bits 4 and 5 = 1]), programming clrmm = prye = 0 (R8, bit 0 = R8, bit 3 = 0) is recommended.
R2	6	ENT	R/W	**Enable Transmit (D Channel).** Setting this bit enables the HDLC transmitter (for TE-to-NT transmission). When the transmitter is disabled, 1s are transmitted. On powerup and reset, the transmitter is disabled. The transmitter must be enabled for correct operation of D-channel local loopback.
R2	7	ENR	R/W	**Enable Receive (D Channel).** Setting this bit enables the HDLC receiver (for NT-to-TE reception). On powerup and reset, the receiver is disabled.
R3	0—7	DBYTE	R/W	**D-Channel Data.** The D-channel data byte to be transmitted is loaded through this register (on write). Also, the D-channel data byte received is accessed through this register.
R4	0	Tpol	R/W	**Time-Out Polarity.** When set, this bit causes the polarity of the time-out signal on TIMOUT to be active-high. Tpol equal to 0 specifies that TIMOUT should be active-low. This bit is set on powerup and reset. **Caution: TIMOUT always defaults to active-high on powerup and reset. System designers need to consider what effect this will have. TIMOUT is asserted (high) on powerup for 1 ms to 15 ms.**
R4	1	Ipol	R/W	**Interrupt Polarity.** Setting this bit specifies that the hardware interrupt signal, INT, is active-high (default). If this bit is 0, the INT signal is active-low.
R4	2	Clkmux	R/W	**Clock Multiplexer.** When this bit is set (default), the hardware clock output signal on MCKB1 is CK192 (192 kHz); otherwise, the clock signal is CKB1, a 192 kHz clock that is active only during the B1 time slot.
R4	3	B2f	R/W	**B2 Framing.** Setting this bit (default) forces the hardware signal on FSEB2 to be a frame strobe (see Table 1 and Figure 20). If B2f = 0, FSEB2 puts out a gating signal (envelope) for the duration of B2-channel data. The timing of the envelope is defined by R4, bit 6.

Register Descriptions (continued)

Table 5. Foreground Registers—Bit Definitions (continued)

Name	Bit	Symbol	Type	Name/Function
R4	4	B1f	R/W	**B1 Framing.** Setting this bit (default) forces the hardware signal on FSEB1 to be a frame strobe (Table 1 and Figure 20). If B1f = 0, FSEB1 puts out a gating signal (envelope) for the duration of B1-channel data. The envelope timing is defined by R4, bit 7.
R4	5	Syscko	R/W	**System Clock.** When 0 (default), this bit specifies that the output SYSCKO (pin 28) is a 6.144 MHz clock; when set, this bit specifies that SYSCKO should be a 192 kHz clock. For minimum power consumption, program this bit to a 1. When the 6.144 MHz clock is not used, it is recommended that SYSCKO be programmed to be 192 kHz because of power and EMI considerations.
R4	6	Codec2	R/W	**B2 Codec Option.** This bit specifies the timing relationship between the B2 envelope (FSEB2 when R4, bit 3 is cleared) and the start of the first bit of B2 data. Setting this bit specifies that FSEB2 occurs one-half clock cycle before the first bit of B2, on the falling edge of the 192 kHz clock; clearing this bit (default) specifies that FSEB2 occurs with the first bit of B2 on the rising edge of the 192 kHz clock. This function does not impact the timing of FSEB2 when it is programmed to be a strobe (i.e., when R4, bit 3 is set).
R4	7	Codec1	R/W	**B1 Codec Option.** This bit specifies the timing relationship between the B1 framing sync and the first bit of B1 data. Setting this bit specifies that FSEB1 occurs one-half clock cycle before the start of the first bit of B1 on the falling edge of the 192 kHz clock; clearing this bit (default) specifies that FSEB1 occurs with the first bit of B1 on the rising edge of the 192 kHz clock. This function does not impact the timing of FSEB1 when it is programmed to be a strobe (i.e., when R4, bit 4 is set).
R5	0—4	RQS[0:4]	R	**Receive Queue Status (D Channel).** These bits tell how many bytes are available in the queue, including the first EOF status byte. If there is no EOF status byte, the number of bytes in the queue is provided.
R5	5	OVERRUN	R	**Overrun.** When set, this bit indicates that overrun has occurred. The bit is cleared when the status is read via register R5.
R5	6	RIDL	R	**Receive Idle (D Channel).** This condition is set when the idle sequence of 15 contiguous 1s is detected.
R5	7	EOF	R	**End of Frame (D Channel).** This flag is set when an EOF exists in the queue. When EOF is set, the receive queue status reflects the number of bytes to the first EOF status.
R6	0—3	TEL[0:3]	R/W	**Transmit Empty Interrupt Trigger Level (D Channel).** These bits specify the minimum number of bytes (1 to 16) that can be added to the transmitter queue when a transmit empty (TE) interrupt occurs. Encoding is in binary, and TEL0 is the LSB. The code 0000 (default value) in this 4-bit field means 16 bytes can be added to the queue.
R6	4—7	RFL[0:3]	R/W	**Receive Full Interrupt Trigger Level (D Channel).** These bits specify the minimum number of bytes in the receiver queue that trigger a receive full interrupt (RFL). Encoding is in binary, and RFL0 is the LSB. A code of 0000 (default) means that the buffer will be full (i.e., 16 bytes are available) when the RFL interrupt occurs.

Register Descriptions (continued)

Table 5. Foreground Registers—Bit Definitions (continued)

Name	Bit	Symbol	Type	Name/Function
R7	0—4	SB[0:4]	R	**S-Channel Data.** In the T7250C, these bits provide one bit each for each of the five S subchannels described in the I.430 specification. If ssm = 0 in register R8, the five data bits, SB[4:0], (R7, bit 4—0) display the five previously received S bits from the last multiframe quadrant, where SB0 is the first bit received. If ssm = 1 in R8, SB[0:3] are the S subchannel #1 bits: SC11, SC12, SC13, SC14. With ssm = 1 in R8, SB4 in R7 is a 0.
R7	5, 6	st[0:1]	R	**Multiframe State Machine Bits.** These bits indicate how many Q bits remain to be sent in the present multiframe and specify which quadrant of S bits is currently being received. Note that the S bits SB[0:4] (R7, bits 0—4) are from the prior quadrant. S-bit groups are identified as shown below: st1 st0 Q Bits to Send Quad. S-Bit Group 0 0 None or four 4 16—20 0 1 One 3 11—15 1 0 Two 2 6—10 1 1 Three 1 1—5 These states change in frames 1, 6, 11, and 16 at the 14th bit of the transmitted frame. In the T7250C, bits st0 and st1 become valid when multiframe synchronization is established as described below.
R7	7	mse	R	**Multiframe Synchronization Established.** The mse goes high (true) when M-bit synchronization has occurred. Requirements are that frame synchronization is established and that the received M bit (bit 26) goes true exactly 20 frames from the previous M bit true. The mse bit goes true in the middle of 28th bit of the received frame with the M bit true and goes false with the same timing for expected M bit missed or when the M bit is in the wrong frame. It also goes false immediately upon loss-of-frame synchronization.
R8	0	clrmm	R/W	**Clear Mismatch.** A 1 on clrmm forces the mismatch flag, mm in R10 to 0. This bit should be set to 1 for remote loopback of the D channel (see R12, bit 2). This bit must be 0 for ISDN I.430 operation. If clrmm = 0 (default), the mm flag in R10 operates normally. When a mismatch occurs, the transmitter automatically forces all 1s on the D channel.
R8	1	b1xb2	R/W	**Exchange B1 with B2.** When 1, data received on the B1 channel from the NT is transmitted to the TE (on RXDATA) on the B2 channel and vice versa. Data from TXB2 is transmitted to the NT in the B1 channel, while data from TXB1 is transmitted in B2. No exchange occurs if this bit is 0 (default). Note that transmitting 1s, i.e., t1b1 and/or t1b2, has priority over b1xb2.
R8	2	pry	R/W	**Priority.** This bit represents the priority class for D-channel access. A 0 specifies the high-priority (signaling) class; a 1 specifies low-priority (data) class. See the ITU-T I.430. This bit is cleared on powerup and reset.

Register Descriptions (continued)

Table 5. Foreground Registers—Bit Definitions (continued)

Name	Bit	Symbol	Type	Name/Function
R8	3	prye	R/W	**Priority Enable.** When 1 (default), the priority mechanism for passive bus operation is active. The device waits for idle D-channel echo bit (i.e., E bit) such that C = X, where C equals the count of consecutive E bits set and X equals the priority number (8, 9, 10, or 11) for the terminal endpoint. Eight is the highest priority. D-channel messages are sent when C ≥ X. When the prye bit is cleared, messages are sent on demand. This bit must be set to 1 for ISDN I.430 operation. See ITU-T I.430 (6.1.4). Priority must be enabled (even for point-to-point) to ensure that D-channel aborts operate correctly. This bit should be cleared to 0 for remote loopback of the D channel (see R12, bit 2).
R8	4	lpry	R	**Low-Priority Status.** This bit indicates the current priority within a priority class: 1 for low priority, 0 for high priority. This bit cannot be changed by the user; it can only be monitored. This bit is set when a D-channel message is successfully transmitted to the network. It is cleared as soon as priority requirements are satisfied.
R8	5	ssm	R/W	**S-Channel State Machine.** The powerup default value of 0 in this bit allows all S-channel bits to be stored in register R7, bits 4—0. Each 5-bit group represents 1 bit from each of the five S subchannels (e.g., SC11, SC21, SC31, SC41, SC51). (See subchannels described in Section 6.3.4 of the I.430 document). When ssm = 1, the state machine assembles the S subchannel #1 (SC1) message as a 4-bit word (i.e., SC11, SC12, SC13, SC14 are stored in R7, bits SB[0:3]) once every multiframe.
R8	6	b2i	R/W	**B2 Invert.** When 1, this bit specifies that all B2 data, both transmit and receive, should be inverted. When 0 (default), data is not inverted. B2 data is the data that is strobed by FSEB2. If b1xb2 = 1, b2i actually inverts data input at TXB1.
R8	7	b1i	R/W	**B1 Invert.** When 1, this bit specifies that all B1 data, both transmit and receive, should be inverted. When 0 (default), data is not inverted. B1 data is the data that is strobed by FSEB1. If b1xb2 = 1, b1i actually inverts data input at TXB2.
R9	0	mmie	R/W	**Mismatch Interrupt Enable.** When the mismatch interrupt enable bit is set, the hardware interrupt signal, INT, is generated if there is a D-channel echo bit mismatch. See R10, bit 0, described below. The mmie bit is cleared on powerup and reset.
R9	1	richgie	R/W	**Received Information Change Interrupt Enable.** When this interrupt enable bit is set, INT is generated when the received INFO pattern from the NT side changes. See R10, bit 1, described below. The richgie bit is cleared on powerup and reset.
R9	2	qdie	R/W	**Q-Done Interrupt Enable.** When this interrupt enable bit is set, INT is generated when a Q data nibble has been transmitted. See R10, bit 2, described below. The qdie bit is cleared on powerup and reset.
R9	3	ssie	R/W	**S-Channel Interrupt Enable.** When this interrupt enable bit is set, INT is generated when a new S word is available. The ssie bit has a default value of 0 on powerup initialization.
R9	4	TDIE	R/W	**Transmit Done Interrupt Enable (D Channel).** When this interrupt enable bit is set, INT is generated when the TDONE status bit is set (i.e., after the last bit of the closing flag). See R10, bit 7, described below. TDIE is cleared on powerup and reset.

Register Descriptions (continued)

Table 5. Foreground Registers—Bit Definitions (continued)

Name	Bit	Symbol	Type	Name/Function
R9	5	TEIE	R/W	**Transmit Empty Interrupt Enable (D Channel).** If this interrupt enable bit is set, INT is generated when HDLC transmit buffers have reached the programmed level of emptiness. See R10, bit 5, described below. TEIE is cleared on powerup and reset.
R9	6	RFIE	R/W	**Receive Fill Interrupt Enable (D Channel).** When this interrupt enable bit is set, INT is generated when HDLC receive buffers have reached their programmed level of fullness. See R10, bit 6, described below. RFIE is cleared on powerup and reset.
R9	7	REOFIE	R/W	**Receive End of Frame Interrupt Enable (D Channel).** When this interrupt enable bit is set, the hardware interrupt signal INT is generated when an end of frame is detected by the HDLC receiver. See R10, bit 4, described below. REOFIE is cleared on powerup and reset.
R10	0	mm	R	**Mismatch.** This bit is set when the received E bit (D-channel echo bit) does not equal the previously sent D bit while a D-channel message is being transmitted (i.e., while the internal clear-to-send signal is active). A hardware interrupt is generated only if the corresponding interrupt enable bit is set in R9. This status bit is cleared after it is read by the microprocessor.
R10	1	richg	R	**Received Information Changed.** If set, the received INFO pattern has changed. Bits r0 and r1 (bits 4 and 5 of R1) contain the new INFO pattern that caused the richg bit to be set. Since rss0 and rss1 (R1, bit 2 and 3) contain the current received INFO pattern, if the received INFO pattern changes after richg = 1 has been read, the software is able to detect that change. A hardware interrupt is generated if the corresponding interrupt enable bit is set in register R9. This status bit is cleared after it is read by the microprocessor. The richg bit can be used to indicate that the NT is activating/deactivating.
R10	2	qdone	R	**Q Done.** This status bit is set when a Q-channel nibble has been transmitted (multiframe, frame #16). A hardware interrupt is generated if the corresponding enable bit (qdie) is set to 1 in R9. The qdone status bit is cleared after R10 is read by the microprocessor.
R10	3	ss	R	**S-Channel Bits Available.** This status bit is set when a group of S bits is available. Note that the ss bit is set only when multiframe synchronization is present. A hardware interrupt is generated if the corresponding enable bit (ssie) is set to 1 in R9.
R10	4	TDONE	R	**Transmit Done (D Channel).** This status bit is set when transmission of the current HDLC frame has been completed, either after the last bit of the closing flag or after the last bit of an abort sequence. A hardware interrupt is generated only if the corresponding interrupt enable bit is set in register R9. This status bit is cleared on a microprocessor read of register R10.
R10	5	TE	R	**Transmit Empty (D Channel).** If this bit is set, the HDLC transmit buffers are at or below the programmed level of emptiness. A hardware interrupt is generated if the corresponding interrupt enable bit is set in register R9. This status bit is cleared after it is read by the microprocessor. Once cleared, TE is not set again until the condition that caused the interrupt goes away and then reoccurs.

Register Descriptions (continued)

Table 5. Foreground Registers—Bit Definitions (continued)

Name	Bit	Symbol	Type	Name/Function
R10	6	RF	R	**Receive Full (D Channel).** This bit is set when the HDLC receive buffers are at the programmed level of fullness. A hardware interrupt is generated if the corresponding interrupt enable bit is set in register 9. This status bit is cleared after it is read by the microprocessor. Once cleared, RF is not set again until the condition that caused the interrupt goes away and then reappears.
R10	7	REOF	R	**Receive End of Frame (D Channel).** This bit indicates that the receiver has finished receiving a frame. It becomes active upon reception of the last bit of the closing flag of a frame or the last bit of an abort. A hardware interrupt is generated if the corresponding interrupt enable bit is set in register R9. This status bit is cleared after it is read by the microprocessor or after a receiver reset (RESET pin asserted, or soft reset via Mres, or RRES in R15).
R11	0—3	qdata	R/W	**Q-Channel Data.** Bit 0 is transmitted first. These 4 bits are transmitted during the 20 frames of a multiframe, 1 bit every five frames. The qdata bit can be written when enflg (R11, bit 4) is 0. If qloop = 1 in R11, the 4-bit nibble is repeatedly transmitted until new Q bits are loaded; if qloop = 0 in R11, the Q nibble is transmitted once, followed by an all 1s pattern.
R11	4	enflg	R/W	**Enable/Flag.** This dual-purpose bit must be set to 1 when writing qdata. This bit is reset to 0 to indicate that new qdata can be written.
R11	5	doneq	R	**Done Q Nibble.** When this status bit is set, it indicates that a 4-bit Q word has been transmitted. This bit stays set until a new 4-bit Q nibble is loaded for transmission. The default value of the doneq bit is 0.
R11	6	qloop	R/W	**Q-Bit Loop.** The default value of this bit is a 0. When set to 1, this allows recirculation of the Q-channel data nibble loaded in register R11. To change the Q-bit nibble, load R11, bits 0—3 with the new data, and set enflg to 1 in R11 (bit 4). **Note:** In Q-bit loop operation, the qdone interrupt status is generated for only the first transfer of new data—the exception is an all 1s data pattern.
R11	7	qse	R	**Q-Bit Synchronization Established.** The qse bit requires M-bit synchronization and received frame FA and N bits to be flipped (FA = 1, N = 0) exactly five frames after the previous FA and N bits flipped. The qse bit goes true at the end of a receive frame, bit 15, and falls immediately with loss of M-bit or frame synchronization.
R12	0	rlb2	R/W	**Remote Loopback B2 Channel.** When 1, the received B2 channel is looped back to the network terminator (NT). When 0 (default), there is no loopback. For correct operation, t1b2 and llb2 must be programmed to 0. t1b2 overrides rlb2. This loopback is not supported in grouped (2B+D) serial data transfer mode. Remote and local loopbacks cannot be performed simultaneously.
R12	1	rlb1	R/W	**Remote Loopback B1 Channel.** When 1, the received B1 channel is looped back to the NT. When 0 (default), there is no loopback. For correct operation, t1b1 and llb1 must be programmed to 0. t1b1 overrides rlb1. Remote and local loopbacks cannot be performed simultaneously.

Register Descriptions (continued)

Table 5. Foreground Registers—Bit Definitions (continued)

Name	Bit	Symbol	Type	Name/Function
R12	2	rld	R/W	**Remote Loopback D Channel.** When 1, D-channel data received from the NT is looped back to NT. When 0 (default), there is no loopback. For correct operation, ENT (R2, bit 6) and clrmm (R8, bit 0) must be programmed to 1 and lld (R12, bit 5) and prye (R8, bit 3) must be programmed to 0. Remote and local loopbacks cannot be performed simultaneously.
R12	3	llb2	R/W	**Local Loopback B2 Channel.** A value of 1 loops the B2-channel data received on the TXB2 input back through the RXDATA output, and a steady stream of 1s is sent to the NT. When 0, there is no loopback. The default value of llb2 is 1. For correct operation, rlb2 and t1b2 must be programmed to 0. Remote and local loopbacks cannot be performed simultaneously.
R12	4	llb1	R/W	**Local Loopback B1 Channel.** A value of 1 loops the B1-channel data received on the TXB1 input back through the RXDATA output, and a stream of 1s is sent to the NT. When 0, there is no loopback. The default value of llb1 is 1. For correct operation, rlb1 and t1b1 must be set to 0. Remote and local loopbacks cannot be performed simultaneously.
R12	5	lld	R/W	**Local Loopback D Channel.** A value of 1 loops the D-channel HDLC transmit data back to the terminal. A continuous stream of 1s is sent from the terminal to the network termination. When 0 (default), there is no loopback. For correct operation, rld must be programmed to 0, and ENT must be programmed to 1. Remote and local loopbacks cannot be performed simultaneously. **Note:** It is necessary to ignore mismatches (R8, bit 0, clrmm = 1) during local loopback D.
R12	6	t1b2	R/W	**Transmit 1s on B2.** When 1, this bit sends a stream of 1s on the B2 channel; when 0, this bit allows normal B2 channel traffic. The default value of t1b2 is 1. If llb2 is also set (default), 1s are transmitted on the S/T interface and on RXDATA during B2 time slots. This can be used to silence codecs.
R12	7	t1b1	R/W	**Transmit 1s on B1.** When 1, this bit sends a stream of 1s on the B1 channel; when 0, this bit allows normal B1 channel traffic. The default value of t1b1 is 1. If llb1 is also set (default), 1s are transmitted on the S/T interface and on RXDATA during B1 time slots. This can be used to silence codecs.
R13	0—3	Tim[0:3]	R/W	**imer Offset.** The internal timer is programmable from 0.127 s to 2.032 s, with a resolution of 0.127 s. These bits specify the time-out interval as follows: Tim3 Tim2 Tim1 Tim0 Definition 1 1 1 1 2.032 s (default) • (Straight binary count + 1) • multiplied by 0.127 s • 0 0 0 0 0.127 s

Register Descriptions (continued)

Table 5. Foreground Registers—Bit Definitions (continued)

Name	Bit	Symbol	Type	Name/Function
R13	4—7	Tm[0:3]	R/W	**Timer Mode.** These bits specify how the timer will be used: Tm3 Tm2 Tm1 Tm0 Definition 0 0 1 0 Programmable timer (default) 0 1 1 0 Programmable one-shot 1 0 1 0 Timer disabled 1 1 1 0 Immediate pulse on TIMOUT All others Maintain previous timer mode The timer is restarted when a valid code is written.
R14	0—4	TQS[0:4]	R	**HDLC Transmit Queue Status.** These bits tell how many bytes can be added to the transmit queue. The bits are encoded in binary, and bit 0 is the LSB. Status is cleared by TRES and RESET.
R14	5	UNDABT	R	**Underrun Abort.** A 1 indicates that an abort was transmitted on the D channel due to transmitter queue underrun. This occurs when the last byte in the queue is not tagged with TFC (R2, bit 3). The bit is cleared when the status is read and by TRES or RESET.
R14	6, 7	—	R	**Not Described.**
R15	0	Mres	W	**Master Reset.** Setting this bit resets the HDLC framer and the S/T interface controller (as if RRES and TRES were activated). Control registers are not reset since the microprocessor interface is assumed to be sane if this bit was accessed. If the timer was in either the disabled mode or the one-shot mode, it will be returned to the normal timer mode when Mres is set. Energizing the RESET pin or powerup initialization (hard reset) resets the microprocessor interface. **Note:** Bits 0—2 in register 15 are used in two modes: control and status. Writes to bits 0—2 control software resets. Priority status is provided when register R15 is read.
R15	1	RRES	W	**Receiver Reset (D-Channel HDLC).** Setting this software bit resets the HDLC receiver. The receiver queue and related status are cleared. The receive end-of-frame (REOF) and receive full (RF) status bits and interrupts are cleared. Receive data is ignored until the next flag.
R15	2	TRES	W	**Transmitter Reset (D-Channel HDLC).** Setting this software bit resets the HDLC transmitter and its related queues and status bits. TDONE and TE are deactivated. UNDABT is cleared. TRES should be used to clear the transmitter when a mismatch occurs. **Note:** Bits 0—2 in register 15 are used in two modes: control and status. Writes to bits 0—2 control software resets. Priority status is provided when register R15 is read.
R15	0—3	ec[a:d]	R	**Priority Mechanism Counter.** Contains a count of the number of consecutive logical 1s received on the D Echo channel.
R15	4	TCRCB	R/W	**Transmit CRC Bad.** Setting this bit forces the HDLC transmitter to produce a bad CRC. This bit should be programmed to 0 (default) for normal operation.
R15	5—7	Bg	W	**Background Bank Selection.** Bits 5—7 must be programmed to 0s for standard features (same as T7250A) and foreground register bank selection. Bits 5—7 must be programmed to 1s for enhanced features via background register selection.

Register Descriptions (continued)

Table 6. Background Register Bank Function Summary

Name	Read/Write	Function
BR1	R/W	Match Address Pattern 1 (SAPI or TEI) (DLCI, TEI location)
BR2	R/W	Match Address Pattern 2 (SAPI or TEI) (DLCI, SAPI location)
BR3	R/W	Match Address Pattern 3 (SAPI or TEI) (DLCI, TEI location)
BR4	R/W	Match Address Pattern 4 (SAPI or TEI) (DLCI, SAPI location)
BR5	R/W	Configuration Control—Address Matching
BR6	R/W	Option Control—Address Recognition (See Figure 9.)
BR7	R/W	Feature Control 1 (powerdown, interrupt masks)
BR8	R/W	Feature Control 2 (clocks, parallel B selection, interrupt status)
BR9	R	Parallel Readout B Channel Byte

Table 7. Background Register Bit Map Summary

Name	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
BR1	Match Address Pattern 1 (SAPI or TEI); (DLCI: TEI)	—	—	—	—	—	—	—	—
BR2	Match Address Pattern 2 (SAPI or TEI); (DLCI:SAPI)	—	—	—	—	—	—	—	—
BR3	Match Address Pattern 3 (SAPI or TEI); (DLCI: TEI)	—	—	—	—	—	—	—	—
BR4	Match Address Pattern 4 (SAPI or TEI); (DLCI:SAPI)	—	—	—	—	—	—	—	—
BR5	Configuration Control—Address Matching	MAP4S1	MAP4S0	MAP3S1	MAP3S0	MAP2S1	MAP2S0	MAP1S1	MAP1S0
BR6	Option Control & Address Recognition	MATBR4	MATBR3	MATBR2	MATBR1	GND	BET	SCRM	DARP
BR7	Feature Control 1—Powerdown, Int. Masks	AAE	APDA	PDIE	BAIE	EDR	PDSC1	PDSC0	SCHL
BR8	Feature Control 2—Clks, Par. B, Int. Status, Grouped (2B+D) Transfer	CKCOD	PBTXB	PD	BA	G2BD	SC1	SC0	PBS
BR9	Parallel Readout—B-Channel Byte (B1/B2)	—	—	—	—	—	—	—	—

Register Descriptions (continued)

Table 8. Background Registers—Bit Definitions

Name	Bit	Symbol	Type	Name/Function
BR1	0—7	MAP1	R/W	**Match Address Pattern 1.** A number loaded in this register is used to recognize a matching SAPI or TEI value in the address field of an incoming D-channel frame. In the link access procedure for D-channel (LAPD), SAPI is the service access point identifier and TEI is the terminal endpoint identifier. A SAPI value identifies the call control (layer 3) procedure being used. A TEI value identifies a specific connection environment. To specify whether the match byte is a SAPI or TEI, see register BR5. **Note 1:** Up to four single-byte addresses may be matched. Desired matching patterns are stored in BR[4:1]. Register pairs (BR1 and BR2) and (BR3 and BR4) may also be used for double-byte (word) address matching. **Note 2:** If an address match occurs, the address fields are also loaded in the D-channel queues as in the T7250A. If there is no match, the D-channel frames are ignored. **Note 3:** When word address matching is desired, BR1 should hold the most significant byte of a 16-bit word, the data link connection identifier (DLCI). The least significant byte in the address field (TEI position) should be loaded in BR2. **Note 4:** When a single-byte address is used in BR[4:1] for SAPI matching, octet two of the LAPD frame must match the value in BR[4:1] bit for bit, with the possible exception of the C/R bit, depending on the value of the BR6, bit 1. For example, if SAPI = 63 is desired for matching and the C/R bit is a don't care, then BR6, bit 1 should be set to 1, and one of the registers BR[4:1] should be set to FC hex along with the appropriate setting in BR5. FC hex = 1111 1100 => SAPI part of octet 2 = 63; C/R = 0; EA = 0 SAPI, EA, C/R **Note 5:** When a single-byte address is used in BR[4:1] for TEI matching, octet three of the LAPD frame must match the value in BR[4:1] bit for bit. For example, if TEI = 64 is desired for matching, then one of the registers BR[4:1] should be set to 81 hex along with the appropriate setting in BR5. 81 hex = 1000 0001 => TEI part of octet 2 = 64; EA = 1 TEI, EA

Register Descriptions (continued)

Table 8. Background Registers—Bit Definitions (continued)

Name	Bit	Symbol	Type	Name/Function
BR2	0—7	MAP2	R/W	**Match Address Pattern 2.** A number loaded in this register is used to recognize a matching SAPI or TEI value in the address field of an incoming D-channel frame. To specify whether the match byte is a SAPI or TEI, see register BR5. When word address matching is desired, BR2 should hold the least significant byte of a 16-bit word, the data link connection identifier (DLCI). The most significant byte (SAPI position in the address field) should be loaded in BR1.
BR3	0—7	MAP3	R/W	**Match Address Pattern 3.** A number loaded in this register is used to recognize a matching SAPI or TEI value in the address field of an incoming D-channel frame. To specify whether the match byte is a SAPI or TEI, see register BR5. When word address matching is desired, BR3 should hold the most significant byte of a 16-bit word, the data link connection identifier (DLCI). The least significant byte should be loaded in BR4.
BR4	0—7	MAP4	R/W	**Match Address Pattern 4.** A number loaded in this register is used to recognize a matching SAPI or TEI value in the address field of an incoming D-channel frame. To specify whether the match byte is a SAPI or TEI, see register BR5. For word address matching, BR4 should hold the least significant byte of a 16-bit word, the DLCI. The most significant byte should be loaded in BR3.
BR5	0, 1	MAP1S	R/W	**Match Address Pattern 1 Selection.** These 2 bits control the type of address recognition desired in BR1. **Bit 1** **Bit 0** **Selection** 0 0 Ignore 0 1 SAPI 1 0 TEI 1 1 DLCI (16-bit) **Note:** When a DLCI address pattern is loaded in the (BR1, BR2) pair, each of the 4 bits (0, 1, 2, and 3) in BR5 must be set to 1.
BR5	2, 3	MAP2S	R/W	**Match Address Pattern 2 Selection.** These 2 bits control the type of address recognition desired in BR2. **Bit 3** **Bit 2** **Selection** 0 0 Ignore 0 1 SAPI 1 0 TEI 1 1 DLCI (16-bit) **Note:** When a DLCI address pattern is loaded in the (BR1, BR2) pair, each of the 4 bits (0, 1, 2, and 3) in BR5 must be set to 1.

Register Descriptions (continued)

Table 8. Background Registers—Bit Definitions (continued)

Name	Bit	Symbol	Type	Name/Function
BR5	4, 5	MAP3S	R/W	**Match Address Pattern 3 Selection.** These 2 bits control the type of address recognition desired in BR3. **Bit 5** **Bit 4** **Selection** 0 0 Ignore 0 1 SAPI 1 0 TEI 1 1 DLCI (16-bit) **Note:** When a DLCI address pattern is loaded in the (BR3, BR4) pair, each of the 4 bits (4, 5, 6, and 7) in BR5 must be set to 1.
BR5	6, 7	MAP4S	R/W	**Match Address Pattern 4 Selection.** These 2 bits control the type of address recognition desired in BR4. **Bit 7** **Bit 6** **Selection** 0 0 Ignore 0 1 SAPI 1 0 TEI 1 1 DLCI (16-bit) **Note:** When a DLCI address pattern is loaded in the (BR3, BR4) pair, each of the 4 bits (4, 5, 6, and 7) in BR5 must be set to 1.
BR6	0	DARP	R/W	**D Address Recognition on Powerup.** Setting this bit allows the device to stay in a partially powered-up state until a matching address is recognized in an incoming LAPD frame (INFO 4 from the NT). Refer to Figure 5. This allows the TE to continue sleeping while other TEs on the passive bus communicate with the NT. Thus, a stepped activation of a given TE is possible during powerup. The default value of the DARP bit is 0, with the device becoming fully active when an INFO 2 or INFO 4 frame is received from the network side.
BR6	1	SCRM	R/W	**SAPI Command/Response Bit Mask.** Setting this bit masks the C/R bit in all SAPI address fields. The default value of the SCRM bit is 0.
BR6	2	BET	R/W	**Broadcast Enable TEI.** The default value of this bit is 1, with the broadcast TEI (decimal value 127) address recognition enabled. Resetting this BET bit to 0 disables address matching for the broadcast TEI value of 127. This bit has no significance when address recognition is disabled.
BR6	3	GND	R/W	**Grouped (2B+D), Normal D.** Setting this bit and setting G2BD in BR8 allows grouped (2B+D) data transfer via RXDATA and TXB1 pins, and normal D-channel HDLC processing using on-chip FIFOs. When GND = 0 (default) and G2BD = 1, D bits arriving on the TXB1 pin are sent directly to the ISDN line interface without any on-chip HDLC D-channel processing.

Register Descriptions (continued)

Table 8. Background Registers—Bit Definitions (continued)

Name	Bit	Symbol	Type	Name/Function
BR6	4—7	MATBRx	R	**Matched Address Pattern in Register BRx (x = 1, 2, 3, 4).** When an address match is detected for patterns loaded in register BRx, the corresponding bits in BR6 are set high. In the word address match mode, MATBR3 is set high when there is a match in the (BR4, BR3) pair; MATBR1 is set high for the (BR2, BR1) pair. MATBRx address match indicators stay set until the end of a received D-channel frame.
BR7	0	SCHL	R/W	**System Clock High or Low.** If the clock output option has been set to a dc level (i.e., {PDSC1, PDSC0 = 1, 1} or {SC1, SC0 = 1, 1}), then by setting the SCHL bit, the signal on pin 28 (SYSCKO) will be held high. The default value of 0 for the SCHL bit holds the SYSCKO output pin low.
BR7	1, 2	PDSC[0:1]	R/W	**Powerdown System Clock.** These 2 bits select the output frequency on the SYSCKO pin in the powered down mode. PDSC1 PDSC0 Selection 0 0 6.144 MHz (default) 0 1 1.536 MHz 1 0 192 kHz 1 1 dc level (polarity control via SCHL above) **Note:** The lowest power dissipation (less than 15 mW) is only obtained with the dc output.
BR7	3	EDR	R/W	**External Drive.** When set, the clocking for the T7250C is derived from an external TTL clock source. To set EDR = 1, the clock must have a ≥3.5 V high and a 25%—75% duty cycle. Once written, standard TTL levels may be used. This optimizes the duty cycle for TTL drivers while saving ~3 mW of power. With EDR = 0 (default), the reference clock is derived from a crystal or from external CMOS drivers.
BR7	4	BAIE	R/W	**B Available Interrupt Enable.** If this bit is set, the interrupt condition is flagged and the hardware interrupt signal is generated. The default value is 0 for no interrupt when B-channel data is available for parallel readout.
BR7	5	PDIE	R/W	**Powerdown Interrupt Enable.** If this bit is set, an interrupt signal is generated when a powerdown condition is detected. The default value of 0 implies that no hardware interrupt signal will be generated on powerdown.
BR7	6	APDA	R/W	**Automatic Powerdown Allowed.** When this bit is set, automatic powerdown is allowed via the S/T line interface. The default value of 0 means such auto powerdown is not permitted. **Note:** Powerdown under microprocessor control is still allowed (see foreground register R0, bit 0).
BR7	7	AAE	R/W	**Auto Activation Enable.** By setting this bit, auto activation is enabled. If this bit is reset to its default value of 0, the auto activation feature is disabled, leaving the activation sequence under microprocessor control, as in the T7250A.

Register Descriptions (continued)

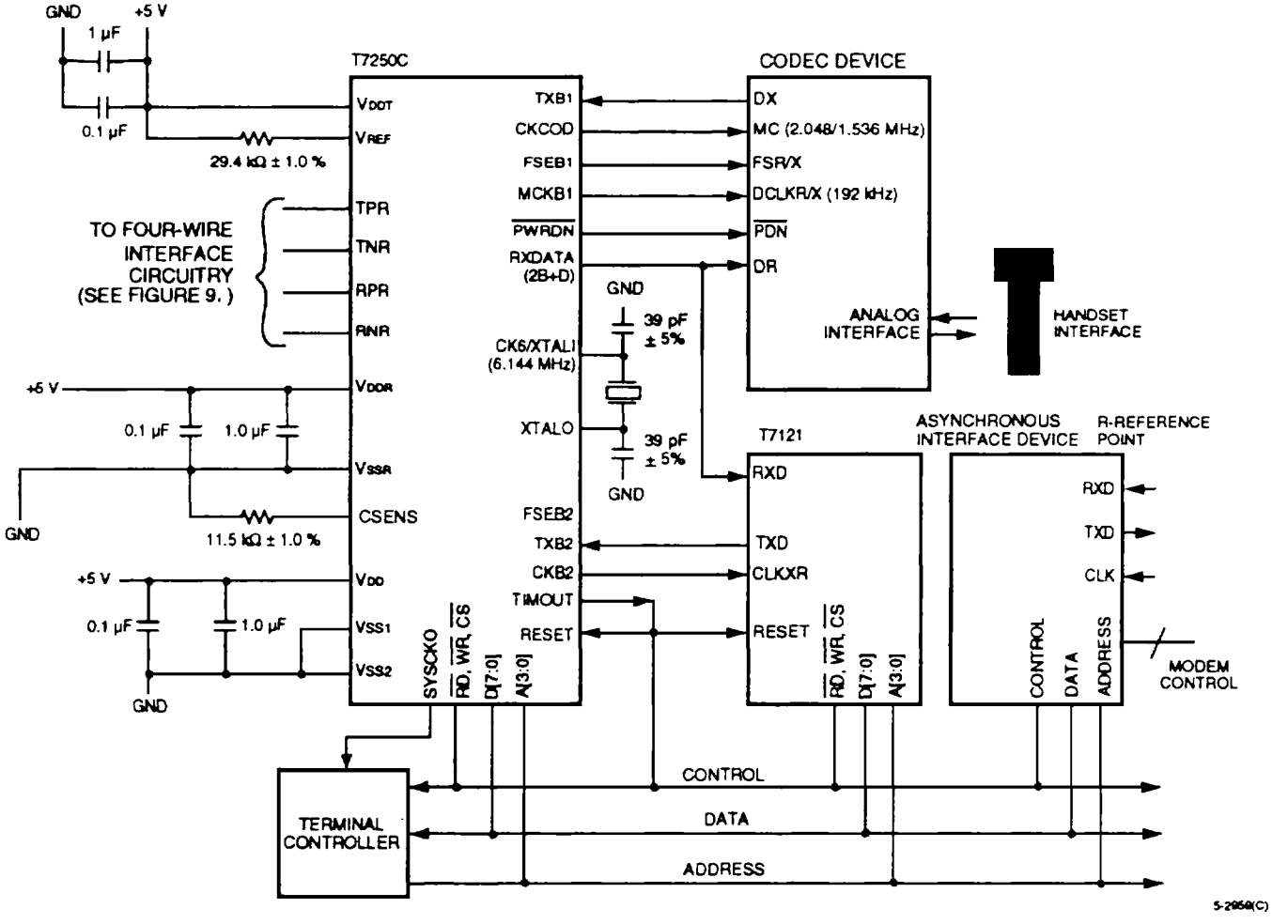
Table 8. Background Registers—Bit Definitions (continued)

Name	Bit	Symbol	Type	Name/Function
BR8	0	PBS	R/W	**Parallel B-Channel Selection.** Setting this bit selects the B2-channel for parallel readout via register BR9. Resetting this bit to 0 selects the B1-channel for parallel readout via BR9. The default value of the PBS bit is 0. **Note:** For B-channel data path selection, see PBTXB, BR8, bit 6 below.
BR8	1, 2	SC[0:1]	R/W	**System Clock Output Frequency.** These 2 bits select the output frequency on the SYSCKO pin in the powered-up mode of operation. SC1 SC0 Selection 0 0 6.144 MHz (if R4, bit 5 = 1) 0 0 192 kHz (if R4, bit 5 = 0) 0 1 1.536 MHz 1 0 192 kHz (independent of R4, bit 5) 1 1 dc level (polarity control via SCHL in BR7, bit 0) The default value of (SC1, SC0) = (0, 0), and the SYSCKO depends on what is programmed in R4, bit 5.
BR8	3	G2BD	R/W	**Grouped (2B+D) Operation.** When this bit is set, grouped (2B+D) serial data transfer is allowed on the RXDATA and TXB1 pins. See Appendix A and Figure 21 for details. The default value of 0 allows the standard mode of operation on RXDATA, TXB1, and TXB2.
BR8	4	BA	R	**B Available.** This status bit is set when the selected B-channel data is available in BR9 for parallel readout. A hardware interrupt signal will also be generated if the interrupt enable bit BAIE is set in BR7. In the interrupt-driven mode, data is held in BR9 for 115 µs. The BA bit is cleared when BR8 is read.
BR8	5	PD	R	**Powerdown.** This status bit is set when the chip enters the powerdown mode via the auto activation/deactivation sequence. A hardware interrupt signal may be generated, depending on the value of the interrupt enable bit PDIE in register BR7. **Note:** In TEs that operate with the richgie (receive information change interrupt enable) masked in the foreground register R9, the powerdown status and the associated interrupt are provided in the background to alert the microprocessor.
BR8	6	PBTXB	R/W	**Parallel Read of B Channel.** When this bit is set, the selected B channel (B1 or B2, see PBS bit in BR8) arriving on the TXB pin is available in register BR9. If PBTXB = 0, the selected B-channel data arriving at the line interface from the NT is available in BR9. The data is held in BR9 for 115 µs.
BR8	7	CKCOD	R/W	**Clock for Codec.** Setting this bit selects the 1.536 MHz output frequency on the CKCOD pin. Resetting this bit to 0 selects the default value of 2.048 MHz (suitable for AT&T codecs).
BR9	0—7	Bb	R	**B-Channel Bits.** This register holds the selected B-channel byte for parallel readout by the microprocessor. Channel selection (B1 or B2) is made by using the PBS bit in BR8. PBS = 0 selects B1, while PBS = 1 selects B2. Once the B-channel is selected, the data path can be programmed to be either the transmit path TXB, or the receive path RXDATA. The PBTXB bit in BR8 provides data path selection. The selected B-channel byte is accessed via BR9. New data is valid for a minimum of 115 µs.

Integrated Voice Data Application

A connection diagram for an integrated voice and data application is shown in Figure 14. A 6.144 MHz crystal provides the system clock. A codec (for example, the AT&T T7501) is used for voice on the B1 channel. The B2 channel is connected to an AT&T T7121 for bit-oriented protocols like HDLC. An asynchronous interface device handles the R-interface inputs. The T7121 and the asynchronous interface device can be used together to implement different rate adaption protocols on the B2 channel.

Also shown are the power and ground considerations for the T7250C device. With the hardware configuration as shown, B1 data transmission or B2 voice transmission can be achieved by instructing the T7250C to exchange B1 and B2 channel information. The TIMOUT pin may be connected to the RESET pin to allow for sanity (watchdog) timer operation and powerup reset.



Notes:
Connect TIMOUT to system reset for powerup and sanity (watchdog) timer.

In an environment in which the +5 V supply is noisy, the addition of a 5 Ω resistor between +5 V and the T7250C power pins (pins 1, 2, 3, and 44) may improve receiver sensitivity. Additionally, a ferrite bead separating V_{DDR} (pin 23) from the other T7250C power pins may help.

Figure 14. Connection Diagram for an Integrated Voice and Data Application

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute maximum ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability. External leads can be soldered safely at temperatures up to 300 °C.

Parameter	Symbol	Min	Max	Unit
dc Supply Voltage	V_{DD}	—	7	V
Input Voltage Range	V_{I1}	V_{SS} – 0.5	V_{DD} + 0.5	V
Ambient Operating Temperature Range	T_A	0	70	°C
Storage Temperature	T_{stg}	–40	150	°C
Maximum Power Dissipation (package limit)	P_D	—	700	mW

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. AT&T employs a human-body model (HBM) and a charged-device model (CDM) for ESD susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. An industry-wide standard has not been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used, and therefore, can be used for comparison. The HBM ESD threshold presented here was obtained by using these circuit parameters. For CDM information, contact AT&T.

Table 9. Human-Body Model ESD Threshold

Device	Voltage
T7250C	>1000 V

Electrical Characteristics

The following conditions apply except where noted: T_A = 0 °C to 70 °C, V_{DD} = 5 V ± 5%, Vss = 0 V, 100 pF each output.

Table 10. Electrical Characteristics

(Subscript identifiers: IL—input low, IH—input high, OL—output low, OH—output high, OZ—output tristate.)

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Current	I_{DD}	T_A = 0 °C	—	19	mA
Input Current:					
High	I_{IH}	$V_{IH} = V_{DD}$	—	7.5	µA
Low	I_{IL}	V_{IL} = 0 V	—	7.5	µA
Input Current Bidirectional Pins:					
High	I_{IH}	$V_{IH} = V_{DD}$	—	–37.5	µA
Low	I_{IL}	V_{IL} = 0 V	—	37.5	µA
Output tristate Leakage Current:					
High	I_{OZH}	$V_{OH} = V_{DD}$	—	–30	µA
Low	I_{OZL}	V_{OL} = 0 V	—	30	µA
Input Voltage (TTL):					
High	V_{IH}	—	2.0	—	V
Low	V_{IL}	—	—	0.8	V
Input Voltage (CMOS):		Crystal input (XTALI) only			
High	V_{IH}	—	3.5	—	V
Low	V_{IL}	—	—	1.5	V
Output Voltage:					
High	V_{OH}	I_{OH} = –2.4 mA	2.4	—	V
Low	V_{OL}	I_{OL} = 2.4 mA*	—	0.4	V
Power Dissipation (45 mW nominal)	PD	—	—	100	mW
Output Current Sink:	I_{OL}	V_{OL} = 0.4 V			
Outputs: D[7:0], CKDM, SYSCKO		V_{DD} = 4.5 V	15	—	mA
Outputs: RXDATA, CKCOD, MCKB1, FSEB1, CKB2, FSEB2, INT, CTSN (POWERDN)			5	—	mA
Outputs: TIMOUT			10	—	mA
Output Current Source:	I_{OH}	V_{OH} = 2.4 V			
Outputs: D[7:0], CKDM, SYSCKO		V_{DD} = 4.5 V	15	—	mA
Outputs: RXDATA, CKCOD, MCKB1, FSEB1, CKB2, FSEB2, INT, CTSN (POWERDN)			5	—	mA
Outputs: TIMOUT			10	—	mA

* Unloaded outputs drive rail to rail.

Electrical Characteristics (continued)

Power Dissipation Estimates

Nominal power dissipation for the T7250C device is 45 mW. Nominal conditions are at 5 V, 20 °C, 50% of the inputs active at the same time, and a 50% duty cycle at the S/T line interface, and SYSCKO programmed to 192 kHz. Maximum power dissipation (assumes worst-case conditions) is 100 mW. Power dissipation is less than 15 mW in the powered down mode, with SYSCKO = dc level.

Timing Characteristics

100 pF load, 5 V ± 5%.

Table 11. Data Input and Output Timing for the System Interface

Symbol	Parameter	Min	Typ	Max	Unit
	Clock Parameters:				
tCKLCKL	MCKB1 and CKB2 Period	4.95	5.21	5.50	µs
tCKHCKL	MCKB1 and CKB2 High (192 kHz)	2.45	2.60	2.75	µs
tCKLCKH	MCKB1 and CKB2 Low	2.45	2.60	2.75	µs
tCKLCKH	CKDM (16 kHz) Low	2.45	2.60	2.75	µs
—	CKDM (8 kHz) High	57.2	—	67.8	µs
—	CKCOD Duty Cycle	45%	50%	55%	—
	Output Transition Delays:				
tLH	Low to High	—	—	55	ns
tHL	High to Low	—	—	35	ns
	Time-out Pulse Width:				
tTOHTOL	Timer Output	57.3	—	68	µs
tTOHTOL	Timer Output (immediate TIMOUT)	57.3	—	136	µs
tTOHTOL	Powerup Reset*	1.5	3.5	7.5	ms
	Reset Parameters:				
tRHOV†	RESET Low to Valid Output	—	—	100	ns
tRHRL	Minimum RESET Pulse Width	175	—	—	ns

* Plus the additional time, if any, for the V_{DD} power supply to reach a minimum of 3.8 V. This promotes an effective powerup reset for systems having a slow ramp-up time for the V_{DD} power supply.
† Not shown in Figure 15.

Timing Characteristics (continued)

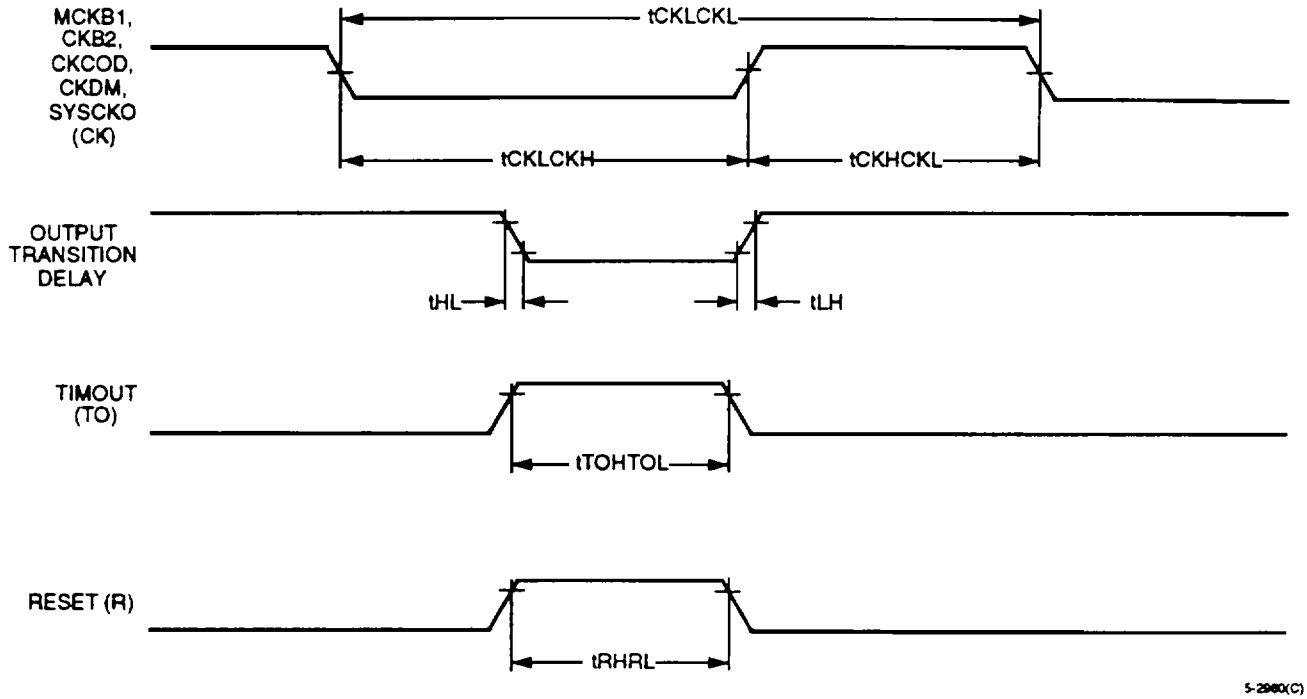


Figure 15. Data Input and Output Timing for the System Interface

Timing Characteristics (continued)

Table 12. Microprocessor Latched Read Cycle

Symbol	Parameter	Min	Max	Unit
	Latched Reads:			
tCSLRDL	$\overline{CS}$, A[3:0] Setup to $\overline{RD}$ Low	30*	—	ns
tRDHCSH	$\overline{CS}$, A[3:0] Hold After $\overline{RD}$ High	0	—	ns
tRDLRDH	$\overline{RD}$ Pulse Width	175	—	ns
tRDLDV	D[7:0] Valid After $\overline{RD}$ Low	—	170	ns
tRDHDX	D[7:0] tristated After $\overline{RD}$ High	5	40†	ns
tCSLCSH	$\overline{CS}$ Pulse Width	200	—	ns

* tCSLRDL is allowed a minimum of 0 ns, which requires tRDLDV and tRDLRDH to have a minimum time of 200 ns.
† T7250B value for tRDHDX is 100 ns.

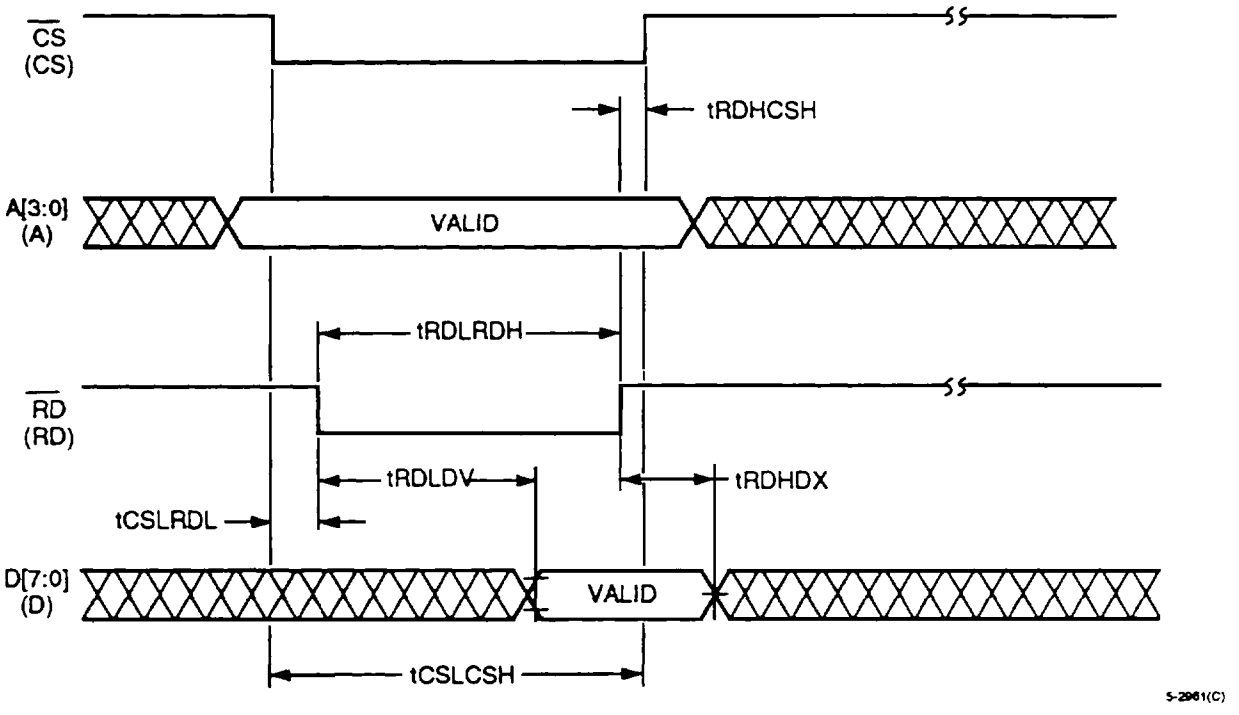


Figure 16. Microprocessor Latched Read Cycle

Timing Characteristics (continued)

Table 13. Microprocessor Dynamic Read Cycle

Symbol	Parameter	Min	Typ	Max	Unit
	Dynamic Reads:				
tAVDV	Access Time from Address Valid to Data Bus Valid (into 100 pF load)	—	100	150	ns
tCSLDV	Access Time from Chip Select for Read	—	—	180	ns
tCSHDX	Chip Select $\overline{CS}$ or Read Strobe $\overline{RD}$ to Data Bus Tristate	5	—	100	ns

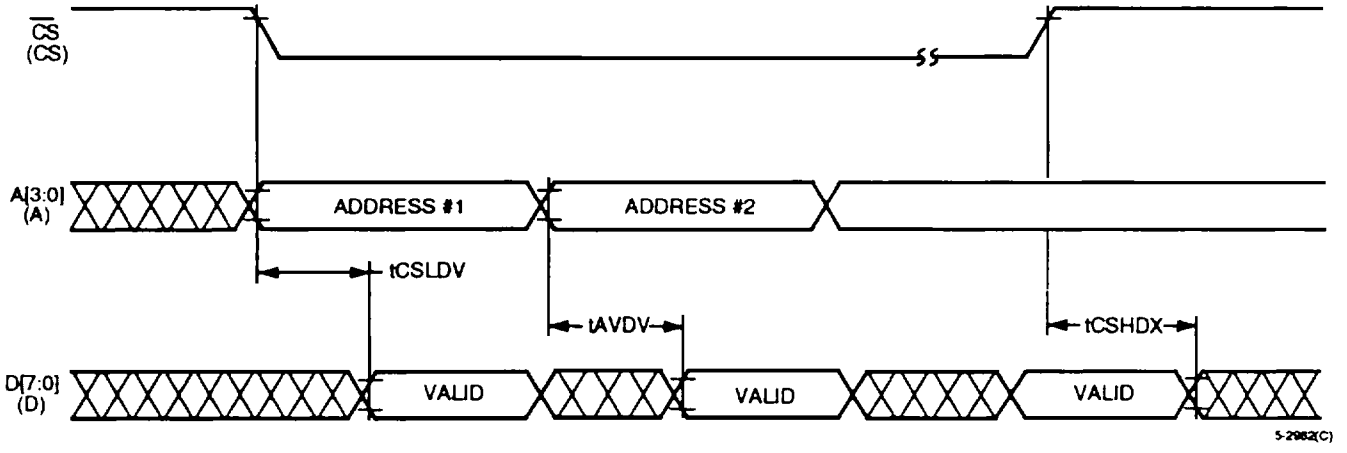


Figure 17. Microprocessor Dynamic Read Cycle

Timing Characteristics (continued)

Table 14. Microprocessor Write Cycle

Symbol	Parameter	Min	Max	Unit
	Write Cycle:			
tCSLWRH	$\overline{CS}$ Setup Before $\overline{WR}$ High	50	—	ns
tWRHCSH	$\overline{CS}$ Hold After $\overline{WR}$ High	0	—	ns
tWRLWRH	$\overline{WR}$ Pulse Width	50	—	ns
tDVWRH	A[3:0], D[7:0] Setup Before $\overline{WR}$ High	30	—	ns
tWRHDV	A[3:0], D[7:0] Hold After $\overline{WR}$ High	30	—	ns
tWRHWRH	Time Before a Next $\overline{WR}$ High	425	—	ns

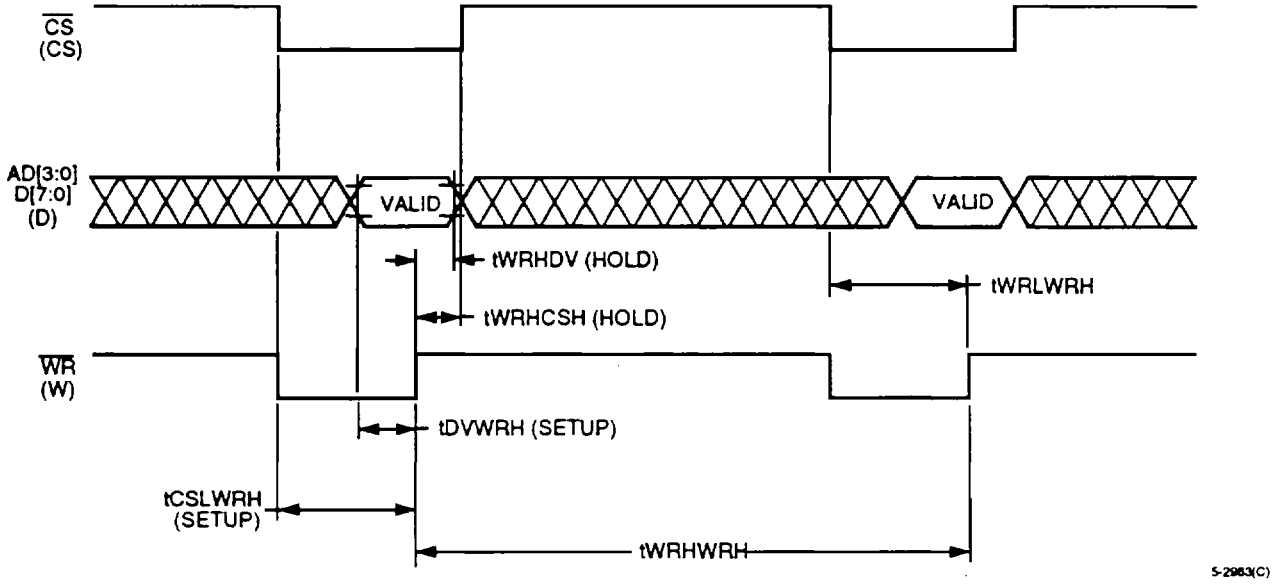


Figure 18. Microprocessor Write Cycle

Timing Characteristics (continued)

Crystal Requirements

Table 15. Crystal Requirements

Parameter	Value
Operating Frequency	6.144 MHz, fundamental mode
Calibration Conditions	Parallel resonant, 22 pF load capacitance
Series Resistance	40 Ω maximum
Shunt Capacitance	7 pF maximum
Stability and Tolerance	55 ppm total from 0 °C to 70 °C including aging
Vendor/Part Number	CTS Corporation Phone: 815-786-8411 Part # 020-3717-0 Saronix Phone: 415-855-6806 Part # SRX5397

The crystal requirements given in Table 15 assume a maximum of 3 pF stray capacitance on each of the board traces going to the crystal. If the actual capacitance is greater than this, 1.0% tolerance 39 pF external capacitors can be used, increasing the allowable stray capacitance to about 5 pF per crystal trace. Another alternative is to recalculate the load capacitance supplied to the crystal vendor by using

$$C_L = \frac{C_{EXT} + C_{STRAY}}{2} + 2\ pF$$

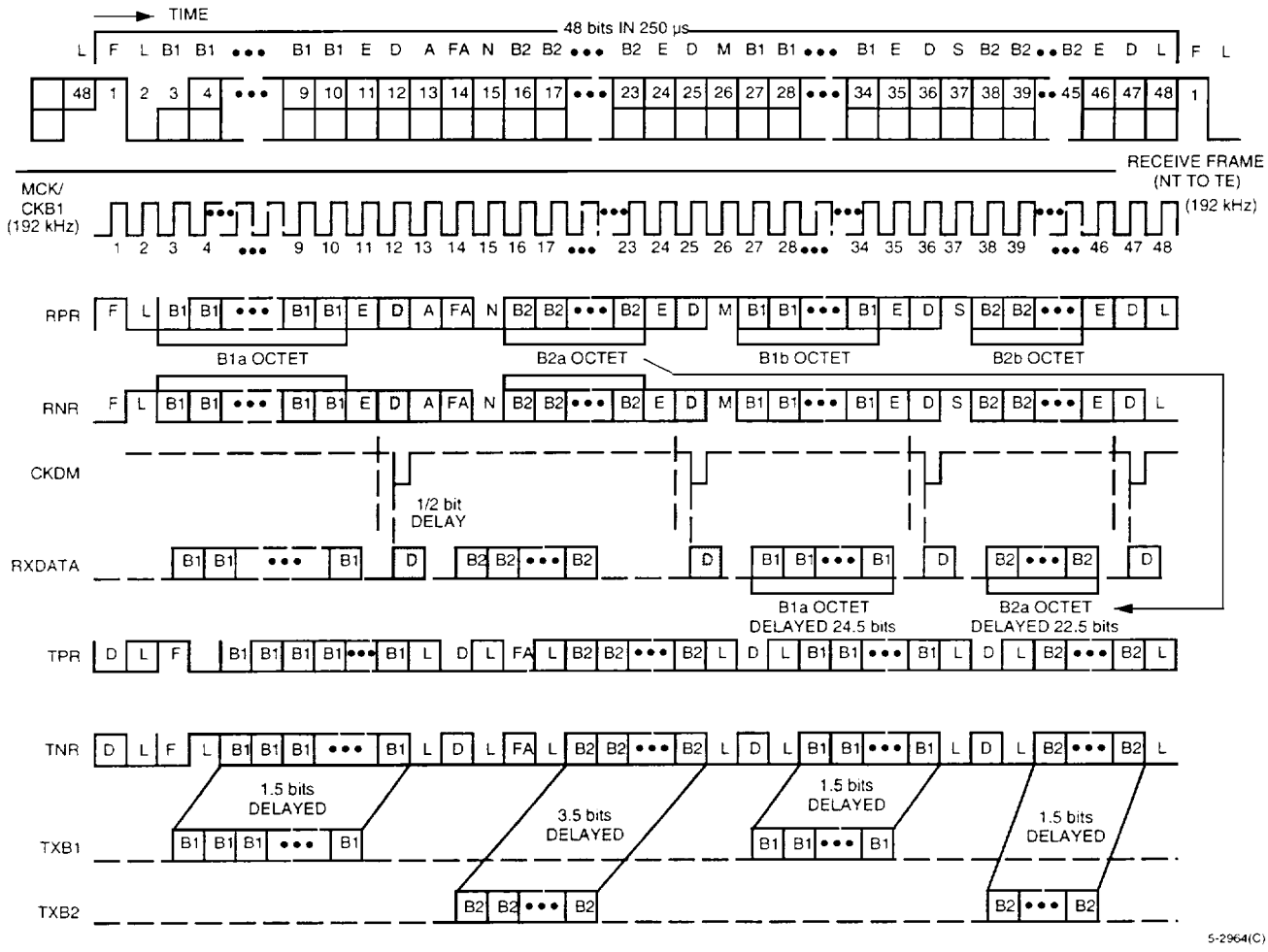
where C_{EXT} is 39 pF and C_{STRAY} is the actual stray capacitance of each board trace going to the crystal.

Other Clock and Control Timing Relationships

Table 16. Other Clock and Control Timing Relationships (100 pF max load)

Parameter	Min	Max	Unit
XTAL Driven to SYSCKO (6.144 MHz)	—	80	ns
SYSCKO (6.144 MHz) Rising Edge to Change In:			
RXDATA	—	100	ns
TIMOUT	—	100	ns
FSEB1	—	50	ns
FSEB2	—	50	ns
MCKB1	—	50	ns
CKB2	—	50	ns
CKCOD	—	50	ns
TPR/TNR	—	150	ns
CKCOD Rising Edge to Change In:			
FSEB1	—	20	ns
FSEB2	—	20	ns
MCKB1	—	20	ns
CKB2	—	20	ns
TXB1, TXB2 Setup Before MCKB1, CKB2 Low (C1pol, C2pol = 0)	550	—	ns
TXB1, TXB2 Hold After MCKB1, CKB2 Low (C1pol, C2pol = 0)	0	—	ns
RXDATA Valid Before MCKB1, CKB2 Low (C1pol, C2pol = 0)	2.5	—	µs
RXDATA Valid After MCKB1, CKB2 Low (C1pol, C2pol = 0)	2.0	—	µs

Timing Characteristics (continued)



Notes:
Pipelined delays of bits received at RPR/RNR to when the bits are available on RXDATA are shown (B2a octet delayed 22 1/2 bits; other B octets delayed 241/2 bits; D bits delayed 1/2 bit).

Pipelined delays of B-channel bits at TXB1, TXB2 to when they are actually transmitted at TPR/TNR are shown (B1 octets delayed 1 1/2 bits; B2 octets delayed 31/2 or 11/2 bits).

RXDATA information is valid in the bit periods shown. In other bit positions, the output is still enabled, but the logic state of the bits is not specified.

Figure 19. Bit Alignment Timing on the S/T Line Interface Relative to the System Interface

Timing Characteristics (continued)

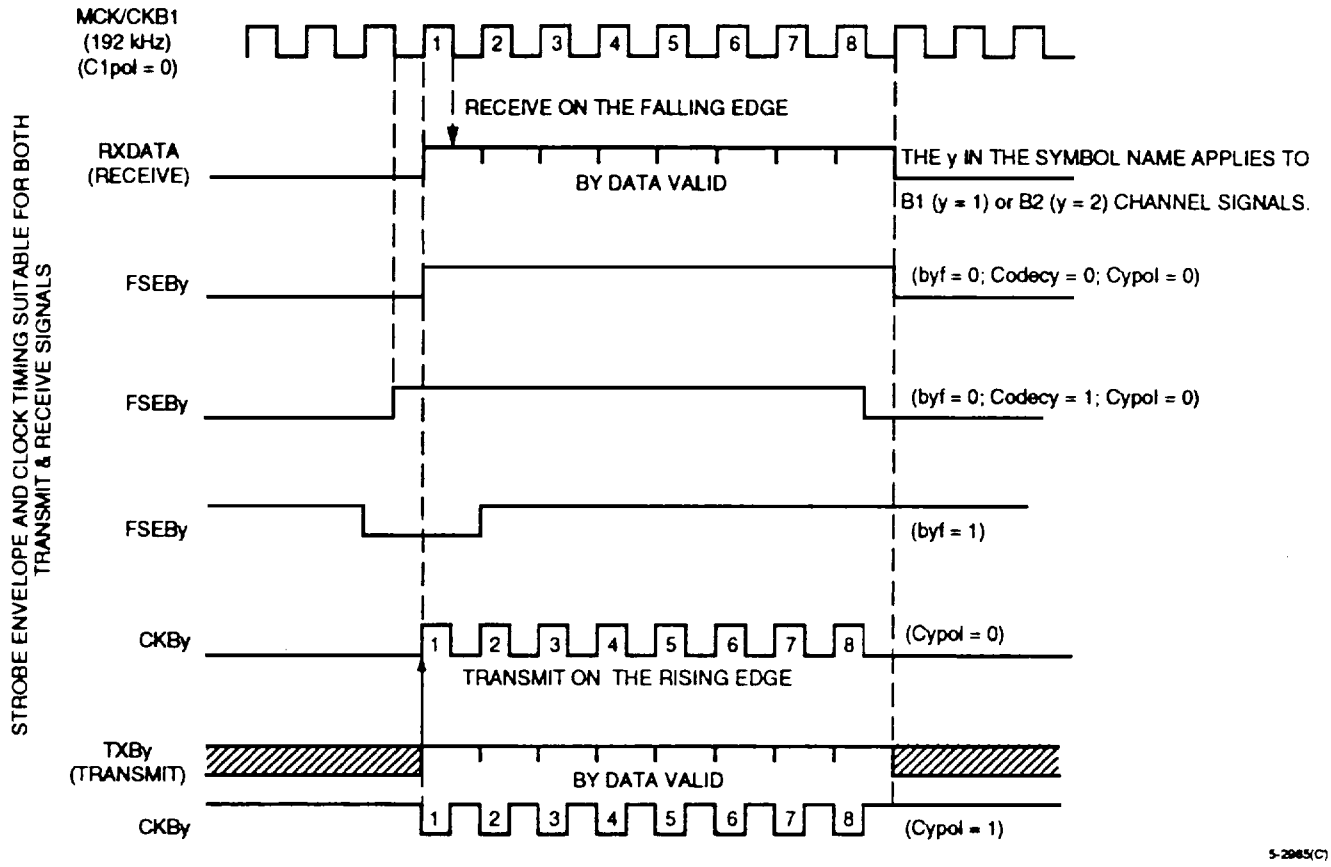
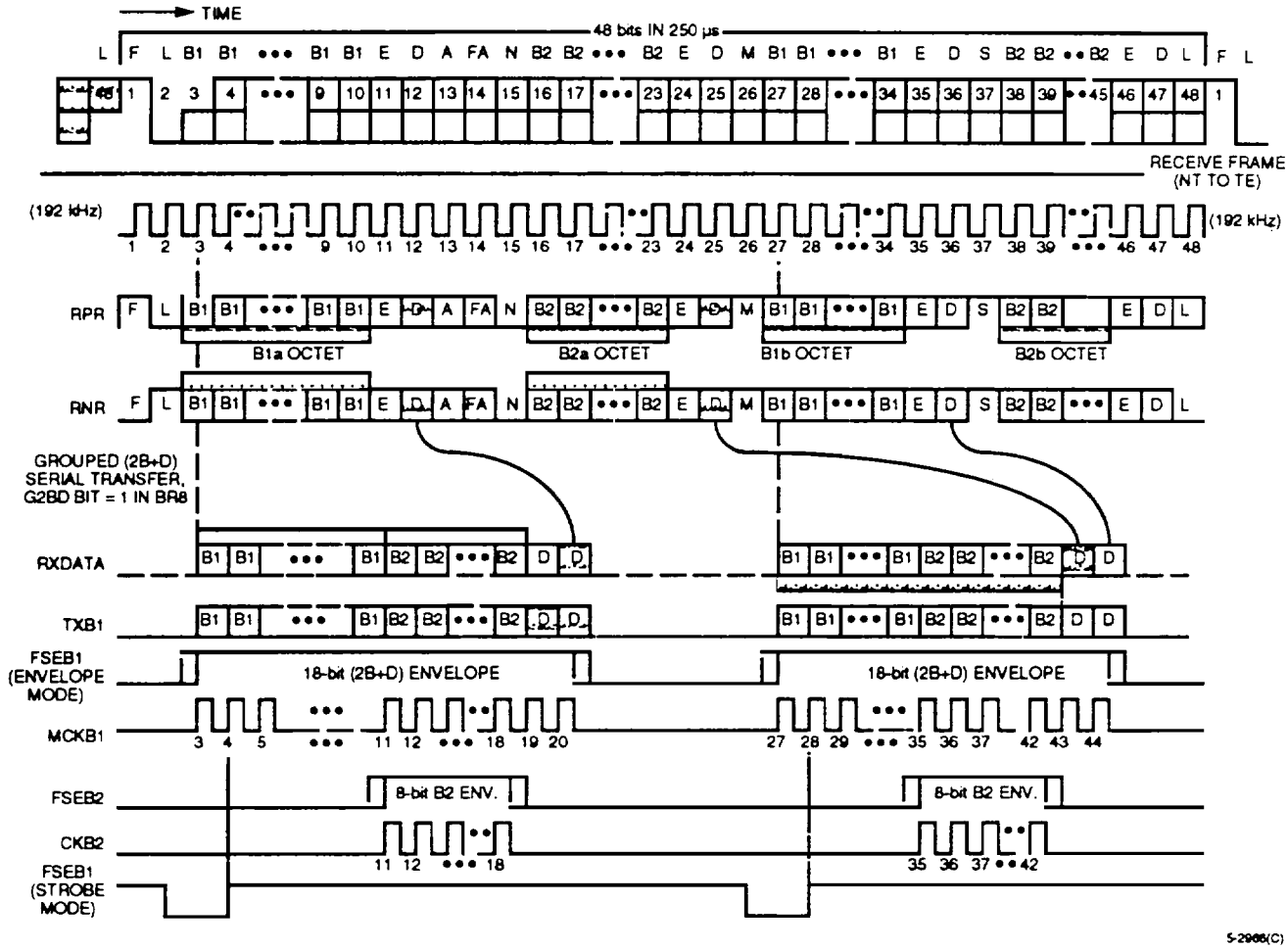


Figure 20. Bit Alignment Timing, with Programmable Options, on the System Interface

Timing Characteristics (continued)



Note: RXDATA information is valid in the bit periods shown. In other bit positions, the output is still enabled, but the logic state of the bits is not specified.

Figure 21. Bit Alignment Timing for the Grouped (2B+D) Serial Data Transfer Mode

Appendix A. Grouped (2B+D) Serial Data Transfer Mode

The Feature

The T7250C provides a serial data transfer option not available in the T7250A. This feature allows 18-bit (2B+D) groups to be transferred in and out of the device, in contiguous time slots. An 18-bit (2B+D) group is treated as a subframe composed of 8 bits each for the B1 and B2 channels, and 2 bits for the D channel. The serial data transfer occurs on the RXDATA and TXB1 pins. Clocking and timing control signals on the FSEB1, MCKB1, FSEB2, and CKB2 pins provide the data transfer. The grouped serial data transfer mode allows the T7250C to connect to devices that support the AT&T Concentration Highway Interface (CHI) running at 192 kHz clock rate (three time slots).

Timing

The grouped (2B+D) serial data transfer mode is programmed by setting the G2BD bit (bit 3) in the background register BR8. The timing relationships are shown in Figure 21. When G2BD = 1, the FSEB1 signal provides an 18-bit envelope over the subframes. In the envelope mode, B1f = 0 (register R4, bit 4). There are two (2B+D) subframes in a 250 µs interval. If the FSEB1 signal is programmed for the strobed mode of operation (B1f = 1), a negative pulse is provided to identify the subframes, as in the T7250A. MCKB1 provides 18 cycles of the 192 kHz clock per subframe interval defined by the FSEB1 envelope when Clkmux (register R4, bit 2) is programmed to 0. When Clkmux = 1, MCKB1 is a free-running 192 kHz clock signal. FSEB2 provides an 8-bit gating envelope for the B2-channel when B2f = 0 (register R4, bit 3). The strobed mode of operation of the FSEB2 signal is not available for the grouped (2B+D) serial data transfer operation.

Programming Considerations

B1 and B2 channel inversion operates normally. Remote loopback of the B2 channel requires that the grouped (2B+D) serial mode be disabled during the time when the B2 channel is in remote loopback. The local loopback functions remain unchanged. The B1 exchange B2 (b1xb2) function to interchange B1 and B2 time slots is not applicable in the grouped serial data transfer mode.

Transmit 1s

During grouped mode operation (G2BD = 1 in register BR8, bit 3), B2 channel transmission is disabled when the transmit 1s on B1 is set (t1b1 = 1 in register R12, bit 7). If 1s transmission on the B1 channel and data transmission on the B2 channel are required simultaneously, the local loopback B1 channel bit (llb1 = 1 in register R12, bit 4) should be used to transmit all 1s on the B1 channel.

Appendix B. Questions and Answers

These questions were compiled from customer inquiries. The questions and answers are divided into six operational categories: D Channel, Line Interface, Programming/Register Features, Applications, Timing, and Miscellaneous.

D Channel

Q1: After a temporary S/T-interface loss of synchronization, the receive status register gave the wrong report on the next received byte. Is there an explanation for this?

A1: It is possible that losing synchronization confused the HDLC receiver so that it no longer understood where it was in the message. A flag is needed to get it realigned. A receiver reset, using RRES, is recommended after resynchronization.

Q2: After a temporary S/T-interface loss of synchronization and resynchronization, a receiver reset is performed. If a message is then sent from the far end, it is not always the first data in the receive FIFO. Sometimes R5 = 81H (valid EOF and 1 byte of data). When the data is read, it reads 50H (abort and bad byte count received). If R5 is read again, it reads 8xH, where x is the size of the frame that was just sent. Another read of the data, however, results in the correct data. What is happening here?

A2: The device has a flag lockout that prevents HDLC reception until a flag is received (except an abort). If, after a receiver reset, a zero shows up on the D channel, followed by the state of all 1s, the seventh 1 generates an abort.

A suggested solution to this problem is to modify the software to look for R5 = 81H (an EOF status byte is in the FIFO, and it is the only byte associated with the received packet) and data = 50H. If this result is received, read R5 again.

Line Interface

Q3: Are the same line interface components used for point-to-point and passive bus?

A3: Yes.

Q4: How does line interface resistance affect transmitter operation?

A4: The T7250C transmitter is a current source that is partially voltage-clamped under nominal 50 Ω load conditions. Therefore, changes in load resistance will affect output current and, consequently, pulse amplitude. The T7250C analog transmitter sees a load that is a combination of both line-side and device-side components. Line-side components include the 50 Ω termination resistance, the TE connecting cord resistance, and the dc resistance of the primary side of the transformer. Device-side load components are the dc resistance of the transformer's secondary coil, relay contact resistance (if a relay is used), and the line interface resistors. Increasing any of these resistances will reduce pulse amplitude, and, conversely, decreasing them will increase amplitude.

The T7250C is designed to transmit pulses within the ITU-T I.430 pulse templates when the following conditions are met:

- External resistors plus the resistance of the relay should equal 112 Ω ± 1%.
- dc resistance of the transformer's secondary (chip side) coil plus the reflected resistance of the transformer's primary coil (line side) should be between 10 Ω and 20 Ω.
- The resistance of the TE connecting cord should be 3 Ω or less per lead (6 Ω per pair).
- The resistors connected to the VREF and CSENS pins should be 29.4 kΩ (±1%) and 11.5 kΩ (±1%), respectively.

Q5: Some transformer manufacturers specify maximum dc resistance values that are higher than those given in **Q4** above. Also, some connecting cords may have more than 3 Ω per lead (6 Ω per pair). Could this be a problem?

A5: Yes, this might be a problem if the resistance is too high (see **Q4** above). If pulse amplitude is low (i.e., the margin to the I.430 templates becomes too small), the external line interface resistors should be decreased accordingly.

Appendix B. Questions and Answers

(continued)

A5: (continued)

For example, if the transformer has a total dc resistance (secondary resistance plus reflected primary resistance) of 24 Ω, the sum total of the line interface resistors should be reduced by 4 Ω (i.e., the amount that the transformer resistance is above 20 Ω). Another example is the case where the TE connecting cord is 7.0 Ω per pair (3.5 Ω per lead). This is 1.0 Ω above the maximum resistance of 6 Ω given above. Since the cord is on the line or primary side of the transformer, the 1 Ω of excess resistance must be reflected to the secondary to find the amount to decrease the interface resistors. This is done by multiplying the excess resistance by 6.25 (the turn ratio squared), giving 6.25 Ω. Therefore, the sum total of the line interface resistors should be reduced by about 6 Ω, using the nearest standard values available.

Q6: Can you recommend any other transformers, besides the 2768A and 2776A, for use with the T7250C?

A6: Preliminary characterization of the following transformers indicates that they may be suitable for use with the AT&T T7250C, T7256, and T7259 devices. It should be noted that accredited layer 1 conformance testing was not performed. Full conformance testing should be completed to ensure compliance.

For applications requiring reinforced insulation:

1. Part No.: APC2050S (Single Transformer) or APC8020D (Dual Transformer)

   Mfg: Advanced Power Components, Ltd.

   U.S. Office: Terry Manton, Inc.
   18 W. Pamrapo Court
   Glen Rock, NJ 07452
   Phone: 201-447-8821
   FAX: 201-670-4818

   European Office: Advanced Power Components, Ltd.
   47 Riverside Sir Thomas Longly Rd.
   Medway City Estate
   Strood, Rochester, Kent ME2 4DP
   ENGLAND
   Phone: 44-634-290588
   FAX: 44-634-290591

2. Part No.: T60403-L4097-X017-80 (Single Transformer)

   Mfg: VACUUMSCHMELZE (VAC)

   U.S. Office: VACUUMSCHMELZE
   186 Wood Avenue South
   Iselin, NJ 08830
   Phone: 908-494-3530
   FAX: 908-603-5994

   European Office: VACUUMSCHMELZE, GmbH
   V-G33, Mr. Heiko Gerberbauer
   37 Gruener Weg
   D-63450 Hanau
   GERMANY
   Phone: 49-6181-38-2026
   FAX: 49-6181-38-2780

3. Part No.: PE-68998 (Single Transformer)

   Mfg: Pulse Engineering, Inc.

   U.S. Office: Pulse Engineering, Inc.
   P.O. Box 12235
   San Diego, CA 92112
   Phone: 619-674-8100
   FAX: 619-674-8262

Note: The PE-68998 transformer has slightly higher dc resistance than the 2768A or 2776A. In T7250C or T7259 designs, this will lower the pulse height. To compensate for this, the sum total of the chip-side line interface resistors should be reduced by about 12 Ω. In other words, the sum of the values of the external resistors plus the relay contact resistance should be about 100 Ω. See Q4 and Q5 above.

For applications **not** requiring reinforced insulation:

1. Part No.: PE-65498 (Dual Transformer)

   Mfg: Pulse Engineering, Inc.

   U.S. Office: Pulse Engineering, Inc.
   P.O. Box 12235
   San Diego, CA 92112
   Phone: 619-674-8100
   FAX: 619-674-8262

Appendix B. Questions and Answers

(continued)

Programming/Register Features

Q7: If the T7250C is programmed to operate in the 2B+D grouped mode, can it still be used in a passive bus configuration?

A7: Yes.

Q8: What happens if INFO4 is being received and the line is disconnected?

A8: The device detects INFO0 and reports this to R1, bits 2 and 3, along with an interrupt in R10, bit 1 (if enabled by R9, bit 1). If auto activation is enabled (BR7, AAE = 1), INFO0 will be transmitted.

Q9: Can R0, bit 0 = 1 be read as an indicator of powerdown?

A9: No. If R0, bit 0 = 1 is written, the device will be placed in powerdown. However, an attempt to read any register brings the device out of powerdown; therefore, on any read, R0, bit 0 = 0.

Q10: Can the T7250C automatically recover from loss of frame?

A10: Frame recovery is always automatic. If the question is whether the device automatically activates, the answer is that it does, if BR7, AAE = 1.

Q11: In group mode, how are D bits dealt with?

A11: The system-side source of the D bits depends on BR6, B3 (GND). If GND = 1, the D bits come from the FIFO; if GND = 0, they come from TXB1. Through the FIFO (GND = 1), HDLC processing always occurs. D-channel transmission to RXDATA and from TXB1 (GND = 0) is transparent; i.e., with no HDLC processing.

Q12: Will the T7250C come out of powerdown mode if one of the registers is written to or read from?

A12: Yes. Any microprocessor access will cause the T7250C to power up. Note that if the T7250C is programmed for auto powerdown (APDA = 1; BR7 bit 6), and is powered up by a microprocessor access, it will not re-enter powerdown mode until either an INFO 0 to INFO 2/4 to INFO 0 sequence occurs or the microprocessor sets the powerdown bit (R0, bit 0). This occurs for both AAE = 1 or AAE = 0 (auto activation enabled/disabled).

Q13: If T7250C register BR8 is read from or written to (causing the device to come out of powerdown mode), then BR8, bit 5, PD = 1, which indicates that the chip is still powered down (but it is not). Please explain.

A13: BR8, bit 5 is the powerdown status indicator and is programmed only by the T7250C. If the device goes into powerdown, this bit is set. A read to this (or any) register will bring the device out of powerdown, but the bit will still be set. This bit is cleared after the read; therefore, a second read will result in BR8, bit 5 = 0 (powerup). This bit functions the same for both AAE = 1 or AAE = 0 (auto activation enabled/disabled).

Q14: During conformance testing, an issue was raised that the T7250C, when configured for auto-activation, sends data in the INFO3 stream when responding to an INFO2 pattern from the NT. This appears to be a CTS2 conformance issue.

A14: The T7250C will allow operational data (from the system interface TXB1/2 pins) to be sent after INFO2 has been identified during the transmission of INFO3. The ETSI and ANSI specifications do not disallow this action; however, some testing organizations may insist that the TE not send any operational data until the INFO4 pattern is received from the NT, indicating that the network is ready to receive data. In order to satisfy these requirements, the T7250C may be programmed to send all 1s in the B channels (T1B1/T1B2 bits must be set to 1 in Register 12, bits 6 and 7) prior to the reception of INFO4. Another way to ensure that no operational data is being sent on the B channels is to force the inputs of pins 5 and 6 (TXB1/2) to be a logical 1 prior to the reception of INFO4.

Appendix B. Questions and Answers

(continued)

Applications

Q15: In order to build an NT2, the T7250C will be used on the network end in the 2B+D grouped mode and connected directly to the T7252 on the other side. Then FSEB1 from the T7250C becomes the FS pulse into the T7252. Is this acceptable?

A15: Not directly. FSEB1 and FSEB2 are retimed by the T7250C to line up with CKCOD (so that clocks into a codec will be synchronous). However, since CKCOD and FS come from different sources (a countdown of a crystal and the network, respectively), FSEB1 will have one CKCOD clock period of extra jitter (488 µs). This already exceeds the NT limit of 5% and is in addition to the jitter from the network and the DPLL of the T7250C. Therefore, for the desired results, FS will have to be passed through another narrow-band PLL before passing it to the T7252 (a low-pass filter of a few tens of Hz should work).

Q16: Does T7250C work in an eight TE passive bus arrangement?

A16: Yes.

Timing

Q17: The FSEB1 and FSEB2 signals are disabled when INFO0 is received. What about CKCOD, MCKB1, CKB2, and CKDM? Are there any other important relationships for these signals?

A17: FSEB1 and FSEB2 are phase-locked to the received signal from the network. They are disabled unless INFO2 or INFO4 is received or B-channel local loopbacks are enabled. They are clocked out of the T7250C by CKCOD.

CKCOD is a countdown of the free-running 6.144 MHz crystal, and is, therefore, also free-running. CKCOD is not affected by the received INFO state.

MCKB1 and CKB2 are phase-locked to the signal received from the network (when INFO2 or INFO4 are received) and are clocked out of the T7250C by CKCOD. If INFO 0 is received, these signals free run.

CKDM is phase-locked to the signal received from the network (when INFO2 or INFO4 are received) and is clocked out of the T7250C by a free-running 6.144 MHz clock. If INFO0 is received, this signal free runs.

Miscellaneous

Q18: Is power consumption affected by passive bus?

A18: No. The outputs are current sources, so the current drawn from the power supply is independent of loading.

Q19: Is TIMOUT (pin 42) tristated when it is just disabled?

A19: No.

Appendix C. Differences Between the T7250C and T7250B

The following sections describe the enhancements that the T7250C provides compared to the T7250B device.

New CTS2 Requirements

Recent developments in European 4-wire basic rate ISDN conformance testing (specifically CTS2) have introduced some new requirements for European compliance.

Frame Alignment

Once frame alignment with the NT is obtained, the T7250B does not lose framing if frames with the second bipolar violation missing, or outside of the ITU-T I.430 14-bit criterion, are received. Some European conformance test suites may send this type of frame and expect the TE to lose framing. The T7250C loss of framing algorithm conforms to this operation.

Analog Transceiver

The analog transmitter and receiver sections are modified to allow the use of a lower-capacitance transformer. This modification provides increased margins to the I.430 impedance templates, thus simplifying the design of external interface circuitry (surge protection, etc.).

New Transformer and Interface Circuitry

To accommodate the analog transceiver modifications, the T7250C uses a new transformer and different interface circuitry, as shown in Figure 10. The AT&T 2718AM transformer is replaced by the AT&T 2768A, which is a dual (both receive and transmit transformers are in the same package), through-hole design. The 2768A has center taps on the line side, but not on the chip side. For this reason, the receiver chip-side center tap capacitor recommended for T7250B designs is not used. Line-side center tap capacitors can be used to enhance common-mode rejection.

Appendix C. Differences Between the T7250C and T7250B (continued)

Standards EN60950 and EN41003 describe the safety requirements for equipment connected to telecommunications networks in Europe. Some interpretations of these standards may classify the S/T reference point as a TNV (telecommunications network voltage) circuit, indicating the presence of dangerous voltage. If so, isolation transformers used in terminal equipment would be required to isolate secondary circuitry from network voltages by using either basic or reinforced insulation (depending on other system characteristics as defined in EN60950). The insulation type used in the AT&T 2768A transformer is classified as operational insulation according to EN60950 and therefore may not meet safety requirements in some countries. In applications requiring reinforced insulation, the AT&T 2776A transformer should be used. Note that this is a single transformer design; therefore, two are required.

Enhanced HDLC Abort Response

The D-channel HDLC formatter has been modified to ensure proper response when an abort sequence is received.

Improved Data Tristate Time

The time to tristate the T7250C data pins (D[7:0]) after a microprocessor read has been reduced to 40 ns (maximum) to allow interfacing to higher-performance processors.

Pin Changes

To accommodate the changes to the analog front end of the T7250C, the location and function of three device pins has changed. These pin changes are summarized in Table 17. Also, the T7250C requires external capacitors from each of the two crystal oscillator pins to V_{SS1} (if a crystal is used). These external capacitors are not required when using the T7250B. The crystal requirements for the T7250C also differ from the T7250B and are given in Table 15.

Table 17. Signal Names and External Circuitry Requirements

Pin Number	T7250B	T7250C
22	VT: 0.1 µF capacitor to V_{SSR}	CSENS: 11.5 kΩ (±1.0%) resistor to V_{SSR}
3	REXT: 2.0 kΩ resistor to V_{DDT}	TPR: transmitter positive rail output
4	TPR: transmitter positive rail output	V_{REF}: 29.4 kΩ (±1.0%) resistor to V_{DDT}
9	XTALO: no external capacitor	XTALO: 39 pF (±5%) capacitor to V_{SS1} (if a crystal is used)
8	CK6/XTALI: no external capacitor	CK6/XTALI: 39 pF (±5%) capacitor to V_{SS1} (if a crystal is used)

Appendix D. Differences Between the T7250C-MC and T7250C-MC2

The following sections describe the enhancements that the T7250C-MC2 provides compared to the T7250C-MC device.

Passive Bus Contention Resolution

When the priority mechanism for passive bus is enabled, the T7250C-MC did not work according to ANSI or ETSI specifications without software intervention. When a mismatch (D-Echo bit error) occurs, the chip is supposed to reset its priority counter (the priority counter counts the consecutive D-Echo bits set to 1 and holds off retransmission on the D channel) until the count again reaches the correct priority level. When a mismatch occurred for the case of D-Echo errored by the NT sending a 1 mismatch (indicating a network error), the T7250C-MC did not reset its counter. The T7250C-MC2 corrected this problem.

Enhanced HDLC Abort Response

The D channel HDLC formatter has been modified to ensure proper response to **all** received abort sequences.

Interframe Fill

The T7250C-MC2 will not report interframe fill as short packets, it will instead ignore interframe fill as described in the HDLC formatter section of this document.

Powerdown Mode Power Consumption

The powerdown mode power consumption has been corrected from 20 mW to <15 mW.

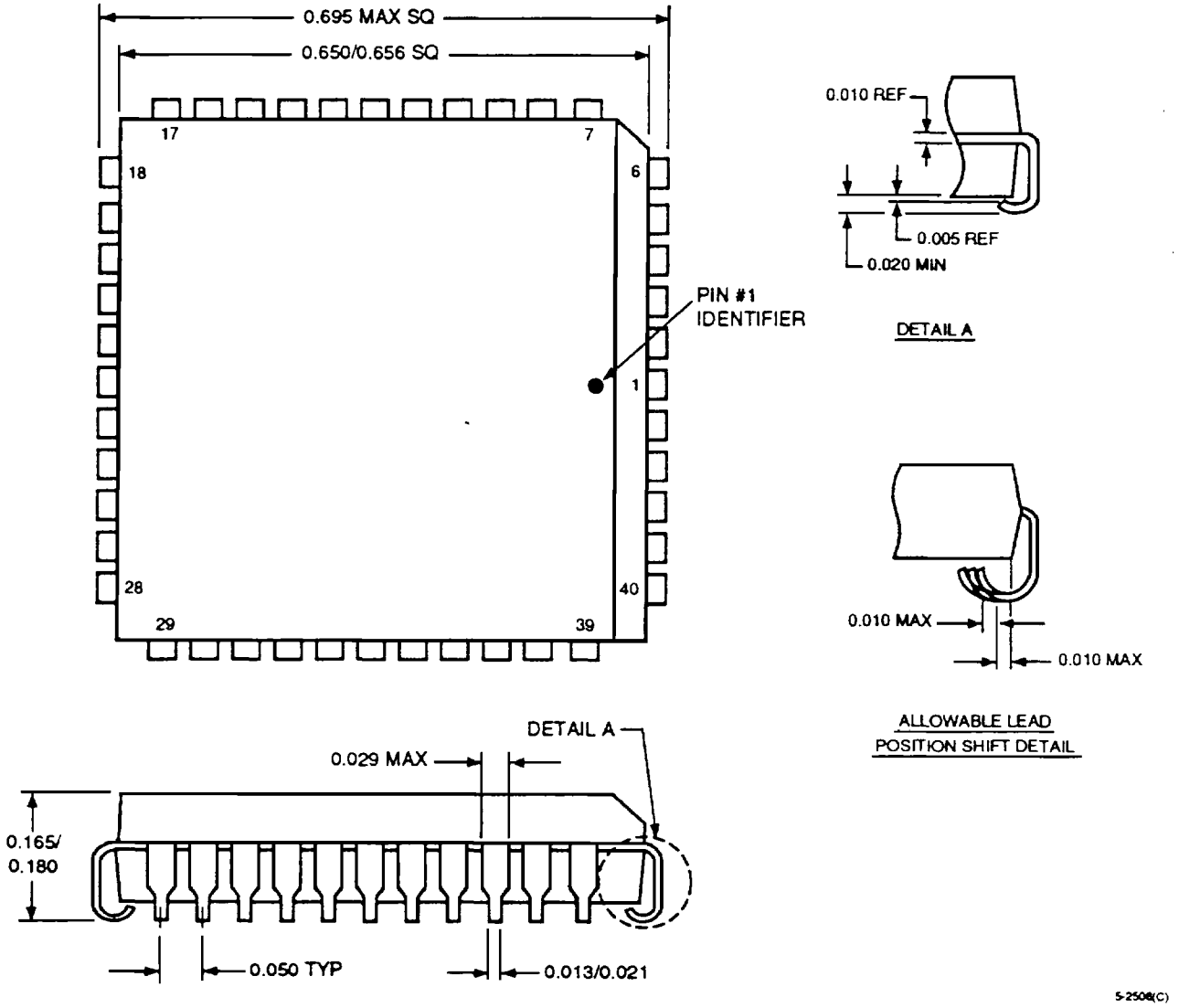
HDLC Receiver Status Byte Bad Byte Count Indicator Temperature Sensitivity

Under certain low-temperature situations, this bit will fail to assert on the T7250C-MC. This problem has been corrected in the T7250C-MC2 device.

Outline Diagrams

44-Pin PLCC

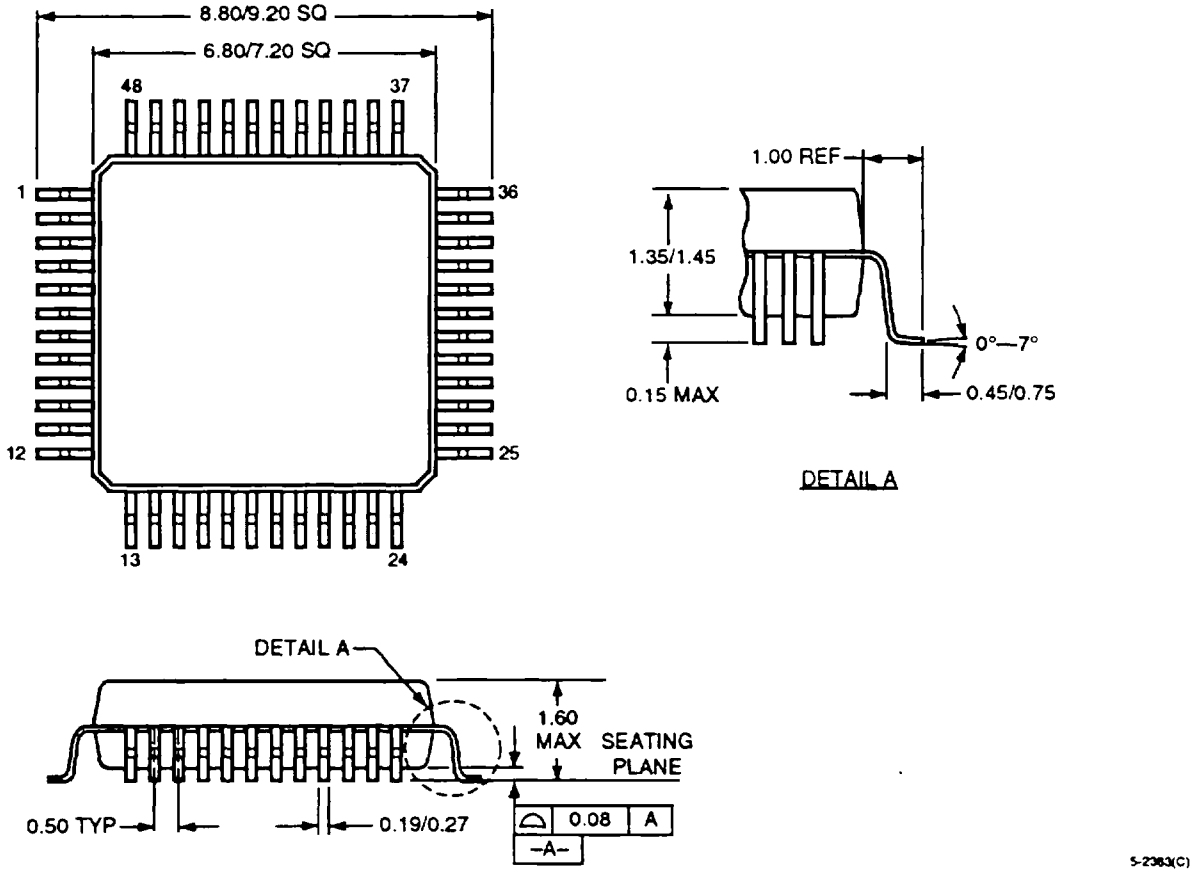
Controlling dimensions are in inches.



Outline Diagrams (continued)

48-Pin TQFP

Controlling dimensions are in millimeters.



Ordering Information

Device Code	Package	Temperature
T-7250C - - MC2	44-pin PLCC	0 °C to 70 °C
T-7250C - - TC2	48-pin TQFP	0 °C to 70 °C

References

[1] *Interfacing the* Motorola *MC68302 to the AT&T T7250C* Application Note (AP93-009TCOM)

[2] *Design of ISDN S/T Line Interface Circuitry Using the T7250C/T7259* Application Note (AP93-008TCOM)

[3] *PCMCIA Applications Using the T7250C* Technical Note (TN95-001TCOM)

Glossary

A[3:0]: Address bus input pins.

AAE: Auto activation enable control register bit (BR7, bit 7).

ANSI: American National Standards Institute.

APDA: Automatic powerdown allowed control register bit (BR7, bit 6).

ASI: Alternate space inversion line code format.

B1f: FSEB1 framing control register bit (R4, bit 4).

b1i: B1 data invert control register bit (R8, bit 7).

b1xb2: Exchange B1 with B2 control register bit (R8, bit 1).

B2f: FSEB2 framing control register bit (R4, bit 3).

b2i: B2 data invert control register bit (R8, bit 6).

BA: B available status register bit (BR8, bit 4).

BAIE: B available interrupt enable control register bit (BR7, bit 4).

BET: Broadcast enable TEI control register bit (BR6, bit 2).

Bb: B-channel data register (BR9).

Bg: Background register bank selection control register bit (R15, bit 5—7).

BRy: Background register y, where y is a number from 1—9 representing one of the ten background registers.

C1pol: MCKB1 clock polarity control register bit (R0, bit 3).

C2pol: CKB2 clock polarity control register bit (R0, bit 2).

CDM: Charged-device model.

CK6/XTALI: 6 MHz clock/crystal input pin.

CKB2: Clock for B2 channel output pin.

CKCOD: Codec clock output pin.

CKCOD: Clock for codec status register bit (BR8, bit 7).

Ckdm: D-channel clock multiplexer control register bit (R0, bit 1).

CKDM: D-channel clock output pin.

Clkmux: MCKB1 clock multiplexer control register bit (R4, bit 2).

clrmm: Clear mismatch control register bit (R8, bit 0).

Codec: Coder/decoder, typically used for analog-to-digital conversion or digital-to-analog conversion.

Codec1: FSEB1 timing option control register bit (R4, bit 7).

Codec2: FSEB2 timing option control register bit (R4, bit 6).

CRC: Cyclic redundancy check.

$\overline{CS}$: Chip select input pin.

CSENS: Current sense.

CTS2: Test requirements for Layer 1 Basic Access in Europe. Based on European Telecommunications Standard ETS 300 012 in concordance with ITU-T Recommendation I.430.

D[7:0]: Data bus I/O pins.

DARP: D address recognition on powerup control register bit (BR6, bit 0).

DBYTE: D-channel data register (R3).

DLCI: Data link connection identifier.

doneq: Q-nibble transmission done status register bit (R11, bit 5).

DSL: Digital subscriber loop.

Dynrd: Dynamic read control register bit (R0, bit 4).

ec[a:d]: ecd priority mechanism counter status register bits (R15, bits 0—3).

EDR: External XTALI drive control register bit (BR7, bit 3).

EMI: Electromagnetic interference.

enflg: Enable/flag for Q-channel transmission status register bit (R11, bit 4).

ENR: Enable receiver (D channel) (R2, bit 7).

ENT: Enable transmit (D channel) control register bit (R2, bit 6).

EOF: End-of-frame (D channel) status register bit (R5, bit 7).

ESD: Electrostatic discharge.

FIFO: A first-in/first-out memory used when it is necessary to read out information in the same order that it was written into memory.

FSEB1: Frame strobe or enable B1 output pin.

FSEB2: Frame strobe or enable B2 output pin.

G2BD: Grouped (2B+D) operation control register bit (BR8, bit 3).

GND: Grouped (2B+D), normal D control register bit (BR6, bit 3).

Glossary (continued)

HBM: Human-body model.

HDLC: High-Level Data Link Control. A standard data link communications protocol used for serial bit synchronous data transfer.

INFO: Information state defined by I.430.

INT: Interrupt output pin.

Ipol: Interrupt polarity control register bit (R4, bit 1).

ISDN: Integrated Services Digital Network. A universal communications network that handles voice, data, and video traffic in digital form. The major purpose of ISDN is to provide worldwide standards of user-to-network and network-to-network interfaces.

ITU-T: Consultative Committee for International Telephone and Telegraph.

llb1: Local loopback B1 channel control register bit (R12, bit 4).

llb2: Local loopback B2 channel control register bit (R12, bit 3).

lld: Local loopback D channel control register bit (R12, bit 5).

lpry: Low-priority status register bit (R8, bit 4).

MAP1: Match address pattern 1 data register (BR1).

MAP2: Match address pattern 2 data register byte (BR2).

MAP3: Match address pattern 3 data register byte (BR3).

MAP4: Match address pattern 4 data register byte (BR4).

MAP1S: Match address pattern 1 selection control register bits (BR5, bits 0 and 1).

MAP2S: Match address pattern 2 selection control register bits (BR5, bits 2 and 3).

MAP3S: Match address pattern 3 selection control register bits (BR5, bits 4 and 5).

MAP4S: Match address pattern 4 selection control register bits (BR5, bits 6 and 7).

MATBRx: Matched address pattern in register BRx (x = 1, 2, 3, 4) status register bit (BR6, bits 4—7).

MCKB1: 192 kHz master clock or B1 clock output pin.

mm: D-channel mismatch contention status register bit (R10, bit 0).

mmie: Mismatch interrupt enable control register bit (R9, bit 0).

Mres: Master reset control register bit (R15, bit 0).

mse: Multiframe synchronization established status register bit (R7, bit 7).

NT: Network Termination. The customer premises equipment that connects to the local phone line.

OVERRUN Overrun (D channel) status register bit (R5, bit 5).

PBS: Parallel access B-channel selection control register bit (BR8, bit 0).

PBTXB: Parallel read of B-channel status register bit (BR8, bit 6).

PD: Powerdown status register bit (BR8, bit 5).

PDIE: Powerdown interrupt enable control register bit (BR7, bit 5).

PDSC[1:0]: Powerdown system clock control register bit (BR7, bit 2 and 1).

ppm: Parts per million.

pry: Priority class control register bit (R8, bit 2).

prye: Priority enable control register bit (R8, bit 3).

Pwrdn: Powerdown control register bit (R0, bit 0).

$\overline{\text{PWRDN}}$: Powerdown status output pin.

qdata: Q-channel data register bits (R11, bits 0—3).

qdie: Q-done interrupt enable control register bit (R9, bit 2).

qdone: Q-channel transmission done status register bit (R10, bit 2).

qloop: Q-bit loop control register bit (R11, bit 6).

qse: Q-bit synchronization established status register bit (R11, bit 7).

r[1:0]: Previous received information pattern status register bit (R1, bit 1 and 0).

$\overline{\text{RD}}$: Read input pin.

Receive: Data from NT to TE.

REOF: Receive end-of-frame (D channel) status register bit (R10, bit 7).

REOFIE: Receive end-of-frame interrupt enable (D channel) control register bit (R9, bit 7).

RESET: Reset input pin.

RF: Receive full (D channel) status register bit (R10, bit 6).

Glossary (continued)

RFIE: Receive fill interrupt enable (D channel) control register bit (R9, bit 6).

RFL[3:0]: Receive fill interrupt trigger level (D channel) control register bits (R6, bits 7—4).

richg: Received INFO state changed status register bit (R10, bit 1).

richgie: Received information change interrupt enable control register bit (R9, bit 1).

RIDL: Receive idle (D channel) status register bit (R5, bit 6).

RINV: Invert received data (D channel) control register bit (R2, bit 5).

rlb1: Remote loopback B1 channel control register bit (R12, bit 1).

rlb2: Remote loopback B2 channel control register bit (R12, bit 0).

rld: Remote loopback D channel control register bit (R12, bit 2).

RPR: Receive positive rail input pin.

RNR: Receive negative rail input pin.

RQS[4:0]: Receive queue status (D channel) register bits (R5, bits 4—0).

RRES: Receiver reset (D-channel HDLC) control register bit (R15, bit 1).

rss[1:0]: Current received information pattern status register bits (R1, bits 3 and 2).

Rx: Register x, where x is a number from 0 to 15 to represent one of the sixteen foreground registers.

RXDATA: Receive data output pin that carries data received from the line.

SAPI: Service access point identifier.

SB[4:0]: S-channel data register bits (R7, bits 4—0).

SC[1:0]: System clock output frequency control register bit (BR8, bits 2—1).

SCHL: System clock high or low dc level control register bit (BR7, bit 0).

SCRM: SAPI command/response bit mask control register bit (BR6, bit 1).

ss: S-channel bits available status register bit (R10, bit 3).

ssie: S-channel interrupt enable control register bit (R9, bit 3).

ssm: S-channel state machine control register bit (R8, bit 5).

st[1:0]: Multiframe state machine status register bits (R7, bits 6 and 5).

Syscko: SYSCKO clock multiplexer control register bit (R4, bit 5).

SYSCKO: System clock output pin.

t1b2: Transmit 1s on B2 control register bit (R12, bit 6).

t1b1: Transmit 1s on B1 control register bit (R12, bit 7).

TABT: Transmit abort (D channel) control register bit (R2, bit 2).

TCRCB: Transmit bad CRC control register bit (R15, bit 4).

TDONE: Transmit done (D channel) status register bit (R10, bit 4).

TDIE: Transmit done interrupt enable (D channel) control register bit (R9, bit 4).

TE: Depending on the context, TE either means terminal endpoint (see description), or it refers to the TE register bit, which is the transmit empty (D channel) status register bit (R10, bit 5).

Terminal Endpoint. A telephone, computer terminal, or other equipment used on ISDN.

TEI: Terminal endpoint identifier.

TEIE: Transmit empty interrupt enable (D channel) control register bit (R9, bit 5).

TEL[3:0]: Transmit empty interrupt trigger level (D channel) control register bits (R6, bits 3—0).

TFC: Transmit frame complete (D channel) control register bit (R2, bit 3).

Tim[3:0]: Timer offset control register bits (R13, bits 3—0).

TIMOUT: Timer time-out output pin.

TINV: Transmit inverted data (D channel) control register bit (R2, bit 4).

Tm[3:0]: Timer mode control register bit (R13, bits 7—4).

TNR: Transmit negative rail output pin.

Tpol: Time-out polarity control register bit (R4, bit 0).

TPR: Transmit positive rail output pin.

TQS[4:0] HDLC Transmit queue status register bit (R14, bit 4—0).

TRES: Transmitter reset (D-channel HDLC) control register bit (R15, bit 2).

Glossary (continued)

Transmit: Data from TE to NT.

tss[1:0]: Transmit INFO pattern (To NT) control register bit (R2, bits 1 and 0).

TXB1: Transmit B1 input pin.

TXB2: Transmit B2 input pin.

TXD: Internal transmit D-channel serial data output pin.

UNDABT: Underrun abort (D channel) status register bit (R14, bit 5).

V_{DD}: 5 V supply (digital) pin.

V_{DDT}: 5 V supply (transmitter) pin.

V_{DDR}: 5 V analog supply (receiver) pin.

V_{SS1}: Digital ground 1 pin.

V_{SS2}: Digital ground 2 pin.

V_{SSR}: Analog ground (receiver) pin.

$\overline{WR}$: Write input pin.

XTALO: Crystal out pin.

Index

Index (continued)

Index (continued)

T

U

V

W

X

Notes

Notes

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June 1995
DS95-029ISDN (Replaces DS93-022TCOM and AY94-017TCOM)

AT&T Microelectronics