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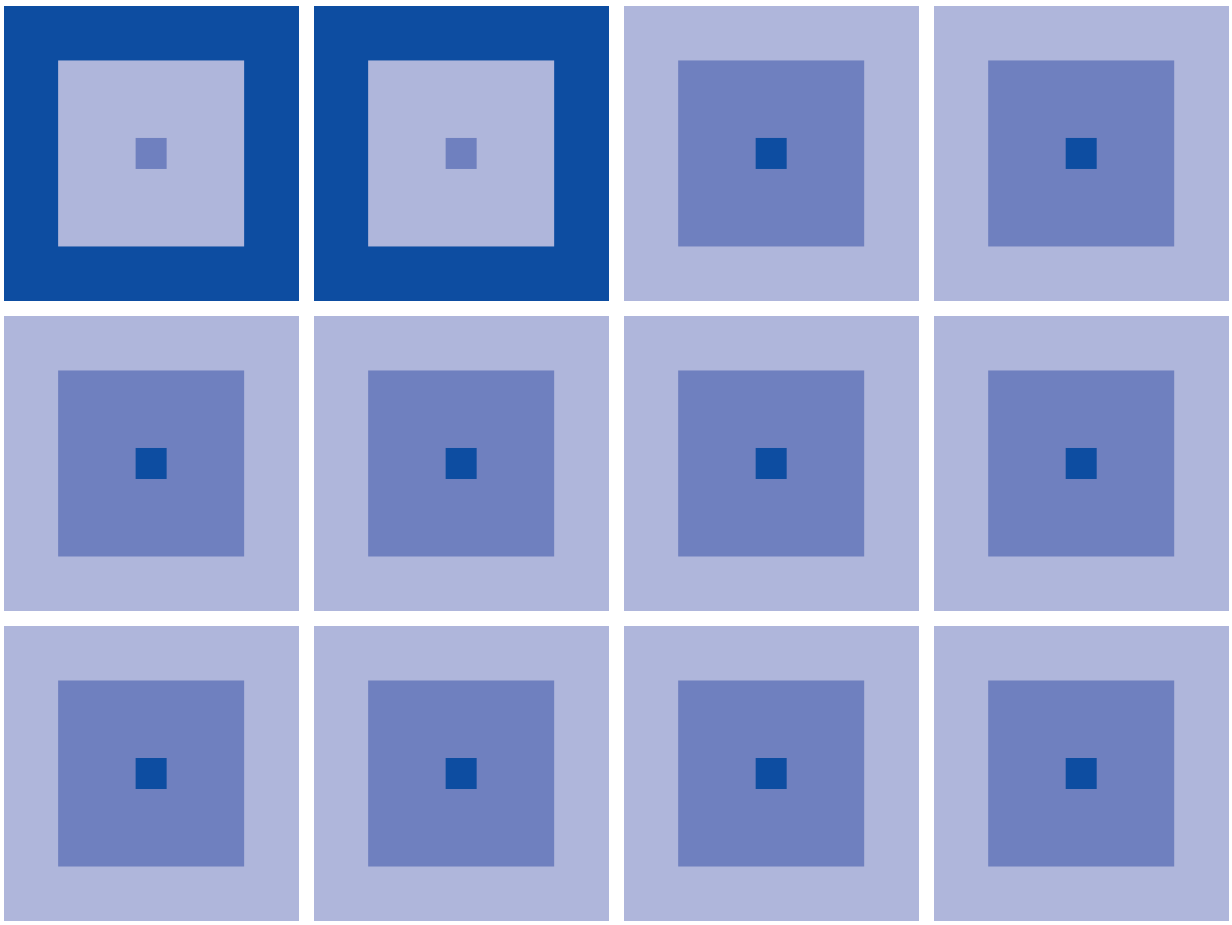
CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

S1C63808

Technical Manual



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Configuration of product number

Devices

S1 C 63158 F 0A01 00

Packing specifications
- 00 : Besides tape & reel
- 0A : TCP BL 2 directions
- 0B : Tape & reel BACK
- 0C : TCP BR 2 directions
- 0D : TCP BT 2 directions
- 0E : TCP BD 2 directions
- 0F : Tape & reel FRONT
- 0G : TCP BT 4 directions
- 0H : TCP BD 4 directions
- 0J : TCP SL 2 directions
- 0K : TCP SR 2 directions
- 0L : Tape & reel LEFT
- 0M : TCP ST 2 directions
- 0N : TCP SD 2 directions
- 0P : TCP ST 4 directions
- 0Q : TCP SD 4 directions
- 0R : Tape & reel RIGHT
- 99 : Specs not fixed

Specification

Package
[D: die form; F: QFP, B: BGA]

Model number

Model name
[C: microcomputer, digital products]

Product classification
[S1: semiconductor]

Development tools

S5U1 C 63000 A1 1 00

Packing specifications
[00: standard packing]

Version
[1: Version 1]

Tool type
- Hx : ICE
- Ex : EVA board
- Px : Peripheral board
- Wx : Flash ROM writer for the microcomputer
- Xx : ROM writer peripheral board
- Cx : C compiler package
- Ax : Assembler package
- Dx : Utility tool by the model
- Qx : Soft simulator

Corresponding model number
[63000: common to S1C63 Family]

Tool classification
[C: microcomputer use]

Product classification
[S5U1: development tool for semiconductor products]

CONTENTS

CHAPTER 1 OUTLINE

The S1C63808 is a microcomputer which has a high-performance 4-bit CPU S1C63000 as the core CPU, ROM (8,192 words × 13 bits), RAM (2,048 words × 4 bits), multiply-divide circuit, serial interface (2 ports), watchdog timer, programmable timer, time base counters (2 systems), and sound generator built-in. The S1C63808 features low current consumption, this makes it suitable for battery driven portable equipment such as clocks and watches.

1.1 Features

OSC1 oscillation circuit	32.768 kHz (Typ.) crystal oscillation circuit
OSC3 oscillation circuit	4 MHz (Typ.) ceramic, 1.1 MHz (Typ.) CR (external R) or 200 kHz (Typ.) CR (built-in R) oscillation circuit (∗1)
Instruction set	Basic instruction: 46 types (411 instructions with all) Addressing mode: 8 types
Instruction execution time	During operation at 32.768 kHz: 61 µsec 122 µsec 183 µsec During operation at 4 MHz: 0.5 µsec 1 µsec 1.5 µsec
ROM capacity	Code ROM: 8,192 words × 13 bits
RAM capacity	Data memory: 2,048 words × 4 bits
Input port	8 bits (Pull-down resistors may be supplemented ∗1)
Output port	8 bits (It is possible to switch the 3 bits to special output ∗2)
I/O port	20 bits (It is possible to switch the 8 bits to serial I/F input/output ∗2)
Serial interface	2 ports(Clock synchronous system or asynchronous system with LSB first or MSB first transfer selectable ∗2)
Time base counter	Clock timer Stopwatch timer (1/1000 sec, with direct key input function)
Programmable timer	8 bits × 2 ch. or 16 bits × 1 ch. with event counter function (K13) (∗2)
Watchdog timer	Built-in
Sound generator	With envelope and 1-shot output functions
Multiply-divide circuit	8-bit accumulator × 1 ch. Multiplication: 8 bits × 8 bits → 16-bit product Division: 16 bits ÷ 8 bits → 8-bit quotient and 8-bit remainder
Supply voltage detection (SVD) circuit	8 criteria voltages (1.05–1.50 V or 1.70–2.90 V are selectable ∗2)
EPD driver IC power supply circuit	V_{C1} = 1.03–1.23 V (∗2), $V_{C2} = 2V_{C1}$, $V_{C3} = 3V_{C1}$ (1/3 bias ∗1) or V_{C1} = 1.08–1.84 V (∗2), $V_{C2} = 2V_{C1}$, $V_{C3} = V_{SS}$ (1/2 bias ∗1)
External interrupt	Input port interrupt: 2 systems
Internal interrupt	Clock timer interrupt: 4 systems Stopwatch timer interrupt: 4 systems Programmable timer interrupt: 2 systems Serial interface interrupt: 6 systems
Power supply voltage	1.0 to 3.6 V (when CR (built-in R) oscillation circuit is selected) 2.1 to 3.6 V (when CR (external R) or ceramic oscillation circuit is selected)
Operating temperature range	-20 to 70°C
Current consumption (Typ.)	Low-speed operation (OSC1 = 32 kHz crystal oscillation, EPD driver IC power supply OFF): During HALT 3.0 V 0.23 µA During operation 3.0 V 1.90 µA High-speed operation (OSC3, EPD driver IC power supply ON): During operation (4 MHz) 3.0 V 850 µA
Package	QFP13-64pin (plastic) or chip

∗1: Can be selected with mask option ∗2: Can be selected with software

1.2 Block Diagram

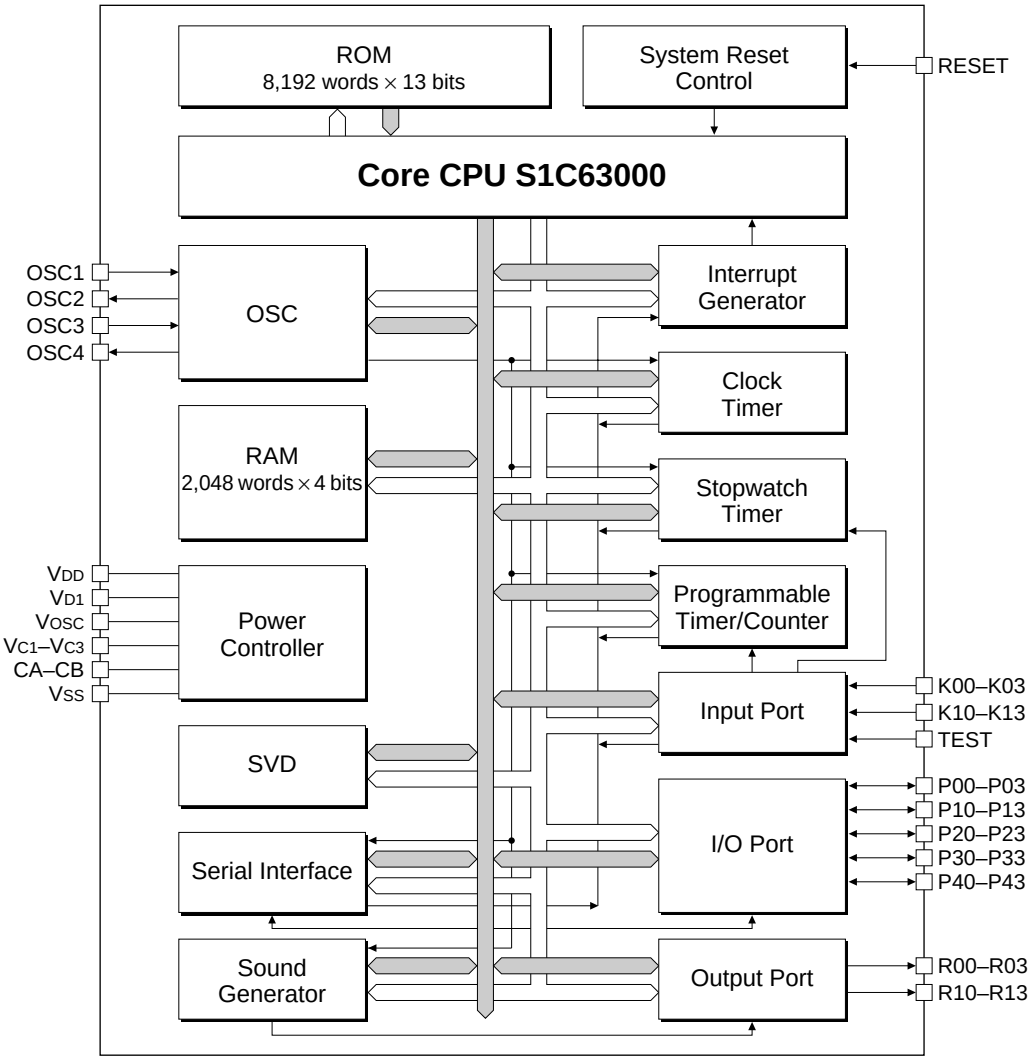
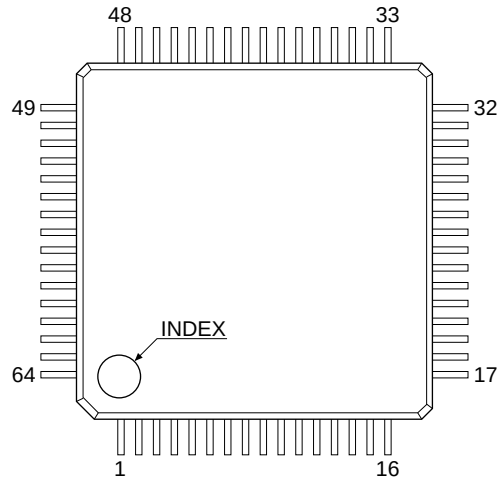


Fig. 1.2.1 Block diagram

1.3 Pin Layout Diagram

QFP13-64pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	N.C.	17	P42	33	V_{C2}	49	N.C.
2	P10/SIN1	18	P43	34	V_{C3}	50	N.C.
3	P11/SOUT1	19	TEST	35	CB	51	N.C.
4	P12/SCLK1	20	RESET	36	CA	52	V_{SS}
5	P13/SRDY1	21	N.C.	37	K00	53	R00
6	P20/SIN2	22	V_{DD}	38	K01	54	R01/BZ
7	P21/SOUT2	23	V_{OSC}	39	K02	55	R02/TOUT
8	P22/SCLK2	24	OSC1	40	K03	56	R03/FOUT
9	P23/SRDY2	25	OSC2	41	K10	57	R10
10	P30	26	V_{D1}	42	K11	58	R11
11	P31	27	OSC3	43	K12	59	R12
12	P32	28	OSC4	44	K13	60	R13
13	P33	29	V_{SS}	45	N.C.	61	P00
14	P40	30	V_{C1}	46	N.C.	62	P01
15	P41	31	N.C.	47	V_{DD}	63	P02
16	N.C.	32	N.C.	48	N.C.	64	P03

N.C. : No Connection

Fig. 1.3.1 Pin layout diagram (QFP13-64pin)

1.4 Pin Description

Table 1.4.1 Pin description

Pin name	Pin No.	I/O	Function
V_{DD}	22, 47	–	Power (+) supply pin
V_{SS}	29, 52	–	Power (–) supply pin
V_{D1}	26	–	Internal logic system regulated voltage output pin
V_{OSC}	23	–	Oscillation system regulated voltage output pin
V_{C1}–V_{C3}	30, 33, 34	–	EPD system power supply pins
CA, CB	36, 35	–	EPD system voltage booster capacitor connecting pins
OSC1	24	I	Crystal oscillation input pin
OSC2	25	O	Crystal oscillation output pin
OSC3	27	I	Ceramic or CR oscillation input pin (selected by mask option)
OSC4	28	O	Ceramic or CR oscillation output pin (selected by mask option)
K00–K03	37–40	I	Input port pins
K10–K13	41–44	I	Input port pins
R00	53	O	Output port pin
R01	54	O	Output port or BZ output pin (selected by software)
R02	55	O	Output port or TOUT output pin (selected by software)
R03	56	O	Output port or FOUT output pin (selected by software)
R10–R13	57–60	O	Output port pins
P00–P03	61–64	I/O	I/O port pins
P10	2	I/O	I/O port or serial I/F 1 data input pin (selected by software)
P11	3	I/O	I/O port or serial I/F 1 data output pin (selected by software)
P12	4	I/O	I/O port or serial I/F 1 clock I/O pin (selected by software)
P13	5	I/O	I/O port or serial I/F 1 ready signal output pin (selected by software)
P20	6	I/O	I/O port or serial I/F 2 data input pin (selected by software)
P21	7	I/O	I/O port or serial I/F 2 data output pin (selected by software)
P22	8	I/O	I/O port or serial I/F 2 clock I/O pin (selected by software)
P23	9	I/O	I/O port or serial I/F 2 ready signal output pin (selected by software)
P30–P33	10–13	I/O	I/O port pins
P40–P43	14, 15, 17, 18	I/O	I/O port pins
RESET	20	I	Initial reset input pin
TEST	19	I	Testing input pin

1.5 Mask Option

Mask options shown below are provided for the S1C63808. Several hardware specifications are prepared in each mask option, and one of them can be selected according to the application. The function option generator winfog, that has been prepared as the development software tool of S1C63808, is used for this selection. Mask pattern of the IC is finally generated based on the data created by winfog. Refer to the "S5U1C63000A Manual" for winfog.

<Outline of the mask option>

(1) OSC3 oscillation circuit

The OSC3 oscillator type can be selected from ceramic oscillation, CR oscillation (external R) and CR oscillation (built-in R). Refer to Section 4.3.3, "OSC3 oscillation circuit", for details.

(2) Input port pull-down resistor

The mask option is used to select whether the pull-down resistor is supplemented to the input ports Kxx or not. It is possible to select for each bit of the input ports.
Refer to Section 4.4.3, "Mask option", for details.

(3) RESET terminal pull-down resistor

The mask option is used to select whether the pull-down resistor is supplemented to the RESET terminal or not.
Refer to Section 2.2.1, "Reset terminal (RESET)", for details.

(4) I/O port pull-down resistor

The mask option is used to select whether the pull-down resistor working in the input mode is supplemented to the I/O ports Pxx or not. It is possible to select for each bit of the input ports.
Refer to Section 4.6.2, "Mask option", for details.

(5) Output specification of the output port

Either complementary output or P-channel open drain output can be selected as the output specification for the output ports Rxx. The selection is done in 1-bit units.
Refer to Section 4.5.2, "Mask option", for details.

(6) Output specification of the I/O port

For the output specification when the I/O ports Pxx are in the output mode, either complementary output or P-channel open drain output can be selected in 1-bit units.
Refer to Section 4.6.2, "Mask option", for details.

(7) External reset by simultaneous high input to the input port (K00–K03)

This function resets the IC when several keys are pressed simultaneously. The mask option is used to select whether this function is used or not. Further when the function is used, a combination of the input ports (K00–K03), which are connected to the keys to be pressed simultaneously, can be selected.
Refer to Section 2.2.2, "Simultaneous high input to terminals K00–K03", for details.

(8) Synchronous clock polarity in the serial interface

The polarity of the synchronous clock SCLKx and the SRDYx signal in slave mode of the serial interface is selected by mask option. Either positive polarity or negative polarity can be selected.
Refer to Section 4.10.2, "Mask option", for details.

(9) Bias in the EPD system voltage circuit

Either 1/2 bias or 1/3 bias can be selected to configure the outputs from the EPD system voltage circuit.
Refer to Section 4.14.2, "Mask option", for details.

<Option list>

The following is the option list for the S1C63808.
Multiple selections are available in each option item as indicated in the option list. Select the specifications that meet the target system and check the appropriate box. Be sure to record the specifications for unused functions too.

1. OSC3 SYSTEM CLOCK

☐ 1. Ceramic
☐ 2. CR (external R)
☐ 3. CR (built-in R)

2. INPUT PORT PULL DOWN RESISTOR

• K00	☐ 1. With Resistor	☐ 2. Gate Direct
• K01	☐ 1. With Resistor	☐ 2. Gate Direct
• K02	☐ 1. With Resistor	☐ 2. Gate Direct
• K03	☐ 1. With Resistor	☐ 2. Gate Direct
• K10	☐ 1. With Resistor	☐ 2. Gate Direct
• K11	☐ 1. With Resistor	☐ 2. Gate Direct
• K12	☐ 1. With Resistor	☐ 2. Gate Direct
• K13	☐ 1. With Resistor	☐ 2. Gate Direct

3. RESET PORT PULL DOWN RESISTOR

• RESET	☐ 1. With Resistor	☐ 2. Gate Direct

4. I/O PORT PULL DOWN RESISTOR

• P00	☐ 1. With Resistor	☐ 2. Gate Direct
• P01	☐ 1. With Resistor	☐ 2. Gate Direct
• P02	☐ 1. With Resistor	☐ 2. Gate Direct
• P03	☐ 1. With Resistor	☐ 2. Gate Direct
• P10	☐ 1. With Resistor	☐ 2. Gate Direct
• P11	☐ 1. With Resistor	☐ 2. Gate Direct
• P12	☐ 1. With Resistor	☐ 2. Gate Direct
• P13	☐ 1. With Resistor	☐ 2. Gate Direct
• P20	☐ 1. With Resistor	☐ 2. Gate Direct
• P21	☐ 1. With Resistor	☐ 2. Gate Direct
• P22	☐ 1. With Resistor	☐ 2. Gate Direct
• P23	☐ 1. With Resistor	☐ 2. Gate Direct
• P30	☐ 1. With Resistor	☐ 2. Gate Direct
• P31	☐ 1. With Resistor	☐ 2. Gate Direct
• P32	☐ 1. With Resistor	☐ 2. Gate Direct
• P33	☐ 1. With Resistor	☐ 2. Gate Direct
• P40	☐ 1. With Resistor	☐ 2. Gate Direct
• P41	☐ 1. With Resistor	☐ 2. Gate Direct
• P42	☐ 1. With Resistor	☐ 2. Gate Direct
• P43	☐ 1. With Resistor	☐ 2. Gate Direct

5. OUTPUT PORT OUTPUT SPECIFICATION

• R00	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• R01	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• R02	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• R03	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• R10	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• R11	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• R12	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• R13	☐ 1. Complementary	☐ 2. Pch-OpenDrain

6. I/O PORT OUTPUT SPECIFICATION

• P00	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• P01	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• P02	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• P03	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• P10	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• P11	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• P12	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• P13	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• P20	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• P21	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• P22	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• P23	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• P30	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• P31	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• P32	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• P33	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• P40	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• P41	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• P42	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• P43	☐ 1. Complementary	☐ 2. Pch-OpenDrain

7. MULTIPLE KEY ENTRY RESET COMBINATION

☐ 1. Not Use
☐ 2. Use (K00, K01)
☐ 3. Use (K00, K01, K02)
☐ 4. Use (K00, K01, K02, K03)

8. SERIAL INTERFACE POLARITY

☐ 1. Negative
☐ 2. Positive

9. EPD DRIVER IC POWER SUPPLY BIAS

☐ 1. 1/3 bias
☐ 2. 1/2 bias

CHAPTER 2 POWER SUPPLY AND INITIAL RESET

2.1 Power Supply

The S1C63808 operating power voltage is as follows:

Table 2.1.1 Operating voltage

OSC1 oscillation circuit	OSC3 oscillation circuit	Operating voltage
Crystal	CR (built-in R)	1.0 V to 3.6 V
	Ceramic or CR (external R)	2.1 V to 3.6 V

The S1C63808 operates by applying a single power supply within the above range between V_{DD} and V_{SS}. The S1C63808 generates the voltages necessary for all the internal circuits and exclusive EPD driver IC by the built-in power supply circuits shown in Table 2.1.2.

Table 2.1.2 Power supply circuits

Circuit	Power supply	Output voltage
OSC1 circuit	Voltage regulator for OSC1 oscillation circuit	V_{OSC}
OSC3 and internal circuits	Voltage regulator for internal logic circuit	V_{D1}
External EPD driver IC	EPD system voltage circuit	V_{C1}–V_{C3}

Notes:
- *Do not drive external loads with the output voltage from the internal power supply circuits except for the exclusive EPD driver IC.*
- *See Chapter 7, "Electrical Characteristics", for voltage values and drive capability.*

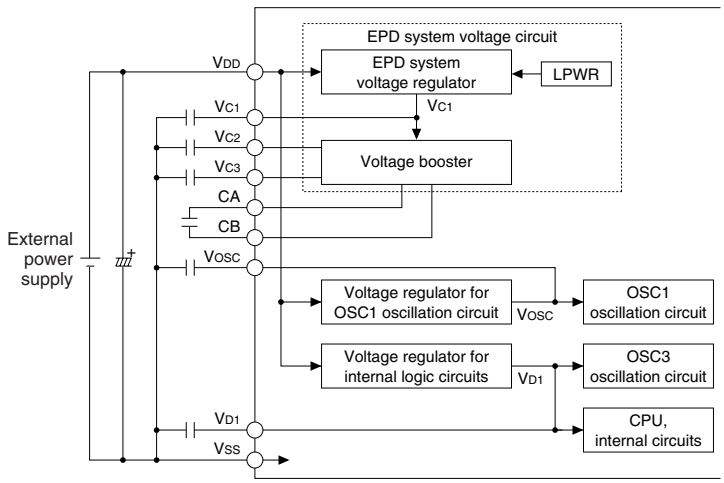


Fig. 2.1.1 Configuration of power supply

2.1.1 Voltage regulator for OSC1 oscillation circuit

This voltage regulator generates the V_{OSC} voltage for driving the OSC1 oscillation circuit and is provided separately with the voltage regulator for the internal logic system to stabilize the oscillation.

2.1.2 Voltage regulator for the internal logic system

This voltage regulator generates the V_{D1} voltage for driving the OSC3 oscillation circuit and the internal logic circuits.

2.1.3 EPD system voltage circuit

The EPD system voltage circuit generates the voltages for an EPD driver IC. This circuit allows the software to turn on and off. Turn this circuit on before starting display on the EPD. The EPD system voltage circuit generates V_{C1} with the voltage regulator built-in, and generates V_{C2} ($V_{C2} = 2V_{C1}$) and V_{C3} ($V_{C3} = 3V_{C1}$ for 1/3 bias, $V_{C3} = V_{SS}$ for 1/2 bias) by boosting V_{C1}. The V_{C1} voltage can be adjusted to 8 steps (1.03–1.23 V) for 1/3 bias or 16 steps (1.08–1.84 V) for 1/2 bias (bias can be selected by mask option). Refer to Section 4.14, "Power Supply for EPD Driver IC", for control of the EPD driver IC voltages.

2.2 Initial Reset

To initialize the S1C63808 circuits, initial reset must be executed. There are three ways of doing this.

(1) External initial reset by the RESET terminal
(2) External initial reset by simultaneous high input to terminals K00–K03 (mask option setting)
(3) Internal initial reset by the oscillation-detect circuit

When the power is turned on, be sure to initialize using the reset function (1) or (2). It is not guaranteed that the circuits are initialized by only turning the power on.

Figure 2.2.1 shows the configuration of the initial reset circuit.

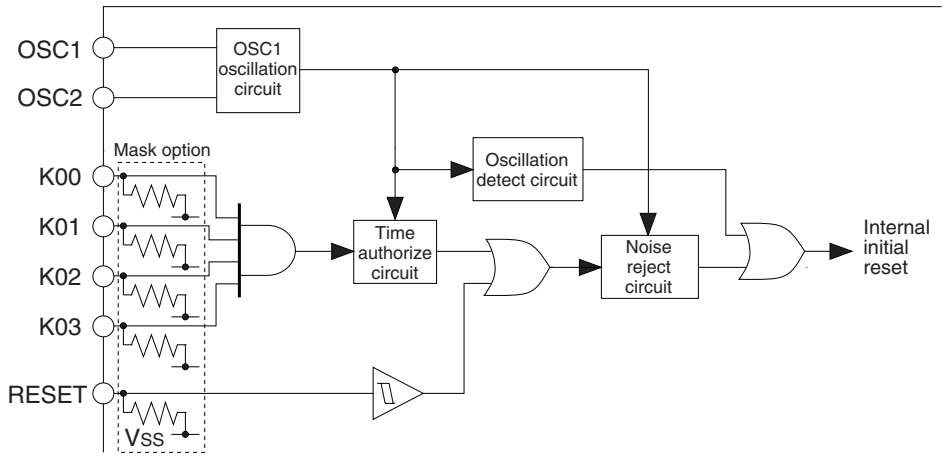


Fig. 2.2.1 Configuration of initial reset circuit

2.2.1 Reset terminal (RESET)

Initial reset can be executed externally by setting the reset terminal to a high level (V_{DD}). After that the initial reset is released by setting the reset terminal to a low level (V_{SS}) and the CPU starts operation. The reset input signal is maintained by the RS latch and becomes the internal initial reset signal. The RS latch is designed to be released by a 2 Hz signal (high) that is divided by the OSC1 clock. Therefore in normal operation, a maximum of 250 msec (when f_{OSC1} = 32.768 kHz) is needed until the internal initial reset is released after the reset terminal goes to low level. Be sure to maintain a reset input of 0.1 msec or more. However, when turning the power on, the reset terminal should be set at a high level as in the timing shown in Figure 2.2.1.1.
Note that a reset pulse shorter than 100 nsec is rejected as noise.

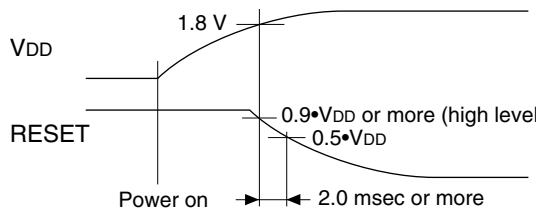


Fig. 2.2.1.1 Initial reset at power on

The reset terminal should be set to 0.9•V_{DD} or more (high level) until the supply voltage becomes 1.8 V or more.
After that, a level of 0.5•V_{DD} or more should be maintained more than 2.0 msec.

The reset terminal incorporates a pull-down resistor and a mask option is provided to select whether the resistor is used or not.

2.2.2 Simultaneous high input to terminals K00–K03

Another way of executing initial reset externally is to input a high signal simultaneously to the input ports (K00–K03) selected with the mask option.
Since this initial reset passes through the noise reject circuit, maintain the specified input port terminals at high level for at least 1.5 msec (when the oscillation frequency f_{OSC1} is 32.768 kHz) during normal operation. The noise reject circuit does not operate immediately after turning the power on until the oscillation circuit starts oscillating. Therefore, maintain the specified input port terminals at high level for at least 1.5 msec (when the oscillation frequency f_{OSC1} is 32.768 kHz) after oscillation starts.
Table 2.2.2.1 shows the combinations of input ports (K00–K03) that can be selected with the mask option.

Table 2.2.2.1 Combinations of input ports

1	Not use
2	K00∗K01
3	K00∗K01∗K02
4	K00∗K01∗K02∗K03

When, for instance, mask option 4 (K00∗K01∗K02∗K03) is selected, initial reset is executed when the signals input to the four ports K00–K03 are all high at the same time. When 2 or 3 is selected, the initial reset is done when a key entry including a combination of selected input ports is made.

Further, the reset circuit has incorporated a time authorize circuit that checks the input time of the simultaneous high input and performs initial reset if that time is the defined time (1 to 2 sec) or more.
If using this function, make sure that the specified ports do not go high at the same time during ordinary operation.

2.2.3 Oscillation-detect circuit

The oscillation-detect circuit outputs the initial reset signal at power-on until the OSC1 oscillation circuit starts oscillating, or when the OSC1 oscillation circuit stops oscillating for some reason.
However, for the initial reset at power-on, use a simultaneous high input of the input ports (K00–K03) or reset terminal, but do not execute it by this function alone.

2.2.4 Internal register at initial resetting

Initial reset initializes the CPU as shown in Table 2.2.4.1.
The registers and flags which are not initialized by initial reset should be initialized in the program if necessary.
In particular, the stack pointers SP1 and SP2 must be set as a pair because all the interrupts including NMI are masked after initial reset until both the SP1 and SP2 stack pointers are set with software.
When data is written to the EXT register, the E flag is set and the following instruction will be executed in the extended addressing mode. If an instruction which does not permit extended operation is used as the following instruction, the operation is not guaranteed. Therefore, do not write data to the EXT register for initialization only.
Refer to the "S1C63000 Core CPU Manual" for extended addressing and usable instructions.

Table 2.2.4.1 Initial values

CPU core			
Name	Symbol	Number of bits	Setting value
Data register A	A	4	Undefined
Data register B	B	4	Undefined
Extension register EXT	EXT	8	Undefined
Index register X	X	16	Undefined
Index register Y	Y	16	Undefined
Program counter	PC	16	0110H
Stack pointer SP1	SP1	8	Undefined
Stack pointer SP2	SP2	8	Undefined
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined
Interrupt flag	I	1	0
Extension flag	E	1	0
Queue register	Q	16	Undefined

Peripheral circuits		
Name	Number of bits	Setting value
RAM	4	Undefined
Display memory	4	Undefined
Other peripheral circuits	–	∗

∗ See Section 4.1, "Memory Map".

2.2.5 Terminal settings at initial resetting

The output port (R) terminals and I/O port (P) terminals are shared with special output terminals and input/output terminals of the serial interface. These functions are selected by the software. At initial reset, these terminals are set to the general purpose output port terminals and I/O port terminals. Set them according to the system in the initial routine. In addition, take care of the initial status of output terminals when designing a system.
Table 2.2.5.1 shows the list of the shared terminal settings.

Table 2.2.5.1 List of shared terminal settings

Terminal name	Terminal status at initial reset	Special output			Serial I/F		
		BZ	TOUT	FOUT	Async.	Clk-sync. Master	Clk-sync. Slave
R00	R00 (LOW output)	R00	R00	R00	R00	R00	R00
R01	R01 (LOW output)	BZ					
R02	R02 (LOW output)		TOUT				
R03	R03 (LOW output)			FOUT			
R10–R13	R10–R13 (LOW output)	R10–R13	R10–R13	R10–R13	R10–R13	R10–R13	R10–R13
P00–P03	P00–P03 (Input & pulled down*)	P00–P03	P00–P03	P00–P03	P00–P03	P00–P03	P00–P03
P10	P10 (Input & pulled down*)				SIN1(I)	SIN1(I)	SIN1(I)
P11	P11 (Input & pulled down*)				SOUT1(O)	SOUT1(O)	SOUT1(O)
P12	P12 (Input & pulled down*)				P12	SCLK1(O)	SCLK1(I)
P13	P13 (Input & pulled down*)				P13	P13	SRDY1(O)
P20	P20 (Input & pulled down*)				SIN2(I)	SIN2(I)	SIN2(I)
P21	P21 (Input & pulled down*)				SOUT2(O)	SOUT2(O)	SOUT2(O)
P22	P22 (Input & pulled down*)				P22	SCLK2(O)	SCLK2(I)
P23	P23 (Input & pulled down*)				P23	P23	SRDY2(O)
P30–P33	P30–P33 (Input & pulled down*)	P30–P33	P30–P33	P30–P33	P30–P33	P30–P33	P30–P33
P40–P43	P40–P43 (Input & pulled down*)	P40–P43	P40–P43	P40–P43	P40–P43	P40–P43	P40–P43

* When "With Pull-Down" is selected by mask option (high impedance when "Gate Direct" is selected)

For setting procedure of the functions, see explanations for each of the peripheral circuits.

2.3 Test Terminal (TEST)

This is the terminal used for the factory inspection of the IC. During normal operation, connect the TEST terminal to Vss.

CHAPTER 3 CPU, ROM, RAM

3.1 CPU

The S1C63808 has a 4-bit core CPU S1C63000 built-in as its CPU part.
Refer to the "S1C63000 Core CPU Manual" for the S1C63000.

Note: The SLP instruction cannot be used because the SLEEP operation is not assumed in the S1C63808.

3.2 Code ROM

The built-in code ROM is a mask ROM for loading programs, and has a capacity of 8,192 steps × 13 bits. The core CPU can linearly access the program space up to step FFFFH from step 0000H, however, the program area of the S1C63808 is step 0000H to step 1FFFH. The program start address after initial reset is assigned to step 0110H. The non-maskable interrupt (NMI) vector and hardware interrupt vectors are allocated to step 0100H and steps 0102H–010EH, respectively.

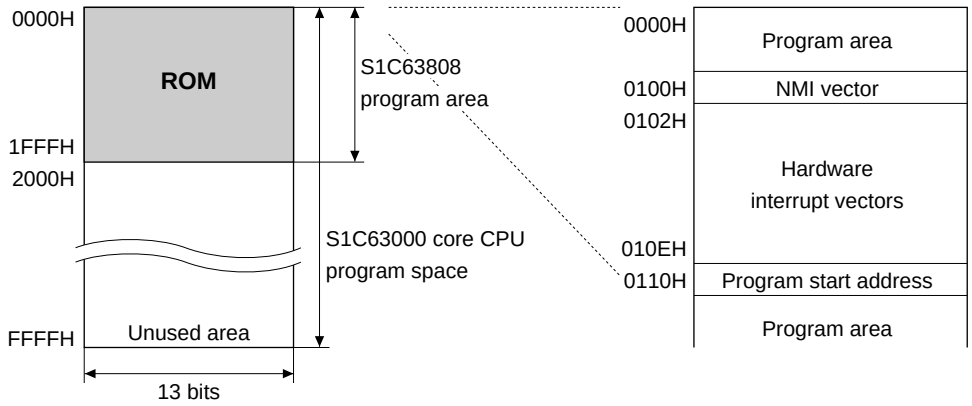


Fig. 3.2.1 Configuration of code ROM

3.3 RAM

The RAM is a data memory for storing various kinds of data, and has a capacity of 2,048 words × 4 bits. The RAM area is assigned to addresses 0000H to 07FFH on the data memory map. Addresses 0100H to 01FFH are 4-bit/16-bit data accessible areas and in other areas it is only possible to access 4-bit data. When programming, keep the following points in mind.

(1) Part of the RAM area is used as a stack area for subroutine call and register evacuation, so pay attention not to overlap the data area and stack area.

(2) The S1C63000 core CPU handles the stack using the stack pointer for 4-bit data (SP2) and the stack pointer for 16-bit data (SP1).
16-bit data are accessed in stack handling by SP1, therefore, this stack area should be allocated to the area where 4-bit/16-bit access is possible (0100H to 01FFH). The stack pointers SP1 and SP2 change cyclically within their respective range: the range of SP1 is 0000H to 03FFH and the range of SP2 is 0000H to 00FFH. Therefore, pay attention to the SP1 value because it may be set to 0200H or more exceeding the 4-bit/16-bit accessible range in the S1C63808 or it may be set to 00FFH or less. Memory accesses except for stack operations by SP1 are 4-bit data access.
After initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set by software. Further, if either SP1 or SP2 is re-set when both are set already, the interrupts including NMI are masked again until the other is re-set. Therefore, the settings of SP1 and SP2 must be done as a pair.

(3) Subroutine calls use 4 words (for PC evacuation) in the stack area for 16-bit data (SP1). Interrupts use 4 words (for PC evacuation) in the stack area for 16-bit data (SP1) and 1 word (for F register evacuation) in the stack area for 4-bit data.

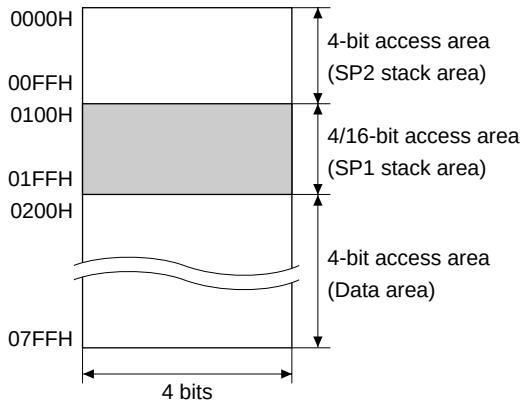


Fig. 3.3.1 Configuration of data RAM

CHAPTER 4 PERIPHERAL CIRCUITS AND OPERATION

The peripheral circuits of S1C63808 (timer, I/O, etc.) are interfaced with the CPU in the memory mapped I/O method. Thus, all the peripheral circuits can be controlled by accessing the I/O memory on the memory map using the memory operation instructions. The following sections explain the detailed operation of each peripheral circuit.

4.1 Memory Map

The S1C63808 data memory consists of 2,048-word RAM and 90-word peripheral I/O memory. Figure 4.1.1 shows the overall memory map of the S1C63808, and Table 4.1.1 the peripheral circuits' (I/O space) memory maps.

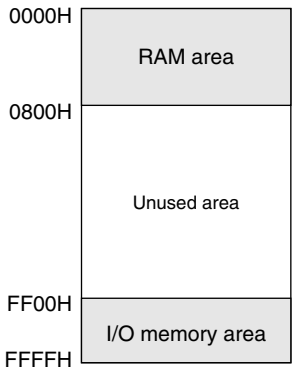


Fig. 4.1.1 Memory map

Note: Memory is not implemented in unused areas within the memory map. Further, some non-implementation areas and unused (access prohibition) areas exist in the peripheral I/O area. If the program that accesses these areas is generated, its operation cannot be guaranteed. Refer to the I/O memory maps shown in Table 4.1.1 for the peripheral I/O area.

Table 4.1.1 (a) I/O memory map (FF01H–FF20H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF01H	CLKCHG	OSCC	0	0	CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W		R		0 *3	– *2			Unused
					0 *3	– *2			Unused
FF04H	SVDCHG	SVDS2	SVDS1	SVDS0	SVDCHG	0	3.0 V	1.5 V	SVD voltage system selection
					SVDS2	0			SVD criteria voltage setting [SVDS2–0] 0 1 2 3 4 5 6 7; 1.5 V (V) 1.05 1.10 1.15 1.20 1.25 1.30 1.40 1.50; 3.0 V (V) 1.70 1.80 1.90 2.00 2.10 2.40 2.70 2.90
	R/W				SVDS1	0			
					SVDS0	0			
FF05H	0	0	SVDDT	SVDON	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	SVDDT	0	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off
FF06H	FOUTE	SWDIR	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT output enable
					SWDIR	0			Stopwatch direct input switch
									0: K00=Run/Stop, K01=Lap 1: K00=Lap, K01=Run/Stop
	R/W				FOFQ1	0			FOUT frequency selection [FOFQ1, 0] 0 1 2 3; Frequency fOSC1/64 fOSC1/8 fOSC1 fOSC3
					FOFQ0	0			
FF07H	0	0	WDEN	WDRST	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W	W	WDEN	1	Enable	Disable	Watchdog timer enable
					WDRST*3	Reset	Reset	Invalid	Watchdog timer reset (writing)
FF14H	0	SMD21	SMD20	ESIF2	0 *3	– *2			Unused
					SMD21	0			Serial I/F 2 mode selection [SMD21, 20] 0 1; Mode Clk-sync. master Clk-sync. slave; [SMD21, 20] 2 3; Mode Async. 7-bit Async. 8-bit
	R	R/W			SMD20	0			
					ESIF2	0	SIF	I/O	Serial I/F 2 enable (P2x port function selection)
FF15H	EPR2	PMD2	SCS21	SCS20	EPR2	0	Enable	Disable	Serial I/F 2 parity enable register
					PMD2	0	Odd	Even	Serial I/F 2 parity mode selection
	R/W				SCS21	0			Serial I/F 2 clock source [SCS21, 20] 0 1 2 3; Mode fOSC3/16 fOSC3/8 fOSC3/4 PT
					SCS20	0			
FF16H	RXTRG2	RXEN2	TXTRG2	TXEN2	RXTRG2	0	Run	Stop	Serial I/F 2 receive status (reading)
							Trigger	–	Serial I/F 2 receive trigger (writing)
					RXEN2	0	Enable	Disable	Serial I/F 2 receive enable
	R/W				TXTRG2	0	Run	Stop	Serial I/F 2 transmit status (reading)
							Trigger	–	Serial I/F 2 transmit trigger (writing)
					TXEN2	0	Enable	Disable	Serial I/F 2 transmit enable
FF17H	0	FER2	PER2	OER2	0 *3	– *2			Unused
					FER2	0	Error	No error	Serial I/F 2 framing error flag status (reading)
							Reset	–	Serial I/F 2 framing error flag reset (writing)
	R	R/W			PER2	0	Error	No error	Serial I/F 2 parity error flag status (reading)
							Reset	–	Serial I/F 2 parity error flag reset (writing)
					OER2	0	Error	No error	Serial I/F 2 overrun error flag status (reading)
							Reset	–	Serial I/F 2 overrun error flag reset (writing)
FF18H	TRXD23	TRXD22	TRXD21	TRXD20	TRXD23	– *2	High	Low	Serial I/F 2 transmit/receive data (low-order 4 bits)
					TRXD22	– *2	High	Low	
	R/W				TRXD21	– *2	High	Low	
					TRXD20	– *2	High	Low	LSB
FF19H	TRXD27	TRXD26	TRXD25	TRXD24	TRXD27	– *2	High	Low	MSB
					TRXD26	– *2	High	Low	Serial I/F 2 transmit/receive data (high-order 4 bits)
	R/W				TRXD25	– *2	High	Low	
					TRXD24	– *2	High	Low	
FF1AH	0	0	STPB2	SDP2	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		STPB2	0	2 bits	1 bit	Serial I/F 2 stop bit selection
					SDP2	0	MSB first	LSB first	Serial I/F 2 data input/output permutation selection
FF20H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
					SIK00	0	Enable	Disable	

Remarks

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.1.1 (b) I/O memory map (FF21H–FF44H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF21H	K03	K02	K01	K00	K03	– *2	High	Low	K00–K03 input port data
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
FF22H	KCP03	KCP02	KCP01	KCP00	KCP03	0	↓	↑	K00–K03 input comparison register
					KCP02	0	↓	↑	
	R/W				KCP01	0	↓	↑	
					KCP00	0	↓	↑	
FF24H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
					SIK12	0	Enable	Disable	
	R/W				SIK11	0	Enable	Disable	
					SIK10	0	Enable	Disable	
FF25H	K13	K12	K11	K10	K13	– *2	High	Low	K10–K13 input port data
					K12	– *2	High	Low	
	R				K11	– *2	High	Low	
					K10	– *2	High	Low	
FF26H	KCP13	KCP12	KCP11	KCP10	KCP13	0	↓	↑	K10–K13 input comparison register
					KCP12	0	↓	↑	
	R/W				KCP11	0	↓	↑	
					KCP10	0	↓	↑	
FF30H	R03HIZ	R02HIZ	R01HIZ	R00HIZ	R03HIZ	0	Hi-Z	Output	R03 (FOUTE=0)/FOUT (FOUTE=1) Hi-Z control
					R02HIZ	0	Hi-Z	Output	R02 (PTOUT=0)/TOUT (PTOUT=1) Hi-Z control
	R/W				R01HIZ	0	Hi-Z	Output	R01 (BZE=0)/BZ (BZE=1) Hi-Z control
					R00HIZ	0	Hi-Z	Output	R00 Hi-Z control
FF31H	R03	R02	R01	R00	R03	0	High	Low	R03 output port data (FOUTE=0) Fix at "1" when FOUT is used.
					R02	0	High	Low	R02 output port data (PTOUT=0) Fix at "1" when TOUT is used.
	R/W				R01	0	High	Low	R01 output port data (BZE=0) Fix at "1" when BZ is used.
					R00	0	High	Low	R00 output port data
FF32H	0	0	0	R1HIZ	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					R1HIZ	0	Hi-Z	Output	R10–R13 Hi-Z control
FF33H	R13	R12	R11	R10	R13	0	High	Low	R10–R13 output port data
					R12	0	High	Low	
	R/W				R11	0	High	Low	
					R10	0	High	Low	
FF40H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	P00–P03 I/O control register
					IOC02	0	Output	Input	
	R/W				IOC01	0	Output	Input	
					IOC00	0	Output	Input	
FF41H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	P00–P03 pull-down control register
					PUL02	1	On	Off	
	R/W				PUL01	1	On	Off	
					PUL00	1	On	Off	
FF42H	P03	P02	P01	P00	P03	– *2	High	Low	P00–P03 I/O port data
					P02	– *2	High	Low	
	R/W				P01	– *2	High	Low	
					P00	– *2	High	Low	
FF44H	IOC13	IOC12	IOC11	IOC10	IOC13	0	Output	Input	P13 I/O control register functions as a general-purpose register when SIF1 (slave) is selected
					IOC12	0	Output	Input	P12 I/O control register (ESIF1=0) functions as a general-purpose register when SIF1 is selected
	R/W				IOC11	0	Output	Input	P11 I/O control register (ESIF1=0) functions as a general-purpose register when SIF1 is selected
					IOC10	0	Output	Input	P10 I/O control register (ESIF1=0) functions as a general-purpose register when SIF1 is selected

Table 4.1.1 (c) I/O memory map (FF45H–FF51H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF45H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P13 pull-down control register functions as a general-purpose register when SIF1 (slave) is selected
					PUL12	1	On	Off	P12 pull-down control register (ESIF1=0) functions as a general-purpose register when SIF1 (master) is selected SCLK1 (I) pull-down control register when SIF1 (slave) is selected
	R/W				PUL11	1	On	Off	P11 pull-down control register (ESIF1=0) functions as a general-purpose register when SIF1 is selected
					PUL10	1	On	Off	P10 pull-down control register (ESIF1=0) SIN1 pull-down control register when SIF1 is selected
FF46H	P13	P12	P11	P10	P13	– *2	High	Low	P13 I/O port data functions as a general-purpose register when SIF1 (slave) is selected
					P12	– *2	High	Low	P12 I/O port data (ESIF1=0) functions as a general-purpose register when SIF1 is selected
	R/W				P11	– *2	High	Low	P11 I/O port data (ESIF1=0) functions as a general-purpose register when SIF1 is selected
					P10	– *2	High	Low	P10 I/O port data (ESIF1=0) functions as a general-purpose register when SIF1 is selected
FF48H	IOC23	IOC22	IOC21	IOC20	IOC23	0	Output	Input	P23 I/O control register functions as a general-purpose register when SIF2 (slave) is selected
					IOC22	0	Output	Input	P22 I/O control register (ESIF2=0) functions as a general-purpose register when SIF2 is selected
	R/W				IOC21	0	Output	Input	P21 I/O control register (ESIF2=0) functions as a general-purpose register when SIF2 is selected
					IOC20	0	Output	Input	P20 I/O control register (ESIF2=0) functions as a general-purpose register when SIF2 is selected
FF49H	PUL23	PUL22	PUL21	PUL20	PUL23	1	On	Off	P23 pull-down control register functions as a general-purpose register when SIF2 (slave) is selected
					PUL22	1	On	Off	P22 pull-down control register (ESIF2=0) functions as a general-purpose register when SIF2 (master) is selected SCLK2 (I) pull-down control register when SIF2 (slave) is selected
	R/W				PUL21	1	On	Off	P21 pull-down control register (ESIF2=0) functions as a general-purpose register when SIF2 is selected
					PUL20	1	On	Off	P20 pull-down control register (ESIF2=0) SIN2 pull-down control register when SIF2 is selected
FF4AH	P23	P22	P21	P20	P23	– *2	High	Low	P23 I/O port data functions as a general-purpose register when SIF2 (slave) is selected
					P22	– *2	High	Low	P22 I/O port data (ESIF2=0) functions as a general-purpose register when SIF2 is selected
	R/W				P21	– *2	High	Low	P21 I/O port data (ESIF2=0) functions as a general-purpose register when SIF2 is selected
					P20	– *2	High	Low	P20 I/O port data (ESIF2=0) functions as a general-purpose register when SIF2 is selected
FF4CH	IOC33	IOC32	IOC31	IOC30	IOC33	0	Output	Input	P30–P33 I/O control register
					IOC32	0	Output	Input	
	R/W				IOC31	0	Output	Input	
					IOC30	0	Output	Input	
FF4DH	PUL33	PUL32	PUL31	PUL30	PUL33	1	On	Off	P30–P33 pull-down control register
					PUL32	1	On	Off	
	R/W				PUL31	1	On	Off	
					PUL30	1	On	Off	
FF4EH	P33	P32	P31	P30	P33	– *2	High	Low	P30–P33 I/O port data
					P32	– *2	High	Low	
	R/W				P31	– *2	High	Low	
					P30	– *2	High	Low	
FF50H	IOC43	IOC42	IOC41	IOC40	IOC33	0	Output	Input	P40–P43 I/O control register
					IOC32	0	Output	Input	
	R/W				IOC31	0	Output	Input	
					IOC30	0	Output	Input	
FF51H	PUL43	PUL42	PUL41	PUL40	PUL43	1	On	Off	P40–P43 pull-down control register
					PUL42	1	On	Off	
	R/W				PUL41	1	On	Off	
					PUL40	1	On	Off	

Table 4.1.1 (d) I/O memory map (FF52H–FF6EH)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF52H	P43	P42	P41	P40	P43	– *2	High	Low	P40–P43 I/O port data
					P42	– *2	High	Low	
	R/W				P41	– *2	High	Low	
					P40	– *2	High	Low	
FF60H	0	0	0	LPWR	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					LPWR	0	On	Off	EPD driver power supply On/Off
FF62H	0	LC2	LC1	LC0	0 *3	– *2			Unused 1/3 bias
					LC2	0			V_{C1} voltage adjustment
	R	R/W			LC1	0			[LC2–0] 0 – 7
					LC0	0			Voltage Low – High
	LC3	LC2	LC1	LC0	LC3	0			V_{C1} voltage adjustment 1/2 bias
					LC2	0			[LC3–0] 0 – 15
	R/W				LC1	0			Voltage Low – High
					LC0	0			
FF64H	0	SMD11	SMD10	ESIF1	0 *3	– *2			Unused [SMD11, 10] 0 1
					SMD11	0			Serial I/F 1 mode selection Mode Clk-sync. master Clk-sync. slave
	R	R/W			SMD10	0			[SMD11, 10] 2 3
					ESIF1	0	SIF	I/O	Mode Async. 7-bit Async. 8-bit
									Serial I/F 1 enable (P1x port function selection)
FF65H	EPR1	PMD1	SCS11	SCS10	EPR1	0	Enable	Disable	Serial I/F 1 parity enable register
					PMD1	0	Odd	Even	Serial I/F 1 parity mode selection
	R/W				SCS11	0			Serial I/F 1 clock source [SCS11, 10] 0 1 2 3
					SCS10	0			Mode f_{OSC3}/16 f_{OSC3}/8 f_{OSC3}/4 PT
FF66H	RXTRG1	RXEN1	TXTRG1	TXEN1	RXTRG1	0	Run	Stop	Serial I/F 1 receive status (reading)
							Trigger	–	Serial I/F 1 receive trigger (writing)
					RXEN1	0	Enable	Disable	Serial I/F 1 receive enable
	R/W				TXTRG1	0	Run	Stop	Serial I/F 1 transmit status (reading)
							Trigger	–	Serial I/F 1 transmit trigger (writing)
					TXEN1	0	Enable	Disable	Serial I/F 1 transmit enable
FF67H	0	FER1	PER1	OER1	0 *3	– *2			Unused
					FER1	0	Error	No error	Serial I/F 1 framing error flag status (reading)
							Reset	–	Serial I/F 1 framing error flag reset (writing)
	R	R/W			PER1	0	Error	No error	Serial I/F 1 parity error flag status (reading)
							Reset	–	Serial I/F 1 parity error flag reset (writing)
					OER1	0	Error	No error	Serial I/F 1 overrun error flag status (reading)
							Reset	–	Serial I/F 1 overrun error flag reset (writing)
FF68H	TRXD13	TRXD12	TRXD11	TRXD10	TRXD13	– *2	High	Low	Serial I/F 1 transmit/receive data (low-order 4 bits)
					TRXD12	– *2	High	Low	
	R/W				TRXD11	– *2	High	Low	
					TRXD10	– *2	High	Low	LSB
FF69H	TRXD17	TRXD16	TRXD15	TRXD14	TRXD17	– *2	High	Low	MSB
					TRXD16	– *2	High	Low	Serial I/F 1 transmit/receive data (high-order 4 bits)
	R/W				TRXD15	– *2	High	Low	
					TRXD14	– *2	High	Low	
FF6AH	0	0	STPB1	SDP1	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		STPB1	0	2 bits	1 bit	Serial I/F 1 stop bit selection
					SDP1	0	MSB first	LSB first	Serial I/F 1 data input/output permutation selection
FF6CH	ENRTM	ENRST	ENON	BZE	ENRTM	0	1 sec	0.5 sec	Envelope releasing time selection
					ENRST*3	Reset	Reset	Invalid	Envelope reset (writing)
	R/W	W	R/W		ENON	0	On	Off	Envelope On/Off
					BZE	0	Enable	Disable	Buzzer output enable
FF6DH	0	BZSTP	BZSHT	SHTPW	0 *3	– *2			Unused
					BZSTP*3	0	Stop	Invalid	1-shot buzzer stop (writing)
					BZSHT	0	Trigger	Invalid	1-shot buzzer trigger (writing)
	R	W	R/W				Busy	Ready	1-shot buzzer status (reading)
					SHTPW	0	125 msec	31.25 msec	1-shot buzzer pulse width setting
FF6EH	0	BZFQ2	BZFQ1	BZFQ0	0 *3	– *2			Unused
					BZFQ2	0			Buzzer frequency selection [BZFQ2, 1, 0] 0 1 2 3
	R	R/W			BZFQ1	0			Frequency (Hz) 4096.0 3276.8 2730.7 2340.6
					BZFQ0	0			[BZFQ2, 1, 0] 4 5 6 7
									Frequency (Hz) 2048.0 1638.4 1365.3 1170.3

Table 4.1.1 (e) I/O memory map (FF6FH–FF85H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF6FH	0	BDTY2	BDTY1	BDTY0	0 *3	– *2			Unused
					BDTY2	0			Buzzer signal duty ratio selection (refer to main manual)
	R	R/W			BDTY1	0			
					BDTY0	0			
FF78H	0	0	TMRST	TMRUN	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		W	R/W	TMRST*3	Reset	Reset	Invalid	Clock timer reset (writing)
					TMRUN	0	Run	Stop	Clock timer Run/Stop
FF79H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
FF7AH	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
FF7BH	EDIR	DKM2	DKM1	DKM0	EDIR	0	Enable	Disable	Direct input enable
					DKM2	0			Key mask selection [DKM2, 1, 0] 0: Key mask None; 1: K02; 2: K02–03; 3: K02–03,10; [DKM2, 1, 0] 4: Key mask K10; 5: K10–11; 6: K10–12; 7: K10–13
	R/W				DKM1	0			
					DKM0	0			
FF7CH	LCURF	CRNWF	SWRUN	SWRST	LCURF	0	Request	No	Lap data carry-up request flag
					CRNWF	0	Renewal	No	Capture renewal flag
	R		R/W	W	SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
					SWRST*3	Reset	Reset	Invalid	Stopwatch timer reset (writing)
FF7DH	SWD3	SWD2	SWD1	SWD0	SWD3	0			Stopwatch timer data BCD (1/1000 sec)
					SWD2	0			
	R				SWD1	0			
					SWD0	0			
FF7EH	SWD7	SWD6	SWD5	SWD4	SWD7	0			Stopwatch timer data BCD (1/100 sec)
					SWD6	0			
	R				SWD5	0			
					SWD4	0			
FF7FH	SWD11	SWD10	SWD9	SWD8	SWD11	0			Stopwatch timer data BCD (1/10 sec)
					SWD10	0			
	R				SWD9	0			
					SWD8	0			
FF80H	SR3	SR2	SR1	SR0	SR3	– *2			Source register (low-order 4 bits) LSB
					SR2	– *2			
	R/W				SR1	– *2			
					SR0	– *2			
FF81H	SR7	SR6	SR5	SR4	SR7	– *2			MSB Source register (high-order 4 bits)
					SR6	– *2			
	R/W				SR5	– *2			
					SR4	– *2			
FF82H	DRL3	DRL2	DRL1	DRL0	DRL3	– *2			Low-order 8-bit destination register (low-order 4 bits) LSB
					DRL2	– *2			
	R/W				DRL1	– *2			
					DRL0	– *2			
FF83H	DRL7	DRL6	DRL5	DRL4	DRL7	– *2			MSB Low-order 8-bit destination register (high-order 4 bits)
					DRL6	– *2			
	R/W				DRL5	– *2			
					DRL4	– *2			
FF84H	DRH3	DRH2	DRH1	DRH0	DRH3	– *2			High-order 8-bit destination register (low-order 4 bits) LSB
					DRH2	– *2			
	R/W				DRH1	– *2			
					DRH0	– *2			
FF85H	DRH7	DRH6	DRH5	DRH4	DRH7	– *2			MSB High-order 8-bit destination register (high-order 4 bits)
					DRH6	– *2			
	R/W				DRH5	– *2			
					DRH4	– *2			

Table 4.1.1 (f) I/O memory map (FF86H–FFE1H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF86H	NF	VF	ZF	CALMD	NF	0	Negative	Positive	Negative flag
					VF	0	Overflow	No	Overflow flag
					ZF	0	Zero	No	Zero flag
	R			R/W	CALMD	0	Run	Stop	Operation status (reading)
							Div.	Mult.	Calculation mode selection (writing)
FFC0H	MOD16	EVCNT	FCSEL	PLPOL	MOD16	0	16 bits	8 bits	16-bit mode selection
					EVCNT	0	Event ct.	Timer	Timer 0 counter mode selection
	R/W				FCSEL	0	With NR	No NR	Timer 0 function selection (for event counter mode)
					PLPOL	0	↑	↓	Timer 0 pulse polarity selection (for event counter mode)
FFC1H	CHSEL0	PTOUT	CKSEL1	CKSEL0	CHSEL0	0	Timer 1	Timer 0	TOUT output selection
					PTOUT	0	On	Off	TOUT output control
	R/W				CKSEL1	0	OSC3	OSC1	Prescaler 1 source clock selection
					CKSEL0	0	OSC3	OSC1	Prescaler 0 source clock selection
FFC2H	PTPS01	PTPS00	PTRST0	PTRUN0	PTPS01	0			Prescaler 0 division ratio selection [PTPS01, 00]: 0 / 1 / 2 / 3; Division ratio: 1/1 / 1/4 / 1/32 / 1/256
					PTPS00	0			
	R/W		W	R/W	PTRST0*3	– *2	Reset	Invalid	Timer 0 reset (reload)
					PTRUN0	0	Run	Stop	Timer 0 Run/Stop
FFC3H	PTPS11	PTPS10	PTRST1	PTRUN1	PTPS11	0			Prescaler 1 division ratio selection [PTPS11, 10]: 0 / 1 / 2 / 3; Division ratio: 1/1 / 1/4 / 1/32 / 1/256
					PTPS10	0			
	R/W		W	R/W	PTRST1*3	– *2	Reset	Invalid	Timer 1 reset (reload)
					PTRUN1	0	Run	Stop	Timer 1 Run/Stop
FFC4H	RLD03	RLD02	RLD01	RLD00	RLD03	0			MSB
					RLD02	0			Programmable timer 0 reload data (low-order 4 bits)
	R/W				RLD01	0			
					RLD00	0			LSB
FFC5H	RLD07	RLD06	RLD05	RLD04	RLD07	0			MSB
					RLD06	0			Programmable timer 0 reload data (high-order 4 bits)
	R/W				RLD05	0			
					RLD04	0			LSB
FFC6H	RLD13	RLD12	RLD11	RLD10	RLD13	0			MSB
					RLD12	0			Programmable timer 1 reload data (low-order 4 bits)
	R/W				RLD11	0			
					RLD10	0			LSB
FFC7H	RLD17	RLD16	RLD15	RLD14	RLD17	0			MSB
					RLD16	0			Programmable timer 1 reload data (high-order 4 bits)
	R/W				RLD15	0			
					RLD14	0			LSB
FFC8H	PTD03	PTD02	PTD01	PTD00	PTD03	0			MSB
					PTD02	0			Programmable timer 0 data (low-order 4 bits)
	R				PTD01	0			
					PTD00	0			LSB
FFC9H	PTD07	PTD06	PTD05	PTD04	PTD07	0			MSB
					PTD06	0			Programmable timer 0 data (high-order 4 bits)
	R				PTD05	0			
					PTD04	0			LSB
FFCAH	PTD13	PTD12	PTD11	PTD10	PTD13	0			MSB
					PTD12	0			Programmable timer 1 data (low-order 4 bits)
	R				PTD11	0			
					PTD10	0			LSB
FFCBH	PTD17	PTD16	PTD15	PTD14	PTD17	0			MSB
					PTD16	0			Programmable timer 1 data (high-order 4 bits)
	R				PTD15	0			
					PTD14	0			LSB
FFE0H	0	EISER2	EISTR2	EISRC2	0 *3	– *2			Unused
					EISER2	0	Enable	Mask	Interrupt mask register (Serial I/F 2 error)
	R	R/W			EISTR2	0	Enable	Mask	Interrupt mask register (Serial I/F 2 transmit completion)
					EISRC2	0	Enable	Mask	Interrupt mask register (Serial I/F 2 receive completion)
FFE1H	0	EISER1	EISTR1	EISRC1	0 *3	– *2			Unused
					EISER1	0	Enable	Mask	Interrupt mask register (Serial I/F 1 error)
	R	R/W			EISTR1	0	Enable	Mask	Interrupt mask register (Serial I/F 1 transmit completion)
					EISRC1	0	Enable	Mask	Interrupt mask register (Serial I/F 1 receive completion)

Table 4.1.1 (g) I/O memory map (FFE2H–FFF8H)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FFE2H	0	0	EIPT1	EIPT0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1)
					EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0)
FFE4H	0	0	0	EIK0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
FFE5H	0	0	0	EIK1	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
FFE6H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
FFE8H	EIRUN	EILAP	EISW1	EISW10	EIRUN	0	Enable	Mask	Interrupt mask register (Stopwatch direct RUN)
					EILAP	0	Enable	Mask	Interrupt mask register (Stopwatch direct LAP)
	R/W				EISW1	0	Enable	Mask	Interrupt mask register (Stopwatch timer 1 Hz)
					EISW10	0	Enable	Mask	Interrupt mask register (Stopwatch timer 10 Hz)
FFF0H	0	ISER2	ISTR2	ISRC2	0 *3	– *2	(R)	(R)	Unused
					ISER2	0	Yes	No	Interrupt factor flag (Serial I/F 2 error)
	R	R/W			ISTR2	0	(W)	(W)	Interrupt factor flag (Serial I/F 2 transmit completion)
					ISRC2	0	Reset	Invalid	Interrupt factor flag (Serial I/F 2 receive completion)
FFF1H	0	ISER1	ISTR1	ISRC1	0 *3	– *2	(R)	(R)	Unused
					ISER1	0	Yes	No	Interrupt factor flag (Serial I/F 1 error)
	R	R/W			ISTR1	0	(W)	(W)	Interrupt factor flag (Serial I/F 1 transmit completion)
					ISRC1	0	Reset	Invalid	Interrupt factor flag (Serial I/F 1 receive completion)
FFF2H	0	0	IPT1	IPT0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1)
					IPT0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0)
FFF4H	0	0	0	IK0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK0	0	Reset	Invalid	Interrupt factor flag (K00–K03)
FFF5H	0	0	0	IK1	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK1	0	Reset	Invalid	Interrupt factor flag (K10–K13)
FFF6H	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
					IT2	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R/W				IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 8 Hz)
					IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 32 Hz)
FFF8H	IRUN	ILAP	ISW1	ISW10	IRUN	0	(R)	(R)	Interrupt factor flag (Stopwatch direct RUN)
					ILAP	0	Yes	No	Interrupt factor flag (Stopwatch direct LAP)
	R/W				ISW1	0	(W)	(W)	Interrupt factor flag (Stopwatch timer 1 Hz)
					ISW10	0	Reset	Invalid	Interrupt factor flag (Stopwatch timer 10 Hz)

4.2 Watchdog Timer

4.2.1 Configuration of watchdog timer

The S1C63808 has a built-in watchdog timer that operates with a 256 Hz divided clock from the OSC1 as the source clock. The watchdog timer starts operating after initial reset, however, it can be stopped by the software. The watchdog timer must be reset cyclically by the software while it operates. If the watchdog timer is not reset in at least 3–4 seconds, it generates a non-maskable interrupt (NMI) to the CPU.
Figure 4.2.1.1 is the block diagram of the watchdog timer.

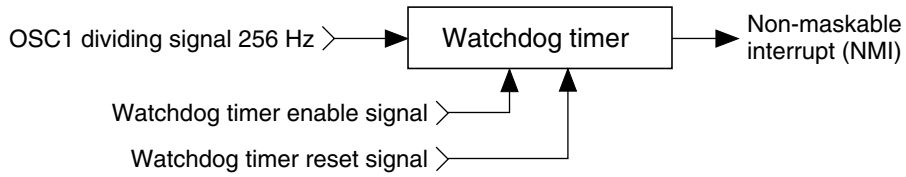


Fig. 4.2.1.1 Watchdog timer block diagram

The watchdog timer contains a 10-bit binary counter, and generates the non-maskable interrupt when the last stage of the counter (0.25 Hz) overflows.
Watchdog timer reset processing in the program's main routine enables detection of program overrun, such as when the main routine's watchdog timer processing is bypassed. Ordinarily this routine is incorporated where periodic processing takes place, just as for the timer interrupt routine.
The watchdog timer operates in the HALT mode. If a HALT status continues for 3–4 seconds, the non-maskable interrupt releases the HALT status.

4.2.2 Interrupt function

If the watchdog timer is not reset periodically, the non-maskable interrupt (NMI) is generated to the core CPU. Since this interrupt cannot be masked, it is accepted even in the interrupt disable status (I flag = "0"). However, it is not accepted when the CPU is in the interrupt mask state until SP1 and SP2 are set as a pair, such as after initial reset or during re-setting the stack pointer. The interrupt vector of NMI is assigned to 0100H in the program memory.

4.2.3 I/O memory of watchdog timer

Table 4.2.3.1 shows the I/O address and control bits for the watchdog timer.

Table 4.2.3.1 Control bits of watchdog timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF07H	0	0	WDEN	WDRST	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W	W	WDEN	1	Enable	Disable	Watchdog timer enable
					WDRST*3	Reset	Reset	Invalid	Watchdog timer reset (writing)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

WDEN: Watchdog timer enable register (FF07H•D1)

Selects whether the watchdog timer is used (enabled) or not (disabled).

When "1" is written: Enabled
When "0" is written: Disabled
Reading: Valid

When "1" is written to the WDEN register, the watchdog timer starts count operation. When "0" is written, the watchdog timer does not count and does not generate the interrupt (NMI).
At initial reset, this register is set to "1".

WDRST: Watchdog timer reset (FF07H•D0)

Resets the watchdog timer.

When "1" is written: Watchdog timer is reset
When "0" is written: No operation
Reading: Always "0"

When "1" is written to WDRST, the watchdog timer is reset and restarts immediately after that. When "0" is written, no operation results.
This bit is dedicated for writing, and is always "0" for reading.

4.2.4 Programming notes

(1) When the watchdog timer is being used, the software must reset it within 3-second cycles.

(2) Because the watchdog timer is set in operation state by initial reset, set the watchdog timer to disabled state (not used) before generating an interrupt (NMI) if it is not used.

4.3 Oscillation Circuit

4.3.1 Configuration of oscillation circuit

The S1C63808 has two oscillation circuits (OSC1 and OSC3). OSC1 is a crystal oscillation circuit that supplies the operating clock to the CPU and peripheral circuits. OSC3 is either a CR or a ceramic oscillation circuit. When processing with the S1C63808 requires high-speed operation, the CPU operating clock can be switched from OSC1 to OSC3 by the software. To stabilize operation of the internal circuits, the operating voltage must be switched according to the oscillation circuit to be used. Figure 4.3.1.1 is the block diagram of this oscillation system.

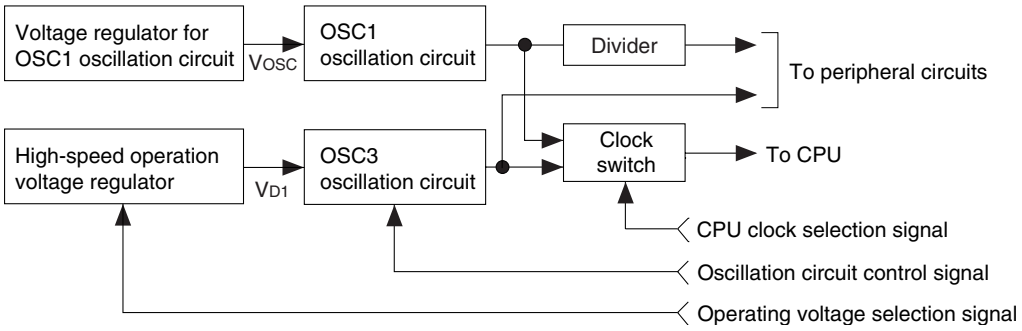


Fig. 4.3.1.1 Oscillation system block diagram

4.3.2 OSC1 oscillation circuit

The OSC1 crystal oscillation circuit generates the main clock for the CPU and the peripheral circuits. The oscillation frequency is 32.768 kHz (Typ.).
Figure 4.3.2.1 is the block diagram of the OSC1 oscillation circuit.

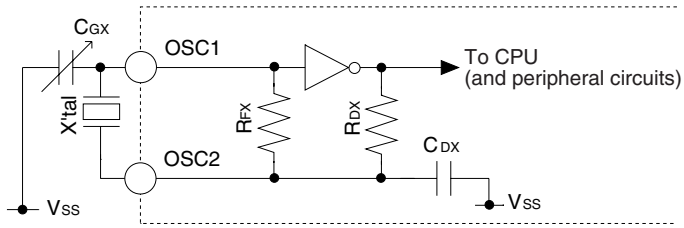


Fig. 4.3.2.1 OSC1 oscillation circuit

As shown in Figure 4.3.2.1, the crystal oscillation circuit can be configured simply by connecting the crystal oscillator (X'tal) of 32.768 kHz (Typ.) between the OSC1 and OSC2 terminals and the trimmer capacitor (C_{GX}) between the OSC1 and V_{SS} terminals.

4.3.3 OSC3 oscillation circuit

The S1C63808 has built-in the OSC3 oscillation circuit that generates the CPU's sub-clock (Max. 4.2 MHz) for high speed operation and the source clock for peripheral circuits needing a high speed clock (programmable timer, FOUT output). The mask option enables selection of the oscillator type from CR (external R type), CR (built-in R type) and ceramic oscillation circuit. When CR oscillation (external R type) is selected, only a resistance is required as an external element. When ceramic oscillation is selected, a ceramic oscillator and two capacitors (gate and drain capacitance) are required. When CR oscillation (built-in R type) is selected, no external element is required.
Figure 4.3.3.1 is the block diagram of the OSC3 oscillation circuit.

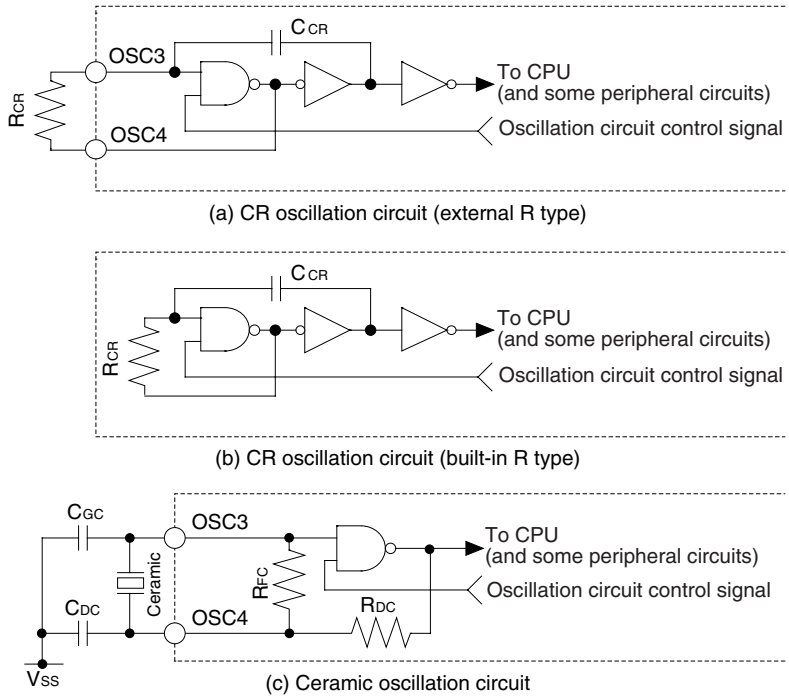


Fig. 4.3.3.1 OSC3 oscillation circuit

As shown in Figure 4.3.3.1, the CR oscillation circuit (external R type) can be configured simply by connecting the resistor RCR between the OSC3 and OSC4 terminals when CR oscillation is selected. See Chapter 7, "Electrical Characteristics" for resistance value of RCR.
When ceramic oscillation is selected, the ceramic oscillation circuit can be configured by connecting the ceramic oscillator (Max. 4.2 MHz) between the OSC3 and OSC4 terminals, capacitor CGC between the OSC3 and OSC4 terminals, and capacitor CDC between the OSC4 and VSS terminals. For both CGC and CDC, connect capacitors that are about 30 pF. To reduce current consumption of the OSC3 oscillation circuit, oscillation can be stopped by the software (OSCC register).

Table 4.3.3.1 OSC3 oscillation frequency

Oscillation circuit	Oscillation frequency
Ceramic oscillation	Max. 4.2 MHz
CR oscillation (built-in R type)	Typ. 200 kHz ±30%
CR oscillation (external R type)	200 kHz to 2.2 MHz

4.3.4 Switching of CPU clock

The system clock can be selected between OSC1 and OSC3 with software (using the CLKCHG register). The CPU clock should be switched using the following procedure. Pay special attention to the stability waiting time for oscillation.

OSC1 → OSC3

1. Set OSCC to "1". (OSC3 oscillation: off → on)
2. Wait 5 msec or more.
3. Set CLKCHG to "1". (CPU clock: OSC1 → OSC3)

Note: It takes at least 5 msec from the time the OSC3 oscillation circuit goes on until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went on.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

OSC3 → OSC1

1. Set CLKCHG to "0". (CPU clock: OSC3 → OSC1)
2. Set OSCC to "0". (OSC3 oscillation: on → off)

Note: When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation off. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

4.3.5 Clock frequency and instruction execution time

Table 4.3.5.1 shows the instruction execution time according to each frequency of the system clock.

Table 4.3.5.1 Clock frequency and instruction execution time

Clock frequency	Instruction execution time (μsec)		
	1-cycle instruction	2-cycle instruction	3-cycle instruction
OSC1: 32.768 kHz	61	122	183
OSC3: 200 kHz	10	20	30
OSC3: 1.1 MHz	1.8	3.6	5.5
OSC3: 2 MHz	1	2	3
OSC3: 4 MHz	0.5	1	1.5

4.3.6 I/O memory of oscillation circuit

Table 4.3.6.1 shows the I/O address and the control bits for the oscillation circuit.

Table 4.3.6.1 Control bits of oscillation circuit

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF01H	CLKCHG	OSCC	0	0	CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W		R		0 *3	– *2			Unused
					0 *3	– *2			Unused

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

OSCC: OSC3 oscillation control register (FF01H•D2)

Turns the OSC3 oscillation circuit on and off.

When "1" is written: OSC3 oscillation On
When "0" is written: OSC3 oscillation Off
Reading: Valid

When it is necessary to operate the CPU at high speed, set OSCC to "1". At other times, set it to "0" to reduce current consumption.
At initial reset, this register is set to "0".

CLKCHG: CPU system clock switching register (FF01H•D3)

The CPU's operation clock is selected with this register.

When "1" is written: OSC3 clock is selected
When "0" is written: OSC1 clock is selected
Reading: Valid

When the CPU clock is to be OSC3, set CLKCHG to "1"; for OSC1, set CLKCHG to "0".
After turning the OSC3 oscillation on (OSCC = "1"), switching of the clock should be done after waiting 5 msec or more.
At initial reset, this register is set to "0".

4.3.7 Programming notes

(1) It takes at least 5 msec from the time the OSC3 oscillation circuit goes on until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went on.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(2) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation off. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

4.4 Input Ports (K00–K03 and K10–K13)

4.4.1 Configuration of input ports

The S1C63808 has eight bits of general-purpose input ports (K00–K03, K10–K13). Each input port terminal provides an internal pull-down resistor that can be enabled by mask option.
Figure 4.4.1.1 shows the configuration of input port.

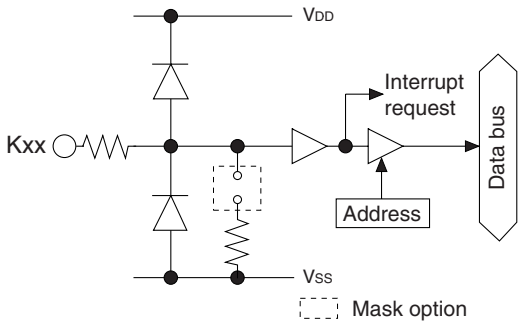


Fig. 4.4.1.1 Configuration of input port

Selection of "With pull-down resistor" with the mask option suits input from the push switch, key matrix, and so forth. When "Gate direct" is selected, the port can be used for slide switch input and interfacing with other LSIs.
The K00 and K01 input ports can also be used as the Run/Stop and Lap direct inputs for the stopwatch timer, and the K13 port can also be used as the event counter input for the programmable timer.

4.4.2 Interrupt function

All eight bits of the input ports (K00–K03, K10–K13) provide the interrupt function. The conditions for issuing an interrupt can be set by the software. Further, whether to mask the interrupt function can be selected by the software.
Figure 4.4.2.1 shows the configuration of K00–K03 (K10–K13) interrupt circuit.

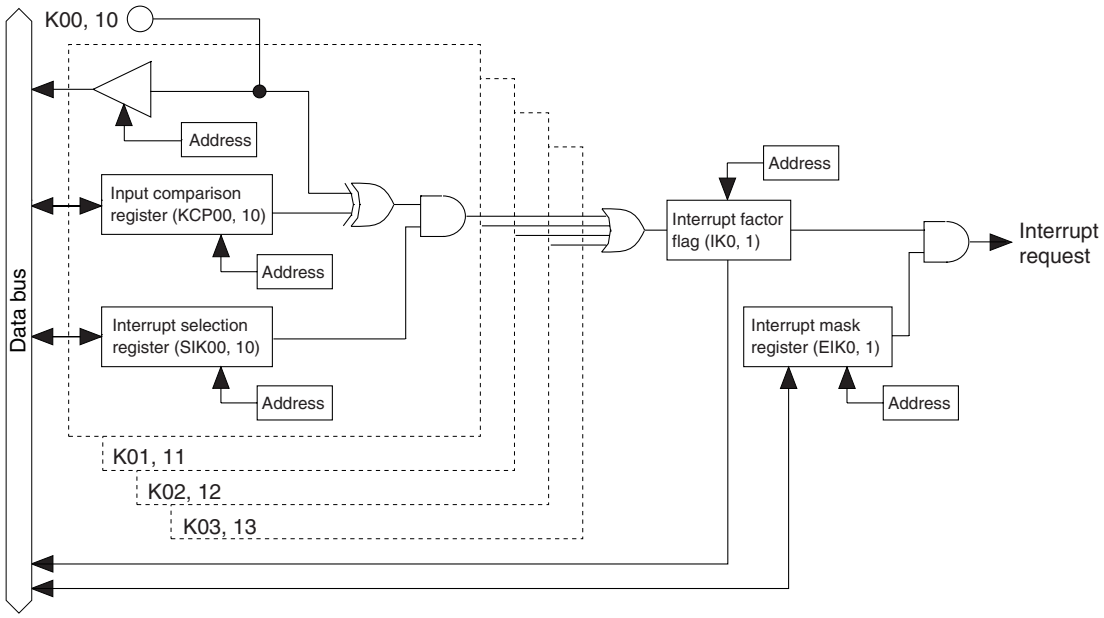


Fig. 4.4.2.1 Input interrupt circuit configuration

The interrupt selection register (SIK) and input comparison register (KCP) are individually set for the input ports K00–K03 and K10–K13, and can specify the terminals for generating interrupt and interrupt timing.
The interrupt selection registers (SIK00–SIK03, SIK10–SIK13) select what input of K00–K03 and K10–K13 to use for the interrupt. Writing "1" into an interrupt selection register incorporates that input port into the interrupt generation conditions. The changing the input port where the interrupt selection register has been set to "0" does not affect the generation of the interrupt.
The input interrupt timing can select that the interrupt be generated at the rising edge of the input or that it be generated at the falling edge according to the set value of the input comparison registers (KCP00–KCP03, KCP10–KCP13).
By setting these two conditions, the interrupt for K00–K03 or K10–K13 is generated when input ports in which an interrupt has been enabled by the input selection registers and the contents of the input comparison registers have been changed from matching to no matching.
The interrupt mask registers (EIK0, EIK1) enable the interrupt mask to be selected for K00–K03 and K10–K13.
When the interrupt is generated, the interrupt factor flag (IK0, IK1) is set to "1".
Figure 4.4.2.2 shows an example of an interrupt for K00–K03.

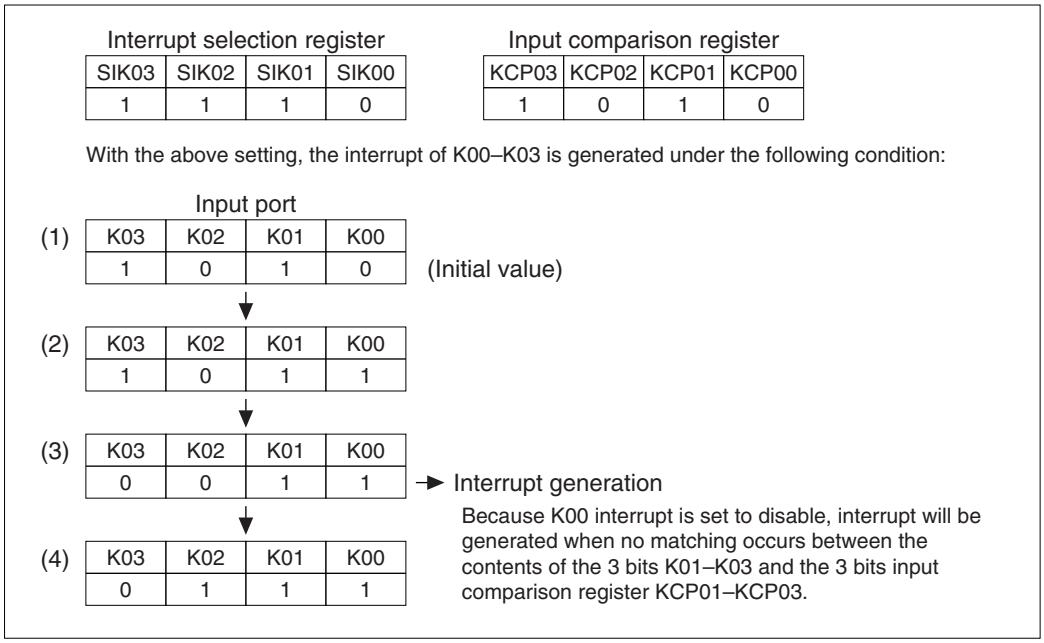


Fig. 4.4.2.2 Example of interrupt of K00–K03

K00 interrupt is disabled by the interrupt selection register (SIK00), so that an interrupt does not occur at (2). At (3), K03 changes to "0"; the data of the terminals that are interrupt enabled no longer match the data of the input comparison registers, so that interrupt occurs. As already explained, the condition for the interrupt to occur is the change in the port data and contents of the input comparison registers from matching to no matching. Hence, in (4), when the no matching status changes to another no matching status, an interrupt does not occur. Further, terminals that have been masked for interrupt do not affect the conditions for interrupt generation.

4.4.3 Mask option

Internal pull-down resistor can be selected for each of the eight bits of the input ports (K00–K03, K10–K13) with the input port mask option.
When "Gate direct" is selected, take care that the floating status does not occur for the input. Select "With pull-down resistor" for input ports that are not being used.

4.4.4 I/O memory of input ports

Table 4.4.4.1 shows the I/O addresses and the control bits for the input ports.

Table 4.4.4.1 Control bits of input ports

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF20H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
					SIK01	0	Enable	Disable	
	R/W				SIK00	0	Enable	Disable	
FF21H	K03	K02	K01	K00	K03	– *2	High	Low	K00–K03 input port data
					K02	– *2	High	Low	
					K01	– *2	High	Low	
	R				K00	– *2	High	Low	
FF22H	KCP03	KCP02	KCP01	KCP00	KCP03	0	↓	↑	K00–K03 input comparison register
					KCP02	0	↓	↑	
					KCP01	0	↓	↑	
	R/W				KCP00	0	↓	↑	
FF24H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
					SIK12	0	Enable	Disable	
					SIK11	0	Enable	Disable	
	R/W				SIK10	0	Enable	Disable	
FF25H	K13	K12	K11	K10	K13	– *2	High	Low	K10–K13 input port data
					K12	– *2	High	Low	
					K11	– *2	High	Low	
	R				K10	– *2	High	Low	
FF26H	KCP13	KCP12	KCP11	KCP10	KCP13	0	↓	↑	K10–K13 input comparison register
					KCP12	0	↓	↑	
					KCP11	0	↓	↑	
	R/W				KCP10	0	↓	↑	
FFE4H	0	0	0	EIK0	0 *3	– *2			Unused
					0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
FFE5H	0	0	0	EIK1	0 *3	– *2			Unused
					0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
FFF4H	0	0	0	IK0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
					0 *3	– *2	(W)	(W)	Unused
	R			R/W	IK0	0	Reset	Invalid	Interrupt factor flag (K00–K03)
FFF5H	0	0	0	IK1	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
					0 *3	– *2	(W)	(W)	Unused
	R			R/W	IK1	0	Reset	Invalid	Interrupt factor flag (K10–K13)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

K00–K03: K0 port input port data (FF21H)
K10–K13: K1 port input port data (FF25H)

Input data of the input port terminals can be read with these registers.

When "1" is read: High level
When "0" is read: Low level
Writing: Invalid

The reading is "1" when the terminal voltage of the eight bits of the input ports (K00–K03, K10–K13) goes high (V_{DD}), and "0" when the voltage goes low (V_{SS}).
These bits are dedicated for reading, so writing cannot be done.

SIK00–SIK03: K0 port interrupt selection register (FF20H)
SIK10–SIK13: K1 port interrupt selection register (FF24H)
Selects the ports to be used for the K00–K03 and K10–K13 input interrupts.

When "1" is written: Enable
When "0" is written: Disable
Reading: Valid

Enables the interrupt for the input ports (K00–K03, K10–K13) for which "1" has been written into the interrupt selection registers (SIK00–SIK03, SIK10–SIK13). The input port set for "0" does not affect the interrupt generation condition.
At initial reset, these registers are set to "0".

KCP00–KCP03: K0 port input comparison register (FF22H)
KCP10–KCP13: K1 port input comparison register (FF26H)
Interrupt conditions for terminals K00–K03 and K10–K13 can be set with these registers.

When "1" is written: Falling edge
When "0" is written: Rising edge
Reading: Valid

The interrupt conditions can be set for the rising or falling edge of input for each of the eight bits (K00–K03 and K10–K13), through the input comparison registers (KCP00–KCP03 and KCP10–KCP13).
For KCP00–KCP03, a comparison is done only with the ports that are enabled by the interrupt among K00–K03 by means of the SIK00–SIK03 registers. For KCP10–KCP13, a comparison is done only with the ports that are enabled by the interrupt among K10–K13 by means of the SIK10–SIK13 registers.
At initial reset, these registers are set to "0".

EIK0: K0 input interrupt mask register (FFE4H•D0)
EIK1: K1 input interrupt mask register (FFE5H•D0)
Masking the interrupt of the input port can be selected with these registers.

When "1" is written: Enable
When "0" is written: Mask
Reading: Valid

With these registers, masking of the input port interrupt can be selected for each of the two systems (K00–K03, K10–K13).
At initial reset, these registers are set to "0".

IK0: K0 input interrupt factor flag (FFF4H•D0)
IK1: K1 input interrupt factor flag (FFF5H•D0)
These flags indicate the occurrence of input interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

The interrupt factor flags IK0 and IK1 are associated with K00–K03 and K10–K13, respectively. From the status of these flags, the software can decide whether an input interrupt has occurred.
The interrupt factor flag is set to "1" when the interrupt condition is established regardless of the interrupt mask register setting. However, the interrupt does not occur to the CPU when the interrupt is masked.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.4.5 Programming notes

(1) When input ports are changed from high to low by pull-down resistors, the fall of the waveform is delayed on account of the time constant of the pull-down resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate waiting time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-down resistance 375 kΩ (Max.)

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.5 Output Ports (R00–R03 and R10–R13)

4.5.1 Configuration of output ports

The S1C63808 has eight bits of general output ports.
Output specifications of the output ports can be selected individually with the mask option. Two kinds of output specifications are available: complementary output and P-channel open drain output.
Figure 4.5.1.1 shows the configuration of the output port.

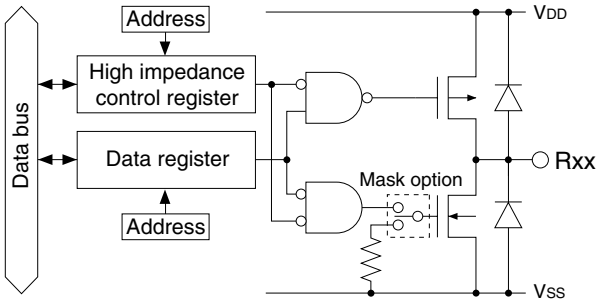


Fig. 4.5.1.1 Configuration of output port

The R01, R02 and R03 output terminals are shared with special output terminals (BZ, TOUT, FOUT), and this function is selected by the software.
At initial reset, these are all set to the general purpose output port.
Table 4.5.1.1 shows the setting of the output terminals by function selection.

Table 4.5.1.1 Function setting of output terminals

Terminal name	Terminal status at initial reset	Special output		
		BZ	TOUT	FOUT
R00	R00 (LOW output)	R00	R00	R00
R01	R01 (LOW output)	BZ		
R02	R02 (LOW output)		TOUT	
R03	R03 (LOW output)			FOUT
R10–R13	R10–R13 (LOW output)	R10–R13	R10–R13	R10–R13

When using the output port (R01, R02, R03) as the special output port, the data register must be fixed at "1" and the high impedance control register must be fixed at "0" (data output).

Note: If an output terminal (including a special output terminal) of this IC is used to drive an external component that consumes a large amount of current such as a bipolar transistor, design the pattern of traces on the printed circuit board so that the operation of the external component does not affect the IC power supply. Refer to <Output Terminals> in Section 5.3, "Precautions on Mounting", for more information.

4.5.2 Mask option

Output specifications of the output ports are selected by mask option.
Either complementary output or P-channel open drain output can be selected individually (in 1-bit units). However, when P-channel open drain output is selected, do not apply a voltage exceeding the power supply voltage to the output port.

4.5.3 High impedance control

The output ports can be set into a high impedance status. This control is done using the high impedance control registers.
The high impedance control registers are provided to correspond with the output ports as shown below.

High impedance control register	Corresponding output port
R00HIZ	R00 (1 bit)
R01HIZ	R01 (1 bit)
R02HIZ	R02 (1 bit)
R03HIZ	R03 (1 bit)
R1HIZ	R10–R13 (4 bits)

When "1" is written to the high impedance control register, the corresponding output port terminal goes into high impedance status. When "0" is written, the port outputs a signal according to the data register.

4.5.4 Special output

In addition to the regular DC output, special output can be selected for the output ports R01, R02 and R03 as shown in Table 4.5.4.1 with the software.

Table 4.5.4.1 Special output

Terminal	Special output	Output control register
R03	FOUT	FOUTE
R02	TOUT	PTOUT
R01	BZ	BZE, BZSHT

At initial reset, the output port data register is set to "0" and the high impedance control register is set to "0". Consequently, the output terminal goes low (VSS).
When using the output port (R01, R02, R03) as the special output port, fix the data register (R01, R02, R03) at "1" and the high impedance control register (R01HIZ, R02HIZ, R03HIZ) at "0" (data output). The respective signal should be turned on and off using the special output control register.

Notes:
- *Be aware that the output terminal is fixed at a low (VSS) level the same as the DC output if "0" is written to the R01, R02 and R03 registers when the special output has been selected.*
- *Be aware that the output terminal shifts into high impedance status when "1" is written to the high impedance control register (R01HIZ, R02HIZ, R03HIZ).*

- **BZ (R01)**

  The R01 terminal can output a BZ signal.
  The BZ signal is the buzzer signal that is output from the sound generator.
  To output the BZ signal, fix the R01 register at "1" and the R01HIZ register at "0", and turn the signal on and off using the BZE or BZSHT register.
  Refer to Section 4.11, "Sound Generator" for details of the buzzer signal and controlling method.

Note: A hazard may occur when the BZ signal is turned on and off.

Figure 4.5.4.1 shows the output waveform of the BZ signal.

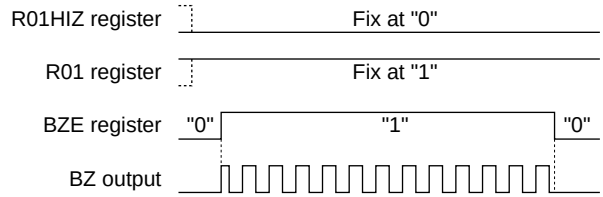


Fig. 4.5.4.1 Output waveform of BZ signal

- **TOUT (R02)**

  The R02 terminal can output a TOUT signal.
  The TOUT signal is the clock that is output from the programmable timer, and can be used to provide a clock signal to an external device.
  To output the TOUT signal, fix the R02 register at "1" and the R02HIZ register at "0", and turn the signal on and off using the PTOUT register. It is, however, necessary to control the programmable timer.
  Refer to Section 4.9, "Programmable Timer" for details of the programmable timer.

Note: A hazard may occur when the TOUT signal is turned on and off.

Figure 4.5.4.2 shows the output waveform of the TOUT signal.

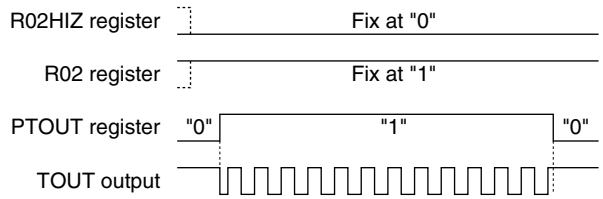


Fig. 4.5.4.2 Output waveform of TOUT signal

- **FOUT (R03)**

  The R03 terminal can output an FOUT signal.
  The FOUT signal is a clock (f_{OSC1} or f_{OSC3}) that is output from the oscillation circuit or a clock that the f_{OSC1} clock has divided in the internal circuit, and can be used to provide a clock signal to an external device.
  To output the FOUT signal, fix the R03 register at "1" and the R03HIZ register at "0", and turn the signal on and off using the FOUTE register.
  The frequency of the output clock may be selected from among 4 types shown in Table 4.5.4.2 by setting the FOFQ0 and FOFQ1 registers.

Table 4.5.4.2 FOUT clock frequency

FOFQ1	FOFQ0	Clock frequency
1	1	f_{OSC3}
1	0	f_{OSC1}
0	1	$f_{OSC1} \times 1/8$
0	0	$f_{OSC1} \times 1/64$

f_{OSC1}: Clock that is output from the OSC1 oscillation circuit
f_{OSC3}: Clock that is output from the OSC3 oscillation circuit

When f_{OSC3} is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit before output.
Refer to Section 4.3, "Oscillation Circuit", for the control and notes.

Note: A hazard may occur when the FOUT signal is turned on and off.

Figure 4.5.4.3 shows the output waveform of the FOUT signal.

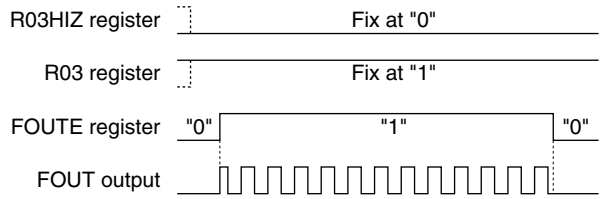


Fig. 4.5.4.3 Output waveform of FOUT signal

4.5.5 I/O memory of output ports

Table 4.5.5.1 shows the I/O addresses and control bits for the output ports.

Table 4.5.5.1 Control bits of output ports

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF06H	FOUTE	SWDIR	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT output enable
					SWDIR	0			Stopwatch direct input switch
									0: K00=Run/Stop, K01=Lap 1: K00=Lap, K01=Run/Stop
	R/W				FOFQ1	0			FOUT frequency selection [FOFQ1, 0] 0 1 2 3
					FOFQ0	0			Frequency fOSC1/64 fOSC1/8 fOSC1 fOSC3
FF30H	R03HIZ	R02HIZ	R01HIZ	R00HIZ	R03HIZ	0	Hi-Z	Output	R03 (FOUTE=0)/FOUT (FOUTE=1) Hi-Z control
					R02HIZ	0	Hi-Z	Output	R02 (PTOUT=0)/TOUT (PTOUT=1) Hi-Z control
	R/W				R01HIZ	0	Hi-Z	Output	R01 (BZE=0)/BZ (BZE=1) Hi-Z control
					R00HIZ	0	Hi-Z	Output	R00 Hi-Z control
FF31H	R03	R02	R01	R00	R03	0	High	Low	R03 output port data (FOUTE=0) Fix at "1" when FOUT is used.
					R02	0	High	Low	R02 output port data (PTOUT=0) Fix at "1" when TOUT is used.
	R/W				R01	0	High	Low	R01 output port data (BZE=0) Fix at "1" when BZ is used.
					R00	0	High	Low	R00 output port data
FF32H	0	0	0	R1HIZ	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					R1HIZ	0	Hi-Z	Output	R10–R13 Hi-Z control
FF33H	R13	R12	R11	R10	R13	0	High	Low	R10–R13 output port data
					R12	0	High	Low	
	R/W				R11	0	High	Low	
					R10	0	High	Low	
FF6CH	ENRTM	ENRST	ENON	BZE	ENRTM	0	1 sec	0.5 sec	Envelope releasing time selection
					ENRST*3	Reset	Reset	Invalid	Envelope reset (writing)
	R/W	W	R/W		ENON	0	On	Off	Envelope On/Off
					BZE	0	Enable	Disable	Buzzer output enable
FF6DH	0	BZSTP	BZSHT	SHTPW	0 *3	– *2			Unused
					BZSTP*3	0	Stop	Invalid	1-shot buzzer stop (writing)
					BZSHT	0	Trigger	Invalid	1-shot buzzer trigger (writing)
	R	W	R/W				Busy	Ready	1-shot buzzer status (reading)
					SHTPW	0	125 msec	31.25 msec	1-shot buzzer pulse width setting
FFC1H	CHSEL0	PTOUT	CKSEL1	CKSEL0	CHSEL0	0	Timer 1	Timer 0	TOUT output selection
					PTOUT	0	On	Off	TOUT output control
	R/W				CKSEL1	0	OSC3	OSC1	Prescaler 1 source clock selection
					CKSEL0	0	OSC3	OSC1	Prescaler 0 source clock selection

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

R00HIZ–R03HIZ: R0 port high impedance control register (FF30H)
R1HIZ: R1 port high impedance control register (FF32H•D0)

Controls high impedance output of the output port.

When "1" is written: High impedance
When "0" is written: Data output
Reading: Valid

By writing "0" to the high impedance control register, the corresponding output terminal outputs according to the data register. When "1" is written, it shifts into high impedance status.
When the output ports R01, R02 and R03 are used for special output (BZ, TOUT, FOUT), fix the R01HIZ register, R02HIZ register and the R03HIZ register at "0" (data output).
At initial reset, these registers are set to "0".

R00–R03: R0 output port data register (FF31H)
R10–R13: R1 output port data register (FF33H)
Set the output data for the output ports.

When "1" is written: High level output
When "0" is written: Low level output
Reading: Valid

The output port terminals output the data written in the corresponding data registers without changing it. When "1" is written to the register, the output port terminal goes high (V_{DD}), and when "0" is written, the output port terminal goes low (V_{SS}).
When the output ports R01, R02 and R03 are used for special output (BZ, TOUT, FOUT), fix the R01 register, R02 register and the R03 register at "1".
At initial reset, these registers are all set to "0".

FOUTE: FOUT output control register (FF06H•D3)
Controls the FOUT output.

When "1" is written: FOUT output On
When "0" is written: FOUT output Off
Reading: Valid

By writing "1" to the FOUTE register when the R03 register has been set to "1" and the R03HIZ register has been set to "0", the FOUT signal is output from the R03 terminal. When "0" is written, the R03 terminal goes low (V_{SS}).
When using the R03 output port for DC output, fix this register at "0".
At initial reset, this register is set to "0".

FOFQ0, FOFQ1: FOUT frequency selection register (FF06H•D0, D1)
Selects a frequency of the FOUT signal.

Table 4.5.5.2 FOUT clock frequency

FOFQ1	FOFQ0	Clock frequency
1	1	f_{OSC3}
1	0	f_{OSC1}
0	1	$f_{OSC1} \times 1/8$
0	0	$f_{OSC1} \times 1/64$

At initial reset, this register is set to "0".

PTOUT: TOUT output control register (FFC1H•D0)
Controls the TOUT output.

When "1" is written: TOUT output On
When "0" is written: TOUT output Off
Reading: Valid

By writing "1" to the PTOUT register when the R02 register has been set to "1" and the R02HIZ register has been set to "0", the TOUT signal is output from the R02 terminal. When "0" is written, the R02 terminal goes high (V_{DD}).
When using the R02 output port for DC output, fix this register at "0".
At initial reset, this register is set to "0".

BZE: Buzzer output control register (FF6CH•D0)

Controls the buzzer signal output.

When "1" is written: Buzzer output On
When "0" is written: Buzzer output Off
Reading: Valid

By writing "1" to the BZE register when the R01 register has been set to "1" and the R01HIZ register has been set to "0", the BZ signal is output from the R01 terminal. When "0" is written, the R01 terminal goes low (V_{SS}).
At initial reset, this register is set to "0".

BZSHT: One-shot buzzer trigger/status (FF6DH•D1)

Controls the one-shot buzzer output.

• ***When writing***

When "1" is written: Trigger
When "0" is written: No operation

Writing "1" into BZSHT causes the one-short output circuit to operate and a buzzer signal to be output from the R01 terminal. To output the buzzer signal, the R01 register must be set to "1" and the R01HIZ register must be set to "0".
This output is automatically turned off after the time set by SHTPW has elapsed. The one-shot output is only valid when the normal buzzer output is off (BZE = "0") and will be invalid when the normal buzzer output is on (BZE = "1"). When a re-trigger is assigned during a one-shot output, the one-shot output time set with SHTPW is measured again from that point (time extension).

• ***When reading***

When "1" is read: BUSY
When "0" is read: READY

During reading BZSHT shows the operation status of the one-shot output circuit. During one-shot output, BZSHT becomes "1" and the output goes off, it shifts to "0".
At initial reset, this bit is set to "0".

4.5.6 Programming notes

(1) When using the output port (R01, R02, R03) as the special output port (BZ, TOUT, FOUT), fix the data register (R01, R02, R03) at "1" and the high impedance control register (R01HIZ, R02HIZ, R03HIZ) at "0" (data output).
Be aware that the output terminal is fixed at a low (V_{SS}) level the same as the DC output if "0" is written to the R01, R02 and R03 registers when the special output has been selected.
Be aware that the output terminal shifts into high impedance status when "1" is written to the high impedance control register (R01HIZ, R02HIZ, R03HIZ).

(2) A hazard may occur when the BZ, FOUT or TOUT signal is turned on and off.

(3) When f_{OSC3} is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit before output.
Refer to Section 4.3, "Oscillation Circuit", for the control and notes.

4.6 I/O Ports (P00–P03, P10–P13, P20–P23, P30–P33 and P40–P43)

4.6.1 Configuration of I/O ports

The S1C63808 has 20 bits of general-purpose I/O ports. Figure 4.6.1.1 shows the configuration of the I/O port.

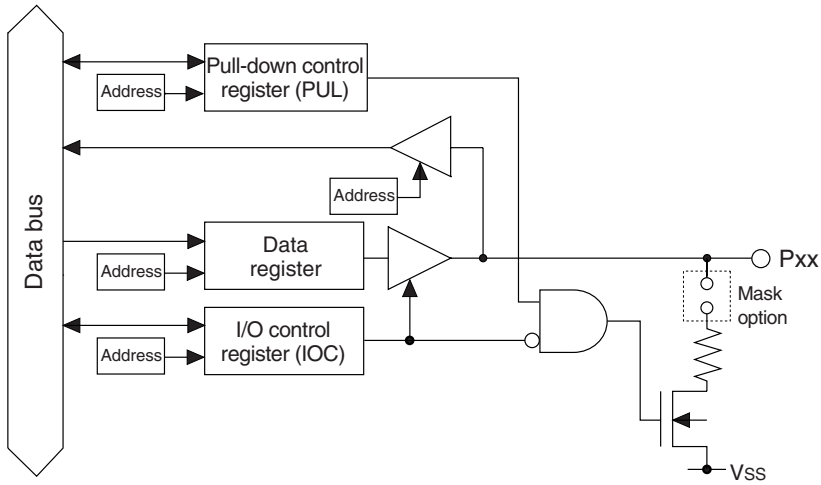


Fig. 4.6.1.1 Configuration of I/O port

The I/O port terminals P10 to P13 and P20 to P23 are shared with the serial interface input/output terminals. The software can select the function to be used.
At initial reset, these terminals are all set to the I/O port.
Table 4.6.1.1 shows the setting of the input/output terminals by function selection.

Table 4.6.1.1 Function setting of input/output terminals

Terminal name	Terminal status at initial reset	Serial I/F		
		Async.	Clk-sync. Master	Clk-sync. Slave
P00–P03	P00–P03 (Input & pulled down*)	P00–P03	P00–P03	P00–P03
P10	P10 (Input & pulled down*)	SIN1(I)	SIN1(I)	SIN1(I)
P11	P11 (Input & pulled down*)	SOUT1(O)	SOUT1(O)	SOUT1(O)
P12	P12 (Input & pulled down*)	P12	SCLK1(O)	SCLK1(I)
P13	P13 (Input & pulled down*)	P13	P13	SRDY1(O)
P20	P20 (Input & pulled down*)	SIN2(I)	SIN2(I)	SIN2(I)
P21	P21 (Input & pulled down*)	SOUT2(O)	SOUT2(O)	SOUT2(O)
P22	P22 (Input & pulled down*)	P22	SCLK2(O)	SCLK2(I)
P23	P23 (Input & pulled down*)	P23	P23	SRDY2(O)
P30–P33	P30–P33 (Input & pulled down*)	P30–P33	P30–P33	P30–P33
P40–P43	P40–P43 (Input & pulled down*)	P40–P43	P40–P43	P40–P43

* When "with pull-down resistor" is selected by the mask option
(high impedance when "gate direct" is set)

When these ports are used as I/O ports, the ports can be set to either input mode or output mode individually (in 1-bit unit). Modes can be set by writing data to the I/O control registers.
Refer to Section 4.10, "Serial Interface", for control of the serial interface.

Note: If an output of this IC is used to drive an external component that consumes a large amount of current such as a bipolar transistor, design the pattern of traces on the printed circuit board so that the operation of the external component does not affect the IC power supply. Refer to <Output Terminals> in Section 5.3, "Precautions on Mounting", for more information.

4.6.2 Mask option

The output specification of each I/O port during output mode can be selected from either complementary output or P-channel open drain output by mask option. This selection can be done in 1-bit units. When P-channel open drain output is selected, do not apply a voltage exceeding the power supply voltage to the port.

The mask option also permits selection of whether the pull-down resistor is used or not during input mode. This selection can be done in 1-bit units.
When "without pull-down" during the input mode is selected, take care that the floating status does not occur.

The pull-down resistor for input mode and output specification (complementary output or P-channel open drain output) selected by mask option are effective even when I/O ports are used for input/output of the serial interface.

4.6.3 I/O control registers and input/output mode

Input or output mode can be set for the I/O ports by writing data into the corresponding I/O control registers IOCxx.

To set the input mode, write "0" to the I/O control register. When an I/O port is set to input mode, it becomes high impedance status and works as an input port.
However, when the pull-down explained in the following section has been set by software, the input line is pulled down only during this input mode.

To set the output mode, write "1" is to the I/O control register. When an I/O port is set to output mode, it works as an output port, it outputs a high level (V_{DD}) when the port output data is "1", and a low level (V_{SS}) when the port output data is "0".

If perform the read out in each mode; when output mode, the register value is read out, and when input mode, the port value is read out.

At initial reset, the I/O control registers are set to "0", and the I/O ports enter the input mode.

The I/O control registers of the ports that are set as input/output for the serial interface can be used as general purpose registers that do not affect the I/O control. (See Table 4.6.1.1.)

4.6.4 Pull-down during input mode

A pull-down resistor that operates during the input mode is built into each I/O port of the S1C63808. Mask option can set the use or non-use of this pull-down.

The pull-down resistor becomes effective by writing "1" to the pull-down control register PULxx that corresponds to each port, and the input line is pulled down during the input mode. When "0" has been written, no pull-down is done.
At initial reset, the pull-down control registers are set to "1".

The pull-down control registers of the ports in which "gate direct" has been selected can be used as general purpose registers.
Even when "with pull-down" has been selected, the pull-down control registers of the ports, that are set as output for the serial interface, can be used as general purpose registers that do not affect the pull-down control. (See Table 4.6.1.1.)
The pull-down control registers of the port, that are set as input for the serial interface, function the same as the I/O port.

4.6.5 I/O memory of I/O ports

Table 4.6.5.1 shows the I/O addresses and the control bits for the I/O ports.

Table 4.6.5.1(a) Control bits of I/O ports

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF40H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	P00–P03 I/O control register
					IOC02	0	Output	Input	
	R/W				IOC01	0	Output	Input	
					IOC00	0	Output	Input	
FF41H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	P00–P03 pull-down control register
					PUL02	1	On	Off	
	R/W				PUL01	1	On	Off	
					PUL00	1	On	Off	
FF42H	P03	P02	P01	P00	P03	– *2	High	Low	P00–P03 I/O port data
					P02	– *2	High	Low	
	R/W				P01	– *2	High	Low	
					P00	– *2	High	Low	
FF44H	IOC13	IOC12	IOC11	IOC10	IOC13	0	Output	Input	P13 I/O control register functions as a general-purpose register when SIF1 (slave) is selected
					IOC12	0	Output	Input	P12 I/O control register (ESIF1=0) functions as a general-purpose register when SIF1 is selected
	R/W				IOC11	0	Output	Input	P11 I/O control register (ESIF1=0) functions as a general-purpose register when SIF1 is selected
					IOC10	0	Output	Input	P10 I/O control register (ESIF1=0) functions as a general-purpose register when SIF1 is selected
FF45H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P13 pull-down control register functions as a general-purpose register when SIF1 (slave) is selected
					PUL12	1	On	Off	P12 pull-down control register (ESIF1=0) functions as a general-purpose register when SIF1 (master) is selected SCLK1 (I) pull-down control register when SIF1 (slave) is selected
	R/W				PUL11	1	On	Off	P11 pull-down control register (ESIF1=0) functions as a general-purpose register when SIF1 is selected
					PUL10	1	On	Off	P10 pull-down control register (ESIF1=0) SIN1 pull-down control register when SIF1 is selected
FF46H	P13	P12	P11	P10	P13	– *2	High	Low	P13 I/O port data functions as a general-purpose register when SIF1 (slave) is selected
					P12	– *2	High	Low	P12 I/O port data (ESIF1=0) functions as a general-purpose register when SIF1 is selected
	R/W				P11	– *2	High	Low	P11 I/O port data (ESIF1=0) functions as a general-purpose register when SIF1 is selected
					P10	– *2	High	Low	P10 I/O port data (ESIF1=0) functions as a general-purpose register when SIF1 is selected
FF48H	IOC23	IOC22	IOC21	IOC20	IOC23	0	Output	Input	P23 I/O control register functions as a general-purpose register when SIF2 (slave) is selected
					IOC22	0	Output	Input	P22 I/O control register (ESIF2=0) functions as a general-purpose register when SIF2 is selected
	R/W				IOC21	0	Output	Input	P21 I/O control register (ESIF2=0) functions as a general-purpose register when SIF2 is selected
					IOC20	0	Output	Input	P20 I/O control register (ESIF2=0) functions as a general-purpose register when SIF2 is selected
FF49H	PUL23	PUL22	PUL21	PUL20	PUL23	1	On	Off	P23 pull-down control register functions as a general-purpose register when SIF2 (slave) is selected
					PUL22	1	On	Off	P22 pull-down control register (ESIF2=0) functions as a general-purpose register when SIF2 (master) is selected SCLK2 (I) pull-down control register when SIF2 (slave) is selected
	R/W				PUL21	1	On	Off	P21 pull-down control register (ESIF2=0) functions as a general-purpose register when SIF2 is selected
					PUL20	1	On	Off	P20 pull-down control register (ESIF2=0) SIN2 pull-down control register when SIF2 is selected

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.6.5.1(b) Control bits of I/O ports

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF4AH	P23	P22	P21	P20	P23	– *2	High	Low	P23 I/O port data functions as a general-purpose register when SIF2 (slave) is selected
					P22	– *2	High	Low	P22 I/O port data (ESIF2=0) functions as a general-purpose register when SIF2 is selected
					P21	– *2	High	Low	P21 I/O port data (ESIF2=0) functions as a general-purpose register when SIF2 is selected
	R/W				P20	– *2	High	Low	P20 I/O port data (ESIF2=0) functions as a general-purpose register when SIF2 is selected
FF4CH	IOC33	IOC32	IOC31	IOC30	IOC33	0	Output	Input	P30–P33 I/O control register
					IOC32	0	Output	Input	
	R/W				IOC31	0	Output	Input	
					IOC30	0	Output	Input	
FF4DH	PUL33	PUL32	PUL31	PUL30	PUL33	1	On	Off	P30–P33 pull-down control register
					PUL32	1	On	Off	
	R/W				PUL31	1	On	Off	
					PUL30	1	On	Off	
FF4EH	P33	P32	P31	P30	P33	– *2	High	Low	P30–P33 I/O port data
					P32	– *2	High	Low	
	R/W				P31	– *2	High	Low	
					P30	– *2	High	Low	
FF50H	IOC43	IOC42	IOC41	IOC40	IOC33	0	Output	Input	P40–P43 I/O control register
					IOC32	0	Output	Input	
	R/W				IOC31	0	Output	Input	
					IOC30	0	Output	Input	
FF51H	PUL43	PUL42	PUL41	PUL40	PUL43	1	On	Off	P40–P43 pull-down control register
					PUL42	1	On	Off	
	R/W				PUL41	1	On	Off	
					PUL40	1	On	Off	
FF52H	P43	P42	P41	P40	P43	– *2	High	Low	P40–P43 I/O port data
					P42	– *2	High	Low	
	R/W				P41	– *2	High	Low	
					P40	– *2	High	Low	
FF14H	0	SMD21	SMD20	ESIF2	0 *3	– *2			Unused Serial I/F 2 mode selection: [SMD21, 20] 0 = Mode Clk-sync. master, 1 = Clk-sync. slave; 2 = Mode Async. 7-bit, 3 = Async. 8-bit Serial I/F 2 enable (P2x port function selection)
					SMD21	0			
	R	R/W			SMD20	0			
					ESIF2	0	SIF	I/O	
FF64H	0	SMD11	SMD10	ESIF1	0 *3	– *2			Unused Serial I/F 1 mode selection: [SMD11, 10] 0 = Mode Clk-sync. master, 1 = Clk-sync. slave; 2 = Mode Async. 7-bit, 3 = Async. 8-bit Serial I/F 1 enable (P1x port function selection)
					SMD11	0			
	R	R/W			SMD10	0			
					ESIF1	0	SIF	I/O	

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

(1) Selection of port function

ESIF1: Serial interface 1 enable register (FF64H•D0)
ESIF2: Serial interface 2 enable register (FF14H•D0)

Selects a function for P10–P13 or P20–P23.

When "1" is written: Serial interface input/output port
When "0" is written: I/O port
Reading: Valid

Serial interface 1 uses the P10–P13 terminals and serial interface 2 uses the P20–P23 terminals. When using the serial interface, write "1" to the ESIFx register . When P10–P13 are used as I/O ports, write "0". The terminal configuration within P10–P13/P20–P23 that are used for the serial interface is decided by the transfer mode (7-bit asynchronous, 8-bit asynchronous, clock synchronous slave, clock synchronous master) selected with the SMDxx register.

In the clock synchronous slave mode, all the P10–P13/P20–P23 ports are set to the serial interface input/output port. In the clock synchronous master mode, P10–P12/P20–P22 are set to the serial interface input/output port and P13/P23 can be used as an I/O port. In the 8/7-bit asynchronous mode, P10/P20 and P11/P21 are set to the serial interface input/output port and P12/P22 and P13/P23 can be used as I/O ports.
At initial reset, these registers are set to "0".

(2) I/O port control

P00–P03: P0 I/O port data register (FF42H)
P10–P13: P1 I/O port data register (FF46H)
P20–P23: P2 I/O port data register (FF4AH)
P30–P33: P3 I/O port data register (FF4EH)
P40–P43: P4 I/O port data register (FF52H)
I/O port data can be read and output data can be set through these registers.

• When writing data

When "1" is written: High level
When "0" is written: Low level

When an I/O port is set to the output mode, the written data is output unchanged from the I/O port terminal. When "1" is written as the port data, the port terminal goes high (V_{DD}), and when "0" is written, the terminal goes low (V_{SS}).
Port data can be written also in the input mode.

• When reading data

When "1" is read: High level
When "0" is read: Low level

The terminal voltage level of the I/O port is read out. When the I/O port is in the input mode the voltage level being input to the port terminal can be read out; in the output mode the register value can be read. When the terminal voltage is high (V_{DD}) the port data that can be read is "1", and when the terminal voltage is low (V_{SS}) the data is "0".
When "with pull-down resistor" has been selected with the mask option and the PUL register is set to "1", the built-in pull-down resistor goes on during input mode, so that the I/O port terminal is pulled down.

The data registers of the port, which are set for the input/output of the serial interface (P10–P13, P20–P23), become general-purpose registers that do not affect the input/output.

Note: When in the input mode, I/O ports are changed from high to low by pull-down resistor, the fall of the waveform is delayed on account of the time constant of the pull-down resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-down resistance 375 kΩ (Max.)

IOC00–IOC03: P0 port I/O control register (FF40H)
IOC10–IOC13: P1 port I/O control register (FF44H)
IOC20–IOC23: P2 port I/O control register (FF48H)
IOC30–IOC33: P3 port I/O control register (FF4CH)
IOC40–IOC43: P4 port I/O control register (FF50H)
The input and output modes of the I/O ports are set with these registers.

When "1" is written: Output mode
When "0" is written: Input mode
Reading: Valid

The input and output modes of the I/O ports are set in 1-bit unit.
Writing "1" to the I/O control register makes the corresponding I/O port enter the output mode, and writing "0" induces the input mode.
At initial reset, these registers are all set to "0", so the I/O ports are in the input mode.
The I/O control registers of the port, which are set for the input/output of the serial interface (P10–P13, P20–P23), become general-purpose registers that do not affect the input/output.

PUL00–PUL03: P0 port pull-down control register (FF41H)
PUL10–PUL13: P1 port pull-down control register (FF45H)
PUL20–PUL23: P2 port pull-down control register (FF49H)
PUL30–PUL33: P3 port pull-down control register (FF4DH)
PUL40–PUL43: P4 port pull-down control register (FF51H)
The pull-down during the input mode are set with these registers.

When "1" is written: Pull-down On
When "0" is written: Pull-down Off
Reading: Valid

The built-in pull-down resistor which is turned on during input mode is set to enable in 1-bit units. (The pull-down resistor is included into the ports selected by mask option.)
By writing "1" to the pull-down control register, the corresponding I/O ports are pulled down (during input mode), while writing "0" disables the pull-down function.
At initial reset, these registers are all set to "1", so the pull-down function is enabled.

The pull-down control registers of the ports in which the pull-down resistor is not included become the general purpose register. The registers of the ports that are set as output for the serial interface can also be used as general purpose registers that do not affect the pull-down control.
The pull-down control registers of the port that are set as input for the serial interface function the same as the I/O port.

4.6.6 Programming note

When in the input mode, I/O ports are changed from high to low by pull-down resistor, the fall of the waveform is delayed on account of the time constant of the pull-down resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-down resistance 375 kΩ (Max.)

4.7 Clock Timer

4.7.1 Configuration of clock timer

The S1C63808 has a built-in clock timer that uses OSC1 (crystal oscillator) as the source oscillator. The clock timer is configured of an 8-bit binary counter that serves as the input clock, fOSC1 divided clock output from the prescaler. Timer data (128–16 Hz and 8–1 Hz) can be read out by the software.
Figure 4.7.1.1 is the block diagram for the clock timer.

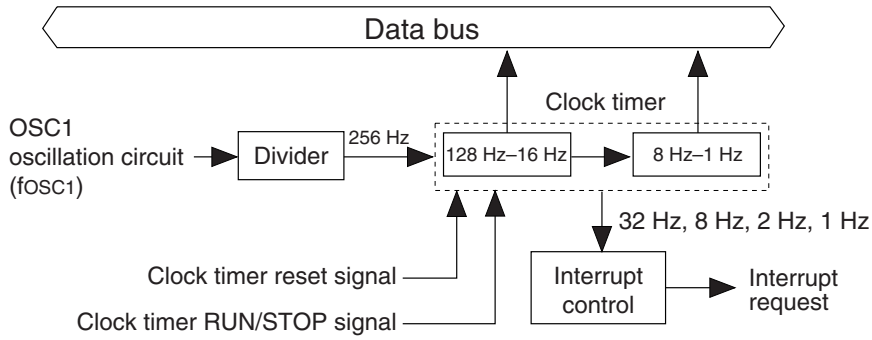


Fig. 4.7.1.1 Block diagram for the clock timer

Ordinarily, this clock timer is used for all types of timing functions such as clocks.

4.7.2 Data reading and hold function

The 8 bits timer data are allocated to the address FF79H and FF7AH.

<FF79H>	D0: TM0 = 128 Hz	D1: TM1 = 64 Hz	D2: TM2 = 32 Hz	D3: TM3 = 16 Hz
<FF7AH>	D0: TM4 = 8 Hz	D1: TM5 = 4 Hz	D2: TM6 = 2 Hz	D3: TM7 = 1 Hz

Since the clock timer data has been allocated to two addresses, a carry is generated from the low-order data within the count (TM0–TM3: 128–16 Hz) to the high-order data (TM4–TM7: 8–1 Hz). When this carry is generated between the reading of the low-order data and the high-order data, a content combining the two does not become the correct value (the low-order data is read as FFH and the high-order data becomes the value that is counted up 1 from that point).
The high-order data hold function in the S1C63808 is designed to operate to avoid this. This function temporarily stops the counting up of the high-order data (by carry from the low-order data) at the point where the low-order data has been read and consequently the time during which the high-order data is held is the shorter of the two indicated here following.

1. Period until it reads the high-order data.
2. 0.48–1.5 msec (Varies due to the read timing.)

Note: Since the low-order data is not held when the high-order data has previously been read, the low-order data should be read first.

4.7.3 Interrupt function

The clock timer can cause interrupts at the falling edge of 32 Hz, 8 Hz, 2 Hz and 1 Hz signals. Software can set whether to mask any of these frequencies.
Figure 4.7.3.1 is the timing chart of the clock timer.

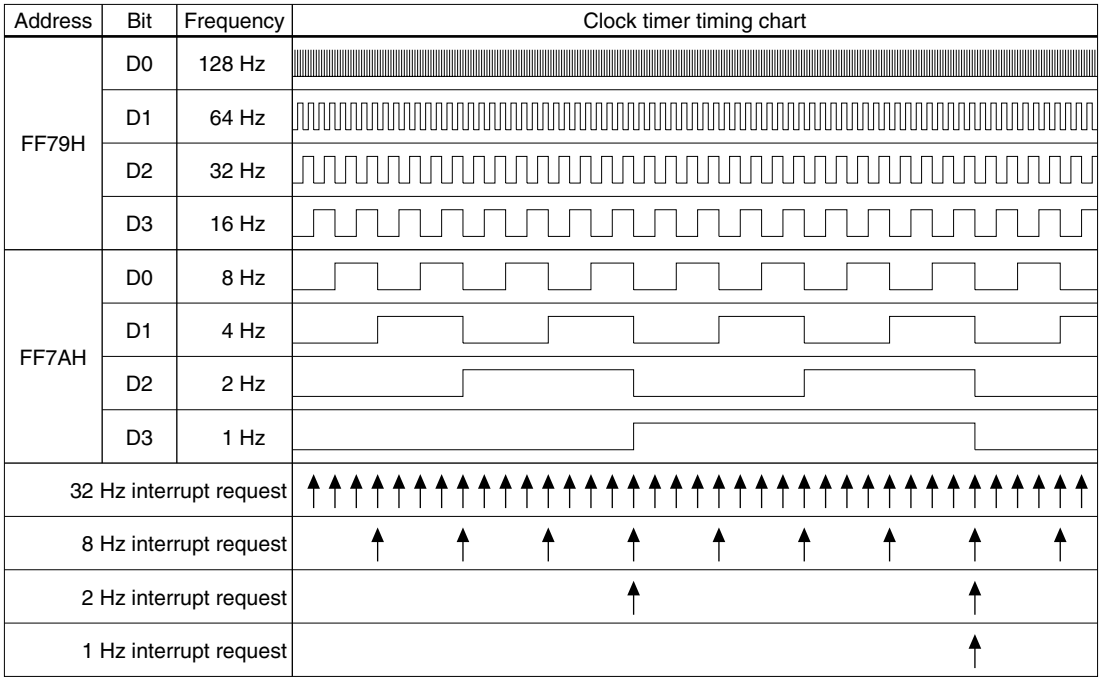


Fig. 4.7.3.1 Timing chart of clock timer

As shown in Figure 4.7.3.1, interrupt is generated at the falling edge of the frequencies (32 Hz, 8 Hz, 2 Hz, 1 Hz). At this time, the corresponding interrupt factor flag (IT0, IT1, IT2, IT3) is set to "1". Selection of whether to mask the separate interrupts can be made with the interrupt mask registers (EIT0, EIT1, EIT2, EIT3). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" at the falling edge of the corresponding signal.

4.7.4 I/O memory of clock timer

Table 4.7.4.1 shows the I/O addresses and the control bits for the clock timer.

Table 4.7.4.1 Control bits of clock timer

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF78H	0	0	TMRST	TMRUN	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		W	R/W	TMRST*3	Reset	Reset	Invalid	Clock timer reset (writing)
					TMRUN	0	Run	Stop	Clock timer Run/Stop
FF79H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
FF7AH	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
FFE6H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
FFF6H	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
					IT2	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R/W				IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 8 Hz)
					IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 32 Hz)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

TM0–TM7: Timer data (FF79H, FF7AH)

The 128–1 Hz timer data of the clock timer can be read out with these registers. These eight bits are read only, and writing operations are invalid.

By reading the low-order data (FF79H), the high-order data (FF7AH) is held until reading or for 0.48–1.5 msec (one of shorter of them).

At initial reset, the timer data is initialized to "00H".

TMRST: Clock timer reset (FF78H•D1)

This bit resets the clock timer.

When "1" is written: Clock timer reset
When "0" is written: No operation
Reading: Always "0"

The clock timer is reset by writing "1" to TMRST. When the clock timer is reset in the RUN status, operation restarts immediately. Also, in the STOP status the reset data is maintained. No operation results when "0" is written to TMRST.

This bit is write-only, and so is always "0" at reading.

TMRUN: Clock timer RUN/STOP control register (FF78H•D0)

Controls RUN/STOP of the clock timer.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

The clock timer enters the RUN status when "1" is written to the TMRUN register, and the STOP status when "0" is written. In the STOP status, the timer data is maintained until the next RUN status or the timer is reset. Also, when the STOP status changes to the RUN status, the data that is maintained can be used for resuming the count.

At initial reset, this register is set to "0".

EIT0: 32 Hz interrupt mask register (FFE6H•D0)
EIT1: 8 Hz interrupt mask register (FFE6H•D1)
EIT2: 2 Hz interrupt mask register (FFE6H•D2)
EIT3: 1 Hz interrupt mask register (FFE6H•D3)
These registers are used to select whether to mask the clock timer interrupt.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

The interrupt mask registers (EIT0, EIT1, EIT2, EIT3) are used to select whether to mask the interrupt to the separate frequencies (32 Hz, 8 Hz, 2 Hz, 1 Hz).
At initial reset, these registers are set to "0".

IT0: 32 Hz interrupt factor flag (FFF6H•D0)
IT1: 8 Hz interrupt factor flag (FFF6H•D1)
IT2: 2 Hz interrupt factor flag (FFF6H•D2)
IT3: 1 Hz interrupt factor flag (FFF6H•D3)
These flags indicate the status of the clock timer interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

The interrupt factor flags (IT0, IT1, IT2, IT3) correspond to the clock timer interrupts of the respective frequencies (32 Hz, 8 Hz, 2 Hz, 1 Hz). The software can judge from these flags whether there is a clock timer interrupt. However, even if the interrupt is masked, the flags are set to "1" at the falling edge of the signal.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.7.5 Programming notes

(1) Be sure to read timer data in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.8 Stopwatch Timer

4.8.1 Configuration of stopwatch timer

The S1C63808 has a 1/1,000 sec stopwatch timer. The stopwatch timer is configured of a 3-stage, 4-bit BCD counter serving as the input clock of a 1,000 Hz signal output from the prescaler. Data can be read out four bits (1/1,000 sec, 1/100 sec and 1/10 sec) at a time by the software.
In addition it has a direct input function that controls the stopwatch timer RUN/STOP and LAP using the input ports K00 and K01.
Figure 4.8.1.1 is the block diagram of the stopwatch timer.

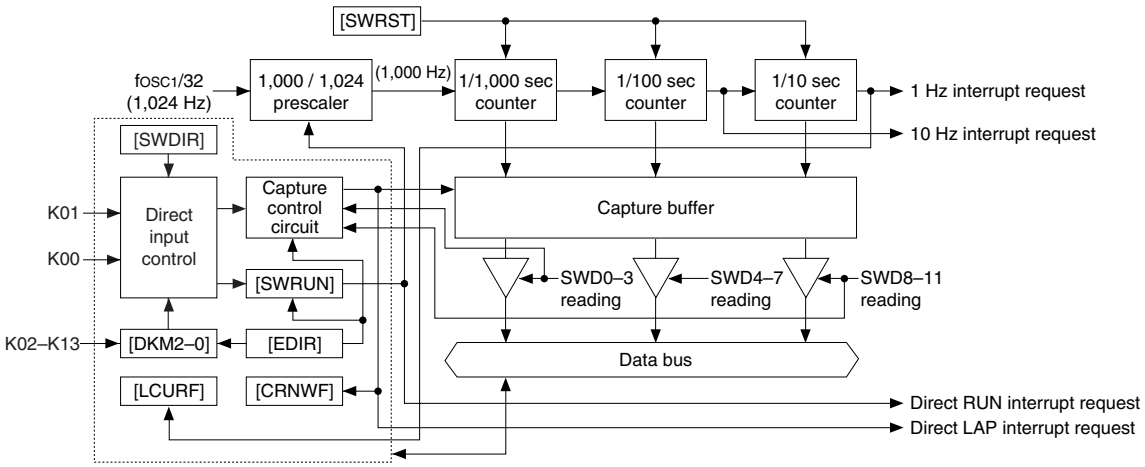


Fig. 4.8.1.1 Block diagram of stopwatch timer

The stopwatch timer can be used as a separate timer from the clock timer. In particular, digital watch stopwatch functions can be realized easily with software.

4.8.2 Counter and prescaler

The stopwatch timer is configured of four-bit BCD counters SWD0–3, SWD4–7 and SWD8–11.
The counter SWD0–3, at the stage preceding the stopwatch timer, has a 1,000 Hz signal generated by the prescaler for the input clock. It counts up every 1/1,000 sec, and generates 100 Hz signal. The counter SWD4–7 has a 100 Hz signal generated by the counter SWD0–3 for the input clock. It count-up every 1/100 sec, and generated 10 Hz signal. The counter SWD8–11 has an approximated 10 Hz signal generated by the counter SWD4–7 for the input clock. It count-up every 1/10 sec, and generated 1 Hz signal.

The prescaler inputs a 1,024 Hz clock dividing fOSC1 (output from the OSC1 oscillation circuit), and outputs 1,000 Hz counting clock for SWD0–3. To generate a 1,000 Hz clock from 1,024 Hz, 24 pulses from 1,024 pulses that are input to the prescaler every second are taken out.
When the counter becomes the value indicated below, one pulse (1,024 Hz) that is input immediately after to the prescaler will be pulled out.

<Counter value (msec) in which the pulse correction is performed>
39, 79, 139, 179, 219, 259, 299, 319, 359, 399, 439, 479, 539, 579, 619, 659, 699, 719, 759, 799, 839, 879, 939, 979

Figure 4.8.2.1 shows the operation of the prescaler.

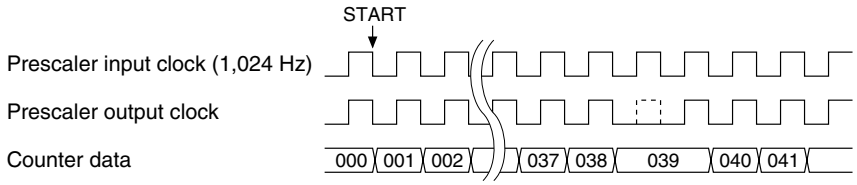


Fig. 4.8.2.1 Timing of the prescaler operation

For the above reason, the counting clock is 1,024 Hz (0.9765625 msec) except during pulse correction. Consequently, frequency of the prescaler output clock (1,000 Hz), 100 Hz generated by SWD0–3 and 10 Hz generated by SWD4–7 are approximate values.

4.8.3 Capture buffer and hold function

The stopwatch data, 1/1,000 sec, 1/100 sec and 1/10 sec, can be read from SWD0–3 (FF7DH), SWD4–7 (FF7EH) and SWD8–11 (FF7FH), respectively. The counter data are latched in the capture buffer when reading, and are held until reading of three words is completed. For this reason, correct data can be read even when a carry from lower digits occurs during reading the three words. Further, three counter data are latched in the capture buffer at the same time when SWD0–3 (1/1,000 sec) is read. The data hold is released when SWD8–11 (1/10 sec) reading is completed. Therefore, data should be read in order of SWD0–3 → SWD4–7 → SWD8–11. If SWD4–7 or SWD8–11 is first read when data have not been held, the hold function does not work and data in the counter is directly read out. When data that has not been held is read in the stopwatch timer RUN status, you cannot judge whether it is correct or not.

The stopwatch timer has a LAP function using an external key input (explained later). The capture buffer is also used to hold LAP data. In this case, data is held until SWD8–11 is read. However, when a LAP input is performed before completing the reading, the content of the capture buffer is renewed at that point. Remaining data that have not been read become invalid by the renewal, and the hold status is not released if SWD8–11 is read. When SWD8–11 is read after the capture buffer is updated, the capture renewal flag is set to "1" at that point. In this case, it is necessary to read from SWD0–3 again. The capture renewal flag is renewed by reading SWD8–11.

Figure 4.8.3.1 shows the timing for data holding and reading.

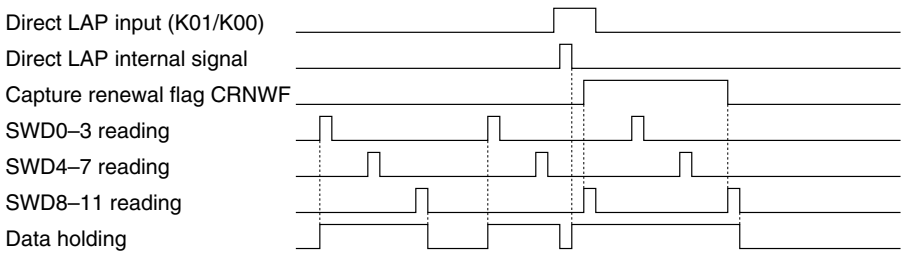


Fig. 4.8.3.1 Timing for data holding and reading

4.8.4 Stopwatch timer RUN/STOP and reset

RUN/STOP control and reset of the stopwatch timer can be done by the software.

Stopwatch timer RUN/STOP

The stopwatch timer enters the RUN status when "1" is written to SWRUN, and the STOP status when "0" is written. In the STOP status, the timer data is maintained until the next RUN status or resets timer. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count. The RUN/STOP operation of the stopwatch timer by writing to the SWRUN register is performed in synchronization with the falling edge of the 1,024 Hz same as the prescaler input clock. The SWRUN register can be read, and in this case it indicates the operating status of the stopwatch timer.

Figure 4.8.4.1 shows the operating timing when controlling the SWRUN register.

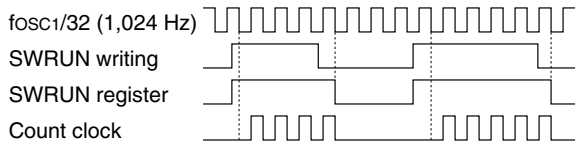


Fig. 4.8.4.1 Operating timing when controlling SWRUN

When the direct input function (explained in next section) is set, RUN/STOP control is done by an external key input. In this case, SWRUN becomes read only register that indicates the operating status of the stopwatch timer.

Stopwatch timer reset

The stopwatch timer is reset when "1" is written to SWRST. With this, the counter value is cleared to "000". Since this resetting does not affect the capture buffer, data that has been held in the capture buffer is not cleared and is maintained as is. When the stopwatch timer is reset in the RUN status, counting restarts from count "000". Also, in the STOP status the reset data "000" is maintained until the next RUN.

4.8.5 Direct input function and key mask

The stopwatch timer has a direct input function that can control the RUN/STOP and LAP operation of the stopwatch timer by external key input. This function is set by writing "1" to the EDIR register. When EDIR is set to "0", only the software control is possible as explained in the previous section.

Input port configuration

In the direct input function, the input ports K00 and K01 are used as the RUN/STOP and LAP input ports. The key assignment can be selected using the SWDIR register.

Table 4.8.5.1 RUN/STOP and LAP input ports

SWDIR	K00	K01
0	RUN/STOP	LAP
1	LAP	RUN/STOP

Direct RUN

When the direct input function is selected, RUN/STOP operation of the stopwatch timer can be controlled by using the key connected to the input port K00/K01 (selected by SWDIR). K00/K01 works as a normal input port, but the input signal is sent to the stopwatch control circuit. The key input signal from the K00/K01 port works as a toggle switch. When it is input in STOP status, the stopwatch timer runs, and in RUN status, the stopwatch timer stops. RUN/STOP status of the stopwatch timer can be checked by reading the SWRUN register. An interrupt is generated by direct RUN input.

The sampling for key input signal is performed at the falling edge of 1,024 Hz signal same as the SWRUN control. The chattering judgment is performed at the point where the key turns off, and a chattering less than 46.8–62.5 msec is removed. Therefore, more time is needed for an interval between RUN and STOP key inputs.

Figure 4.8.5.1 shows the operating timing for the direct RUN input.

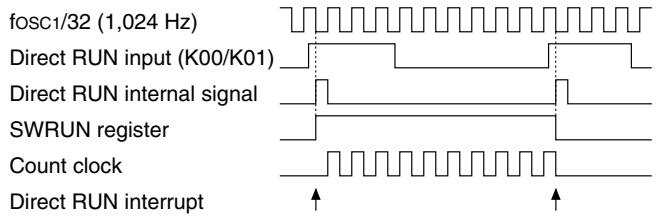


Fig. 4.8.5.1 Operating timing for direct RUN input

Direct LAP

Control for the LAP can also be done by key input same as the direct RUN. When the direct input function is selected, the input port K01/K00 (selected by SWDIR) becomes the LAP key input port. Sampling for the input signal and the chattering judgment are the same as a direct RUN.
By entering the LAP key, the counter data at that point is latched into the capture buffer and is held. The counter continues counting operation. Furthermore, an interrupt occurs by direct LAP input.
As stated above, the capture buffer data is held until SWD8–11 is read. If the LAP key is input when data has been already held, it renews the content of the capture buffer. When SWD8–11 is read after renewing, the capture renewal flag is set to "1". In this case, the hold status is not released by reading SWD8–11, and it continues. Normally the LAP data should be read after the interrupt is generated. After that, be sure to check the capture renewal flag. When the capture renewal flag is set, renewed data is held in the capture buffer. So it is necessary to read from SWD0–3 again.
The stopwatch timer sets the 1 Hz interrupt factor flag ISW1 to "1" when requiring a carry-up to 1-sec digit by an SWD8–11 overflow. If the capture buffer shifts into hold status (when SWD0–3 is read or when LAP is input) while the 1 Hz interrupt factor flag ISW1 is set to "1", the lap data carry-up request flag LCURF is set to "1" to indicate that a carry-up to 1-sec digit is required for the processing of LAP input. In normal software processing, LAP processing may take precedence over 1-sec or higher digits processing by a 1 Hz interrupt, therefore carry-up processing using this flag should be used for time display in the LAP processing to prevent the 1-sec digit data decreasing by 1 second. This flag is renewed when the capture buffer shifts into hold status.
Figure 4.8.5.2 shows the operating timing for the direct LAP input, and Figure 4.8.5.3 shows the timings for data holding and reading during a direct LAP input and reading.

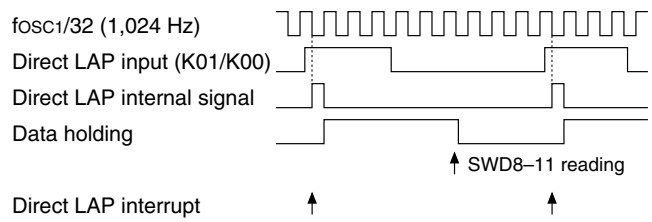


Fig. 4.8.5.2 Operating timing for direct LAP input

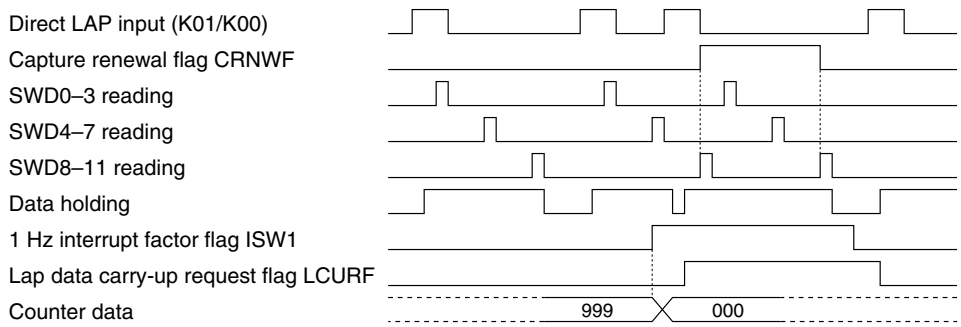


Fig. 4.8.5.3 Timing for data holding and reading during direct LAP input

Key mask

In stopwatch applications, some functions may be controlled by a combination of keys including direct RUN or direct LAP. For instance, the RUN key can be used for other functions, such as reset and setting a watch, by pressing the RUN key with another key. In this case, the direct RUN function or direct LAP function must be invalid so that it does not function. For this purpose, the key mask function is set so that it judges concurrence of input keys and invalidates RUN and LAP functions. A combination of the key inputs for this judgment can be selected using the DKM0–DKM2 registers.

Table 4.8.5.2 Key mask selection

DKM2	DKM1	DKM0	Mask key combination
0	0	0	None (at initial reset)
0	0	1	K02
0	1	0	K02, K03
0	1	1	K02, K03, K10
1	0	0	K10
1	0	1	K10, K11
1	1	0	K10, K11, K12
1	1	1	K10, K11, K12, K13

RUN or LAP inputs become invalid in the following status.

1. The RUN or LAP key is pressed when one or more keys that are included in the selected combination (here in after referred to as mask) are held down.
2. The RUN or LAP key has been pressed when the mask is released.

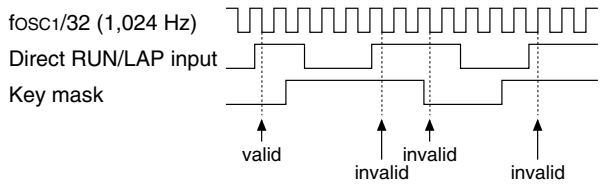


Fig. 4.8.5.4 Operation of key mask

RUN or LAP inputs become valid in the following status.

1. Either the RUN or LAP key is pressed independently if no other key is been held down.
2. Both the RUN and LAP keys are pressed at the same time if no other key is held down. (RUN and LAP functions are effective.)
3. The RUN or LAP key is pressed if either is held down. (RUN and LAP functions are effective.)
4. Either the RUN or LAP key and the mask key are pressed at the same time if no other key is held down.
5. Both the RUN and LAP keys and the mask key are pressed at the same time if no other key is held down. (RUN and LAP functions are effective.)

* Simultaneous key input is referred to as two or more key inputs are sampled at the same falling edge of 1,024 Hz clock.

4.8.6 Interrupt function

10 Hz and 1 Hz interrupts

The 10 Hz and 1 Hz interrupts can be generated through the overflow of stopwatch timers SWD4–7 and SWD8–11 respectively. Also, software can set whether to separately mask the frequencies described earlier.

Figure 4.8.6.1 is the timing chart for the counters.

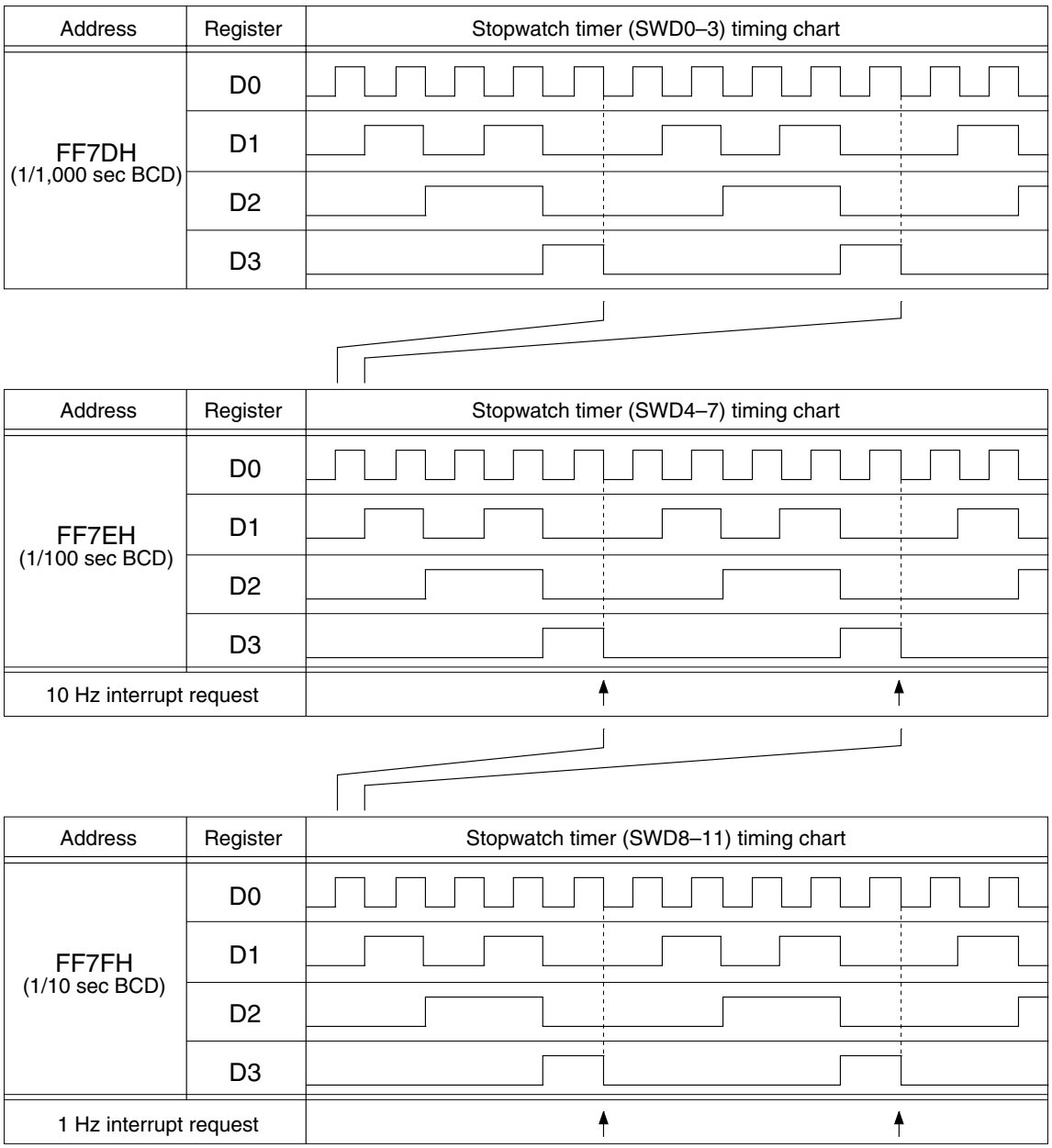


Fig. 4.8.6.1 Timing chart for counters

As shown in Figure 4.8.6.1, the interrupts are generated by the overflow of their respective counters ("9" changing to "0"). Also, at this time the corresponding interrupt factor flag (ISW10, ISW1) is set to "1". The respective interrupts can be masked separately through the interrupt mask registers (EISW10, EISW1). However, regardless of the setting of the interrupt mask registers, the interrupt factor flags are set to "1" by the overflow of their corresponding counters.

Direct RUN and direct LAP interrupts

When the direct input function is selected, the direct RUN and direct LAP interrupts can be generated. The respective interrupts occur at the rising edge of the internal signal for direct RUN and direct LAP after sampling the direct input signal in the falling edge of 1,024 Hz signal. Also, at this time the corresponding interrupt factor flag (IRUN, ILAP) is set to "1".
The respective interrupts can be masked separately through the interrupt mask registers (EIRUN, EILAP). However, regardless of the setting of the interrupt mask registers, the interrupt factor flags are set to "1" by the inputs of the RUN and LAP.

The direct RUN and LAP functions use the K00 and K01 ports. Therefore, the direct input interrupt and the K00–K03 inputs interrupt may generate at the same time depending on the interrupt condition setting for the input port K00–K03. Consequently, when using the direct input interrupt, set the interrupt selection registers SIK00 and SIK01 to "0" so that the input interrupt does not generate by K00 and K01 inputs.

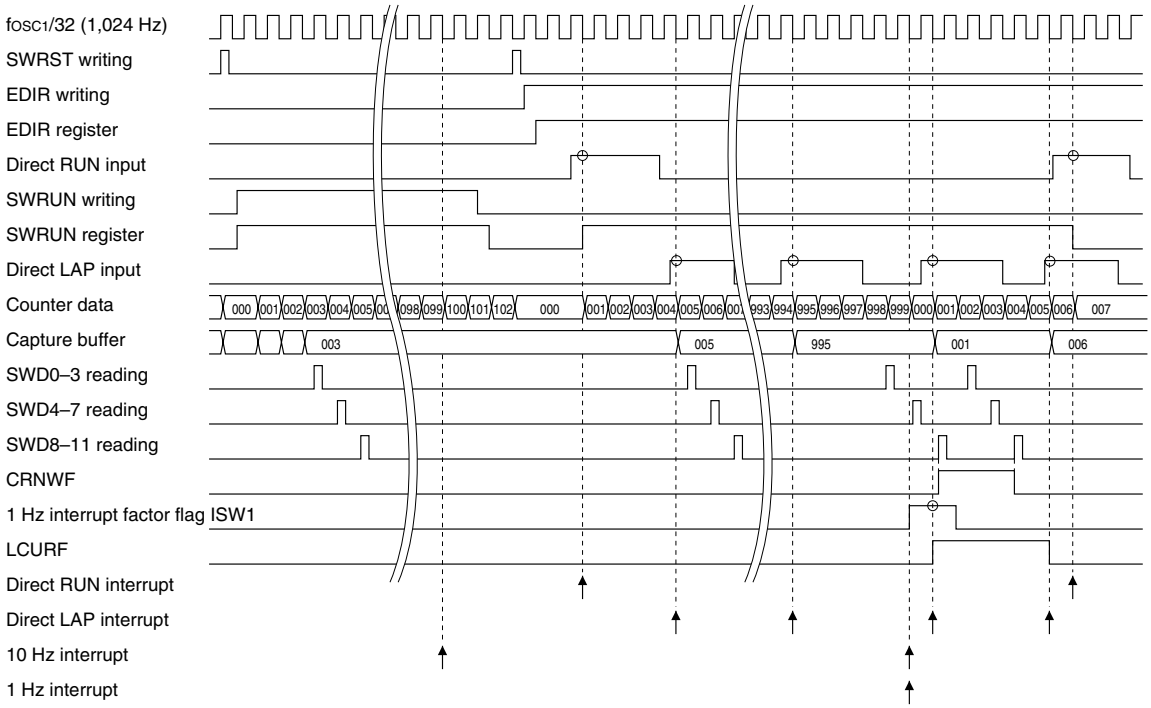


Fig. 4.8.6.2 Timing chart for stopwatch timer

4.8.7 I/O memory of stopwatch timer

Table 4.8.7.1 shows the I/O addresses and the control bits for the stopwatch timer.

Table 4.8.7.1 Control bits of stopwatch timer

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF06H	FOUTE	SWDIR	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT output enable
					SWDIR	0			Stopwatch direct input switch
									0: K00=Run/Stop, K01=Lap 1: K00=Lap, K01=Run/Stop
	R/W				FOFQ1	0			FOUT frequency selection [FOFQ1, 0] 0 1 2 3
					FOFQ0	0			Frequency fOSC1/64 fOSC1/8 fOSC1 fOSC3
FF7BH	EDIR	DKM2	DKM1	DKM0	EDIR	0	Enable	Disable	Direct input enable
					DKM2	0			Key mask selection [DKM2, 1, 0] 0 1 2 3
	R/W				DKM1	0			Key mask None K02 K02–03 K02–03,10
					DKM0	0			[DKM2, 1, 0] 4 5 6 7
									Key mask K10 K10–11 K10–12 K10–13
FF7CH	LCURF	CRNWF	SWRUN	SWRST	LCURF	0	Request	No	Lap data carry-up request flag
					CRNWF	0	Renewal	No	Capture renewal flag
	R		R/W	W	SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
					SWRST*3	Reset	Reset	Invalid	Stopwatch timer reset (writing)
FF7DH	SWD3	SWD2	SWD1	SWD0	SWD3	0			Stopwatch timer data BCD (1/1000 sec)
					SWD2	0			
	R				SWD1	0			
					SWD0	0			
FF7EH	SWD7	SWD6	SWD5	SWD4	SWD7	0			Stopwatch timer data BCD (1/100 sec)
					SWD6	0			
	R				SWD5	0			
					SWD4	0			
FF7FH	SWD11	SWD10	SWD9	SWD8	SWD11	0			Stopwatch timer data BCD (1/10 sec)
					SWD10	0			
	R				SWD9	0			
					SWD8	0			
FFE8H	EIRUN	EILAP	EISW1	EISW10	EIRUN	0	Enable	Mask	Interrupt mask register (Stopwatch direct RUN)
					EILAP	0	Enable	Mask	Interrupt mask register (Stopwatch direct LAP)
	R/W				EISW1	0	Enable	Mask	Interrupt mask register (Stopwatch timer 1 Hz)
					EISW10	0	Enable	Mask	Interrupt mask register (Stopwatch timer 10 Hz)
FFF8H	IRUN	ILAP	ISW1	ISW10	IRUN	0	(R)	(R)	Interrupt factor flag (Stopwatch direct RUN)
					ILAP	0	Yes	No	Interrupt factor flag (Stopwatch direct LAP)
	R/W				ISW1	0	(W)	(W)	Interrupt factor flag (Stopwatch timer 1 Hz)
					ISW10	0	Reset	Invalid	Interrupt factor flag (Stopwatch timer 10 Hz)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

SWD0–SWD3: Stopwatch timer data 1/1,000 sec (FF7DH)

Data (BCD) of the 1/1,000 sec column of the capture buffer can be read out.
The hold function of the capture buffer works by reading this data.
These 4 bits are read-only, and cannot be used for writing operations.
At initial reset, the timer data is set to "0".

SWD4–SWD7: Stopwatch timer data 1/100 sec (FF7EH)

Data (BCD) of the 1/100 sec column of the capture buffer can be read out. These 4 bits are read-only, and cannot be used for writing operations.
At initial reset, the timer data is set to "0".

SWD8–SWD11: Stopwatch timer data 1/10 sec (FF7FH)

Data (BCD) of the 1/10 sec column of the capture buffer can be read out. These 4 bits are read-only, and cannot be used for writing operations.
At initial reset, the timer data is set to "0".

Note: Be sure to data reading in the order of SWD0–3 → SWD4–7 → SWD8–11.

EDIR: Direct input function enable register (FF7BH•D3)

Enables the direct input (RUN/LAP) function.

When "1" is written: Enabled
When "0" is written: Disabled
Reading: Valid

The direct input function is enabled by writing "1" to EDIR, and then RUN/STOP and LAP control can be done by external key input. When "0" is written, the direct input function is disabled, and the stopwatch timer is controlled by the software only.
Further the function switching is actually done by synchronizing with the falling edge of $f_{OSC1}/32$ (1,024 Hz) after the data is written to this register (after 977 µsec maximum).
At initial reset, this register is set to "0".

SWDIR: Direct input switch register (FF06H•D2)

Switches the direct-input key assignment for the K00 and K01 ports.

When "1" is written: K00 = LAP, K01 = RUN/STOP
When "0" is written: K00 = RUN/STOP, K01 = LAP
Reading: Valid

The direct-input key assignment is selected using this register. The K00 and K01 port statuses are input to the stopwatch timer as the RUN/STOP and LAP inputs according to this selection.
At initial reset, this register is set to "0".

DKM0–DKM2: Direct key mask selection register (FF7BH•D0–D2)

Selects a combination of the key inputs for concurrence judgment with RUN and LAP inputs when the direct input function is set.

Table 4.8.7.2 Key mask selection

DKM2	DKM1	DKM0	Mask key combination
0	0	0	None (at initial reset)
0	0	1	K02
0	1	0	K02, K03
0	1	1	K02, K03, K10
1	0	0	K10
1	0	1	K10, K11
1	1	0	K10, K11, K12
1	1	1	K10, K11, K12, K13

When the concurrence is detected, RUN and LAP inputs cannot be accepted until the concurrence is released.
At initial reset, this register is set to "0".

SWRST: Stopwatch timer reset (FF7CH•D0)

This bit resets the stopwatch timer.

When "1" is written: Stopwatch timer reset
When "0" is written: No operation
Reading: Always "0"

The stopwatch timer is reset when "1" is written to SWRST. When the stopwatch timer is reset in the RUN status, operation restarts immediately. Also, in the STOP status the reset data is maintained.
Since this reset does not affect the capture buffer, the capture buffer data in hold status is not cleared and is maintained.
This bit is write-only, and is always "0" at reading.

SWRUN: Stopwatch timer RUN/STOP (FF7CH•D1)

This register controls the RUN/STOP of the stopwatch timer, and the operating status can be monitored by reading this register.

• ***When writing data***

When "1" is written: RUN
When "0" is written: STOP

The stopwatch timer enters the RUN status when "1" is written to SWRUN, and the STOP status when "0" is written. In the STOP status, the timer data is maintained until the next RUN status or resets timer. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count. RUN/STOP control with this register is valid only when the direct input function is set to disable. When the direct input function is set, it becomes invalid.

• ***When reading data***

When "1" is read: RUN
When "0" is read: STOP

Reading is always valid regardless of the direct input function setting. "1" is read when the stopwatch timer is in the RUN status, and "0" is read in the STOP status.
At initial reset, this register is set to "0".

LCURF: Lap data carry-up request flag (FF7CH•D3)

This flag indicates a carry that has been generated to 1 sec-digit when the data is held. Note that this flag is invalid when the direct input function is disabled.

When "1" is read: Carry is required
When "0" is read: Carry is not required
Writing: Invalid

If the capture buffer shifts into hold status while the 1 Hz interrupt factor flag ISW1 is set to "1", LCURF is set to "1" to indicate that a carry-up to 1-sec digit is required. When performing a processing such as a LAP input preceding with 1 Hz interrupt processing, read this flag before processing and check whether carry-up is needed or not.
This flag is renewed (set/reset) every time the capture buffer shifts into hold status.
At initial reset, this flag is set to "0".

CRNWF: Capture renewal flag (FF7CH•D2)

This flag indicates that the content of the capture buffer has been renewed.

When "1" is read: Renewed
When "0" is read: Not renewed
Writing: Invalid

The content of the capture buffer is renewed if the LAP key is input when the data held into the capture buffer has not yet been read. Reading SWD8–11 in that status sets this flag to "1", and the hold status is maintained. Consequently, when data that is held by a LAP input is read, read this flag after reading the SWD8–11 and check whether the data has been renewed or not.
This flag is renewed when SWD8–11 is read.
At initial reset, this flag is set to "0".

EIRUN, EILAP, EISW1, EISW10: Interrupt mask registers (FFE8H)

These registers are used to select whether to mask the stopwatch timer interrupt.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

The interrupt mask registers EIRUN, EILAP, EISW1 and EISW10 are used to separately select whether to mask the direct RUN, direct LAP, 1 Hz and 10 Hz interrupts.
At initial reset, these registers are set to "0".

IRUN, ILAP, ISW1, ISW10: Interrupt factor flags (FFF8H)

These flags indicate the status of the stopwatch timer interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

The interrupt factor flags IRUN, ILAP, ISW1 and ISW10 correspond to the direct RUN, direct LAP, 1 Hz and 10 Hz interrupts respectively. The software can judge from these flags whether there is a stopwatch timer interrupt. However, even if the interrupt is masked, the flags are set to "1" when the timing condition is established.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.8.8 Programming notes

(1) The interrupt factor flag should be reset after resetting the stopwatch timer.

(2) Be sure to data reading in the order of SWD0–3 → SWD4–7 → SWD8–11.

(3) When data that is held by a LAP input is read, read the capture buffer renewal flag CRNWF after reading the SWD8–11 and check whether the data has been renewed or not.

(4) When performing a processing such as a LAP input preceding with 1 Hz interrupt processing, read the LAP data carry-up request flag LCURF before processing and check whether carry-up is needed or not.

(5) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.9 Programmable Timer

4.9.1 Configuration of programmable timer

The S1C63808 has two 8-bit programmable timer systems (timer 0 and timer 1) built-in.
The timers are composed of 8-bit presettable down counters and they can be used as 8 bits × 2 channels or 16 bits × 1 channel of programmable timers. Timer 0 also has an event counter function using the K13 input port terminal.
Figure 4.9.1.1 shows the configuration of the programmable timer.

The programmable timer is designed to count down from the initial value set in the counter with software. An underflow according to the initial value occurs by counting down and is used for the following functions:

- Presetting the initial value to the counter to generate the periodical underflow signal
- Generating an interrupt
- Generating a TOUT signal output from the R02 output port terminal
- Generating the synchronous clock source for the serial interface (timer 1 underflow is used, and it is possible to set the transfer rate)

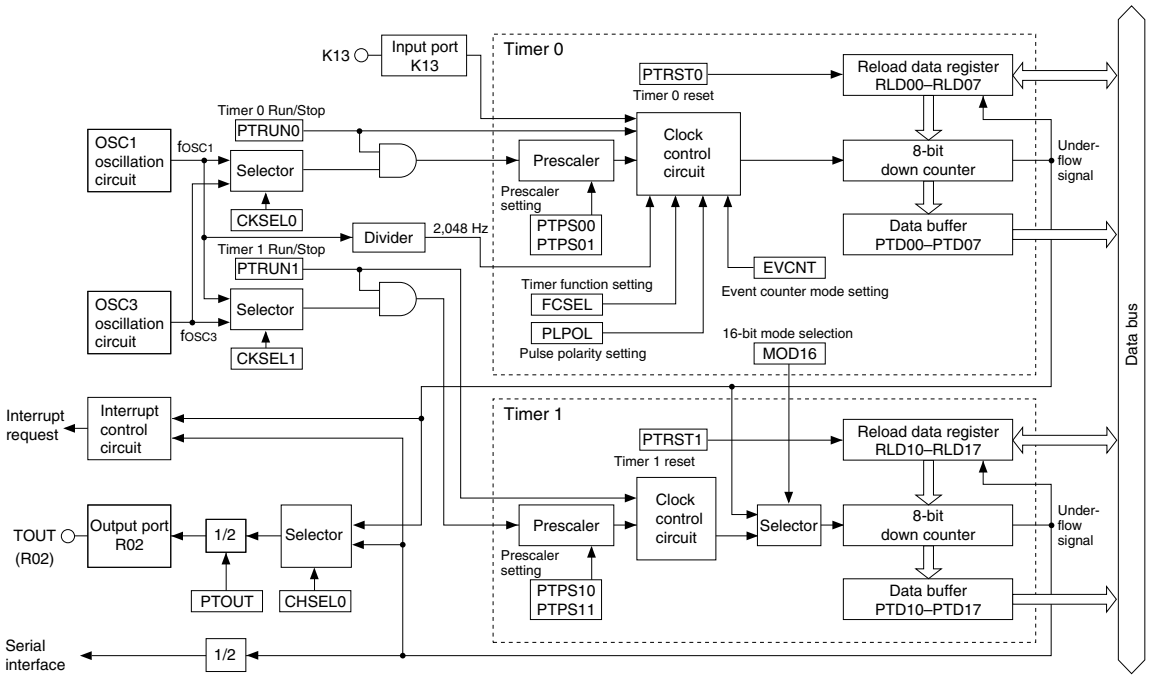


Fig. 4.9.1.1 Configuration of programmable timer

Note: If the TOUT terminal is used to drive an external component that consumes a large amount of current such as a bipolar transistor, design the pattern of traces on the printed circuit board so that the operation of the external component does not affect the IC power supply. Refer to <Output Terminals> in Section 5.3, "Precautions on Mounting", for more information.

4.9.2 Basic count operation

This section explains the basic count operation when each timer is used as an individual 8-bit timer.

Each timer has an 8-bit down counter and an 8-bit reload data register.
The reload data register RLDx0–RLDx7 (x = timer number) is used to set the initial value to the down counter.
By writing "1" to the timer reset bit PTRSTx, the down counter loads the initial value set in the reload register. Therefore, down-counting is executed from the stored initial value by the input clock.
The PTRUNx register is provided to control the RUN/STOP for each timer. By writing "1" to this register after presetting the reload data to the down counter, the down counter starts counting down. Writing "0" stops the input count clock and the down counter stops counting. This control (RUN/STOP) does not affect the counter data. The counter maintains its data while stopped, and can restart counting continuing from that data.
The counter data can be read via the data buffer PTDx0–PTDx7 in optional timing. However, the counter has the data hold function the same as the clock timer, that holds the high-order data (PTDx4–PTDx7) when the low-order data (PTDx0–PTDx3) is read in order to prevent the borrowing operation between low- and high-order reading, therefore be sure to read the low-order data first.
The counter reloads the initial value set in the reload data register when an underflow occurs through the count down. It continues counting down from the initial value after reloading.
In addition to reloading the counter, this underflow signal controls the interrupt generation, pulse (TOUT signal) output and clock supplying to the serial interface.

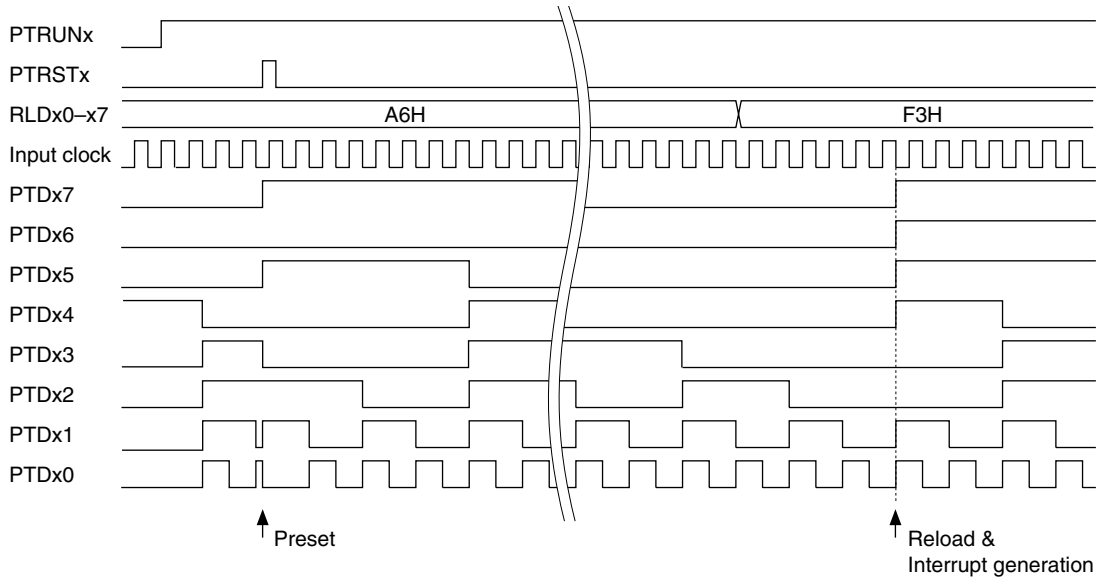


Fig. 4.9.2.1 Basic operation timing of down counter

4.9.3 Setting the input clock

A prescaler is provided for each timer. The prescaler generates the input clock for the timer by dividing the source clock supplied from the OSC1 or OSC3 oscillation circuit.
The source clock (OSC1 or OSC3) and the division ratio of the prescaler can be selected with software for each timer individually.
The input clock is set in the following sequence.

Selection of source clock

Select the source clock input to each prescaler from either OSC1 or OSC3. This selection is done using the source clock selection register CKSELx; when "0" is written to the register, OSC1 is selected and when "1" is written, OSC3 is selected.
When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation on, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time at least 5 msec from turning the circuit on until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit on to starting the programmable timer. Refer to Section 4.3, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit.
At initial reset, the OSC3 oscillation circuit is set in off state.

Selection of prescaler division ratio

Select the division ratio for each prescaler from among 4 types. This selection is done using the prescaler division ratio selection register PTPSx0/PTPSx1. Table 4.9.3.1 shows the correspondence between the setting value and the division ratio.

Table 4.9.3.1 Selection of prescaler division ratio

PTPSx1	PTPSx0	Prescaler division ratio
1	1	Source clock / 256
1	0	Source clock / 32
0	1	Source clock / 4
0	0	Source clock / 1

By writing "1" to the PTRUNx register, the prescaler inputs the source clock and outputs the clock divided by the selected division ratio. The counter starts counting down by inputting the clock.

4.9.4 Event counter mode (timer 0)

Timer 0 has an event counter function that counts an external clock input to the input port K13. This function is selected by writing "1" to timer 0 counter mode selection register EVCNT. At initial reset, EVCNT is set to "0" and timer 0 is configured as a normal timer that counts the internal clock.
In the event counter mode, the clock is supplied to timer 0 from outside the IC, therefore, the settings of the timer 0 prescaler division ratio selection register PTPS00–PTPS01 and the settings of the timer 0 source clock selection register CKSEL0 become invalid.
Count down timing can be selected from either the falling or rising edge of the input clock using the timer 0 pulse polarity selection register PLPOL. When "0" is written to the PLPOL register, the falling edge is selected, and when "1" is written, the rising edge is selected. The count down timing is shown in Figure 4.9.4.1.

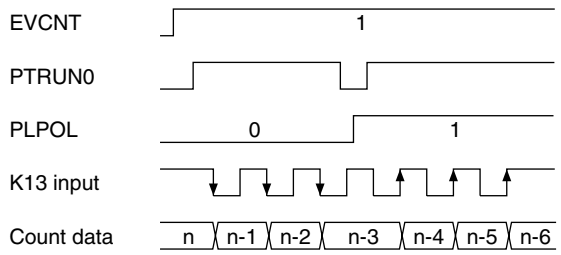


Fig. 4.9.4.1 Timing chart in event counter mode

The event counter mode also allows use of a noise reject function to eliminate noise such as chattering on the external clock (K13 input signal). This function is selected by writing "1" to the timer 0 function selection register FCSEL.
When "with noise rejector" is selected, an input pulse width for both low and high levels must be 0.98 msec∗ or more to count reliably. The noise rejector allows the counter to input the clock at the second falling edge of the internal 2,048 Hz∗ signal after changing the input level of the K13 input port terminal. Consequently, the pulse width of noise that can reliably be rejected is 0.48 msec∗ or less.
(∗: f_{OSC1} = 32.768 kHz)
Figure 4.9.4.2 shows the count down timing with noise rejector.

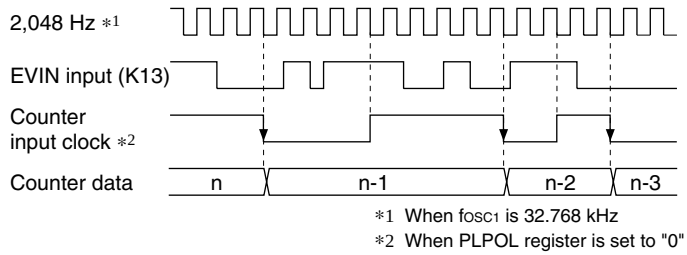


Fig. 4.9.4.2 Count down timing with noise rejector

The operation of the event counter mode is the same as the normal timer except it uses the K13 input as the clock. Refer to Section 4.9.2, "Basic count operation" for basic operation and control.

4.9.5 16-bit timer (timer 0 + timer 1)

Timers 0 and 1 can be used as a 16-bit timer.
To use the 16-bit timer, write "1" to the timer 0 16-bit mode selection register MOD16.
The 16-bit timer is configured with timer 0 for low-order byte and timer 1 for high-order byte as shown in Figure 4.9.5.1.

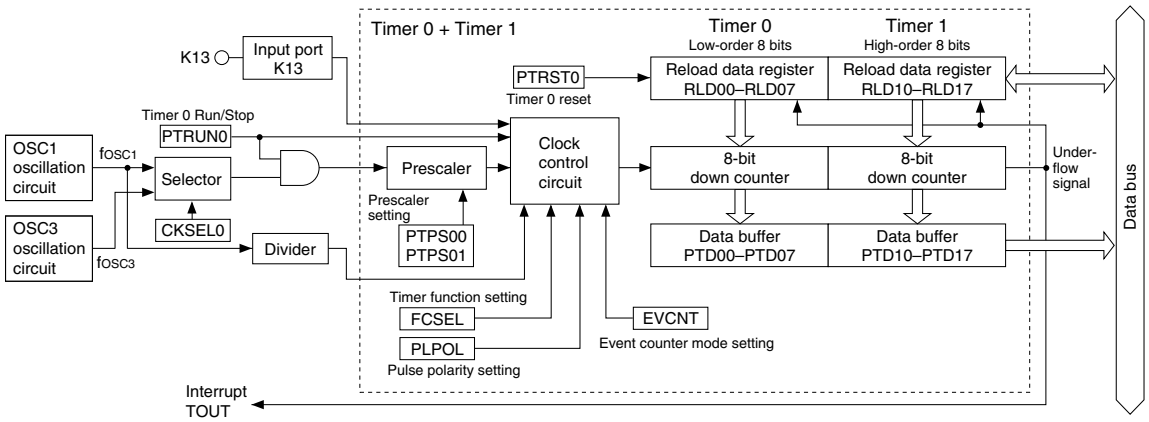


Fig. 4.9.5.1 Configuration of 16-bit timer

The registers for timer 0 are used to control the timer. Thus the event counter function can also be used. Timer 1 operates with the timer 0 underflow signal as the count clock, so the clock and RUN/STOP control registers for timer 1 become invalid.
The counter data in 16-bit mode must be read in the order below.
PTD00–PTD03 → PTD04–PDT07 → PTD10–PTD13 → PTD14–PTD17

4.9.6 Interrupt function

The programmable timer can generate an interrupt due to an underflow of each timer. See Figure 4.9.2.1 for the interrupt timing.

An underflow of timer x sets the corresponding interrupt factor flag IPTx to "1", and generates an interrupt. The interrupt can also be masked by setting the corresponding interrupt mask register EIPTx. However, the interrupt factor flag is set to "1" by an underflow of the corresponding timer regardless of the interrupt mask register setting.

When timers 0 and 1 are used as a 16-bit timer, an interrupt is generated by an underflow of timer 1. In this case, IPT0 is not set to "1" by a timer 0 underflow.

4.9.7 Control of TOUT output

The programmable timer can generate a TOUT signal due to an underflow of a timer. The TOUT signal is generated by dividing the underflows in 1/2. It is possible to select which timer's underflow is to be used by the TOUT output channel selection register CHSEL0.

Table 4.9.7.1 Selecting a timer for TOUT output

CHSEL0	TOUT output timer
1	Timer 1
0	Timer 0

Select timer 1 when generating the TOUT signal from the 16-bit timer output.

The TOUT signal can be output from the R02 output port terminal. Programmable clocks can be supplied to external devices.
Figure 4.9.7.1 shows the configuration of the output port R02.

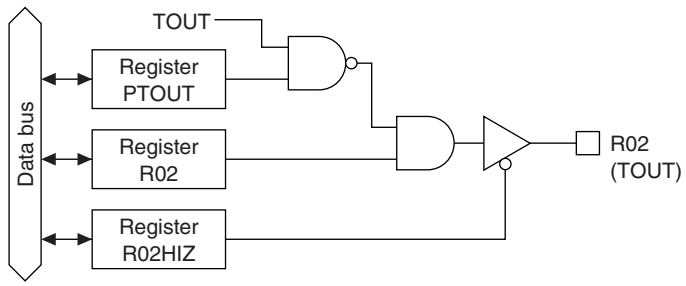


Fig. 4.9.7.1 Configuration of R02

The output of a TOUT signal is controlled by the PTOUT register. When "1" is written to the PTOUT register, the TOUT signal is output from the R02 output port terminal and when "0" is written, the terminal goes to a high (V_{DD}) level. However, the data register R02 must always be "1" and the high impedance control register R02HIZ must always be "0" (data output state).

Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned on and off by setting the register.
Figure 4.9.7.2 shows the output waveform of the TOUT signal.

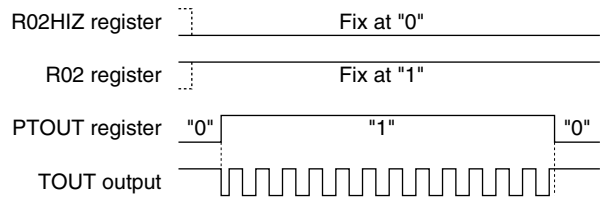


Fig. 4.9.7.2 Output waveform of the TOUT signal

4.9.8 Transfer rate setting for serial interface

The signal that is made from underflows of timer 2 by dividing them in 1/2, can be used as the clock source for the serial interface.
The programmable timer outputs the clock to the serial interface by setting timer 1 into RUN state (PTRUN1 = "1", or PTRUN0 = "1" in 16-bit mode). It is not necessary to control with the PTOUT register.

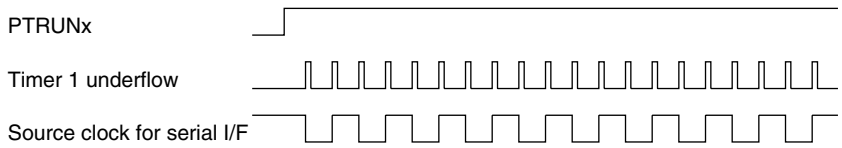


Fig. 4.9.8.1 Synchronous clock of serial interface

A setting value for the RLD1x register according to a transfer rate is calculated by the following expression:

RLD1x = fosc / (32 ∗ bps ∗ division ratio of the prescaler) - 1

fosc: Oscillation frequency (OSC1/OSC3)
bps: Transfer rate
(00H can be set to RLD1x)

Be aware that the maximum clock frequency for the serial interface is limited to 2 MHz when OSC3 is used as the clock source.

4.9.9 I/O memory of programmable timer

Table 4.9.9.1 shows the I/O addresses and the control bits for the programmable timer.

Table 4.9.9.1 Control bits of programmable timer

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FFC0H	MOD16	EVCNT	FCSEL	PLPOL	MOD16	0	16 bits	8 bits	16-bit mode selection
					EVCNT	0	Event ct.	Timer	Timer 0 counter mode selection
					FCSEL	0	With NR	No NR	Timer 0 function selection (for event counter mode)
	R/W				PLPOL	0	↑	↓	Timer 0 pulse polarity selection (for event counter mode)
FFC1H	CHSEL0	PTOUT	CKSEL1	CKSEL0	CHSEL0	0	Timer 1	Timer 0	TOUT output selection
					PTOUT	0	On	Off	TOUT output control
					CKSEL1	0	OSC3	OSC1	Prescaler 1 source clock selection
	R/W				CKSEL0	0	OSC3	OSC1	Prescaler 0 source clock selection
FFC2H	PTPS01	PTPS00	PTRST0	PTRUN0	PTPS01	0			Prescaler 0 division ratio selection [PTPS01, 00]: 0 / 1 / 2 / 3 — Division ratio: 1/1 / 1/4 / 1/32 / 1/256
					PTPS00	0			
					PTRST0*3	– *2	Reset	Invalid	Timer 0 reset (reload)
	R/W		W	R/W	PTRUN0	0	Run	Stop	Timer 0 Run/Stop
FFC3H	PTPS11	PTPS10	PTRST1	PTRUN1	PTPS11	0			Prescaler 1 division ratio selection [PTPS11, 10]: 0 / 1 / 2 / 3 — Division ratio: 1/1 / 1/4 / 1/32 / 1/256
					PTPS10	0			
					PTRST1*3	– *2	Reset	Invalid	Timer 1 reset (reload)
	R/W		W	R/W	PTRUN1	0	Run	Stop	Timer 1 Run/Stop
FFC4H	RLD03	RLD02	RLD01	RLD00	RLD03	0			MSB
					RLD02	0			Programmable timer 0 reload data (low-order 4 bits)
					RLD01	0			
	R/W				RLD00	0			LSB
FFC5H	RLD07	RLD06	RLD05	RLD04	RLD07	0			MSB
					RLD06	0			Programmable timer 0 reload data (high-order 4 bits)
					RLD05	0			
	R/W				RLD04	0			LSB
FFC6H	RLD13	RLD12	RLD11	RLD10	RLD13	0			MSB
					RLD12	0			Programmable timer 1 reload data (low-order 4 bits)
					RLD11	0			
	R/W				RLD10	0			LSB
FFC7H	RLD17	RLD16	RLD15	RLD14	RLD17	0			MSB
					RLD16	0			Programmable timer 1 reload data (high-order 4 bits)
					RLD15	0			
	R/W				RLD14	0			LSB
FFC8H	PTD03	PTD02	PTD01	PTD00	PTD03	0			MSB
					PTD02	0			Programmable timer 0 data (low-order 4 bits)
					PTD01	0			
	R				PTD00	0			LSB
FFC9H	PTD07	PTD06	PTD05	PTD04	PTD07	0			MSB
					PTD06	0			Programmable timer 0 data (high-order 4 bits)
					PTD05	0			
	R				PTD04	0			LSB
FFCAH	PTD13	PTD12	PTD11	PTD10	PTD13	0			MSB
					PTD12	0			Programmable timer 1 data (low-order 4 bits)
					PTD11	0			
	R				PTD10	0			LSB
FFCBH	PTD17	PTD16	PTD15	PTD14	PTD17	0			MSB
					PTD16	0			Programmable timer 1 data (high-order 4 bits)
					PTD15	0			
	R				PTD14	0			LSB
FFE2H	0	0	EIPT1	EIPT0	0 *3	– *2			Unused
					0 *3	– *2			Unused
					EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1)
	R		R/W		EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0)
FFF2H	0	0	IPT1	IPT0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
					IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1)
	R		R/W		IPT0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

CKSEL0: Prescaler 0 source clock selection register (FFC1H•D0)
CKSEL1: Prescaler 1 source clock selection register (FFC1H•D1)
Selects the source clock of the prescaler.

When "1" is written: OSC3 clock
When "0" is written: OSC1 clock
Reading: Valid

The source clock for the prescaler is selected from OSC1 or OSC3. When "0" is written to the CKSELx register, the OSC1 clock is selected as the input clock for the prescaler x (for timer x) and when "1" is written, the OSC3 clock is selected.
When the event counter mode is selected for timer 0, the setting of CKSEL0 becomes invalid.
When timers 0 and 1 are used as a 16-bit timer, the setting of CKSEL1 becomes invalid.
At initial reset, these registers are set to "0".

PTPS00, PTPS01: Timer 0 prescaler division ratio selection register (FFC2H•D2, D3)
PTPS10, PTPS11: Timer 1 prescaler division ratio selection register (FFC3H•D2, D3)
Sets the division ratio of the prescaler as shown in Table 4.9.9.2.

Table 4.9.9.2 Selection of prescaler division ratio

PTPSx1	PTPSx0	Prescaler division ratio
1	1	Source clock / 256
1	0	Source clock / 32
0	1	Source clock / 4
0	0	Source clock / 1

When the event counter mode is selected to timer 0, the setting of PTPS00 and PTPS01 becomes invalid.
When timers 0 and 1 are used as a 16-bit timer, the setting of PTPS10 and PTPS11 becomes invalid.
At initial reset, these registers are set to "0".

MOD16: 16-bit mode selection register (FFC0H•D3)
Selects whether timers 0 and 1 are used as a 16-bit timer or 2 channels of 8-bit timer.

When "1" is written: 16-bit timer
When "0" is written: 8-bit timer
Reading: Valid

When "1" is written to MOD16, a 16-bit timer is configured with timer 0 for low-order byte and timer 1 for high-order byte. Use the timer 0 registers for control. When "0" is written to MOD16, timer 0 and timer 1 are used as independent 8-bit timers.
At initial reset, this register is set to "0".

EVCNT: Timer 0 counter mode selection register (FFC0H•D2)
Selects a counter mode for timer 0.

When "1" is written: Event counter mode
When "0" is written: Timer mode
Reading: Valid

The counter mode for timer 0 is selected from either the event counter mode or timer mode. When "1" is written to the EVCNT register, the event counter mode is selected and when "0" is written, the timer mode is selected.
At initial reset, this register is set to "0".

FCSEL: Timer 0 function selection register (FFC0H•D1)

Selects whether the noise rejector of the clock input circuit will be used or not in the event counter mode.

When "1" is written: With noise rejector
When "0" is written: Without noise rejector
Reading: Valid

When "1" is written to the FCSEL register, the noise rejector is used and counting is done by an external clock (K13) with 0.98 msec* or more pulse width. The noise rejector allows the counter to input the clock at the second falling edge of the internal 2,048 Hz* signal after changing the input level of the K13 input port terminal. Consequently, the pulse width of noise that can reliably be rejected is 0.48 msec* or less.
(*: f_{OSC1} = 32.768 kHz)
When "0" is written to the FCSEL register, the noise rejector is not used and the counting is done directly by an external clock input to the K13 input port terminal.
Setting of this register is effective only when timer 0 is used in the event counter mode.
At initial reset, this register is set to "0".

PLPOL: Timer 0 pulse polarity selection register (FFC0H•D0)

Selects the count pulse polarity in the event counter mode.

When "1" is written: Rising edge
When "0" is written: Falling edge
Reading: Valid

The count timing in the event counter mode (timer 0) is selected from either the falling edge of the external clock input to the K13 input port terminal or the rising edge. When "0" is written to the PLPOL register, the falling edge is selected and when "1" is written, the rising edge is selected.
Setting of this register is effective only when timer 0 is used in the event counter mode.
At initial reset, this register is set to "0".

RLD00–RLD07: Timer 0 reload data register (FFC4H, FFC5H)
RLD10–RLD17: Timer 1 reload data register (FFC6H, FFC7H)

Sets the initial value for the counter.
The reload data written in this register is loaded to the respective counters. The counter counts down using the data as the initial value for counting.
Reload data is loaded to the counter when the counter is reset by writing "1" to the PTRSTx register, or when counter underflow occurs.
At initial reset, these registers are set to "00H".

PTD00–PTD07: Timer 0 counter data (FFC8H, FFC9H)
PTD10–PTD17: Timer 1 counter data (FFCAH, FFCBH)

Count data in the programmable timer can be read from these latches.
The low-order 4 bits of the count data in timer x can be read from PTDx0–PTDx3, and the high-order data can be read from PTDx4–PTDx7. Since the high-order 4 bits are held by reading the low-order 4 bits, be sure to read the low-order 4 bits first.
Since these latches are exclusively for reading, the writing operation is invalid.
At initial reset, these counter data are set to "00H".

PTRST0: Timer 0 reset (reload) (FFC2H•D1)
PTRST1: Timer 1 reset (reload) (FFC3H•D1)
Resets the timer and presets reload data to the counter.

When "1" is written: Reset
When "0" is written: No operation
Reading: Always "0"

By writing "1" to PTRSTx, the reload data in the reload register RLDx0–RLDx7 is preset to the counter in timer x. When the counter is preset in the RUN status, the counter restarts immediately after presetting. In the case of STOP status, the reload data is preset to the counter and is maintained.
No operation results when "0" is written.
Since these bits are exclusively for writing, always set to "0" during reading.

PTRUN0: Timer 0 RUN/STOP control register (FFC2H•D0)
PTRUN1: Timer 1 RUN/STOP control register (FFC3H•D0)
Controls the RUN/STOP of the counter.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

The counter in timer x starts counting down by writing "1" to the PTRUNx register and stops by writing "0". In STOP status, the counter data is maintained until the counter is reset or is set in the next RUN status. When STOP status changes to RUN status, the data that has been maintained can be used for resuming the count.
At initial reset, these registers are set to "0".

CHSEL0: TOUT output channel selection register (FFC1H•D3)
Selects the channel used for TOUT signal output.

When "1" is written: Timer 1
When "0" is written: Timer 0
Reading: Valid

This register selects which timer's output (timer 0 or timer 1) is used to generate a TOUT signal. When "0" is written to the CHSEL0 register, timer 0 is selected and when "1" is written, timer 1 is selected. In the 16-bit mode (MOD16 = "1"), timer 1 is always selected regardless of this register setting.
At initial reset, this register is set to "0".

PTOUT: TOUT output control register (FFC1H•D2)
Turns TOUT signal output on and off.

When "1" is written: On
When "0" is written: Off
Reading: Valid

PTOUT is the output control register for the TOUT signal. When "1" is written to the register, the TOUT signal is output from the output port terminal R02 and when "0" is written, the terminal goes to a high (V_{DD}) level. However, the data register R02 must always be "1" and the high impedance control register R02HIZ must always be "0" (data output state).
At initial reset, this register is set to "0".

EIPT0: Timer 0 interrupt mask register (FFE2H•D0)
EIPT1: Timer 1 interrupt mask register (FFE2H•D1)

These registers are used to select whether to mask the programmable timer interrupt or not.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

The timer x interrupt can be masked individually by the interrupt mask registers EIPTx.
At initial reset, these registers are set to "0".

IPT0: Timer 0 interrupt factor flag (FFF2H•D0)
IPT1: Timer 1 interrupt factor flag (FFF2H•D1)

These flags indicate the status of the programmable timer interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

The interrupt factor flags IPTx correspond to the timer x interrupt. The software can judge from these flags whether there is a programmable timer interrupt. However, even if the interrupt is masked, the flags are set to "1" by the underflows of the corresponding counters.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.9.10 Programming notes

(1) When reading counter data, be sure to read the low-order 4 bits (PTDx0–PTDx3) first. Furthermore, the high-order 4 bits (PTDx4–PTDx7) should be read within 0.73 msec (when f_{OSC1} is 32.768 kHz) of reading the low-order 4 bits (PTDx0–PTDx3).
The counter data in 16-bit mode must be read in the order below.
PTD00–PTD03 → PTD04–PDT07 → PTD10–PTD13 → PTD14–PTD17

(2) The programmable timer actually enters RUN/STOP status in synchronization with the falling edge of the input clock after writing to the PTRUNx register. Consequently, when "0" is written to the PTRUNx register, the timer enters STOP status at the point where the counter is decremented (-1). The PTRUNx register maintains "1" for reading until the timer actually stops.
Figure 4.9.10.1 shows the timing chart for the RUN/STOP control.

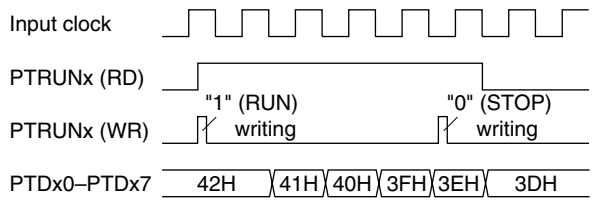


Fig. 4.9.10.1 Timing chart for RUN/STOP control

It is the same even in the event counter mode. Therefore, be aware that the counter does not enter RUN/STOP status if a clock is not input after setting the RUN/STOP control register (PTRUN0).

(3) Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned on and off by setting the register.

(4) When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time at least 5 msec from turning the circuit ON until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit ON to starting the programmable timer. Refer to Section 4.3, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit.
At initial reset, the OSC3 oscillation circuit is set in the off state.

(5) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(6) For the reason below, pay attention to the reload data write timing when changing the interval of the programmable timer interrupts while the programmable timer is running.
The programmable timer counts down at the falling edge of the input clock and at the same time it generates an interrupt if the counter underflows. Then it starts loading the reload data to the counter and the counter data is determined at the next rising edge of the input clock (period shown in as ① in the figure).

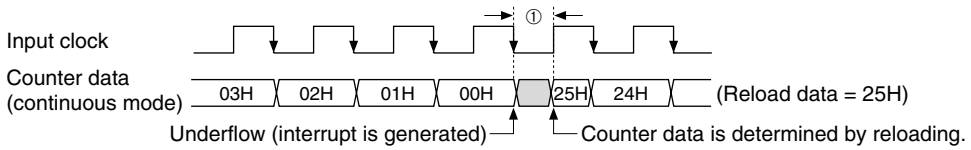


Fig. 4.9.10.2 Reload timing for programmable timer

To avoid improper reloading, do not rewrite the reload data after an interrupt occurs until the counter data is determined including the reloading period ①. Be especially careful when using the OSC1 (low-speed clock) as the clock source of the programmable timer and the CPU is operating with the OSC3 (high-speed clock).

4.10 Serial Interface

4.10.1 Configuration of serial interface

The S1C63808 incorporates two channels of full duplex serial interface ports (when asynchronous system is selected) that allows the user to select either clock synchronous system or asynchronous system.
The data transfer method can be selected in software.
When the clock synchronous system is selected, 8-bit data transfer is possible.
When the asynchronous system is selected, either 7-bit or 8-bit data transfer is possible, and a parity check of received data and the addition of a parity bit for transmitting data can automatically be done by selecting in software.
Figure 4.10.1.1 shows the configuration of the serial interface.

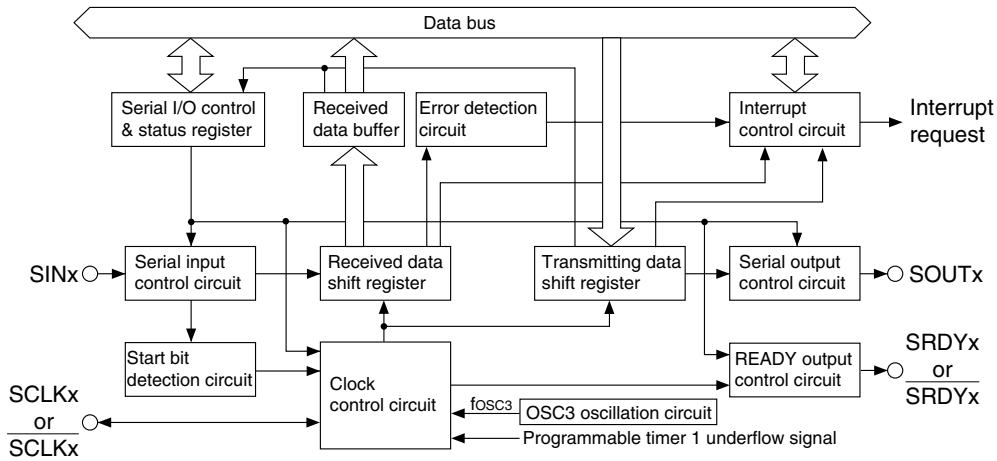


Fig. 4.10.1.1 Configuration of serial interface

Note: Channels 1 and 2 of the serial interface are precisely identical, and the signal and register names are identified by the channel number (1 or 2) attached (e.g. the SIN1 terminal is for channel 1 and SIN2 terminal is for channel 2). This section explains the serial interface functions in common to both channels using common signal names with "x" attached as a substitute for the channel number (e.g. SIN1/SIN2 → SINx) except the part that needs distinction.

Serial interface 1 input/output terminals, SIN1, SOUT1, SCLK1 and SRDY1 are shared with the I/O ports P10–P13. Serial interface 2 input/output terminals, SIN2, SOUT2, SCLK2 and SRDY2 are shared with the I/O ports P20–P23. In order to utilize these terminals for the serial interface input/output terminals, proper settings have to be made with registers ESIFx, SMDx0 and SMDx1. (At initial reset, these terminals are set as I/O port terminals.)
The direction of I/O port terminals set for serial interface input/output terminals are determined by the signal and transfer mode for each terminal. Furthermore, the settings for the corresponding I/O control registers for the I/O ports become invalid.

Table 4.10.1.1 Configuration of input/output terminals

Terminal	When serial interface is selected
P10	SIN1
P11	SOUT1
P12	SCLK1
P13	SRDY1
P20	SIN2
P21	SOUT2
P22	SCLK2
P23	SRDY2

* The terminals used may change according to the transfer mode.

SINx and SOUTx are serial data input and output terminals which function identically in clock synchronous system and asynchronous system. SCLKx is exclusively for use with clock synchronous system and functions as a synchronous clock input/output terminal. SRDYx is exclusively for use in clock synchronous slave mode and functions as a send-receive ready signal output terminal.
When asynchronous system is selected, since SCLKx and SRDYx are superfluous, the I/O port terminals P12/P22 and P13/P23 can be used as I/O ports.
In the same way, when clock synchronous master mode is selected, since SRDYx is superfluous, the I/O port terminal P13/P23 can be used as I/O port.

4.10.2 Mask option

Since the input/output terminals of the serial interface is shared with the I/O ports (P10–P13, P20–P23), the mask option that selects the terminal specification for the I/O port is also applied to the serial interface.

Output specification

The output specification of the terminals SOUTx, SCLKx (for clock synchronous master mode) and SRDYx (for clock synchronous slave mode) that are used as output in the input/output port of the serial interface is respectively selected by the mask options of P11/P21, P12/P22 and P13/P23. Either complementary output or P-channel open drain output can be selected as the output specification. However, when P-channel open drain output is selected, do not apply a voltage exceeding the power supply voltage to the terminal.

Pull-down resistor

The pull-down resistors for the SINx terminal and the SCLKx terminal (during slave mode) that are used as input terminals can be selected by mask option. The pull-down resistor can be added by the mask options of P10/P20 and P12/P22. When "gate direct" is selected, take care that the floating status does not occur.

Polarity of synchronous clock and ready signal in clock synchronous slave mode

Polarity of the synchronous clock and the ready signal that is output in the clock synchronous slave mode can be selected from either positive polarity (high active, SCLKx & SRDYx) or negative polarity (low active, $\overline{\text{SCLKx}}$ & $\overline{\text{SRDYx}}$).
When operating the serial interface in the slave mode, the synchronous clock is input from a external device. Be aware that the terminal specification is pull-down only and a pull-up resistor cannot be built in if negative polarity is selected.
In the following explanation, it is assumed that positive polarity (SCLKx, SRDYx) has been selected.

4.10.3 Transfer modes

There are four transfer modes for the serial interface and mode selection is made by setting the two bits of the mode selection registers SMDx0 and SMDx1 as shown in the table below.

Table 4.10.3.1 Transfer modes

SMDx1	SMDx0	Mode
1	1	8-bit asynchronous
1	0	7-bit asynchronous
0	1	Clock synchronous slave
0	0	Clock synchronous master

Table 4.10.3.2 Terminal settings corresponding to each transfer mode

Mode	SIN	SOUTx	SCLKx	SRDYx
Asynchronous 8-bit	Input	Output	P12/P22	P13/P23
Asynchronous 7-bit	Input	Output	P12/P22	P13/P23
Clock synchronous slave	Input	Output	Input	Output
Clock synchronous master	Input	Output	Output	P13/P23

At initial reset, transfer mode is set to clock synchronous master mode.

Clock synchronous master mode

In this mode, the internal clock is utilized as a synchronous clock for the built-in shift registers, and 8-bit clock synchronous serial transfers can be performed with this serial interface as the master.
The synchronous clock is also output from the SCLKx terminal which enables control of the external (slave side) serial I/O device. Since the SRDYx terminal is not utilized in this mode, it can be used as an I/O port.
Figure 4.10.3.1(a) shows the connection example of input/output terminals in the clock synchronous master mode.

Clock synchronous slave mode

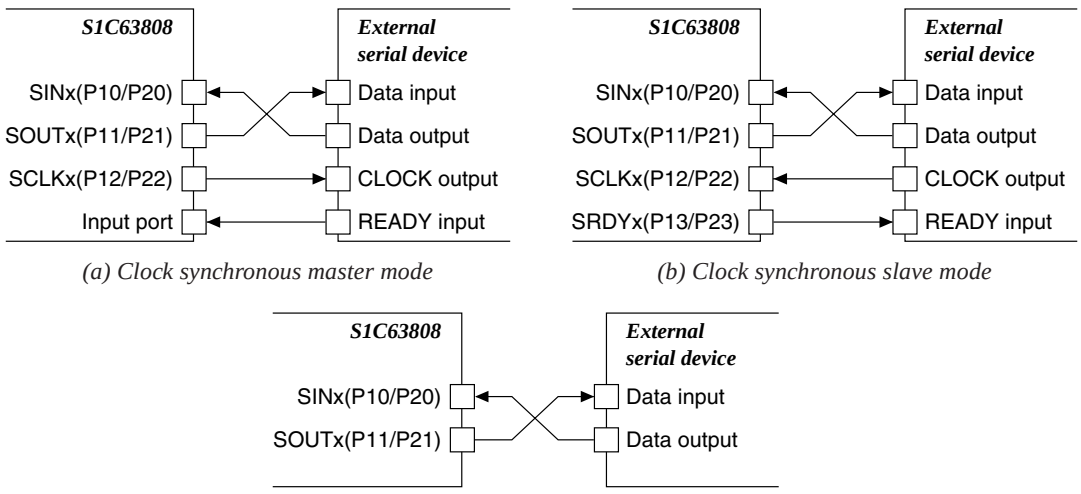
In this mode, a synchronous clock from the external (master side) serial input/output device is utilized and 8-bit clock synchronous serial transfers can be performed with this serial interface as the slave. The synchronous clock is input to the SCLKx terminal and is utilized by this interface as the synchronous clock. Furthermore, the SRDYx signal indicating the transmit-receive ready status is output from the SRDYx terminal in accordance with the serial interface operating status.
In the slave mode, the settings for registers SCSx0 and SCSx1 used to select the clock source are invalid. Figure 4.10.3.1(b) shows the connection example of input/output terminals in the clock synchronous slave mode.

7-bit asynchronous mode

In this mode, 7-bit asynchronous transfer can be performed. Parity check during data reception and addition of parity bit (odd/even/none) during transmitting can be specified and data processed in 7 bits with or without parity. Since this mode employs the internal clock, the SCLKx terminal is not used. Furthermore, since the SRDYx terminal is not utilized either, both of these terminals can be used as I/O ports. Figure 4.10.3.1(c) shows the connection example of input/output terminals in the asynchronous mode.

8-bit asynchronous mode

In this mode, 8-bit asynchronous transfer can be performed. Parity check during data reception and addition of parity bit (odd/even/none) during transmitting can be specified and data processed in 8 bits with or without parity. Since this mode employs the internal clock, the SCLKx terminal is not used. Furthermore, since the SRDYx terminal is not utilized either, both of these terminals can be used as I/O ports. Figure 4.10.3.1(c) shows the connection example of input/output terminals in the asynchronous mode.



(a) Clock synchronous master mode

(b) Clock synchronous slave mode

(c) Asynchronous 7-bit/8-bit mode

Fig. 4.10.3.1 Connection examples of serial interface I/O terminals

4.10.4 Clock source

There are four clock sources and selection is made by setting the two bits of the clock source selection register SCSx0 and SCSx1 as shown in table below.

Table 4.10.4.1 Clock source

SCSx1	SCSx0	Clock source
1	1	Programmable timer
1	0	fOSC3 / 4
0	1	fOSC3 / 8
0	0	fOSC3 / 16

This register setting is invalid in clock synchronous slave mode and the external clock input from the SCLKx terminal is used.
When the "programmable timer" is selected, the programmable timer 1 underflow signal is divided by 4 and this signal used as the clock source. With respect to the transfer rate setting, see "4.9 Programmable Timer". At initial reset, the synchronous clock is set to "fOSC3/16".
Whichever clock is selected, the signal is further divided by 1/16 and then used as the synchronous clock. Furthermore, external clock input is used as is for SCLKx in clock synchronous slave mode.

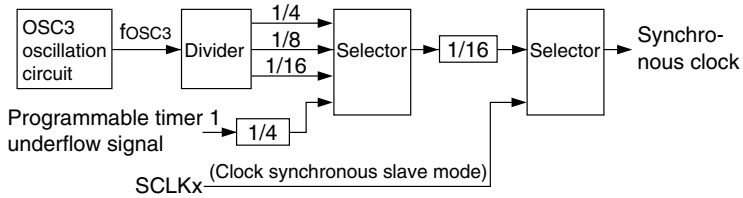


Fig. 4.10.4.1 Division of the synchronous clock

Table 4.10.4.2 shows an examples of transfer rates and OSC3 oscillation frequencies when the clock source is set to programmable timer.

Table 4.10.4.2 OSC3 oscillation frequencies and transfer rates

Transfer rate	fOSC3 = 3.072 MHz	
(bps)	PTPS1x	RLD1x
9,600	0 (1/1)	04H
4,800	0 (1/1)	09H
2,400	0 (1/1)	13H
1,200	0 (1/1)	27H
600	0 (1/1)	4FH
300	0 (1/1)	9FH
150	2 (1/32)	09H
75	2 (1/32)	13H

When the demultiplied signal of the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the serial interface.
A time interval of 5 msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before starting transmitting/receiving of serial interface. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 7, "Electrical Characteristics".)
At initial reset, the OSC3 oscillation circuit is set to OFF status.

4.10.5 Transmit-receive control

Below is a description of the registers which handle transmit-receive control. With respect to transmit-receive control procedures and operations, please refer to the following sections in which these are discussed on a mode by mode basis.

Shift register and receive data buffer

Exclusive shift registers for transmitting and receiving are installed in this serial interface. Consequently, duplex communication simultaneous transmit and receive is possible when the asynchronous system is selected.
Data being transmitted are written to TRXDx0–TRXDx7 and converted to serial through the shift register and is output from the SOUTx terminal.
In the reception section, a receive data buffer is installed separate from the shift register.
Data being received are input to the SINx terminal and is converted to parallel through the shift register and written to the receive data buffer.
Since the receive data buffer can be read even during serial input operation, the continuous data is received efficiently.
However, since buffer functions are not used in clock synchronous mode, be sure to read out data before the next data reception begins.

Transmit enable register and transmit control bit

For transmit control, use the transmit enable register TXENx and transmit control bit TXTRGx.

The transmit enable register TXENx is used to set the transmit enable/disable status. When "1" is written to this register to set the transmitting enable status, clock input to the shift register is enabled and the system is ready to transmit data. In the clock synchronous mode, synchronous clock input/output from the SCLKx terminal is also enabled.
The transmit control bit TXTRGx is used as the trigger to start transmitting data.
Data to be transmitted is written to the transmit data shift register, and when transmitting preparations a recomplete, "1" is written to TXTRGx whereupon data transmitting begins.
When interrupt has been enabled, an interrupt is generated when the transmission is completed. If there is subsequent data to be transmitted it can be sent using this interrupt.
In addition, TXTRGx can be read as a status bit. When set to "1", it indicates transmitting operation, and "0" indicates transmitting stop.
For details on timing, see the timing chart which gives the timing for each mode.
When not transmitting, set TXENx to "0" to disable transmission.

Receive enable register and receive control bit

For receiving control, use the receive enable register RXENx and receive control bit RXTRGx.
Receive enable register RXENx is used to set receiving enable/disable status. When "1" is written into this register to set the receiving enable status, clock input to the shift register is enabled and the system is ready to receive data. In the clock synchronous mode, synchronous clock input/output from the SCLKx terminal is also enabled. With the above setting, receiving begins and serial data input from the SINx terminal goes to the shift register.
The operation of the receive control bit RXTRGx is slightly different depending on whether a clock synchronous system or an asynchronous system is being used.
In clock synchronous system, the receive control bit RXTRGx is used as the trigger to start receiving data. When received data has been read and the preparation for next data receiving is completed, write "1" into RXTRGx to start receiving. (When "1" is written to RXTRGx in slave mode, SRDYx is asserted.)
In asynchronous system, RXTRGx is used to prepare for next data receiving. After reading the received data from the receive data buffer, write "1" into RXTRGx to signify that the receive data buffer is empty. If "1" is not written into RXTRGx, the overrun error flag OERx will be set to "1" when the next receiving operation is completed. (An overrun error will be generated when receiving is completed between reading the received data and the writing of "1" to RXTRGx.)

In addition, RXTRGx can be read as a status bit. In either clock synchronous mode or asynchronous mode, when RXTRGx is set to "1", it indicates receiving operation and when set to "0", it indicates that receiving has stopped.
For details on timing, see the timing chart which gives the timing for each mode.

When you do not receive, set RXENx to "0" to disable receiving.

4.10.6 Operation of clock synchronous transfer

Clock synchronous transfer involves the transfer of 8-bit data by synchronizing it to eight clocks. The same synchronous clock is used by both the transmitting and receiving sides.
When the serial interface is used in the master mode, the clock signal selected using SCSx0 and SCSx1 is further divided by 1/16 and employed as the synchronous clock. This signal is then sent via the SCLKx terminal to the slave side (external serial I/O device).
When used in the slave mode, the clock input to the SCLKx terminal from the master side (external serial input/output device) is used as the synchronous clock.
In the clock synchronous mode, since one clock line (SCLKx) is shared for both transmitting and receiving, transmitting and receiving cannot be performed simultaneously. (Half duplex only is possible in clock synchronous mode.)
The transfer data length is fixed at 8 bits. Data can be switched using a register whether it is transmitted/received from LSB (bit 0) or MSB (bit 7).

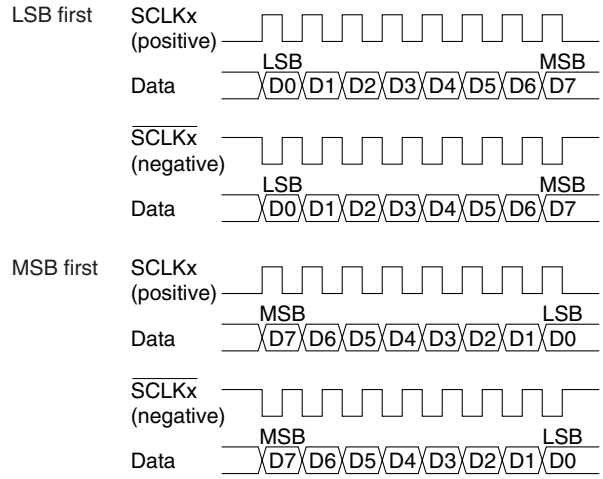


Fig. 4.10.6.1 Transfer data configuration using clock synchronous mode

Below is a description of initialization when performing clock synchronous transfer, transmit-receive control procedures and operations.
With respect to serial interface interrupt, see "4.10.8 Interrupt function".

Initialization of serial interface

When performing clock synchronous transfer, the following initial settings must be made.

(1) Setting of transmitting/receiving disable

To set the serial interface into a status in which both transmitting and receiving are disabled, "0" must be written to both the transmit enable register TXENx and the receive enable register RXENx. Fix these two registers to a disable status until data transfer actually begins.

(2) Port selection

Because serial interface input/output ports SINx, SOUTx, SCLKx and SRDYx are set as I/O port terminals P10–P13 and P20–P23 at initial reset, "1" must be written to the serial interface enable register ESIFx in order to set these terminals for serial interface use.

(3) Setting of transfer mode

Select the clock synchronous mode by writing the data as indicated below to the two bits of the mode selection registers SMDx0 and SMDx1.

Master mode: SMDx0 = "0", SMDx1 = "0"
Slave mode: SMDx0 = "1", SMDx1 = "0"

(4) Clock source selection

In the master mode, select the synchronous clock source by writing data to the two bits of the clock source selection registers SCSx0 and SCSx1. (See Table 4.10.4.1.)
This selection is not necessary in the slave mode.

The parity enable register EPRx is also assigned to this address, however, since parity is not necessary in the clock synchronous mode, parity check will not take place regardless of how they are set.

(5) Clock source control

When the master mode is selected and programmable timer for the clock source is selected, set transfer rate on the programmable timer side. (See "4.9 Programmable Timer".)
When the divided signal of OSC3 oscillation circuit is selected for the clock source, be sure that the OSC3 oscillation circuit is turned ON prior to commencing data transfer. (See "4.3 Oscillation Circuit".)
Note that the frequency of the serial interface clock is limited to a maximum of 2 MHz.

(6) Serial data input/output permutation

The S1C63808 provides the data input/output permutation select register SDPx to select whether the serial data bits are transferred from the LSB or MSB. The SDPx register should be set before writing data to TRXDx0–TRXDx7.

Data transmit procedure

The control procedure and operation during transmitting is as follows.

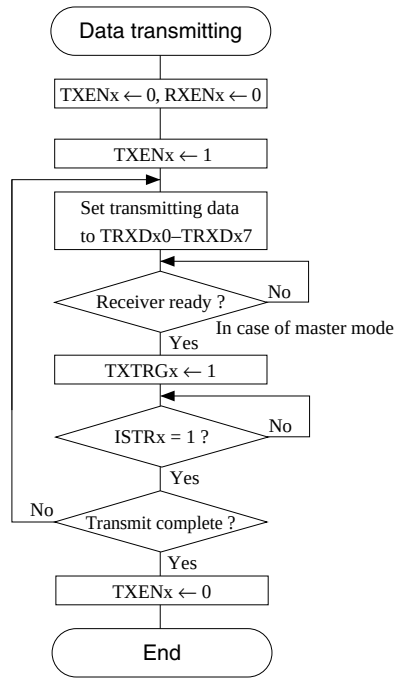


Fig. 4.10.6.2 Transmit procedure in clock synchronous mode

(1) Write "0" in the transmit enable register TXENx and the receive enable register RXENx to reset the serial interface.

(2) Write "1" in the transmit enable register TXENx to set into the transmitting enable status.

(3) Write the transmitting data into TRXDx0–TRXDx7.

(4) In case of the master mode, confirm the receive ready status on the slave side (external serial input/output device), if necessary. Wait until it reaches the receive ready status.

(5) Write "1" in the transmit control bit TXTRGx and start transmitting.
In the master mode, this control causes the synchronous clock to change to enable and to be provided to the shift register for transmitting and output from the SCLKx terminal.
In the slave mode, it waits for the synchronous clock to be input from the SCLKx terminal.
The transmitting data of the shift register shifts one bit at a time at each falling edge of the synchronous clock and is output from the SOUTx terminal. When the final bit is output, the SOUTx terminal is maintained at that level, until the next transmitting begins.
The transmitting complete interrupt factor flag ISTRx is set to "1" at the point where the data transmitting of the shift register is completed. When interrupt has been enabled, a transmitting complete interrupt is generated at this point.
Set the following transmitting data using this interrupt.

(6) Repeat steps (3) to (5) for the number of bytes of transmitting data, and then set the transmit disable status by writing "0" to the transmit enable register TXENx, when the transmitting is completed.

Data receive procedure

The control procedure and operation during receiving is as follows.

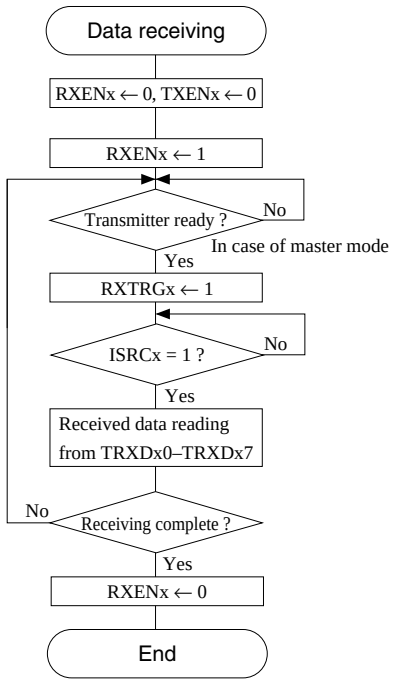


Fig. 4.10.6.3 Receiving procedure in clock synchronous mode

(1) Write "0" in the receive enable register RXENx and transmit enable register TXENx to reset the serial interface.

(2) Write "1" in the receive enable register RXENx to set into the receiving enable status.

(3) In case of the master mode, confirm the transmit ready status on the slave side (external serial input/output device), if necessary. Wait until it reaches the transmit ready status.

(4) Write "1" in the receive control bit RXTRGx and start receiving.
In the master mode, this control causes the synchronous clock to change to enable and is provided to the shift register for receiving and output from the SCLKx terminal.
In the slave mode, it waits for the synchronous clock to be input from the SCLKx terminal. The received data input from the SINx terminal is successively incorporated into the shift register in synchronization with the rising edge of the synchronous clock.
At the point where the data of the 8th bit has been incorporated at the final (8th) falling edge (when positive polarity is selected) or rising edge (when negative polarity is selected) of the synchronous clock, the content of the shift register is sent to the receive data buffer and the receiving complete interrupt factor flag ISRCx is set to "1". When interrupt has been enabled, a receiving complete interrupt is generated at this point.

(5) Read the received data from TRXDx0–TRXDx7 using receiving complete interrupt.

(6) Repeat steps (3) to (5) for the number of bytes of receiving data, and then set the receive disable status by writing "0" to the receive enable register RXENx, when the receiving is completed.

Transmit/receive ready (SRDYx) signal

When this serial interface is used in the clock synchronous slave mode (external clock input), an SRDYx signal is output from the SRDYx terminal to indicate whether or not this serial interface can transmit/receive to the master side (external serial input/output device).

When positive polarity is selected

The SRDYx signal goes "1" (high level) when this interface enters the transmit or receive enable (READY) status, and it goes "0" (low level) when the interface is in a BUSY status, such as during transmit/receive operation.
The SRDYx signal changes "0" to "1" immediately after writing "1" into the transmit control bit TXTRGx or the receive control bit RXTRGx and it returns to "0" at the point where the first synchronous clock is input (rising edge).

When negative polarity is selected

The $\overline{\text{SRDYx}}$ signal goes "0" (low level) when this interface enters the transmit or receive enable (READY) status, and it goes "1" (high level) when the interface is in a BUSY status, such as during transmit/receive operation.
The $\overline{\text{SRDYx}}$ signal changes "1" to "0" immediately after writing "1" into the transmit control bit TXTRGx or the receive control bit RXTRGx and it returns to "1" at the point where the first synchronous clock is input (falling edge).

When you have set in the master mode, control the transfer by inputting the same signal from the slave side using the input port or I/O port. At this time, since the SRDYx terminal is not set and instead P13/P23 functions as the I/O port, you can apply this port for said control.

Timing chart

The timing chart for the clock synchronous system transmission is shown in Figure 4.10.6.4.

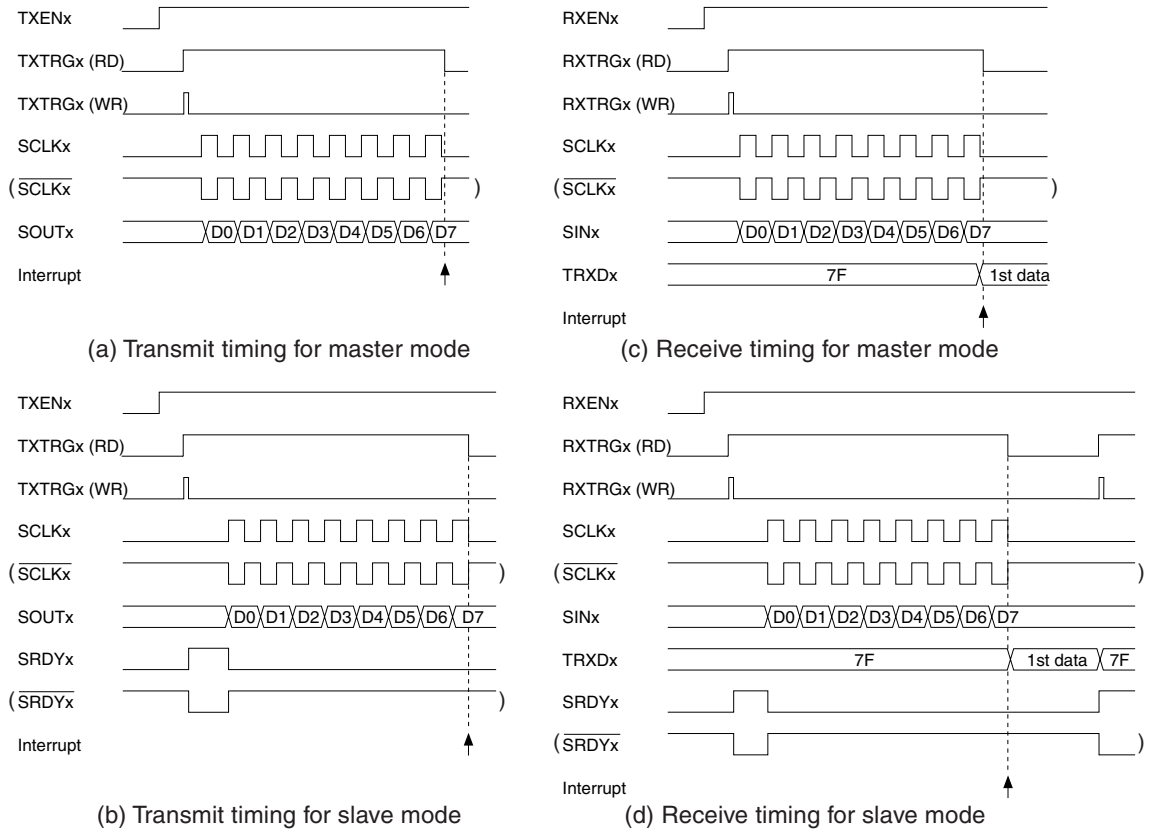


Fig. 4.10.6.4 Timing chart (clock synchronous system transmission)

4.10.7 Operation of asynchronous transfer

Asynchronous transfer is a mode that transfers by adding a start bit and a stop bit to the front and the back of each piece of serial converted data. In this mode, there is no need to use a clock that is fully synchronized clock on the transmit side and the receive side, but rather transmission is done while adopting the synchronization at the start/stop bits that have attached before and after each piece of data. The RS-232C interface functions can be easily realized by selecting this transfer mode.
This interface has separate transmit and receive shift registers and is designed to permit full duplex transmission to be done simultaneously for transmitting and receiving.
For transfer data in the 7-bit asynchronous mode, either 7 bits data (no parity) or 7 bits data + parity bit can be selected. In the 8-bit asynchronous mode, either 8 bits data (no parity) or 8 bits data + parity bit can be selected.
Parity can be even or odd, and parity checking of received data and adding a party bit to transmitting data will be done automatically. Thereafter, it is not necessary to be conscious of parity itself in the program.
The start bit length is fixed at 1 bit. For the stop bit length, either 1 bit or 2 bits can be selected using the stop bit select register STPBx. Whether data is transmitted/received from LSB (bit 0) or MSB (bit 7) it can be switched using the data input/output permutation select register SDPx.

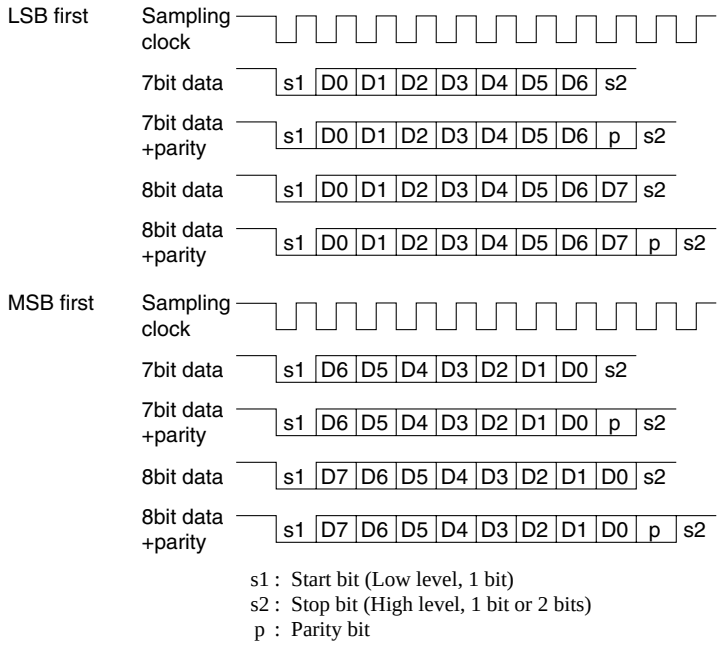


Fig. 4.10.7.1 Transfer data configuration for asynchronous system

Here following, we will explain the control sequence and operation for initialization and transmitting / receiving in case of asynchronous data transfer. See "4.10.8 Interrupt function" for the serial interface interrupts.

Initialization of serial interface

The below initialization must be done in cases of asynchronous system transfer.

(1) Setting of transmitting/receiving disable

To set the serial interface into a status in which both transmitting and receiving are disabled, "0" must be written to both the transmit enable register TXENx and the receive enable register RXENx. Fix these two registers to a disable status until data transfer actually begins.

(2) Port selection

Because serial interface input/output terminals SINx and SOUTx are set as I/O port terminals P10/P20 and P11/P21 at initial reset, "1" must be written to the serial interface enable register ESIFx in order to set these terminals for serial interface use.
SCLKx and SRDYx terminals set in the clock synchronous mode are not used in the asynchronous mode. These terminals function as I/O port terminals P12/P22 and P13/P23.

(3) Setting of transfer mode

Select the asynchronous mode by writing the data as indicated below to the two bits of the mode selection registers SMDx0 and SMDx1.

7-bit mode: SMDx0 = "0", SMDx1 = "1"
8-bit mode: SMDx0 = "1", SMDx1 = "1"

(4) Parity bit selection

When checking and adding parity bits, write "1" into the parity enable register EPRx to set to "with parity check". As a result of this setting, in the 7-bit asynchronous mode, it has a 7 bits data + parity bit configuration and in the 8-bit asynchronous mode it has an 8 bits data + parity bit configuration. In this case, parity checking for receiving and adding a party bit for transmitting is done automatically in hardware. Moreover, when "with parity check" has been selected, "odd" or "even" parity must be further selected in the parity mode selection register PMDx.
When "0" is written to the EPRx register to select "without parity check" in the 7-bit asynchronous mode, data configuration is set to 7 bits data (no parity) and in the 8-bit asynchronous mode (no parity) it is set to 8 bits data (no parity) and parity checking and parity bit adding will not be done.

(5) Clock source selection

Select the clock source by writing data to the two bits of the clock source selection registers SCSx0 and SCSx1. (See Table 4.10.4.1.)

(6) Clock source control

When the programmable timer is selected for the clock source, set transfer rate on the programmable timer side. (See "4.9 Programmable Timer".)
When the divided signal of OSC3 oscillation circuit is selected for the clock source, be sure that the OSC3 oscillation circuit is turned ON prior to commencing data transfer. (See "4.3 Oscillation Circuit".)

(7) Stop bit length selection

The stop bit length can be configured to 1 bit or 2 bits using the stop bit select register STPBx.

Table 4.10.7.1 Stop bit and parity bit settings

STPBx	EPRx	PMDx	Settings	
			Stop bit	Parity bit
1	1	1	2 bits	Odd
		0	2 bits	Even
	0	–	2 bits	Non parity
0	1	1	1 bit	Odd
		0	1 bit	Even
	0	–	1 bit	Non parity

(8) Serial data input/output permutation

The S1C63808 provides the data input/output permutation select register SDPx to select whether the serial data bits are transferred from the LSB or MSB. The SDPx register should be set before writing data to TRXDx0–TRXDx7.

Data transmit procedure

The control procedure and operation during transmitting is as follows.

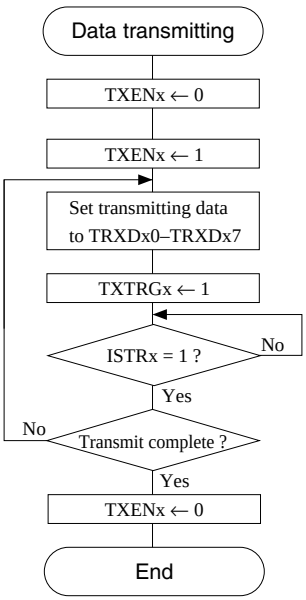


Fig. 4.10.7.2 Transmit procedure in asynchronous mode

(1) Write "0" in the transmit enable register TXENx to reset the serial interface.

(2) Write "1" in the transmit enable register TXENx to set into the transmitting enable status.

(3) Write the transmitting data into TRXDx0–TRXDx7.
Also, when 7-bit data is selected, the TRXDx7 data becomes invalid.

(4) Write "1" in the transmit control bit TXTRGx and start transmitting.
This control causes the shift clock to change to enable and a start bit (low) is output to the SOUTx terminal in synchronize to its falling edge. The transmitting data set to the shift register is shifted one bit at a time at each falling edge of the clock thereafter and is output from the SOUTx terminal. After the data output, it outputs a stop bit (high) and high level is maintained until the next start bit is output.
The transmitting complete interrupt factor flag ISTRx is set to "1" at the point where the data transmitting is completed. When interrupt has been enabled, a transmitting complete interrupt is generated at this point.
Set the following transmitting data using this interrupt.

(5) Repeat steps (3) to (4) for the number of bytes of transmitting data, and then set the transmit disable status by writing "0" to the transmit enable register TXENx, when the transmitting is completed.

Data receive procedure

The control procedure and operation during receiving is as follows.

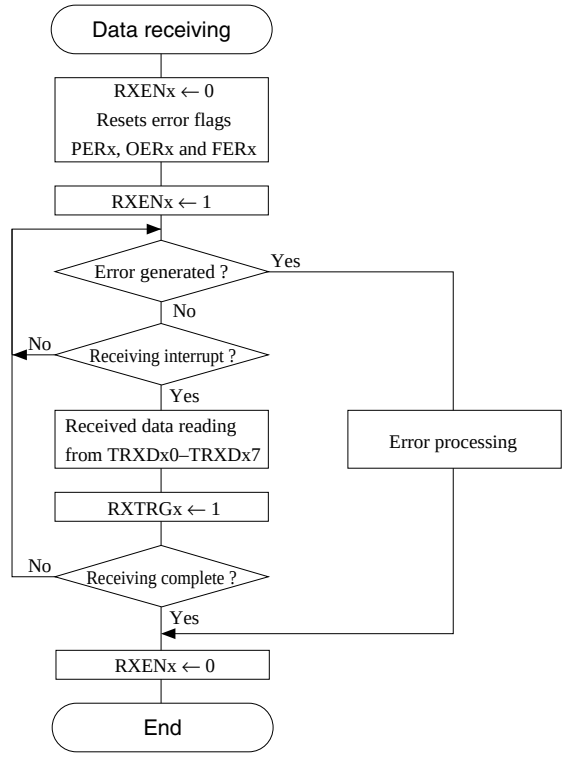


Fig. 4.10.7.3 Receiving procedure in asynchronous mode

(1) Write "0" in the receive enable register RXENx to set the receiving disable status and to reset the respective PERx, OERx, FERx flags that indicate parity, overrun and framing errors.

(2) Write "1" in the receive enable register RXENx to set into the receiving enable status.

(3) The shift clock will change to enable from the point where the start bit (low) has been input from the SINx terminal and the receive data will be synchronized to the rising edge following the second clock, and will thus be successively incorporated into the shift register.
After data bits have been incorporated, the stop bit is checked and, if it is not high, it becomes a framing error and the error interrupt factor flag ISERx is set to "1". When interrupt has been enabled, an error interrupt is generated at this point.
When receiving is completed, data in the shift register is transferred to the receive data buffer and the receiving complete interrupt flag ISRCx is set to "1". When interrupt has been enabled, a receiving complete interrupt is generated at this point. (When an overrun error is generated, the interrupt factor flag ISRCx is not set to "1" and a receiving complete interrupt is not generated.)
If "with parity check" has been selected, a parity check is executed when data is transferred into the receive data buffer from the shift register and if a parity error is detected, the error interrupt factor flag is set to "1". When the interrupt has been enabled, an error interrupt is generated at this point just as in the framing error mentioned above.

(4) Read the received data from TRXDx0–TRXDx7 using receiving complete interrupt.

(5) Write "1" to the receive control bit RXTRGx to inform that the receive data has been read out.
When the following data is received prior to writing "1" to RXTRGx, it is recognized as an overrun error and the error interrupt factor flag is set to "1". When the interrupt has been enabled, an error interrupt is generated at this point just as in the framing error and parity error mentioned above.

(6) Repeat steps (3) to (5) for the number of bytes of receiving data, and then set the receive disable status by writing "0" to the receive enable register RXENx, when the receiving is completed.

Receive error

During receiving the following three types of errors can be detected by an interrupt.

(1) Parity error

When writing "1" to the EPRx register to select "with parity check", a parity check (vertical parity check) is executed during receiving. After each data bit is sent a parity check bit is sent. The parity check bit is a "0" or a "1". Even parity checking will cause the sum of the parity bit and the other bits to be even. Odd parity causes the sum to be odd. This is checked on the receiving side.
The parity check is performed when data received in the shift register is transferred to the receive data buffer. It checks whether the parity check bit is a "1" or a "0" (the sum of the bits including the parity bit) and the parity set in the PMDx register match. When it does not match, it is recognized as an parity error and the parity error flag PERx and the error interrupt factor flag ISERx are set to "1".
When interrupt has been enabled, an error interrupt is generated at this point.
The PERx flag is reset to "0" by writing "1".
Even when this error has been generated, the received data corresponding to the error is transferred in the receive data buffer and the receive operation also continues.
The received data at this point cannot assured because of the parity error.

(2) Framing error

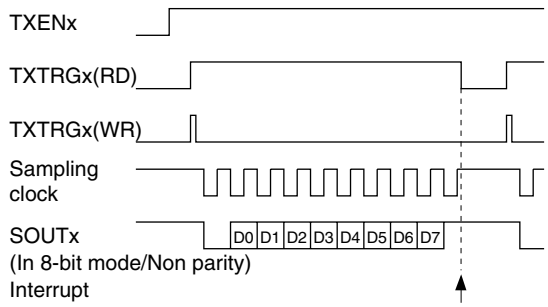
In asynchronous transfer, synchronization is adopted for each character at the start bit ("0") and the stop bit ("1"). When receiving has been done with the stop bit set at "0", the serial interface judges the synchronization to be off and a framing error is generated. When this error is generated, the framing error flag FERx and the error interrupt factor flag ISERx are set to "1". When interrupt has been enabled, an error interrupt is generated at this point.
The FERx flag is reset to "0" by writing "1".
Even when this error has been generated, the received data corresponding to the error is transferred in the receive data buffer and the receive operation also continues. However, even when it does not become a framing error with the following data receiving, such data cannot be assured.

(3) Overrun error

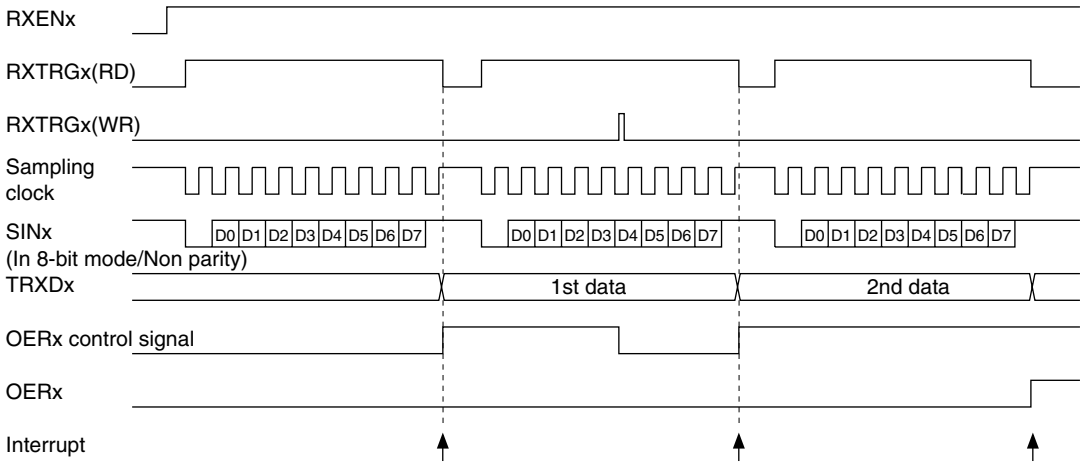
When the next data is received before "1" is written to RXTRGx, an overrun error will be generated, because the previous receive data will be overwritten. When this error is generated, the overrun error flag OERx and the error interrupt factor flag ISERx are set to "1". When interrupt has been enabled, an error interrupt is generated at this point. The OERx flag is reset to "0" by writing "1" into it.
Even when this error has been generated, the received data corresponding to the error is transferred in the receive data buffer and the receive operation also continues.
Furthermore, when the timing for writing "1" to RXTRGx and the timing for the received data transfer to the receive data buffer overlap, it will be recognized as an overrun error.

Timing chart

Figure 4.10.7.4 show the asynchronous transfer timing chart.



(a) Transmit timing



(b) Receive timing

Fig. 4.10.7.4 Timing chart (asynchronous transfer)

4.10.8 Interrupt function

This serial interface includes a function that generates the below indicated three types of interrupts.

- Transmitting complete interrupt
- Receiving complete interrupt
- Error interrupt

The interrupt factor flag and the interrupt mask register for the respective interrupt factors are provided and then the interrupt can be disabled/enabled by the software.
Figure 4.10.8.1 shows the configuration of the serial interface interrupt circuit.

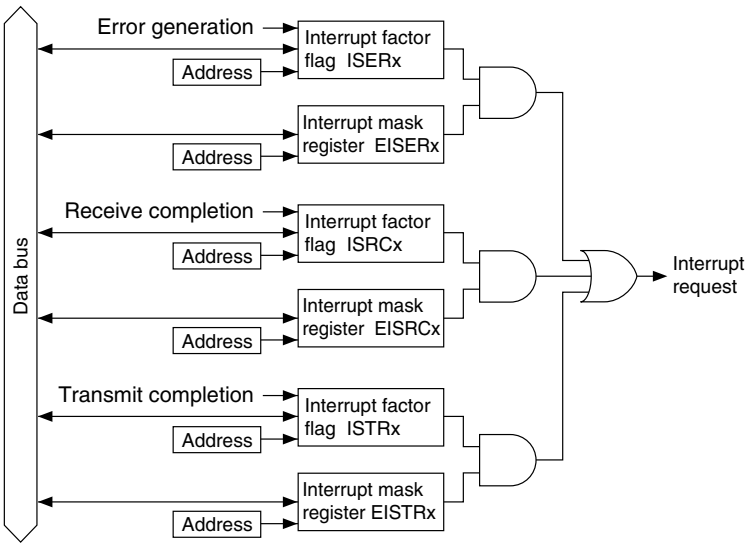


Fig. 4.10.8.1 Configuration of serial interface interrupt circuit

Transmit completion interrupt

This interrupt factor is generated at the point where the sending of the data written into the shift register has been completed and sets the interrupt factor flag ISTRx to "1". When set in this manner, if the corresponding interrupt mask register EISTRx is set to "1" and the CPU is set to interrupt enabled status (I flag = "1"), an interrupt will be generated to the CPU.
When the interrupt mask register EISTRx has been set to "0" and interrupt has been disabled, no interrupt is generated to the CPU. Even in this case, the interrupt factor flag ISTRx is set to "1".
The interrupt factor flag ISTRx is reset to "0" by writing "1".
The following transmitting data can be set and the transmitting can be started (writing "1" to TXTRGx) after this interrupt factor occurs.

Receive completion interrupt

This interrupt factor is generated at the point where receiving has been completed and the receive data incorporated into the shift register has been transferred into the receive data buffer and it sets the interrupt factor flag ISRCx to "1". When set in this manner, if the corresponding interrupt mask register EISRCx is set to "1" and the CPU is set to interrupt enabled status (I flag = "1"), an interrupt will be generated to the CPU.
When the interrupt mask register EISRCx has been set to "0" and interrupt has been disabled, no interrupt is generated to the CPU. Even in this case, the interrupt factor flag ISRCx is set to "1".
The interrupt factor flag ISRCx is reset to "0" by writing "1".
The generation of this interrupt factor allows reading of the received data.
Also, the interrupt factor flag ISRCx is set to "1" when a parity error or framing error is generated.

Error interrupt

This interrupt factor is generated at the point where a parity error, framing error or overrun error is detected during receiving and it sets the interrupt factor flag ISERx to "1". When set in this manner, if the corresponding interrupt mask register EISERx is set to "1" and the CPU is set to interrupt enabled status (I flag = "1"), an interrupt will be generated to the CPU.
When the interrupt mask register EISERx has been set to "0" and interrupt has been disabled, an interrupt is not generated to the CPU. Even in this case, the interrupt factor flag ISERx is set to "1".
The interrupt factor flag ISERx is reset to "0" by writing "1".
Since all three types of errors result in the same interrupt factor, you should identify the error that has been generated by the error flags PERx (parity error), OERx (overrun error) and FERx (framing error).

4.10.9 I/O memory of serial interface

Table 4.10.9.1 show the serial interface control bits and their addresses.

Table 4.10.9.1(a) Serial interface control bits

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF14H	0	SMD21	SMD20	ESIF2	0 *3	– *2			Unused
					SMD21	0			Serial I/F 2 mode selection [SMD21, 20] 0: Mode Clk-sync. master; 1: Mode Clk-sync. slave
					SMD20	0			Serial I/F 2 mode selection [SMD21, 20] 2: Mode Async. 7-bit; 3: Mode Async. 8-bit
	R	R/W			ESIF2	0	SIF	I/O	Serial I/F 2 enable (P2x port function selection)
FF15H	EPR2	PMD2	SCS21	SCS20	EPR2	0	Enable	Disable	Serial I/F 2 parity enable register
					PMD2	0	Odd	Even	Serial I/F 2 parity mode selection
	R/W				SCS21	0			Serial I/F 2 clock source [SCS21, 20] 0: Mode fOSC3/16; 1: Mode fOSC3/8; 2: Mode fOSC3/4; 3: Mode PT
					SCS20	0			Serial I/F 2 clock source [SCS21, 20] 0: Mode fOSC3/16; 1: Mode fOSC3/8; 2: Mode fOSC3/4; 3: Mode PT
FF16H	RXTRG2	RXEN2	TXTRG2	TXEN2	RXTRG2	0	Run	Stop	Serial I/F 2 receive status (reading)
							Trigger	–	Serial I/F 2 receive trigger (writing)
					RXEN2	0	Enable	Disable	Serial I/F 2 receive enable
	R/W				TXTRG2	0	Run	Stop	Serial I/F 2 transmit status (reading)
							Trigger	–	Serial I/F 2 transmit trigger (writing)
					TXEN2	0	Enable	Disable	Serial I/F 2 transmit enable
FF17H	0	FER2	PER2	OER2	0 *3	– *2			Unused
					FER2	0	Error	No error	Serial I/F 2 framing error flag status (reading)
							Reset	–	Serial I/F 2 framing error flag reset (writing)
					PER2	0	Error	No error	Serial I/F 2 parity error flag status (reading)
	R	R/W					Reset	–	Serial I/F 2 parity error flag reset (writing)
					OER2	0	Error	No error	Serial I/F 2 overrun error flag status (reading)
							Reset	–	Serial I/F 2 overrun error flag reset (writing)
FF18H	TRXD23	TRXD22	TRXD21	TRXD20	TRXD23	– *2	High	Low	Serial I/F 2 transmit/receive data (low-order 4 bits) MSB
					TRXD22	– *2	High	Low	
	R/W				TRXD21	– *2	High	Low	
					TRXD20	– *2	High	Low	LSB
FF19H	TRXD27	TRXD26	TRXD25	TRXD24	TRXD27	– *2	High	Low	Serial I/F 2 transmit/receive data (high-order 4 bits) MSB
					TRXD26	– *2	High	Low	
	R/W				TRXD25	– *2	High	Low	
					TRXD24	– *2	High	Low	LSB
FF1AH	0	0	STPB2	SDP2	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		STPB2	0	2 bits	1 bit	Serial I/F 2 stop bit selection
					SDP2	0	MSB first	LSB first	Serial I/F 2 data input/output permutation selection
FF45H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P13 pull-down control register functions as a general-purpose register when SIF1 (slave) is selected
					PUL12	1	On	Off	P12 pull-down control register (ESIF1=0) functions as a general-purpose register when SIF1 (master) is selected SCLK1 (I) pull-down control register when SIF1 (slave) is selected
	R/W				PUL11	1	On	Off	P11 pull-down control register (ESIF1=0) functions as a general-purpose register when SIF1 is selected
					PUL10	1	On	Off	P10 pull-down control register (ESIF1=0) SIN1 pull-down control register when SIF1 is selected
FF49H	PUL23	PUL22	PUL21	PUL20	PUL23	1	On	Off	P23 pull-down control register functions as a general-purpose register when SIF2 (slave) is selected
					PUL22	1	On	Off	P22 pull-down control register (ESIF2=0) functions as a general-purpose register when SIF2 (master) is selected SCLK2 (I) pull-down control register when SIF2 (slave) is selected
	R/W				PUL21	1	On	Off	P21 pull-down control register (ESIF2=0) functions as a general-purpose register when SIF2 is selected
					PUL20	1	On	Off	P20 pull-down control register (ESIF2=0) SIN2 pull-down control register when SIF2 is selected

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.10.9.1(b) Serial interface control bits

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF64H	0	SMD11	SMD10	ESIF1	0 *3	– *2			Unused
					SMD11	0			Serial I/F 1 mode selection [SMD11, 10] 0: Mode Clk-sync. master; 1: Clk-sync. slave; 2: Mode Async. 7-bit; 3: Async. 8-bit
					SMD10	0			
	R	R/W			ESIF1	0	SIF	I/O	Serial I/F 1 enable (P1x port function selection)
FF65H	EPR1	PMD1	SCS11	SCS10	EPR1	0	Enable	Disable	Serial I/F 1 parity enable register
					PMD1	0	Odd	Even	Serial I/F 1 parity mode selection
	R/W				SCS11	0			Serial I/F 1 clock source [SCS11, 10] 0: Mode fosc3/16; 1: fosc3/8; 2: fosc3/4; 3: PT
					SCS10	0			
FF66H	RXTRG1	RXEN1	TXTRG1	TXEN1	RXTRG1	0	Run	Stop	Serial I/F 1 receive status (reading)
							Trigger	–	Serial I/F 1 receive trigger (writing)
					RXEN1	0	Enable	Disable	Serial I/F 1 receive enable
					TXTRG1	0	Run	Stop	Serial I/F 1 transmit status (reading)
	R/W						Trigger	–	Serial I/F 1 transmit trigger (writing)
					TXEN1	0	Enable	Disable	Serial I/F 1 transmit enable
FF67H	0	FER1	PER1	OER1	0 *3	– *2			Unused
					FER1	0	Error	No error	Serial I/F 1 framing error flag status (reading)
							Reset	–	Serial I/F 1 framing error flag reset (writing)
					PER1	0	Error	No error	Serial I/F 1 parity error flag status (reading)
							Reset	–	Serial I/F 1 parity error flag reset (writing)
	R	R/W			OER1	0	Error	No error	Serial I/F 1 overrun error flag status (reading)
							Reset	–	Serial I/F 1 overrun error flag reset (writing)
FF68H	TRXD13	TRXD12	TRXD11	TRXD10	TRXD13	– *2	High	Low	Serial I/F 1 transmit/receive data (low-order 4 bits)
					TRXD12	– *2	High	Low	
					TRXD11	– *2	High	Low	
	R/W				TRXD10	– *2	High	Low	LSB
FF69H	TRXD17	TRXD16	TRXD15	TRXD14	TRXD17	– *2	High	Low	MSB
					TRXD16	– *2	High	Low	Serial I/F 1 transmit/receive data (high-order 4 bits)
					TRXD15	– *2	High	Low	
	R/W				TRXD14	– *2	High	Low	
FF6AH	0	0	STPB1	SDP1	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		STPB1	0	2 bits	1 bit	Serial I/F 1 stop bit selection
					SDP1	0	MSB first	LSB first	Serial I/F 1 data input/output permutation selection
FFE0H	0	EISER2	EISTR2	EISRC2	0 *3	– *2			Unused
					EISER2	0	Enable	Mask	Interrupt mask register (Serial I/F 2 error)
	R	R/W			EISTR2	0	Enable	Mask	Interrupt mask register (Serial I/F 2 transmit completion)
					EISRC2	0	Enable	Mask	Interrupt mask register (Serial I/F 2 receive completion)
FFE1H	0	EISER1	EISTR1	EISRC1	0 *3	– *2			Unused
					EISER1	0	Enable	Mask	Interrupt mask register (Serial I/F 1 error)
	R	R/W			EISTR1	0	Enable	Mask	Interrupt mask register (Serial I/F 1 transmit completion)
					EISRC1	0	Enable	Mask	Interrupt mask register (Serial I/F 1 receive completion)
FFF0H	0	ISER2	ISTR2	ISRC2	0 *3	– *2	(R)	(R)	Unused
					ISER2	0	Yes	No	Interrupt factor flag (Serial I/F 2 error)
	R	R/W			ISTR2	0	(W)	(W)	Interrupt factor flag (Serial I/F 2 transmit completion)
					ISRC2	0	Reset	Invalid	Interrupt factor flag (Serial I/F 2 receive completion)
FFF1H	0	ISER1	ISTR1	ISRC1	0 *3	– *2	(R)	(R)	Unused
					ISER1	0	Yes	No	Interrupt factor flag (Serial I/F 1 error)
	R	R/W			ISTR1	0	(W)	(W)	Interrupt factor flag (Serial I/F 1 transmit completion)
					ISRC1	0	Reset	Invalid	Interrupt factor flag (Serial I/F 1 receive completion)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

ESIF1: Serial interface 1 enable register (P1 port function selection) (FF64H•D0)
ESIF2: Serial interface 2 enable register (P2 port function selection) (FF14H•D0)
Sets P10–P13 and P20–P23 to the input/output ports for the serial interface.

When "1" is written: Serial interface
When "0" is written: I/O port
Reading: Valid

The ESIF1 is the serial interface 1 enable register and P10–P13 terminals become serial input/output terminals (SIN1, SOUT1, SCLK1, SRDY1) when "1" is written. The ESIF2 is the serial interface 2 enable register and P20–P23 terminals become serial input/output terminals (SIN2, SOUT2, SCLK2, SRDY2) when "1" is written. They become I/O port terminals when "0" is written.
Also, see Table 4.10.3.2 for the terminal settings according to the transfer modes.
At initial reset, this register is set to "0".

PUL10: SIN1 pull-down control register (FF45H•D0)
PUL20: SIN2 pull-down control register (FF49H•D0)
PUL12: SCLK1 pull-down control register (FF45H•D2)
PUL22: SCLK2 pull-down control register (FF49H•D2)
Sets the pull-down of the SINx terminal and the SCLKx terminals (in the slave mode).

When "1" is written: Pull-down ON
When "0" is written: Pull-down OFF
Reading: Valid

Sets the pull-down resistor built into the SINx (P10/P20) and SCLKx (P12/P22) terminals to ON or OFF. SCLKx pull-down is effective only in the slave mode. In the master mode, the PUL12/PULL22 register can be used as a general purpose register.
At initial reset, these registers are set to "1" and the lines are pulled down.

SMD10, SMD11: Serial interface 1 mode selection registers (FF64H•D1, D2)
SMD20, SMD21: Serial interface 2 mode selection registers (FF14H•D1, D2)
Set the transfer modes as shown in Table 4.10.9.2.

Table 4.10.9.2 Transfer mode settings

SMDx1	SMDx0	Mode
1	1	8-bit asynchronous
1	0	7-bit asynchronous
0	1	Clock synchronous slave
0	0	Clock synchronous master

SMDx0 and SMDx1 can also read out.
At initial reset, these registers are set to "0".

SCS10, SCS11: Serial interface 1 clock source selection registers (FF65H•D0, D1)
SCS20, SCS21: Serial interface 2 clock source selection registers (FF15H•D0, D1)
Select the clock source as shown in Table 4.10.9.3.

Table 4.10.9.3 Clock source selection

SCSx1	SCSx0	Clock source
1	1	Programmable timer
1	0	f_{OSC3} / 4
0	1	f_{OSC3} / 8
0	0	f_{OSC3} / 16

SCSx0 and SCSx1 can also be read out.
In the clock synchronous slave mode, setting of these registers are invalid.
At initial reset, these registers are set to "0".

SDP1: Serial interface 1 data input/output permutation select register (FF6AH•D0)
SDP2: Serial interface 2 data input/output permutation select register (FF1AH•D0)
Selects the serial data input/output permutation.

When "1" is written: MSB first
When "0" is written: LSB first
Reading: Valid

Select whether the data input/output permutation will be MSB first or LSB first.
At initial reset, this register is set to "0".

STPB1: Serial interface 1 stop bit select register (FF6AH•D1)
STPB2: Serial interface 2 stop bit select register (FF1AH•D1)
Selects the stop bit length for asynchronous data transfer.

When "1" is written: 2 bits
When "0" is written: 1 bit
Reading: Valid

STPBx is the stop bit select register that is effective in asynchronous mode. When "1" is written to STPBx, the stop bit length is set to 2 bits, and when "0" is written, it is set to 1 bit.
In clock synchronous mode, no start/stop bits can be added to transfer data. Therefore, STPBx is ineffective.
At initial reset, STPBx is set to "0" (1 bit).

EPR1: Serial interface 1 parity enable register (FF65H•D3)
EPR2: Serial interface 2 parity enable register (FF15H•D3)
Selects the parity function.

When "1" is written: With parity
When "0" is written: Non parity
Reading: Valid

Selects whether or not to check parity of the received data and to add a parity bit to the transmitting data. When "1" is written to EPRx, the most significant bit of the received data is considered to be the parity bit and a parity check is executed. A parity bit is added to the transmitting data. When "0" is written, neither checking is done nor is a parity bit added.
Parity is valid only in asynchronous mode and the EPRx setting becomes invalid in the clock synchronous mode.
At initial reset, this register is set to "0".

PMD1: Serial interface 1 parity mode selection register (FF65H•D2)
PMD2: Serial interface 2 parity mode selection register (FF15H•D2)
Selects odd parity/even parity.

When "1" is written: Odd parity
When "0" is written: Even parity
Reading: Valid

When "1" is written to PMDx, odd parity is selected and even parity is selected when "0" is written. The parity check and addition of a parity bit is only valid when "1" has been written to EPRx. When "0" has been written to EPRx, the parity setting by PMDx becomes invalid.
At initial reset, this register is set to "0".

TXEN1: Serial interface 1 transmit enable register (FF66H•D0)
TXEN2: Serial interface 2 transmit enable register (FF16H•D0)
Sets the serial interface to the transmit enabled status.

When "1" is written: Transmit enabled
When "0" is written: Transmit disabled
Reading: Valid

When "1" is written to TXENx, the serial interface shifts to the transmit enabled status and shifts to the transmit disabled status when "0" is written.
Set TXENx to "0" when making the initial settings of the serial interface and similar operations.
At initial reset, this register is set to "0".

TXTRG1: Serial interface 1 transmit trigger/status (FF66H•D1)
TXTRG2: Serial interface 2 transmit trigger/status (FF16H•D1)
Functions as the transmit start trigger and the operation status indicator (transmitting/stop status).

When "1" is read: During transmitting
When "0" is read: During stop

When "1" is written: Start transmitting
When "0" is written: Invalid

Starts transmitting when "1" is written to TXTRGx after writing the transmitting data.
TXTRGx can be read as the status. When set to "1", it indicates transmitting operation, and "0" indicates transmitting stop.
At initial reset, TXTRGx is set to "0".

RXEN1: Serial interface 1 receive enable register (FF66H•D2)
RXEN2: Serial interface 2 receive enable register (FF16H•D2)
Sets the serial interface to the receive enabled status.

When "1" is written: Receive enabled
When "0" is written: Receive disabled
Reading: Valid

When "1" is written to RXENx, the serial interface shifts to the receive enabled status and shifts to the receive disabled status when "0" is written.
Set RXENx to "0" when making the initial settings of the serial interface and similar operations.
At initial reset, this register is set to "0".

RXTRG1: Serial interface 1 receive trigger/status (FF66H•D3)
RXTRG2: Serial interface 2 receive trigger/status (FF16H•D3)
Functions as the receive start trigger or preparation for the following data receiving and the operation status indicator (during receiving/during stop).

When "1" is read: During receiving
When "0" is read: During stop

When "1" is written: Start receiving/following data receiving preparation
When "0" is written: Invalid

RXTRGx has a slightly different operation in the clock synchronous system and the asynchronous system.
The RXTRGx in the clock synchronous system is used as the trigger for starting receive operation.
Write "1" into RXTRGx to start receiving at the point where the receive data has been read and the following receive preparation has been done. (In the slave mode, SRDYx is asserted at the point where "1" has been written into the RXTRGx.)

In the asynchronous system, RXTRGx is used for preparation of the following data receiving. Read the received data located in the receive data buffer and write "1" into RXTRGx to inform that the receive data buffer has shifted to empty. When "1" has not been written to RXTRGx, the overrun error flag OERx is set to "1" at the point where the following receiving has been completed. (When the receiving has been completed between the operation to read the received data and the operation to write "1" into RXTRGx, an overrun error occurs.)
In addition, RXTRGx can be read as the status. In either clock synchronous mode or asynchronous mode, when RXTRGx is set to "1", it indicates receiving operation and when set to "0", it indicates that receiving has stopped.
At initial reset, RXTRGx is set to "0".

TRXD10–TRXD17: Serial interface 1 transmit/receive data (FF68H, FF69H)
TRXD20–TRXD27: Serial interface 2 transmit/receive data (FF18H, FF19H)

During transmitting

Transmitting data is set.

When "1" is written: High level
When "0" is written: Low level

Write the transmitting data prior to starting transmission.
In the case of continuous transmitting, wait for the transmit completion interrupt, then write the data.
The TRXDx7 becomes invalid for the 7-bit asynchronous mode.
Converted serial data for which the bits set at "1" as high (V_{DD}) level and for which the bits set at "0" as low (V_{SS}) level are output from the SOUTx terminal.

During receiving

The received data is stored.

When "1" is read: High level
When "0" is read: Low level

The data from the receive data buffer can be read out.
Since the sift register is provided separately from this buffer, reading can be done during a receive operation in the asynchronous mode. (The buffer function is not used in the clock synchronous mode.)
Read the data after waiting for a receive completion interrupt.
When performing parity check in the 7-bit asynchronous mode, "0" is loaded into the 8th bit (TRXDx7) that corresponds to the parity bit.
The serial data input from the SINx terminal is level converted, making the high (V_{DD}) level bit "1" and the low (V_{SS}) level bit "0" and is then loaded into this buffer.
At initial reset, the buffer content is undefined.

OER1: Serial interface 1 overrun error flag (FF67H•D0)
OER2: Serial interface 2 overrun error flag (FF17H•D0)

Indicates the generation of an overrun error.

When "1" is read: Error
When "0" is read: No error

When "1" is written: Reset to "0"
When "0" is written: Invalid

OERx is an error flag that indicates the generation of an overrun error and becomes "1" when an error has been generated.
An overrun error is generated when a receiving of data has completed prior to writing "1" to RXTRGx in the asynchronous mode.
OERx is reset to "0" by writing "1".
OERx is set to "0" at initial reset or when RXENx is set to "0".

PER1: Serial interface 1 parity error flag (FF67H•D1)
PER2: Serial interface 2 parity error flag (FF17H•D1)
Indicates the generation of a parity error.

When "1" is read: Error
When "0" is read: No error

When "1" is written: Reset to "0"
When "0" is written: Invalid

PERx is an error flag that indicates the generation of a parity error and becomes "1" when an error has been generated.
When a parity check is performed in the asynchronous mode, a parity error will be generated if data that does not match the parity is received.
PERx is reset to "0" by writing "1".
PERx is set to "0" at initial reset or when RXENx is set to "0".

FER1: Serial interface 1 framing error flag (FF67H•D2)
FER2: Serial interface 2 framing error flag (FF17H•D2)
Indicates the generation of a framing error.

When "1" is read: Error
When "0" is read: No error

When "1" is written: Reset to "0"
When "0" is written: Invalid

FERx is an error flag that indicates the generation of a framing error and becomes "1" when an error has been generated.
When the stop bit for the receiving in the asynchronous mode has become "0", a framing error is generated.
FERx is reset to "0" by writing "1".
FERx is set to "0" at initial reset or when RXENx is set to "0".

EISRC1, EISTR1, EISER1: Serial interface 1 interrupt mask registers (FFE1H•D0, D1, D2)
EISRC2, EISTR2, EISER2: Serial interface 2 interrupt mask registers (FFE0H•D0, D1, D2)
Enables or disables the generation of an interrupt for the CPU.

When "1" is written: Enabled
When "0" is written: Disabled
Reading: Valid

EISRCx, EISTRx and EISERx are interrupt mask registers that respectively correspond to the interrupt factors for receive completion, transmit completion and receive error. Interrupts set to "1" are enabled and interrupts set to "0" are disabled.
At initial reset, these registers are set to "0".

ISRC1, ISTR1, ISER1: Serial interface 1 interrupt factor flags (FFF1H•D0, D1, D2)
ISRC2, ISTR2, ISER2: Serial interface 2 interrupt factor flags (FFF0H•D0, D1, D2)
Indicates the serial interface interrupt generation status.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

ISRCx, ISTRx and ISERx are interrupt factor flags that respectively correspond to the interrupts for receive completion, transmit completion and receive error, and are set to "1" by generation of each factor.
Transmit completion interrupt factor is generated at the point where the data transmission of the shift register has been completed.
Receive completion interrupt factor is generated at the point where the received data has been transferred into the receive data buffer.

Receive error interrupt factor is generated when a parity error, framing error or overrun error has been detected during data receiving.
When set in this manner, if the corresponding interrupt enable mask is set to "1" and the CPU is set to interrupt enabled status (I flag = "1"), an interrupt will be generated to the CPU.
Regardless of the interrupt mask register setting, the interrupt factor flag will be set to "1" by the occurrence of an interrupt generation condition.
The interrupt factor flag is reset to "0" by writing "1".
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.10.10 Programming notes

(1) Be sure to initialize the serial interface mode in the transmit/receive disabled status (TXENx = RXENx = "0").

(2) Do not perform double trigger (writing "1") to TXTRGx (RXTRGx) when the serial interface is in the transmitting (receiving) operation.

(3) In the clock synchronous mode, since one clock line (SCLKx) is shared for both transmitting and receiving, transmitting and receiving cannot be performed simultaneously. (Half duplex only is possible in clock synchronous mode.)
Consequently, be sure not to write "1" to RXTRGx (TXTRGx) when TXTRGx (RXTRGx) is "1".

(4) When a parity error or framing error is generated during receiving in the asynchronous mode, the receiving error interrupt factor flag ISERx is set to "1" prior to the receive completion interrupt factor flag ISRCx for the time indicated in Table 4.10.10.1. Consequently, when an error is generated, you should reset the receiving complete interrupt factor flag ISRCx to "0" by providing a wait time in error processing routines and similar routines.
When an overrun error is generated, the receiving complete interrupt factor flag ISRCx is not set to "1" and a receiving complete interrupt is not generated.

Table 4.10.10.1 Time difference between ISERx and ISRCx on error generation

Clock source	Time difference
f_{OSC3} / n	1/2 cycles of f_{OSC3} / n
Programmable timer	1 cycle of timer 1 underflow

(5) When the demultiplied signal of the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the serial interface.
A time interval of 5 msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before starting transmitting/receiving of serial interface. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 7, "Electrical Characteristics".)
At initial reset, the OSC3 oscillation circuit is set to OFF status.

(6) Be aware that the maximum clock frequency for the serial interface is limited to 2 MHz.

(7) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.11 Sound Generator

4.11.1 Configuration of sound generator

The S1C63808 has a built-in sound generator for generating a buzzer signal.
Hence, the generated buzzer signal can be output from the R01 (BZ) terminal.
Aside permitting the respective setting of the buzzer signal frequency and sound level to 8 stages, it permits the adding of a digital envelope by means of duty ratio control. It also has a one-shot output function for outputting key operated sounds.
Figure 4.11.1.1 shows the configuration of the sound generator.

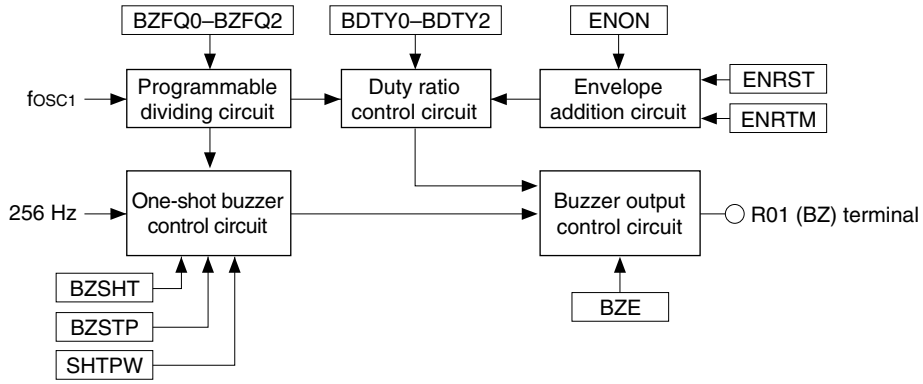


Fig. 4.11.1.1 Configuration of sound generator

Note: If the BZ terminal is used to drive an external component that consumes a large amount of current such as a bipolar transistor, design the pattern of traces on the printed circuit board so that the operation of the external component does not affect the IC power supply. Refer to <Output Terminals> in Section 5.3, "Precautions on Mounting", for more information.

4.11.2 Control of buzzer output

The BZ signal generated by the sound generator is output from the R01 (BZ) terminal by setting "1" for the buzzer output enable register BZE. When "0" is set to BZE register, the R01 (BZ) terminal goes low (VSS).

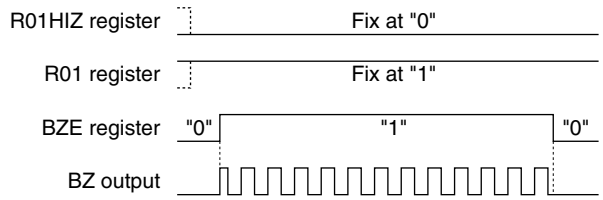


Fig. 4.11.2.1 Buzzer signal output timing chart

Notes: • When using the R01 port as the BZ output port, fix the data register R01 at "1" and the high impedance control register R01HIZ at "0" (data output).

• Since it generates the buzzer signal that is out of synchronization with the BZE register, hazards may at times be produced when the signal goes on/off due to the setting of the BZE register.

4.11.3 Setting of buzzer frequency and sound level

The divided signal of the OSC1 oscillation clock (32.768 kHz) is used for the buzzer signal and it is set up such that 8 types of frequencies can be selected by changing this division ratio. Frequency selection is done by setting the buzzer frequency selection registers BZFQ0–BZFQ2 as shown in Table 4.11.3.1.

Table 4.11.3.1 Buzzer signal frequency setting

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

The buzzer sound level is changed by controlling the duty ratio of the buzzer signal.
The duty ratio can be selected from among the 8 types shown in Table 4.11.3.2 according to the setting of the buzzer duty selection registers BDTY0–BDTY2.

Table 4.11.3.2 Duty ratio setting

Level	BDTY2	BDTY1	BDTY0	Duty ratio by buzzer frequency (Hz)			
				4096.0 2048.0	3276.8 1638.4	2730.7 1365.3	2340.6 1170.3
Level 1 (Max.)	0	0	0	8/16	8/20	12/24	12/28
Level 2	0	0	1	7/16	7/20	11/24	11/28
Level 3	0	1	0	6/16	6/20	10/24	10/28
Level 4	0	1	1	5/16	5/20	9/24	9/28
Level 5	1	0	0	4/16	4/20	8/24	8/28
Level 6	1	0	1	3/16	3/20	7/24	7/28
Level 7	1	1	0	2/16	2/20	6/24	6/28
Level 8 (Min.)	1	1	1	1/16	1/20	5/24	5/28

When the high level output time has been made TH and when the low level output time has been made TL due to the ratio of the pulse width to the pulse synchronization, the duty ratio becomes TH/(TH+TL).
When BDTY0–BDTY2 have all been set to "0", the duty ratio becomes maximum and the sound level also becomes maximum. Conversely, when BDTY0–BDTY2 have all been set to "1", the duty ratio becomes minimum and the sound level also becomes minimum.
The duty ratio that can be set is different depending on the frequency that has been set, so see Table 4.11.3.2.

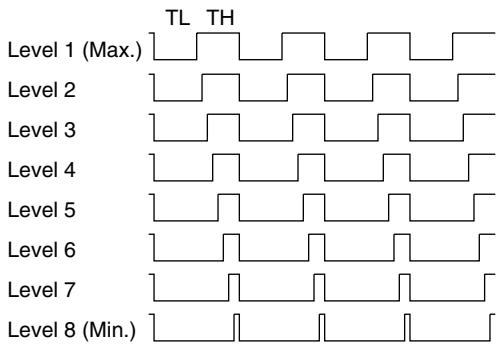


Fig. 4.11.3.1 Duty ratio of the buzzer signal waveform

Note: When a digital envelope has been added to the buzzer signal, the BDTY0–BDTY2 settings will be invalid due to the control of the duty ratio.

4.11.4 Digital envelope

A digital envelope for duty control can be added to the buzzer signal.
The envelope can be controlled by staged changing of the same duty envelope as detailed in Table 4.11.3.2 in the preceding item from level 1 (maximum) to level 8 (minimum).
The addition of an envelope to the buzzer signal can be done by writing "1" into ENON, but when "0" has been written it is not added.
When a buzzer signal output is begun (writing "1" into BZE) after setting ENON, the duty ratio shifts to level 1 (maximum) and changes in stages to level 8.
When attenuated down to level 8 (minimum), it is retained at that level. The duty ratio can be returned to maximum, by writing "1" into register ENRST during output of a envelope attached buzzer signal.
The envelope attenuation time (time for changing of the duty ratio) can be selected by the register ENRTM. The time for a 1 stage level change is 62.5 msec (16 Hz), when "0" has been written into ENRTM and 125 msec (8 Hz), when to "1" has been written. However, there is also a max. 4 msec error from envelope ON, up to the first change.
Figure 4.11.4.1 shows the timing chart of the digital envelope.

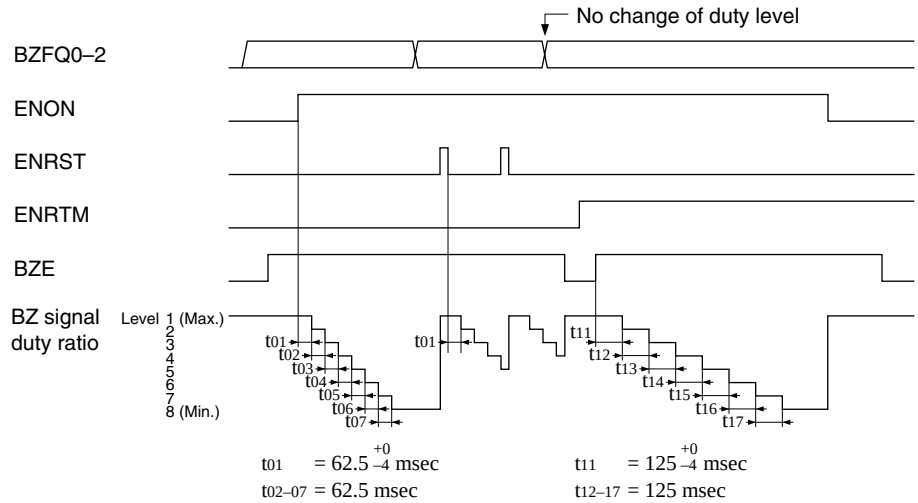


Fig. 4.11.4.1 Timing chart for digital envelope

4.11.5 One-shot output

The sound generator has a one-shot output function for outputting a short duration buzzer signal for key operation sounds and similar effects. Either 125 msec or 31.25 msec can be selected by SHTPW register for one-shot buzzer signal output time.
The output of the one-shot buzzer is controlled by writing "1" into the one-shot buzzer trigger BZSHT. When this trigger has been assigned, a buzzer signal in synchronization with the internal 256 Hz signal is output from the buzzer output terminal. Thereafter, when the set time has elapsed, a buzzer signal in synchronization with the 256 Hz signal goes off in the same manner as for the start of output.
The BZSHT also permits reading. When BZSHT is "1", the one-shot output circuit is in operation (during one-shot output) and when it is "0", it shows that the circuit is in the ready (outputtable) status.

In addition, it can also terminate one-shot output prior to the elapsing of the set time. This is done by writing a "1" into the one-shot buzzer stop BZSTP. In this case as well, the buzzer signal goes off in synchronization with the 256 Hz signal.

When "1" is written to BZSHT again during a one-shot output, a new one-shot output for 125 msec or 31.25 msec starts from that point (in synchronization with the 256 Hz signal).

The one-shot output cannot add an envelope for short durations. However, the sound level can be set by selecting the duty ratio, and the frequency can also be set.
One-shot output is invalid during normal buzzer output (during BZE = "1").

Figure 4.11.5.1 shows timing chart for one-shot output.

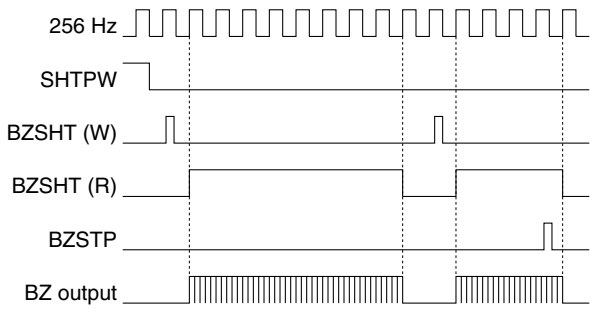


Fig. 4.11.5.1 Timing chart for one-shot output

4.11.6 I/O memory of sound generator

Table 4.11.6.1 shows the I/O addresses and the control bits for the sound generator.

Table 4.11.6.1 Control bits of sound generator

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF6CH	ENRTM	ENRST	ENON	BZE	ENRTM	0	1 sec	0.5 sec	Envelope releasing time selection
					ENRST*3	Reset	Reset	Invalid	Envelope reset (writing)
	R/W	W	R/W		ENON	0	On	Off	Envelope On/Off
					BZE	0	Enable	Disable	Buzzer output enable
FF6DH	0	BZSTP	BZSHT	SHTPW	0 *3	– *2			Unused
					BZSTP*3	0	Stop	Invalid	1-shot buzzer stop (writing)
					BZSHT	0	Trigger	Invalid	1-shot buzzer trigger (writing)
	R	W	R/W				Busy	Ready	1-shot buzzer status (reading)
					SHTPW	0	125msec	31.25msec	1-shot buzzer pulse width setting
FF6EH	0	BZFQ2	BZFQ1	BZFQ0	0 *3	– *2			Unused
					BZFQ2	0			Buzzer frequency selection [BZFQ2, 1, 0] 0 1 2 3 / Frequency (Hz) 4096.0 3276.8 2730.7 2340.6 / [BZFQ2, 1, 0] 4 5 6 7 / Frequency (Hz) 2048.0 1638.4 1365.3 1170.3
	R	R/W			BZFQ1	0			
					BZFQ0	0			
FF6FH	0	BDTY2	BDTY1	BDTY0	0 *3	– *2			Unused
					BDTY2	0			Buzzer signal duty ratio selection (refer to main manual)
	R	R/W			BDTY1	0			
					BDTY0	0			

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

BZE: Buzzer output control register (FF6CH•D0)

Controls the buzzer signal output.

When "1" is written: Buzzer output On
When "0" is written: Buzzer output Off
Reading: Valid

When "1" is written to BZE, the BZ signal is output from the R01 (BZ) terminal.
When "0" is written, the R01 (BZ) terminal goes to low (VSS).
At initial reset, this register is set to "0".

Note: When using the R01 port as the BZ output port, fix the data register R01 at "1" and the high impedance control register R01HIZ at "0" (data output).

BZFQ0–BZFQ2: Buzzer frequency selection registers (FF6EH•D0–D2)

Selects the buzzer signal frequency.

Table 4.11.6.2 Buzzer signal frequency setting

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

Select the buzzer frequency from among the above 8 types that have divided the oscillation clock.
At initial reset, these registers are set to "0".

BDTY0–BDTY2: Duty level selection registers (FF6FH•D0–D2)

Selects the duty ratio of the buzzer signal as shown in Table 4.11.6.3.

Table 4.11.6.3 Duty ratio setting

Level	BDTY2	BDTY1	BDTY0	Duty ratio by buzzer frequency (Hz)			
				4096.0 2048.0	3276.8 1638.4	2730.7 1365.3	2340.6 1170.3
Level 1 (Max.)	0	0	0	8/16	8/20	12/24	12/28
Level 2	0	0	1	7/16	7/20	11/24	11/28
Level 3	0	1	0	6/16	6/20	10/24	10/28
Level 4	0	1	1	5/16	5/20	9/24	9/28
Level 5	1	0	0	4/16	4/20	8/24	8/28
Level 6	1	0	1	3/16	3/20	7/24	7/28
Level 7	1	1	0	2/16	2/20	6/24	6/28
Level 8 (Min.)	1	1	1	1/16	1/20	5/24	5/28

The sound level of this buzzer can be set by selecting this duty ratio.
However, when the envelope has been set to on (ENON = "1"), this setting becomes invalid.
At initial reset, these registers are set to "0".

ENRST: Envelope reset (FF6CH•D2)

Resets the envelope.

When "1" is written: Reset
When "0" is written: No operation
Reading: Always "0"

Writing "1" into ENRST resets envelope and the duty ratio becomes maximum. If an envelope has not been added (ENON = "0") and if no buzzer signal is being output, the reset becomes invalid. Writing "0" is also invalid.
This bit is dedicated for writing, and is always "0" for reading.

ENON: Envelope On/Off control register (FF6CH•D1)

Controls the addition of an envelope onto the buzzer signal.

When "1" is written: On
When "0" is written: Off
Reading: Valid

Writing "1" into the ENON causes an envelope to be added during buzzer signal output. When a "0" has been written, an envelope is not added.
At initial reset, this register is set to "0".

ENRTM: Envelope releasing time selection register (FF6CH•D3)

Selects the envelope releasing time that is added to the buzzer signal.

When "1" is written: 1.0 sec (125 msec × 7 = 875 msec)
When "0" is written: 0.5 sec (62.5 msec × 7 = 437.5 msec)
Reading: Valid

The releasing time of the digital envelope is determined by the time for converting the duty ratio.
When "1" has been written in ENRTM, it becomes 125 msec (8 Hz) units and when "0" has been written, it becomes 62.5 msec (16 Hz) units.
At initial reset, this register is set to "0".

SHTPW: One-shot buzzer pulse width setting register (FF6DH•D0)

Selects the output time of the one-shot buzzer.

When "1" is written: 125 msec
When "0" is written: 31.25 msec
Reading: Valid

Writing "1" into SHTPW causes the one-short output time to be set at 125 msec, and writing "0" causes it to be set to 31.25 msec. It does not affect normal buzzer output.
At initial reset, this register is set to "0".

BZSHT: One-shot buzzer trigger/status (FF6DH•D1)

Controls the one-shot buzzer output.

• ***When writing***

When "1" is written: Trigger
When "0" is written: No operation

Writing "1" into BZSHT causes the one-short output circuit to operate and a buzzer signal to be output. This output is automatically turned off after the time set by SHTPW has elapsed. The one-shot output is only valid when the normal buzzer output is off (BZE = "0") and will be invalid when the normal buzzer output is on (BZE = "1"). When a re-trigger is assigned during a one-shot output, the one-shot output time set with SHTPW is measured again from that point (time extension).

• ***When reading***

When "1" is read: BUSY
When "0" is read: READY

During reading BZSHT shows the operation status of the one-shot output circuit. During one-shot output, BZSHT becomes "1" and the output goes off, it shifts to "0".
At initial reset, this bit is set to "0".

BZSTP: One-shot buzzer stop (FF6DH•D2)

Stops the one-shot buzzer output.

When "1" is written: Stop
When "0" is written: No operation
Reading: Always "0"

Writing "1" into BZSTP permits the one-shot buzzer output to be turned off prior to the elapsing of the time set by SHTPW. Writing "0" is invalid and writing "1" is also invalid except during one-shot output. This bit is dedicated for writing, and is always "0" for reading.

4.11.7 Programming notes

(1) When using the R01 port as the BZ output port, fix the data register R01 at "1" and the high impedance control register R01HIZ at "0" (data output).

(2) Since it generates a buzzer signal that is out of synchronization with the BZE register, hazards may at times be produced when the signal goes on/off due to the setting of the BZE register.

(3) The one-shot output is only valid when the normal buzzer output is off (BZE = "0") and will be invalid when the normal buzzer output is on (BZE = "1").

4.12 Integer Multiplier

4.12.1 Configuration of integer multiplier

The S1C63808 has a built-in unsigned-integer multiplier. This multiplier performs 8 bits × 8 bits of multiplication or 16 bits ÷ 8 bits of division and returns the results and three flag states.
Figure 4.12.1.1 shows the configuration of the integer multiplier.

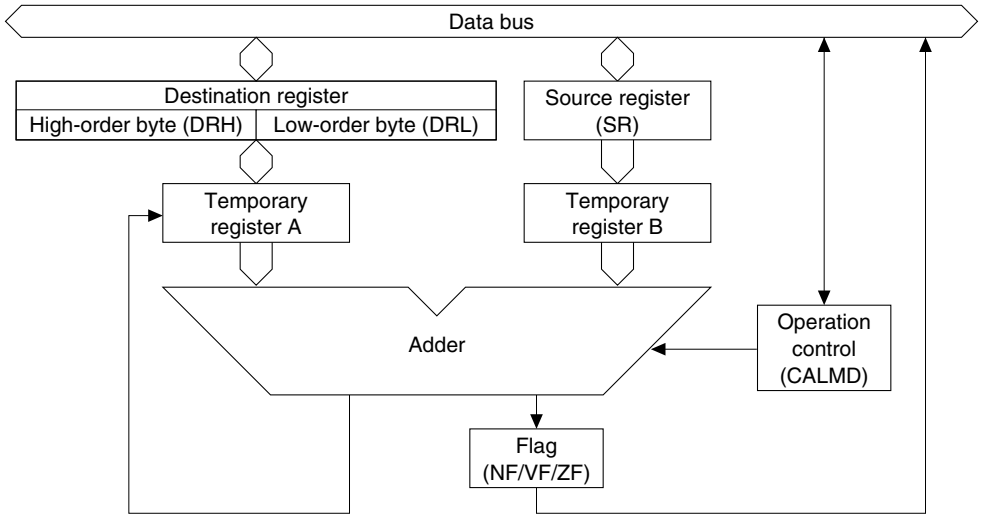


Fig. 4.12.1.1 Configuration of the integer multiplier

4.12.2 Multiplication mode

To perform a multiplication, set the multiplier to the source register (SR) and the multiplicand to the low-order 8 bits (DRL) of the destination register, then write "0" to the calculation mode selection register (CALMD). The multiplication takes 10 CPU clock cycles from writing "0" to CALMD until the 16-bit product is loaded into the destination register (DRH and DRL). At the same time the result is loaded, the operation flags (NF, VF and ZF) are updated.
The following shows the conditions that change the operation flag states and examples of multiplication.

N flag: Set when the MSB of DRH is "1" and reset when it is "0".
V flag: Always reset after a multiplication.
Z flag: Set when the 16-bit value in DRH/DRL is 0000H and reset when it is not 0000H.

<Examples of multiplication>

DRL (multiplicand)	SR (multiplier)	DRH/DRL (product)	NF	VF	ZF
00H	64H	0000H	0	0	1
64H	58H	2260H	0	0	0
C8H	58H	44C0H	0	0	0
C8H	A5H	80E8H	1	0	0

4.12.3 Division mode

To perform a division, set the divisor to the source register (SR) and the dividend to the destination register (DRH and DRL), then write "1" to the calculation mode selection register (CALMD). The division takes 10 CPU clock cycles from writing "1" to CALMD until the quotient is loaded into the low-order 8 bits (DRL) of the destination register and the remainder is loaded into the high-order 8 bits (DRH) of the destination register. At the same time the result is loaded, the operation flags (NF, VF and ZF) are updated.
However, when an overflow results (if the quotient exceeds the 8-bit range), the destination register (DRH and DRL) does not change its contents as it maintains the dividend.
The following shows the conditions that change the operation flag states and examples of division.

N flag: Set when the MSB of DRL is "1" and reset when it is "0".
V flag: Set when the quotient exceeds the 8-bit range and reset when it is within the 8-bit range.
Z flag: Set when the 8-bit value in DRL is 00H and reset when it is not 00H.

<Examples of division>

DRH/DRL (dividend)	SR (divisor)	DRL (quotient)	DRH (remainder)	NF	VF	ZF
1A16H	64H	42H	4EH	0	0	0
332CH	64H	83H	00H	1	0	0
0000H	58H	00H	00H	0	0	1
2468H	13H	68H	24H	1	1	0

In the example of "2468H" ÷ "13H" shown above, DRH/DRL maintains the dividend because the quotient overflows the 8-bit. To get the correct results when an overflow has occurred, perform the division with two steps as shown below.

1. Divide the high-order 8 bits of the dividend (24H) by the divisor (13H) and then store the quotient (01H) to memory.

DRH/DRL (dividend)	SR (divisor)	DRL (quotient)	DRH (remainder)	NF	VF	ZF
0024H	13H	01H	11H	0	0	0

2. Keep the remainder (11H) in DRH and load the low-order 8 bits of the dividend (68H) to DRL, then perform division again.

DRH/DRL (dividend)	SR (divisor)	DRL (quotient)	DRH (remainder)	NF	VF	ZF
1168H	13H	EAH	0AH	1	0	0

The correct result is obtained as the quotient = 01EAH (the first and second results of DRL are merged) and the remainder = 0AH. However, since the operation flags (NF/VF/ZF) are changed in each step, they cannot indicate the states according to the final operation results.

Note: Make sure that the division results are correct using software as the hardware does not check.

4.12.4 Execution cycle

Both the multiplication and division take 10 CPU cycles for an operation. Therefore, before the results can be read from the destination register DRH/DRL, wait at least 5 bus cycles after writing to CALMD. The same applies to reading the operation flags NF/VF/ZF.
The following shows a sample program.

```
      ldb  %ext, src_data@h
      ldb  %xl, src_data@l      ; Set RAM address for operand
      ldb  %ext, au@h
      ldb  %yl, au@l            ; Set multiplier I/O memory address
;
      ldb  %ba, [%x]+
      ldb  [%y]+, %ba           ; Set data to SR
      ldb  %ba, [%x]+
      ldb  [%y]+, %ba           ; Set data to DRL
      ldb  %ba, [%x]+
      ldb  [%y]+, %ba           ; Set data to DRH
;
      ld   [%y], 0b0001         ; Start operation (select calculation mode)
;
      ldb  %ext, rslt_data@h
      ldb  %xl, rslt_data@l     ; Set result store address
      nop
      nop
      nop                       ; Dummy instructions to wait end of operation
;
      bit  [%y], 0b0100
      jrnz overflow             ; Jump to error routine if VF = "1"
;
      add  %y, -4               ; Set DRL again
;
      ldb  %ba, [%y]+
      ldb  [%x]+, %ba           ; Store result (quotient) into RAM
      ldb  %ba, [%y]+
      ldb  [%x]+, %ba           ; Store result (remainder) into RAM
```

4.12.5 I/O memory of integer multiplier

Table 4.12.5.1 shows the I/O addresses and the control bits for the integer multiplier.

Table 4.12.5.1 Control bits of integer multiplier

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF80H	SR3	SR2	SR1	SR0	SR3	– *2			Source register (low-order 4 bits)
					SR2	– *2			
					SR1	– *2			
	R/W				SR0	– *2			LSB
FF81H	SR7	SR6	SR5	SR4	SR7	– *2			MSB
					SR6	– *2			Source register (high-order 4 bits)
					SR5	– *2			
	R/W				SR4	– *2			
FF82H	DRL3	DRL2	DRL1	DRL0	DRL3	– *2			Low-order 8-bit destination register
					DRL2	– *2			
					DRL1	– *2			(low-order 4 bits)
	R/W				DRL0	– *2			LSB
FF83H	DRL7	DRL6	DRL5	DRL4	DRL7	– *2			MSB
					DRL6	– *2			Low-order 8-bit destination register
					DRL5	– *2			
	R/W				DRL4	– *2			(high-order 4 bits)
FF84H	DRH3	DRH2	DRH1	DRH0	DRH3	– *2			High-order 8-bit destination register
					DRH2	– *2			
					DRH1	– *2			(low-order 4 bits)
	R/W				DRH0	– *2			LSB
FF85H	DRH7	DRH6	DRH5	DRH4	DRH7	– *2			MSB
					DRH6	– *2			High-order 8-bit destination register
					DRH5	– *2			
	R/W				DRH4	– *2			(high-order 4 bits)
FF86H	NF	VF	ZF	CALMD	NF	0	Negative	Positive	Negative flag
					VF	0	Overflow	No	Overflow flag
					ZF	0	Zero	No	Zero flag
	R			R/W	CALMD	0	Run	Stop	Operation status (reading)
							Div.	Mult.	Calculation mode selection (writing)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

SR0–SR7: Source register (FF80H, FF81H)

Used to set multipliers and divisors.
Set the low-order 4 bits of data to SR0–SR3 and the high-order 4 bits to SR4–SR7.
This register maintains the latest set value until the next writing, so it is not necessary to set data for each operation if the same multiplier and divisor is used in a series of operations.
At initial reset, this register is undefined.

DRL0–DRL7: Destination register low-order 8 bits (FF82H, FF83H)

Used to set multiplicands and low-order 8 bits of dividends.
Set the low-order 4 bits of data to DRL0–DRL3 and the high-order 4 bits to DRL4–DRL7.
Data written to this register is loaded to the arithmetic circuit when an operation starts (by writing to FF86H•D0), and then a multiplication or a division is performed in 10 CPU clock cycles (5 bus cycles).
After the operation has finished, the low-order 8 bits of the product or the quotient are loaded to this register.
However, if an overflow occurs in a division process, the quotient is not loaded and the low-order 8 bits of the dividend remains.
At initial reset, this register is undefined.

DRH0–DRH7: Destination register high-order 8 bits (FF84H, FF85H)

Used to set high-order 8 bits of dividends.
Set the low-order 4 bits of data to DRH0–DRH3 and the high-order 4 bits to DRH4–DRH7.
At the start of a multiplication (by writing "0" to FF86H•D0), the contents in this register are ignored.
After 10 CPU cycles (5 bus cycles) of multiplication process has finished, the high-order 8 bits of the product are loaded in this register.
In a division process, data written to this register is loaded to the arithmetic circuit when an operation starts (by writing "1" to FF86H•D0), and then a division is performed in 10 CPU clock cycles (5 bus cycles). After the operation has finished, the remainder is loaded to this register. However, if an overflow occurs in a division process, the remainder is not loaded and the high-order 8 bits of the dividend remains.
At initial reset, this register is undefined.

NF: Negative flag (FF86H•D3)

Indicates whether the operation result is a positive value or a negative value.

When "1" is read: Negative value (MSB of the results is "1")
When "0" is read: Positive value (MSB of the results is "0")
Writing: Invalid

NF is a read-only bit, so writing operation is invalid.
At initial reset, this flag is set to "0".

VF: Overflow flag (FF86H•D2)

Indicates whether an overflow has occurred or not in a division process.

When "1" is read: Overflow occurred
When "0" is read: Overflow has not occurred
Writing: Invalid

When a multiplication process has finished, this flag is always set to "0".
VF is a read-only bit, so writing operation is invalid.
At initial reset, this flag is set to "0".

ZF: Zero flag (FF86H•D1)

Indicates whether the operation result is zero or not.

When "1" is read: Zero
When "0" is read: Not zero
Writing: Invalid

ZF is a read-only bit, so writing operation is invalid.
At initial reset, this flag is set to "0".

CALMD: Calculation mode selection register/operation status (FF86H•D0)

Selects multiplication or division mode and starts operation.

When "1" is written: Selects/starts division
When "0" is written: Selects/starts multiplication
When "1" is read: Under operating
When "0" is read: Operation has finished

Writing to this register starts the specified operation. After that, this register is set to "1" and returns to "0" when the multiplication or division process has finished.
At initial reset, this register is reset to "0".

4.12.6 Programming note

An operation process takes 10 CPU clock cycles (5 bus cycles) after writing to the calculation mode selection register CALMD until the operation result is set to the destination register DRH/DRL and the operation flags. While this operation is in process, do not read/write from/to the destination register DRH/DRL and do not read NF/VF/ZF.

4.13 SVD (Supply Voltage Detection) Circuit

4.13.1 Configuration of SVD circuit

The S1C63808 has a built-in SVD (supply voltage detection) circuit, so that the software can find when the source voltage lowers. Turning the SVD circuit on/off and the SVD criteria voltage setting can be done with software. Figure 4.13.1.1 shows the configuration of the SVD circuit.

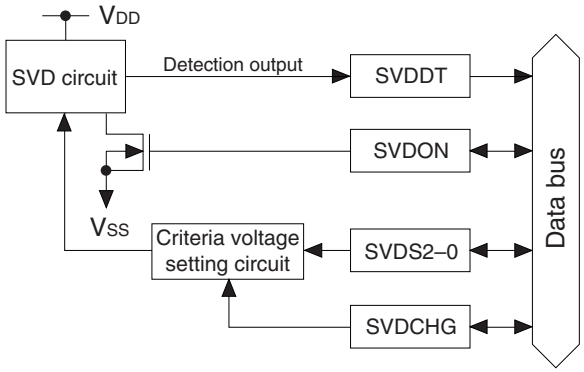


Fig. 4.13.1.1 Configuration of SVD circuit

4.13.2 SVD operation

The SVD circuit compares the criteria voltage set by software and the supply voltage (VDD terminal–VSS terminal) and sets its results into the SVDDT latch. By reading the data of this SVDDT latch, it can be determined by means of software whether the supply voltage is normal or has dropped.
The criteria voltage to be used can be selected from 8 levels using SVDS2–SVDS0. Furthermore, two types of 8-voltage combinations for 3.0 V and 1.5 V supply voltages are available and either one can be selected using SVDCHG. Set SVDCHG to "1" when 3.0 V (typ.) supply voltage is used or to "0" when 1.5 V (typ.) supply voltage is used.
Table 4.13.2.1 lists the criteria voltages.

Table 4.13.2.1 Criteria voltage

SVDS2	SVDS1	SVDS0	Criteria voltage (V)	
			1.5 V system (SVDCHG = "0")	3.0 V system (SVDCHG = "1")
1	1	1	1.50	2.90
1	1	0	1.40	2.70
1	0	1	1.30	2.40
1	0	0	1.25	2.10
0	1	1	1.20	2.00
0	1	0	1.15	1.90
0	0	1	1.10	1.80
0	0	0	1.05	1.70

When the SVDON register is set to "1", source voltage or external voltage detection by the SVD circuit is executed. As soon as the SVDON register is reset to "0", the result is loaded to the SVDDT latch and the SVD circuit goes off.
To obtain a stable detection result, the SVD circuit must be on for at least 1 msec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 1 msec minimum
3. Set SVDON to "0"
4. Read SVDDT

When the SVD circuit is on, the IC draws a large current, so keep the SVD circuit off unless it is.

4.13.3 I/O memory of SVD circuit

Table 4.13.3.1 shows the I/O addresses and the control bits for the SVD circuit.

Table 4.13.3.1 Control bits of SVD circuit

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF04H	SVDCHG	SVDS2	SVDS1	SVDS0	SVDCHG	0	3.0 V	1.5 V	SVD voltage system selection
					SVDS2	0			SVD criteria voltage setting
					SVDS1	0			[SVDS2–0] 0 1 2 3 4 5 6 7
	R/W								1.5 V (V) 1.05 1.10 1.15 1.20 1.25 1.30 1.40 1.50
					SVDS0	0			3.0 V (V) 1.70 1.80 1.90 2.00 2.10 2.40 2.70 2.90
FF05H	0	0	SVDDT	SVDON	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	SVDDT	0	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

SVDCHG: SVD voltage set selection register (FF04H•D3)

Selects an SVD criteria voltage combination according to the supply voltage.

When "1" is written: 3.0 V (typ.)
When "0" is written: 1.5 V (typ.)
Reading: Valid

When SVDCHG is set to "1", the 8-level criteria voltage set is configured for a 3.0 V supply voltage and when it is set to "0", voltages are configured for a 1.5 V supply voltage.
At initial reset, this register is set to "0".

SVDS2–SVDS0: SVD criteria voltage setting registers (FF04H•D2–D0)

Criteria voltage for SVD is set as shown in Table 4.13.2.1.
At initial reset, these registers are set to "0".

SVDON: SVD control (on/off) register (FF05H•D0)

Turns the SVD circuit on and off.

When "1" is written: SVD circuit ON
When "0" is written: SVD circuit OFF
Reading: Valid

When SVDON is set to "1", a source voltage detection is executed by the SVD circuit. As soon as SVDON is reset to "0", the result is loaded to the SVDDT latch. To obtain a stable detection result, the SVD circuit must be on for at least 1 msec.
At initial reset, this register is set to "0".

SVDDT: SVD data (FF05H•D1)

This is the result of supply voltage detection.

When "0" is read: Supply voltage (V_{DD}–V_{SS}) ≥ Criteria voltage
When "1" is read: Supply voltage (V_{DD}–V_{SS}) < Criteria voltage
Writing: Invalid

The result of supply voltage detection at time of SVDON is set to "0" can be read from this latch.
At initial reset, SVDDT is set to "0".

4.13.4 Programming notes

(1) To obtain a stable detection result, the SVD circuit must be on for at least 1 msec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 1 msec minimum
3. Set SVDON to "0"
4. Read SVDDT

(2) The SVD circuit should normally be turned off because SVD operation increase current consumption.

4.14 Power Supply for EPD Driver IC (V_{C1}–V_{C3})

4.14.1 Configuration of EPD system voltage circuit

The S1C63808 has a built-in power supply circuit that generates the voltages (V_{C1}–V_{C3}) for EPD driver ICs. Figure 4.14.1.1 shows the configuration of the EPD system voltage circuit.

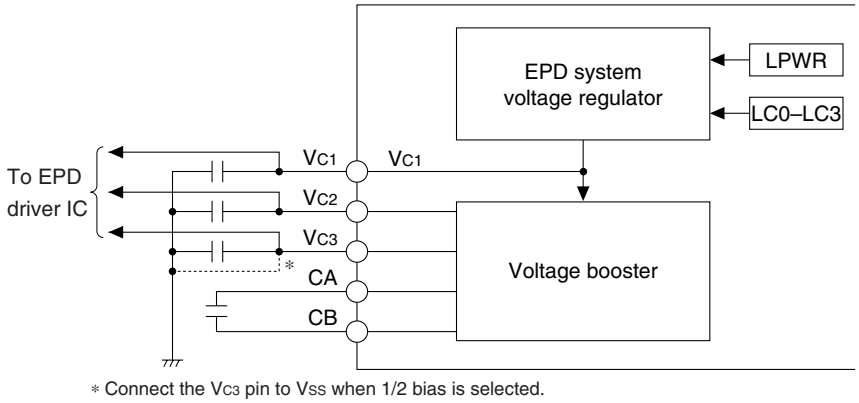


Fig. 4.14.1.1 Configuration of EPD system voltage circuit

The EPD system voltage circuit generates V_{C1} with the voltage regulator built-in, and generates two other voltages ($V_{C2} = 2V_{C1}$, $V_{C3} = 3V_{C1}$, $V_{C3} = V_{SS}$ when 1/2 bias is selected) by boosting V_{C1}.

Note: Do not drive external loads with the output voltage from the EPD system voltage circuit except for the exclusive EPD driver IC.

4.14.2 Mask option

Either 1/2 bias or 1/3 bias can be selected to configure the outputs from the EPD system voltage circuit.
When 1/3 bias is selected: V_{C1} = 1.03 to 1.23 V, $V_{C2} = 2 \times V_{C1}$, $V_{C3} = 3 \times V_{C1}$
When 1/2 bias is selected: V_{C1} = 1.08 to 1.84 V, $V_{C2} = 2 \times V_{C1}$, $V_{C3} = V_{SS}$

4.14.3 Turning EPD system voltage circuit on and off

The EPD system voltage circuit is turned on and off using the LPWR register. When LPWR is set to "1", the EPD system voltage circuit outputs the V_{C1}–V_{C3} voltages to the EPD driver IC. When LPWR is set to "0", the EPD system voltage circuit goes off and the V_{C1}–V_{C3} terminals go to V_{SS} level.

4.14.4 Adjustment of EPD driver voltages

The EPD driver voltages (V_{C1}–V_{C3}) can be adjusted in the software.
It is realized by controlling the voltages V_{C1} output from the EPD system voltage circuit.
The V_{C1} voltage for 1/3 bias can be adjusted to 8 levels as shown in Table 4.14.4.1 using the LC2–LC0 register. The V_{C1} voltage varies within the range from 1.03 to 1.23 V, and other voltages change according to V_{C1}.
The V_{C1} voltage for 1/2 bias can be adjusted to 16 levels as shown in Table 4.14.4.1 using the LC3–LC0 register. The V_{C1} voltage varies within the range from 1.08 to 1.84 V, and V_{C2} changes according to V_{C1}.

Table 4.14.4.1 V_{C1} voltage value

No.	LC3	LC2	LC1	LC0	V_{C1} (V)	
					1/2 bias	1/3 bias
0	0	0	0	0	1.08	1.03
1	0	0	0	1	1.14	1.06
2	0	0	1	0	1.20	1.09
3	0	0	1	1	1.27	1.12
4	0	1	0	0	1.33	1.15
5	0	1	0	1	1.39	1.18
6	0	1	1	0	1.43	1.20
7	0	1	1	1	1.49	1.23
8	1	0	0	0	1.55	–
9	1	0	0	1	1.59	–
10	1	0	1	0	1.63	–
11	1	0	1	1	1.67	–
12	1	1	0	0	1.72	–
13	1	1	0	1	1.76	–
14	1	1	1	0	1.80	–
15	1	1	1	1	1.84	–

When 1/2 bias is selected: $V_{C2} = 2 \times V_{C1}$, $V_{C3} = V_{SS}$
When 1/3 bias is selected: $V_{C2} = 2 \times V_{C1}$, $V_{C3} = 3 \times V_{C1}$, LC3 is ineffective.

At initial reset, the LC3(LC2)–LC0 register is set to 0000B. The software should initialize the register to get the desired contrast.

Note: To generate stable EPD driver voltages, the V_{DD} voltage to be supplied to the IC must be higher than the V_{C1} voltage that will be generated by setting the LC3–LC0 register to the maximum value (7 for 1/3 bias or 15 for 1/2 bias).

4.14.5 I/O memory of Power supply for EPD driver IC

Table 4.14.5.1 shows the I/O addresses and the control bits of the power supply for EPD driver ICs.

Table 4.14.5.1 Control bits of power supply for EPD driver ICs

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF60H	0	0	0	LPWR	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					LPWR	0	On	Off	EPD driver power supply On/Off
FF62H	0	LC2	LC1	LC0	0 *3	– *2			Unused 1/3 bias
					LC2	0			V_{C1} voltage adjustment
	R	R/W			LC1	0			[LC2–0] 0 – 7
					LC0	0			Voltage Low – High
	LC3	LC2	LC1	LC0	LC3	0			V_{C1} voltage adjustment 1/2 bias
					LC2	0			[LC3–0] 0 – 15
	R/W				LC1	0			Voltage Low – High
					LC0	0			

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

LPWR: EPD driver power control (on/off) register (FF60H•D0)

Turns the EPD system voltage circuit on and off.

When "1" is written: On
When "0" is written: Off
Reading: Valid

When "1" is written to the LPWR register, the EPD system voltage circuit goes on and generates the V_{C1}–V_{C3} voltages for EPD driver ICs. When "0" is written, all the EPD driver voltages go to V_{SS} level.
It takes about 100 msec for the EPD driver voltages to stabilize after starting up the EPD system voltage circuit by writing "1" to the LPWR register.
At initial reset, this register is set to "0".

LC3–LC0: V_{C1} voltage adjustment register (FF62H)

Adjusts the V_{C1} voltage as shown in Table 4.14.5.2. When 1/3 bias is selected, LC3 is ineffective.

Table 4.14.5.2 V_{C1} voltage value

No.	LC3	LC2	LC1	LC0	V_{C1} (V) 1/2 bias	V_{C1} (V) 1/3 bias
0	0	0	0	0	1.08	1.03
1	0	0	0	1	1.14	1.06
2	0	0	1	0	1.20	1.09
3	0	0	1	1	1.27	1.12
4	0	1	0	0	1.33	1.15
5	0	1	0	1	1.39	1.18
6	0	1	1	0	1.43	1.20
7	0	1	1	1	1.49	1.23
8	1	0	0	0	1.55	–
9	1	0	0	1	1.59	–
10	1	0	1	0	1.63	–
11	1	0	1	1	1.67	–
12	1	1	0	0	1.72	–
13	1	1	0	1	1.76	–
14	1	1	1	0	1.80	–
15	1	1	1	1	1.84	–

When 1/2 bias is selected: $V_{C2} = 2 \times V_{C1}$, $V_{C3} = V_{SS}$
When 1/3 bias is selected: $V_{C2} = 2 \times V_{C1}$, $V_{C3} = 3 \times V_{C1}$, LC3 is ineffective.

At initial reset, this register is set to 0000B.

4.14.6 Programming note

Because at initial reset, the LC3–LC0 register is set to 0000B (V_{C1} = 1.03 V when 1/3 bias is selected or 1.08 V when 1/2 bias is selected), it is necessary to initialize by the software. Furthermore, the EPD system voltage circuit is turned off and the V_{C1}–V_{C3} terminals go to V_{SS} level.

4.15 Interrupt and HALT

<Interrupt types>

The S1C63808 provides the following interrupt functions.

External interrupt:	• Input interrupt	(2 systems)
Internal interrupt:	• Watchdog timer interrupt	(NMI, 1 system)
	• Programmable timer interrupt	(2 systems)
	• Serial interface interrupt	(6 systems)
	• Clock timer interrupt	(4 systems)
	• Stopwatch timer interrupt	(4 systems)

To authorize interrupt, the interrupt flag must be set to "1" (EI) and the necessary related interrupt mask registers must be set to "1" (enable).
When an interrupt occurs the interrupt flag is automatically reset to "0" (DI), and interrupts after that are inhibited.

The watchdog timer interrupt is an NMI (non-maskable interrupt), therefore, the interrupt is generated regardless of the interrupt flag setting. Also the interrupt mask register is not provided. However, it is possible to not generate NMI since software can stop the watchdog timer operation.

Figure 4.15.1 shows the configuration of the interrupt circuit.

Note: After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine. Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

<HALT>

The S1C63808 has HALT functions that considerably reduce the current consumption when it is not necessary.
The CPU enters HALT status when the HALT instruction is executed.
In HALT status, the operation of the CPU is stopped. However, timers continue counting since the oscillation circuit operates. Reactivating the CPU from HALT status is done by generating a hardware interrupt request including NMI.

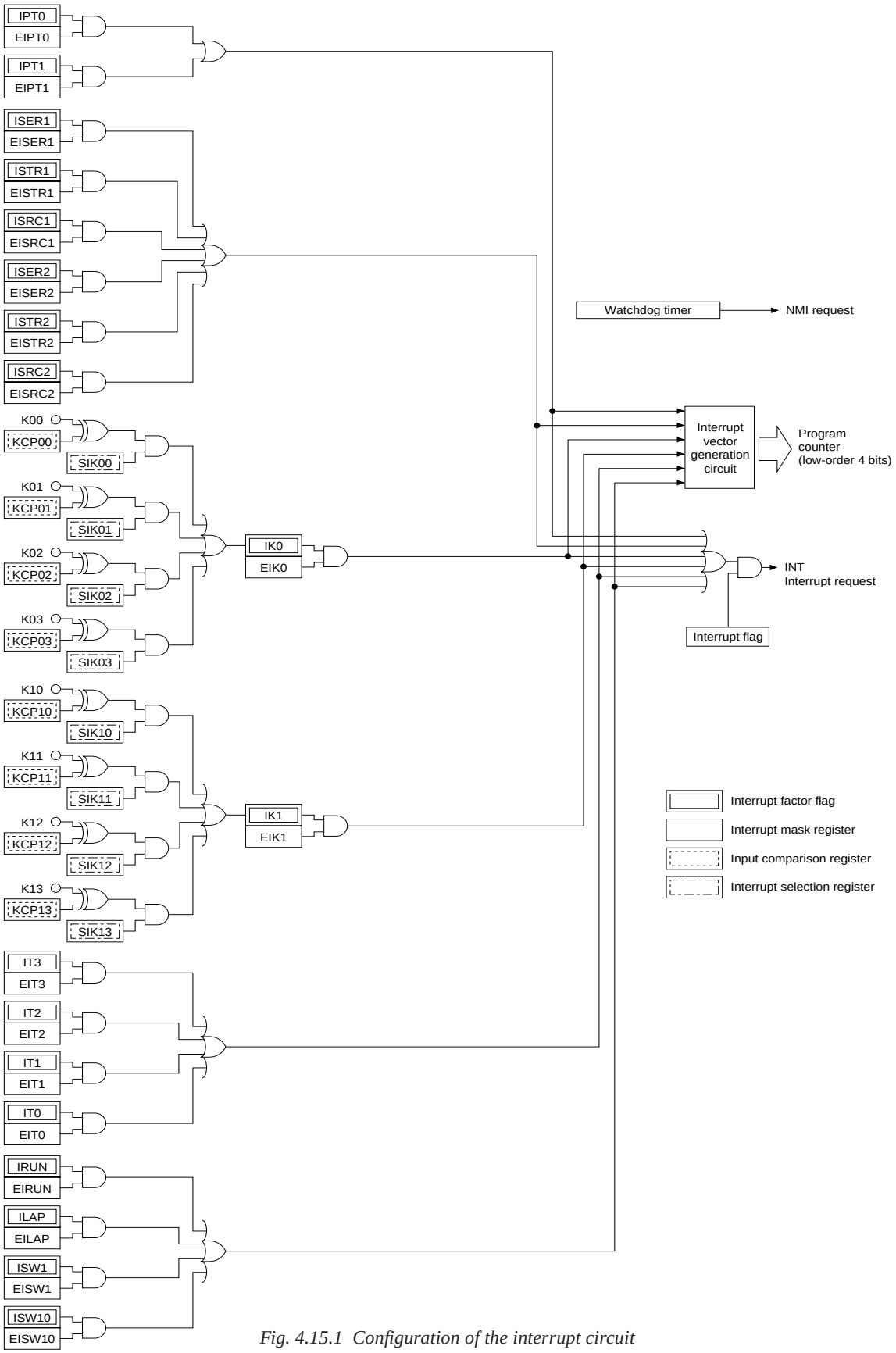


Fig. 4.15.1 Configuration of the interrupt circuit

4.15.1 Interrupt factor

Table 4.15.1.1 shows the factors for generating interrupt requests.

The interrupt flags are set to "1" depending on the corresponding interrupt factors.
The CPU operation is interrupted when an interrupt factor flag is set to "1" if the following conditions are established.

- The corresponding mask register is "1" (enabled)
- The interrupt flag is "1" (EI)

The interrupt factor flag is reset to "0" when "1" is written.
At initial reset, the interrupt factor flags are reset to "0".

* Since the watchdog timer's interrupt is NMI, the interrupt is generated regardless of the setting above, and no interrupt factor flag is provided.

Table 4.15.1.1 Interrupt factors

Interrupt factor	Interrupt factor flag	
Programmable timer 1 (counter = 0)	IPT1	(FFF2H•D1)
Programmable timer 0 (counter = 0)	IPT0	(FFF2H•D0)
Serial interface 1 (receive error)	ISER1	(FFF1H•D2)
Serial interface 1 (transmit completion)	ISTR1	(FFF1H•D1)
Serial interface 1 (receive completion)	ISRC1	(FFF1H•D0)
Serial interface 2 (receive error)	ISER2	(FFF0H•D2)
Serial interface 2 (transmit completion)	ISTR2	(FFF0H•D1)
Serial interface 2 (receive completion)	ISRC2	(FFF0H•D0)
K00–K03 input (falling edge or rising edge)	IK0	(FFF4H•D0)
K10–K13 input (falling edge or rising edge)	IK1	(FFF5H•D0)
Clock timer 1 Hz (falling edge)	IT3	(FFF6H•D3)
Clock timer 2 Hz (falling edge)	IT2	(FFF6H•D2)
Clock timer 8 Hz (falling edge)	IT1	(FFF6H•D1)
Clock timer 32 Hz (falling edge)	IT0	(FFF6H•D0)
Stopwatch timer (Direct RUN)	IRUN	(FFF8H•D3)
Stopwatch timer (Direct LAP)	ILAP	(FFF8H•D2)
Stopwatch timer (1 Hz)	ISW1	(FFF8H•D1)
Stopwatch timer (10 Hz)	ISW10	(FFF8H•D0)

Note: After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.15.2 Interrupt mask

The interrupt factor flags can be masked by the corresponding interrupt mask registers.
The interrupt mask registers are read/write registers. They are enabled (interrupt authorized) when "1" is written to them, and masked (interrupt inhibited) when "0" is written to them.
At initial reset, the interrupt mask register is reset to "0".
Table 4.15.2.1 shows the correspondence between interrupt mask registers and interrupt factor flags.

Table 4.15.2.1 Interrupt mask registers and interrupt factor flags

Interrupt mask register		Interrupt factor flag	
EIPT1	(FFE2H•D1)	IPT1	(FFF2H•D1)
EIPT0	(FFE2H•D0)	IPT0	(FFF2H•D0)
EISER1	(FFE1H•D2)	ISER1	(FFF1H•D2)
EISTR1	(FFE1H•D1)	ISTR1	(FFF1H•D1)
EISRC1	(FFE1H•D0)	ISRC1	(FFF1H•D0)
EISER2	(FFE0H•D2)	ISER2	(FFF0H•D2)
EISTR2	(FFE0H•D1)	ISTR2	(FFF0H•D1)
EISRC2	(FFE0H•D0)	ISRC2	(FFF0H•D0)
EIK0	(FFE4H•D0)	IK0	(FFF4H•D0)
EIK1	(FFE5H•D0)	IK1	(FFF5H•D0)
EIT3	(FFE6H•D3)	IT3	(FFF6H•D3)
EIT2	(FFE6H•D2)	IT2	(FFF6H•D2)
EIT1	(FFE6H•D1)	IT1	(FFF6H•D1)
EIT0	(FFE6H•D0)	IT0	(FFF6H•D0)
EIRUN	(FFE8H•D3)	IRUN	(FFF8H•D3)
EILAP	(FFE8H•D2)	ILAP	(FFF8H•D2)
EISW1	(FFE8H•D1)	ISW1	(FFF8H•D1)
EISW10	(FFE8H•D0)	ISW10	(FFF8H•D0)

4.15.3 Interrupt vector

When an interrupt request is input to the CPU, the CPU begins interrupt processing. After the program being executed is terminated, the interrupt processing is executed in the following order.

1 The content of the flag register is evacuated, then the I flag is reset.

2 The address data (value of program counter) of the program to be executed next is saved in the stack area (RAM).

3 The interrupt request causes the value of the interrupt vector (0100H–010CH) to be set in the program counter.

4 The program at the specified address is executed (execution of interrupt processing routine by software).

Table 4.15.3.1 shows the correspondence of interrupt requests and interrupt vectors.

Table 4.15.3.1 Interrupt request and interrupt vectors

Interrupt vector	Interrupt factor	Priority
0100H	Watchdog timer	High
0102H	–	↑
0104H	Programmable timer	
0106H	Serial interface	
0108H	K00–K03, K10–K13 input	
010AH	Clock timer	
010CH	Stopwatch timer	↓
010EH	–	Low

The four low-order bits of the program counter are indirectly addressed through the interrupt request.

4.15.4 I/O memory of interrupt

Tables 4.15.4.1 shows the I/O addresses and the control bits for controlling interrupts.

Table 4.15.4.1(a) Control bits of interrupt

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF20H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
					SIK00	0	Enable	Disable	
FF22H	KCP03	KCP02	KCP01	KCP00	KCP03	0	↓	↑	K00–K03 input comparison register
					KCP02	0	↓	↑	
	R/W				KCP01	0	↓	↑	
					KCP00	0	↓	↑	
FF24H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
					SIK12	0	Enable	Disable	
	R/W				SIK11	0	Enable	Disable	
					SIK10	0	Enable	Disable	
FF26H	KCP13	KCP12	KCP11	KCP10	KCP13	0	↓	↑	K10–K13 input comparison register
					KCP12	0	↓	↑	
	R/W				KCP11	0	↓	↑	
					KCP10	0	↓	↑	
FFE0H	0	EISER2	EISTR2	EISRC2	0 *3	– *2			Unused
					EISER2	0	Enable	Mask	Interrupt mask register (Serial I/F 2 error)
	R	R/W			EISTR2	0	Enable	Mask	Interrupt mask register (Serial I/F 2 transmit completion)
					EISRC2	0	Enable	Mask	Interrupt mask register (Serial I/F 2 receive completion)
FFE1H	0	EISER1	EISTR1	EISRC1	0 *3	– *2			Unused
					EISER1	0	Enable	Mask	Interrupt mask register (Serial I/F 1 error)
	R	R/W			EISTR1	0	Enable	Mask	Interrupt mask register (Serial I/F 1 transmit completion)
					EISRC1	0	Enable	Mask	Interrupt mask register (Serial I/F 1 receive completion)
FFE2H	0	0	EIPT1	EIPT0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1)
					EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0)
FFE4H	0	0	0	EIK0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
FFE5H	0	0	0	EIK1	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
FFE6H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
FFE8H	EIRUN	EILAP	EISW1	EISW10	EIRUN	0	Enable	Mask	Interrupt mask register (Stopwatch direct RUN)
					EILAP	0	Enable	Mask	Interrupt mask register (Stopwatch direct LAP)
	R/W				EISW1	0	Enable	Mask	Interrupt mask register (Stopwatch timer 1 Hz)
					EISW10	0	Enable	Mask	Interrupt mask register (Stopwatch timer 10 Hz)
FFF0H	0	ISER2	ISTR2	ISRC2	0 *3	– *2	(R)	(R)	Unused
					ISER2	0	Yes	No	Interrupt factor flag (Serial I/F 2 error)
	R	R/W			ISTR2	0	(W)	(W)	Interrupt factor flag (Serial I/F 2 transmit completion)
					ISRC2	0	Reset	Invalid	Interrupt factor flag (Serial I/F 2 receive completion)
FFF1H	0	ISER1	ISTR1	ISRC1	0 *3	– *2	(R)	(R)	Unused
					ISER1	0	Yes	No	Interrupt factor flag (Serial I/F 1 error)
	R	R/W			ISTR1	0	(W)	(W)	Interrupt factor flag (Serial I/F 1 transmit completion)
					ISRC1	0	Reset	Invalid	Interrupt factor flag (Serial I/F 1 receive completion)
FFF2H	0	0	IPT1	IPT0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1)
					IPT0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0)

*1 Initial value at initial reset *2 Not set in the circuit *3 Constantly "0" when being read

Table 4.15.4.1(b) Control bits of interrupt

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FFF4H	0	0	0	IK0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK0	0	Reset	Invalid	Interrupt factor flag (K00–K03)
FFF5H	0	0	0	IK1	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK1	0	Reset	Invalid	Interrupt factor flag (K10–K13)
FFF6H	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
					IT2	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R/W				IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 8 Hz)
					IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 32 Hz)
FFF8H	IRUN	ILAP	ISW1	ISW10	IRUN	0	(R)	(R)	Interrupt factor flag (Stopwatch direct RUN)
					ILAP	0	Yes	No	Interrupt factor flag (Stopwatch direct LAP)
	R/W				ISW1	0	(W)	(W)	Interrupt factor flag (Stopwatch timer 1 Hz)
					ISW10	0	Reset	Invalid	Interrupt factor flag (Stopwatch timer 10 Hz)

*1 Initial value at initial reset *2 Not set in the circuit *3 Constantly "0" when being read

EIPT1, EIPT0: Interrupt mask registers (FFE2H•D2, D1, D0)
IPT1, IPT0: Interrupt factor flags (FFF2H•D2, D1, D0)
Refer to Section 4.9, "Programmable Timer".

EISER1, EISTR1, EISRC1: Interrupt mask registers (FFE1H•D2, D1, D0)
EISER2, EISTR2, EISRC2: Interrupt mask registers (FFE0H•D2, D1, D0)
ISER1, ISTR1, ISRC1: Interrupt factor flags (FFF1H•D2, D1, D0)
ISER2, ISTR2, ISRC2: Interrupt factor flags (FFF0H•D2, D1, D0)
Refer to Section 4.10, "Serial Interface".

KCP03–KCP00, KCP13–KCP10: Input comparison registers (FF22H, FF26H)
SIK03–SIK00, SIK13–SIK10: Interrupt selection registers (FF20H, FF24H)
EIK0, EIK1: Interrupt mask registers (FFE4H•D0, FFE5H•D0)
IK0, IK1: Interrupt factor flags (FFF4H•D0, FFF5H•D0)
Refer to Section 4.4, "Input Ports".

EIT3–EIT0: Interrupt mask registers (FFE6H)
IT3–IT0: Interrupt factor flags (FFF6H)
Refer to Section 4.7, "Clock Timer".

EIRUN, EILAP, EISW1, EISW10: Interrupt mask registers (FFE8H)
IRUN, ILAP, ISW1, ISW10: Interrupt factor flags (FFF8H)
Refer to Section 4.8, "Stopwatch Timer".

4.15.5 Programming notes

(1) The interrupt factor flags are set when the interrupt condition is established, even if the interrupt mask registers are set to "0".

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(3) After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine. Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

CHAPTER 5 SUMMARY OF NOTES

5.1 Notes for Low Current Consumption

The S1C63808 contains control registers for each of the circuits so that current consumption can be reduced.
These control registers reduce the current consumption through programs that operate the circuits at the minimum levels.
The following lists the circuits that can control operation and their control registers. Refer to these when programming.

Table 5.1.1 Circuits and control registers

Circuit (and item)	Control register
CPU	HALT instruction
CPU operating frequency	CLKCHG, OSCC
SVD circuit	SVDON
EPD system voltage circuit	LPWR

Refer to Chapter 7, "Electrical Characteristics" for current consumption.

Below are the circuit statuses at initial reset.

CPU: Operating status

CPU operating frequency: Low speed side (CLKCHG = "0")
OSC3 oscillation circuit is in off status (OSCC = "0")

SVD circuit: Off status (SVDON = "0")

EPD system voltage circuit: Off status (LPWR = "0")

5.2 Summary of Notes by Function

Here, the cautionary notes are summed up by function category. Keep these notes well in mind when programming.

Memory and stack

(1) Memory is not implemented in unused areas within the memory map. Further, some non-implementation areas and unused (access prohibition) areas exist in the peripheral I/O area. If the program that accesses these areas is generated, its operation cannot be guaranteed. Refer to the I/O memory maps shown in Table 4.1.1 for the peripheral I/O area.

(2) Part of the RAM area is used as a stack area for subroutine call and register evacuation, so pay attention not to overlap the data area and stack area.

(3) The S1C63000 core CPU handles the stack using the stack pointer for 4-bit data (SP2) and the stack pointer for 16-bit data (SP1).
16-bit data are accessed in stack handling by SP1, therefore, this stack area should be allocated to the area where 4-bit/16-bit access is possible (0100H to 01FFH). The stack pointers SP1 and SP2 change cyclically within their respective range: the range of SP1 is 0000H to 03FFH and the range of SP2 is 0000H to 00FFH. Therefore, pay attention to the SP1 value because it may be set to 0200H or more exceeding the 4-bit/16-bit accessible range in the S1C63808 or it may be set to 00FFH or less. Memory accesses except for stack operations by SP1 are 4-bit data access. After initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set by software. Further, if either SP1 or SP2 is re-set when both are set already, the interrupts including NMI are masked again until the other is re-set. Therefore, the settings of SP1 and SP2 must be done as a pair.

Watchdog timer

(1) When the watchdog timer is being used, the software must reset it within 3-second cycles.

(2) Because the watchdog timer is set in operation state by initial reset, set the watchdog timer to disabled state (not used) before generating an interrupt (NMI) if it is not used.

Oscillation circuit

(1) It takes at least 5 msec from the time the OSC3 oscillation circuit goes on until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went on.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(2) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation off. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

Input port

When input ports are changed from high to low by pull-down resistors, the fall of the waveform is delayed on account of the time constant of the pull-down resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate waiting time. Particular care needs to be taken of the key scan during key matrix configuration. Make this waiting time the amount of time or more calculated by the following expression.

$10 \times C \times R$ C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-down resistance 375 kΩ (Max.)

Output port

(1) When using the output port (R01, R02, R03) as the special output port (BZ, TOUT, FOUT), fix the data register (R01, R02, R03) at "1" and the high impedance control register (R01HIZ, R02HIZ, R03HIZ) at "0" (data output).
Be aware that the output terminal is fixed at a low (V_{SS}) level the same as the DC output if "0" is written to the R01, R02 and R03 registers when the special output has been selected.
Be aware that the output terminal shifts into high impedance status when "1" is written to the high impedance control register (R01HIZ, R02HIZ, R03HIZ).

(2) A hazard may occur when the BZ signal, FOUT signal and the TOUT signal are turned on and off.

(3) When f_{OSC3} is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit before output.
Refer to Section 4.3, "Oscillation Circuit", for the control and notes.

I/O port

When in the input mode, I/O ports are changed from high to low by pull-down resistor, the fall of the waveform is delayed on account of the time constant of the pull-down resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.

$10 \times C \times R$ C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-down resistance 375 kΩ (Max.)

Clock timer

Be sure to read timer data in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

Stopwatch timer

(1) The interrupt factor flag should be reset after resetting the stopwatch timer.

(2) Be sure to data reading in the order of SWD0–3 → SWD4–7 → SWD8–11.

(3) When data that is held by a LAP input is read, read the capture buffer renewal flag CRNWF after reading the SWD8–11 and check whether the data has been renewed or not.

(4) When performing a processing such as a LAP input preceding with 1 Hz interrupt processing, read the LAP data carry-up request flag LCURF before processing and check whether carry-up is needed or not.

Programmable timer

(1) When reading counter data, be sure to read the low-order 4 bits (PTDx0–PTDx3) first. Furthermore, the high-order 4 bits (PTDx4–PTDx7) should be read within 0.73 msec (when f_{OSC1} is 32.768 kHz) of reading the low-order 4 bits (PTDx0–PTDx3).
The counter data in 16-bit mode must be read in the order below.
PTD00–PTD03 → PTD04–PDT07 → PTD10–PTD13 → PTD14–PTD17

(2) The programmable timer actually enters RUN/STOP status in synchronization with the falling edge of the input clock after writing to the PTRUNx register. Consequently, when "0" is written to the PTRUNx register, the timer enters STOP status at the point where the counter is decremented (-1).
The PTRUNx register maintains "1" for reading until the timer actually stops.
Figure 5.2.1 shows the timing chart for the RUN/STOP control.

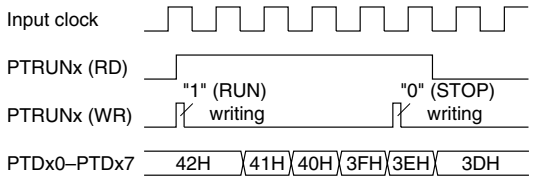


Fig. 5.2.1 Timing chart for RUN/STOP control

It is the same even in the event counter mode. Therefore, be aware that the counter does not enter RUN/STOP status if a clock is not input after setting the RUN/STOP control register (PTRUN0).

(3) Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned on and off by setting the register.

(4) When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time at least 5 msec from turning the circuit ON until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit ON to starting the programmable timer. Refer to Section 4.3, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit. At initial reset, the OSC3 oscillation circuit is set in the off state.

(5) For the reason below, pay attention to the reload data write timing when changing the interval of the programmable timer interrupts while the programmable timer is running.
The programmable timer counts down at the falling edge of the input clock and at the same time it generates an interrupt if the counter underflows. Then it starts loading the reload data to the counter and the counter data is determined at the next rising edge of the input clock (period shown in as ¿ in the figure).

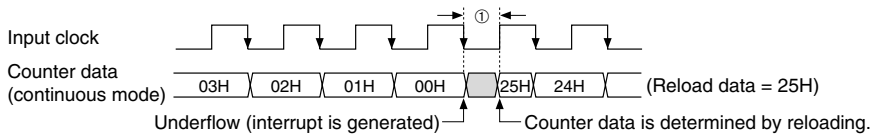


Fig. 5.2.2 Reload timing for programmable timer

To avoid improper reloading, do not rewrite the reload data after an interrupt occurs until the counter data is determined including the reloading period ¿. Be especially careful when using the OSC1 (low-speed clock) as the clock source of the programmable timer and the CPU is operating with the OSC3 (high-speed clock).

Serial interface

(1) Be sure to initialize the serial interface mode in the transmit/receive disabled status (TXENx = RXENx = "0").

(2) Do not perform double trigger (writing "1") to TXTRGx (RXTRGx) when the serial interface is in the transmitting (receiving) operation.

(3) In the clock synchronous mode, since one clock line (SCLKx) is shared for both transmitting and receiving, transmitting and receiving cannot be performed simultaneously. (Half duplex only is possible in clock synchronous mode.)
Consequently, be sure not to write "1" to RXTRGx (TXTRGx) when TXTRGx (RXTRGx) is "1".

(4) When a parity error or framing error is generated during receiving in the asynchronous mode, the receiving error interrupt factor flag ISERx is set to "1" prior to the receive completion interrupt factor flag ISRCx for the time indicated in Table 5.2.1. Consequently, when an error is generated, you should reset the receiving complete interrupt factor flag ISRCx to "0" by providing a wait time in error processing routines and similar routines.
When an overrun error is generated, the receiving complete interrupt factor flag ISRCx is not set to "1" and a receiving complete interrupt is not generated.

Table 5.2.1 Time difference between ISERx and ISRCx on error generation

Clock source	Time difference
f_{OSC3} / n	1/2 cycles of f_{OSC3} / n
Programmable timer	1 cycle of timer 1 underflow

(5) When the demultiplied signal of the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the serial interface.
A time interval of 5 msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before starting transmitting/receiving of serial interface. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 7, "Electrical Characteristics".)
At initial reset, the OSC3 oscillation circuit is set to OFF status.

(6) Be aware that the maximum clock frequency for the serial interface is limited to 2 MHz.

Sound generator

(1) When using the R01 port as the BZ output port, fix the data register R01 at "1" and the high impedance control register R01HIZ at "0" (data output).

(2) Since it generates a buzzer signal that is out of synchronization with the BZE register, hazards may at times be produced when the signal goes on/off due to the setting of the BZE register.

(3) The one-shot output is only valid when the normal buzzer output is off (BZE = "0") and will be invalid when the normal buzzer output is on (BZE = "1").

Integer multiplier

An operation process takes 10 CPU clock cycles (5 bus cycles) after writing to the calculation mode selection register CALMD until the operation result is set to the destination register DRH/DRL and the operation flags. While this operation process, do not read/write from/to the destination register DRH/DRL and do not read NF/VF/ZF.

SVD circuit

(1) To obtain a stable detection result, the SVD circuit must be on for at least 1 msec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 1 msec minimum
3. Set SVDON to "0"
4. Read SVDDT

(2) The SVD circuit should normally be turned off because SVD operation increase current consumption.

Power supply for EPD driver IC

Because at initial reset, the LC3–LC0 register is set to 0000B (V_{C1} = 1.03 V when 1/3 bias is selected or 1.08 V when 1/2 bias is selected), it is necessary to initialize by the software. Furthermore, the EPD system voltage circuit is turned off and the V_{C1}–V_{C3} terminals go to V_{SS} level.

Interrupt

(1) The interrupt factor flags are set when the interrupt condition is established, even if the interrupt mask registers are set to "0".

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(3) After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine. Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

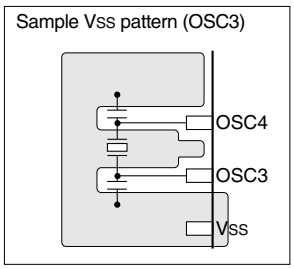
5.3 Precautions on Mounting

<Oscillation Circuit>

- Oscillation characteristics change depending on conditions (board pattern, components used, etc.). In particular, when a ceramic oscillator or crystal oscillator is used, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance.
- Disturbances of the oscillation clock due to noise may cause a malfunction. Consider the following points to prevent this:

  (1) Components which are connected to the OSC1, OSC2, OSC3 and OSC4 terminals, such as oscillators, resistors and capacitors, should be connected in the shortest line.

  (2) As shown in the right hand figure, make a VSS pattern as large as possible at circumscription of the OSC1, OSC2, OSC3 and OSC4 terminals and the components connected to these terminals. Furthermore, do not use this VSS pattern for any purpose other than the oscillation system.



- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC1/OSC3 and VDD, please keep enough distance between OSC1/OSC3 and VDD or other signals on the board pattern.

<Reset Circuit>

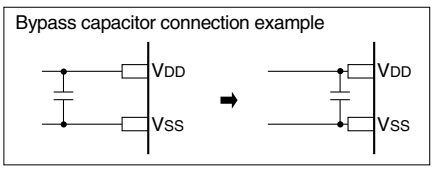
- The power-on reset signal which is input to the RESET terminal changes depending on conditions (power rise time, components used, board pattern, etc.).
  Decide the time constant of the capacitor and resistor after enough tests have been completed with the application product. When using the built-in pull-down resistor of the RESET terminal, take into consideration dispersion of the resistance for setting the constant.
- In order to prevent any occurrences of unnecessary resetting caused by noise during operating, components such as capacitors and resistors should be connected to the RESET terminal in the shortest line.

<Power Supply Circuit>

- Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:

  (1) The power supply should be connected to the VDD and VSS terminals with patterns as short and large as possible.

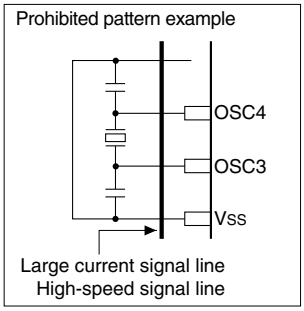
  (2) When connecting between the VDD and VSS terminals with a bypass capacitor, the terminals should be connected as short as possible.



  (3) Components which are connected to the VD1 and VOSC terminals, such as capacitors, should be connected in the shortest line.

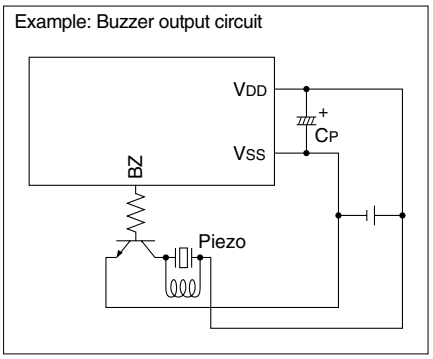
<Arrangement of Signal Lines>

- In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation unit.
- When a signal line is parallel with a high-speed line in long distance or intersects a high-speed line, noise may generated by mutual interference between the signals and it may cause a malfunction. Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation unit.



<Output Terminals>

- When an output terminal is used to drive an external component that consumes a large amount of current, the operation of the external component affects the built-in power supply circuit of this IC and the output voltage may vary. When driving a bipolar transistor by a periodic signal such as the BZ or timer output in particular, it may cause variations in the voltage output from the EPD system voltage circuit that affects the EPD contrast. To prevent this, separate the traces on the printed circuit board. Put one between the power supply and the IC's VDD and VSS terminals, and another between the power supply and the external component that consumes the large amount of current. Furthermore, use an external component with as low a current consumption as possible.



<Precautions for Visible Radiation (when bare chip is mounted)>

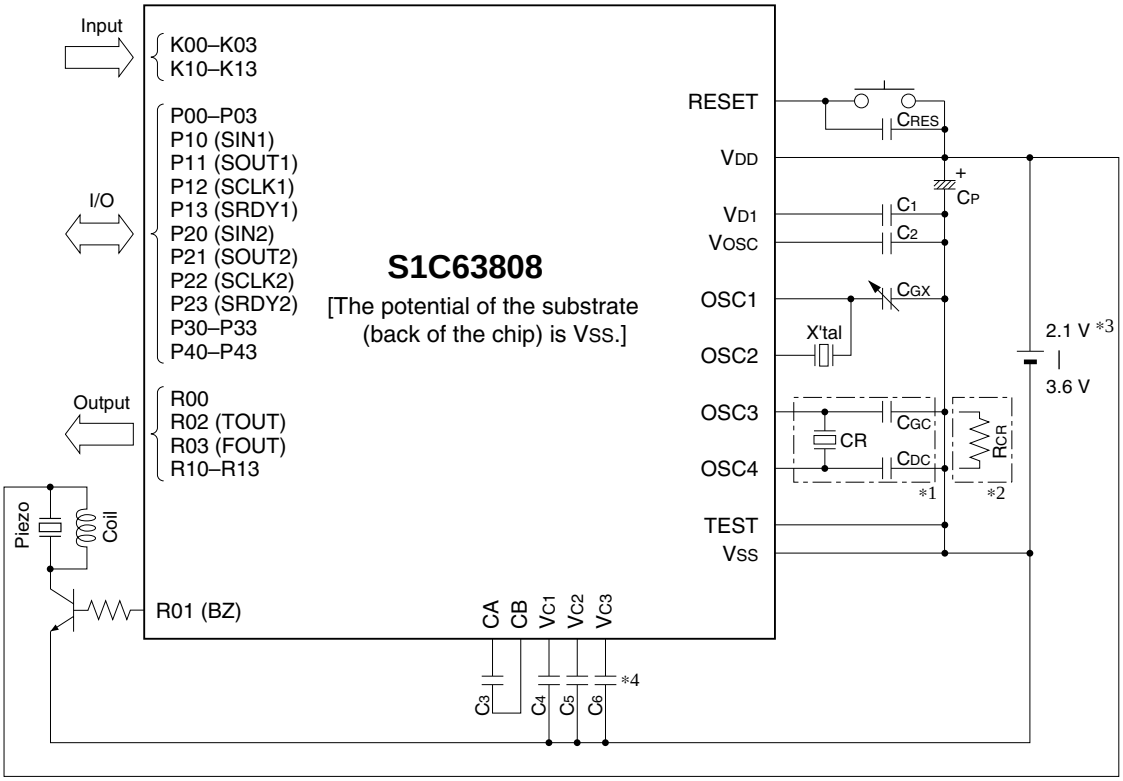
- Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.

  (1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.

  (2) The inspection process of the product needs an environment that shields the IC from visible radiation.

  (3) As well as the face of the IC, shield the back and side too.

CHAPTER 6 BASIC EXTERNAL WIRING DIAGRAM



X'tal	Crystal oscillator	32.768 kHz, CI(Max.) = 34 kΩ
CGX	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	4 MHz (3.0 V)
CGC	Gate capacitor	30 pF
CDC	Drain capacitor	30 pF
RCR	Resistor for OSC3 CR oscillation	30 kΩ (2 MHz)
C1–C6	Capacitor	0.2 µF
CP	Capacitor	3.3 µF
CRES	RESET terminal capacitor	0.1 µF

Note: The above table is simply an example, and is not guaranteed to work.

∗1: Ceramic oscillation
∗2: CR oscillation (external R)
∗3: 1.0–3.6 V when OSC3 (ceramic or CR with external R) is not used
∗4: C6 is required when1/3 bias is selected. Connect VC3 to VSS when 1/2 bias is selected.

CHAPTER 7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Rating

(V_{SS}=0V)

Item	Symbol	Rated value	Unit
Supply voltage	V_{DD}	-0.5 to 4.5	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{D1} + 0.3	V
Permissible total output current *1	ΣI_{VDD}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

*1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pin (or is drawn in).

*2 In case of plastic package (QFP13-64pin).

7.2 Recommended Operating Conditions

(Ta=-20 to 70°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	V_{SS}=0V	when OSC3 is not used	1.0		3.6	V
			when OSC3 is used, 260kHz (Max.)	1.0		3.6	V
			when OSC3 is used, 4.2MHz (Max.)	2.1		3.6	V
Oscillation frequency	f_{OSC1}	Crystal oscillation		–	32.768	–	kHz
	f_{OSC3}	CR oscillation (built-in R), V_{DD}=1.0 to 3.6V		140	200	260	kHz
		CR oscillation (external R), V_{DD}=2.1 to 3.6V		200		2,200	kHz
		Ceramic oscillation, V_{DD}=2.1 to 3.6V				4,200	kHz

7.3 DC Characteristics

Unless otherwise specified:

V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}–V_{C3} are internal voltage, C_1–C_6=0.2µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		Kxx, Pxx	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		RESET, TEST	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		Kxx, Pxx	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		RESET, TEST	0		0.1·V_{DD}	V
High level input current (1)	I_{IH1}	V_{IH1}=3.0V No pull down	Kxx, Pxx RESET, TEST	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=3.0V With pull down	Kxx, Pxx RESET, TEST	8	12	20	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No pull down	Kxx, Pxx RESET, TEST	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With pull down	Kxx, Pxx RESET, TEST	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9·V_{DD}	Pxx, Rxx			-0.5	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1·V_{DD}	Pxx, Rxx	0.5			mA

7.4 Analog Circuit Characteristics and Power Current Consumption

Unless otherwise specified:
V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}–V_{C3} are internal voltage, C_1–C_6=0.2µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Voltages for EPD driver IC (1/3 bias)	V_{C1}	Connect 1 MΩ load resistor between V_{SS} and V_{C1}	LC0–2="0"		1.03		V
			LC0–2="1"		1.06		
			LC0–2="2"		1.09		
			LC0–2="3"	Typ.	1.12	Typ.	
			LC0–2="4"	-100mV	1.15	+100mV	
			LC0–2="5"		1.18		
			LC0–2="6"		1.20		
			LC0–2="7"		1.23		
	V_{C2}	Connect 1 MΩ load resistor between V_{SS} and V_{C2}		$2 \cdot V_{C1}$ ×0.9		$2 \cdot V_{C1}$	V
	V_{C3}	Connect 1 MΩ load resistor between V_{SS} and V_{C3}		$3 \cdot V_{C1}$ ×0.9		$3 \cdot V_{C1}$	V
Voltages for EPD driver IC (1/2 bias)	V_{C1}	Connect 1 MΩ load resistor between V_{SS} and V_{C1}	LC0–3="0"		1.08		V
			LC0–3="1"		1.14		
			LC0–3="2"		1.20		
			LC0–3="3"		1.27		
			LC0–3="4"		1.33		
			LC0–3="5"		1.39		
			LC0–3="6"		1.43		
			LC0–3="7"	Typ.	1.49	Typ.	
			LC0–3="8"	-150mV	1.55	+100mV	
			LC0–3="9"		1.59		
			LC0–3="10"		1.63		
			LC0–3="11"		1.67		
			LC0–3="12"		1.72		
			LC0–3="13"		1.76		
			LC0–3="14"		1.80		
			LC0–3="15"		1.84		
	V_{C2}	Connect 1 MΩ load resistor between V_{SS} and V_{C2}		$2 \cdot V_{C1}$ ×0.9		$2 \cdot V_{C1}$	V
	V_{C3}	Always V_{SS} level			V_{SS}		V
1.5 V system SVD voltage	V_{SVD1}	SVDS0–2="0"		1.00	1.05		V
		SVDS0–2="1"			1.10		
		SVDS0–2="2"			1.15		
		SVDS0–2="3"		Typ.	1.20	Typ.	
		SVDS0–2="4"		-100mV	1.25	+100mV	
		SVDS0–2="5"			1.30		
		SVDS0–2="6"			1.40		
		SVDS0–2="7"			1.50		
3.0 V system SVD voltage	V_{SVD2}	SVDS0–2="0"			1.70		V
		SVDS0–2="1"			1.80		
		SVDS0–2="2"			1.90		
		SVDS0–2="3"		Typ.	2.00	Typ.	
		SVDS0–2="4"		-100mV	2.10	+100mV	
		SVDS0–2="5"			2.40		
		SVDS0–2="6"			2.70		
		SVDS0–2="7"			2.90		
SVD circuit response time	t_{SVD}					1	ms

Unless otherwise specified:
V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}–V_{C3} are internal voltage, C_1–C_6=0.2µF

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption in HALT mode	I_{HALT}	32kHz crystal, EPD driver IC power supply OFF *1, *2		0.23	0.45	µA
		32kHz crystal, EPD driver IC power supply ON (1/3 bias) *1, *2		0.90	1.60	µA
		32kHz crystal, EPD driver IC power supply ON (1/2 bias) *1, *2		0.85	1.50	µA
		32kHz crystal, EPD driver IC power supply OFF *1, *3		0.60	1.10	µA
		32kHz crystal, EPD driver IC power supply ON (1/3 bias) *1, *3		1.10	2.00	µA
		32kHz crystal, EPD driver IC power supply ON (1/2 bias) *1, *3		1.00	1.90	µA
Current consumption in Run state	I_{EXE}	32kHz crystal, EPD driver IC power supply OFF *1, *2		1.90	2.20	µA
		32kHz crystal, EPD driver IC power supply ON *1, *2, *4		2.65	3.20	µA
		32kHz crystal, EPD driver IC power supply OFF *1, *3		4.80	5.80	µA
		32kHz crystal, EPD driver IC power supply ON *1, *3, *4		5.80	7.10	µA
		200kHz CR, EPD driver IC power supply ON *1, *2		25	40	µA
		1.1MHz CR, EPD driver IC power supply ON *1, *3		550	700	µA
		2MHz ceramic, EPD driver IC power supply ON *1, *3		600	850	µA
		4MHz ceramic, EPD driver IC power supply ON *1, *3		850	1100	µA
SVD circuit current	I_{SVD}	During voltage detection, V_{DD}=1.0 to 3.6V		2.0	3.0	µA

*1 No load on the power supply for the EPD driver IC and when the SVD circuit is in OFF status
*2 When CR (built-in R type) is selected for the OSC3 oscillation circuit by mask option
*3 When CR (external R type) is selected for the OSC3 oscillation circuit by mask option
*4 When 1/3 bias is selected by mask option

7.5 Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation circuit

Unless otherwise specified:

V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, C_D=built-in, Ta=-20 to 70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤3sec (V_{DD})	1.0			V
Oscillation stop voltage	Vstp	tstp≤10sec (V_{DD})	1.0			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the IC (in chip)		11		pF
Frequency/voltage deviation	∂f/∂V	V_{DD}=1.0 to 3.6V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	10	20		ppm
Harmonic oscillation start voltage	V_{hho}	C_G=5pF (V_{DD})	3.6			V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{SS}	200			MΩ

OSC3 ceramic oscillation circuit

Unless otherwise specified:

V_{DD}=3.0V, V_{SS}=0V, Ceramic oscillator: 4MHz, C_{GC}=C_{DC}=30pF, Ta=-20 to 70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	(V_{DD})	2.1			V
Oscillation start time	tsta	V_{DD}=2.1 to 3.6V			5	ms
Oscillation stop voltage	Vstp	(V_{DD})	2.1			V

OSC3 CR oscillation circuit (built-in R type)

Unless otherwise specified:

V_{DD}=3.0V, V_{SS}=0V, R_{CR}=built-in, Ta=-20 to 70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	200kHz	30	%
Oscillation start voltage	Vsta	(V_{DD})	1.0			V
Oscillation start time	tsta	V_{DD}=1.0 to 3.6V			3	ms
Oscillation stop voltage	Vstp	(V_{DD})	1.0			V

OSC3 CR oscillation circuit (external R type)

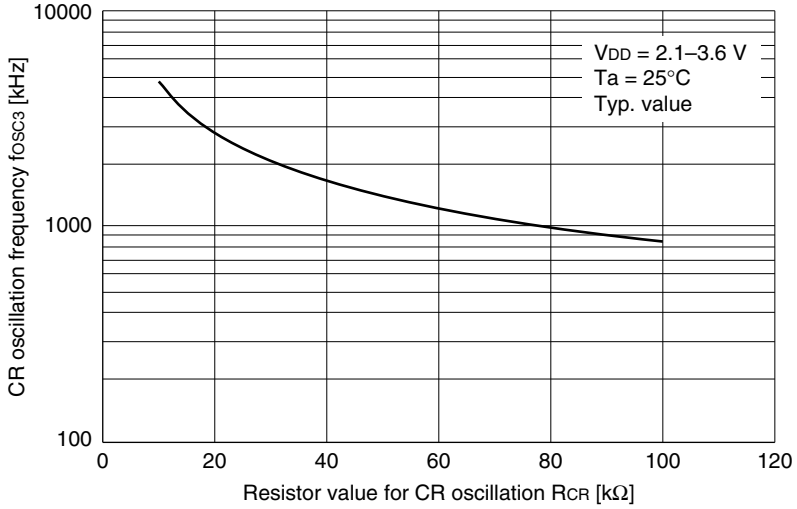
Unless otherwise specified:

V_{DD}=3.0V, V_{SS}=0V, R_{CR}=30kΩ (2MHz), Ta=-20 to 70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30		30	%
Oscillation start voltage	Vsta	(V_{DD})	2.1			V
Oscillation start time	tsta	V_{DD}=2.1 to 3.6V			3	ms
Oscillation stop voltage	Vstp	(V_{DD})	2.1			V

OSC3 CR oscillation frequency-resistance characteristic (external R type)

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values and evaluate the characteristics on the actual product.



7.6 Serial Interface AC Characteristics

Clock synchronous master mode

• During 32 kHz operation

Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=-20 to 70°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			5	µs
Receiving data input set-up time	tsms	10			µs
Receiving data input hold time	tsmh	5			µs

• During 4 MHz operation

Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=-20 to 70°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			200	ns
Receiving data input set-up time	tsms	400			ns
Receiving data input hold time	tsmh	200			ns

Note that the maximum clock frequency is limited to 2 MHz.

Clock synchronous slave mode

• During 32 kHz operation

Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=-20 to 70°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			10	µs
Receiving data input set-up time	tsss	10			µs
Receiving data input hold time	tssh	5			µs

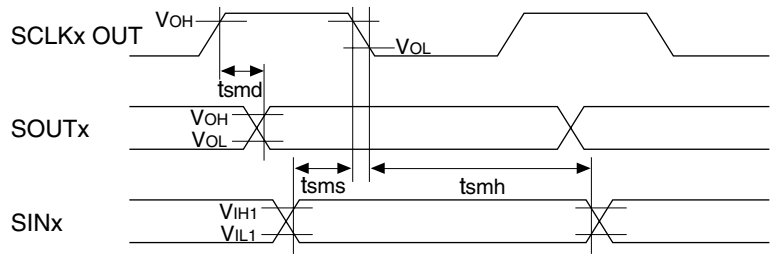
• During 4 MHz operation

Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=-20 to 70°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

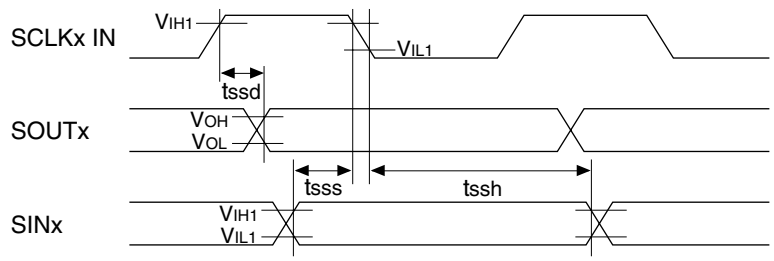
Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			500	ns
Receiving data input set-up time	tsss	400			ns
Receiving data input hold time	tssh	200			ns

Note that the maximum clock frequency is limited to 2 MHz.

<Master mode>

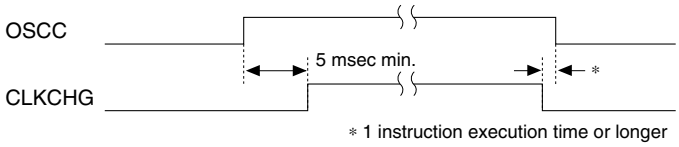


<Slave mode>



7.7 Timing Chart

System clock switching

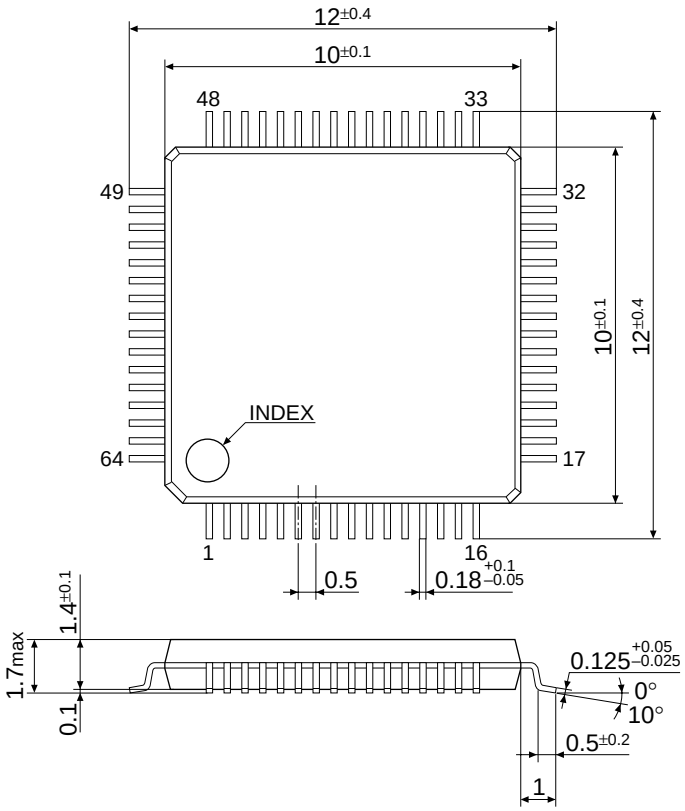


CHAPTER 8 PACKAGE

8.1 Plastic Package

QFP13-64pin

(Unit: mm)

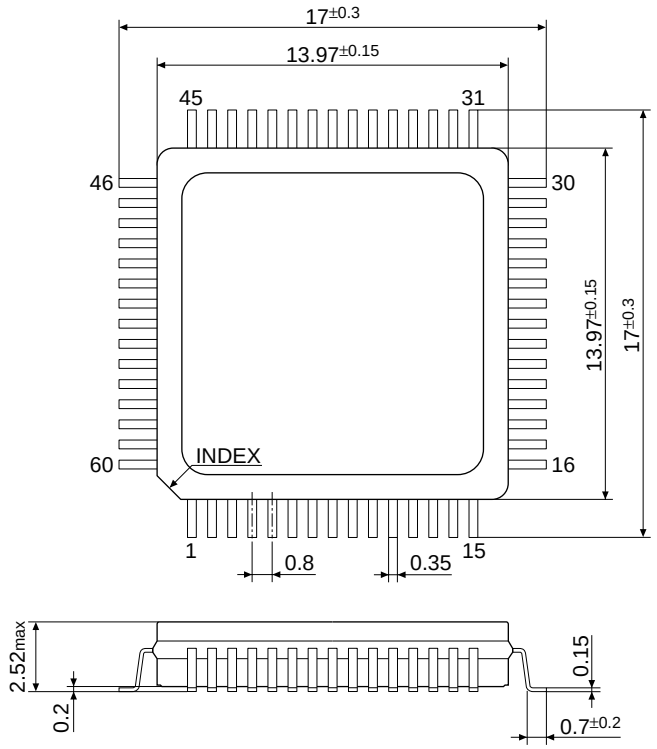


The dimensions are subject to change without notice.

8.2 Ceramic Package for Test Samples

QFP6-60pin

(Unit: mm)

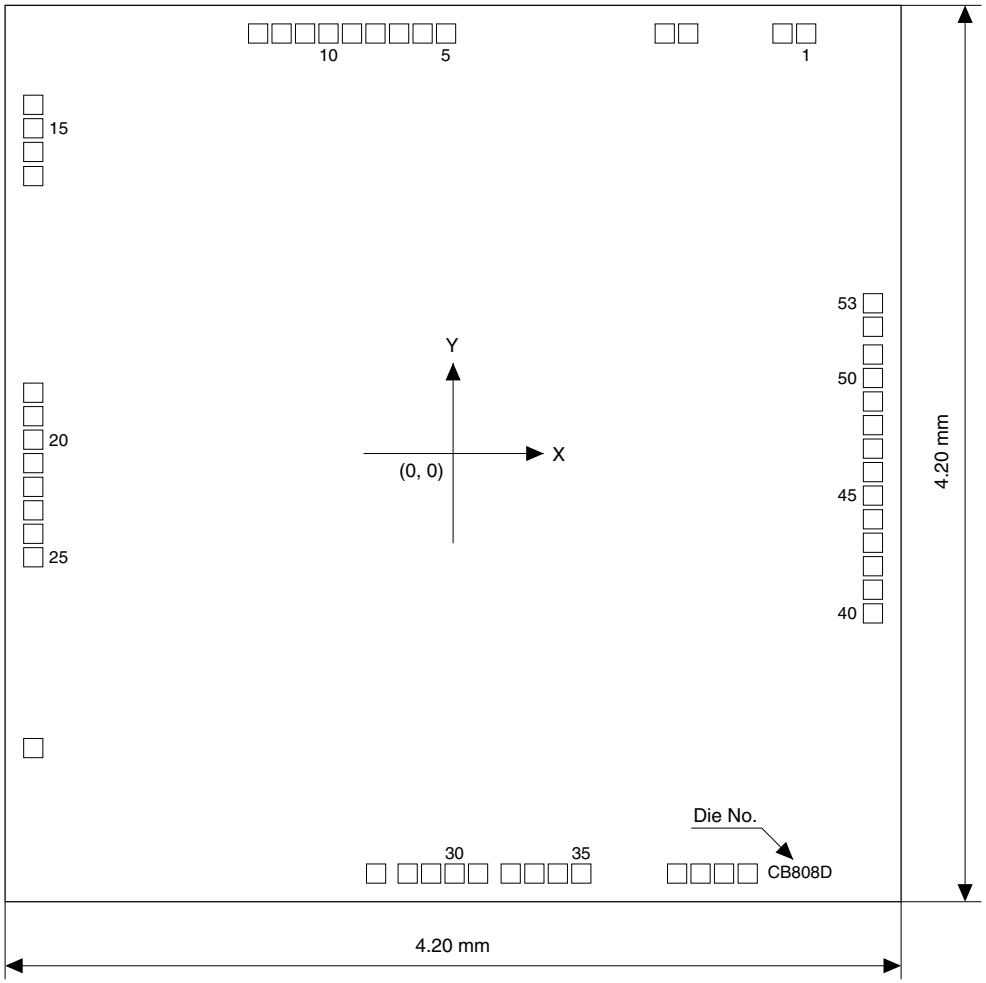


No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	P10/SIN1	16	P42	31	V_{C2}	46	N.C.
2	P11/SOUT1	17	P43	32	V_{C3}	47	N.C.
3	P12/SCLK1	18	TEST	33	CB	48	V_{SS}
4	P13/SRDY1	19	RESET	34	CA	49	R00
5	P20/SIN2	20	N.C.	35	K00	50	R01/BZ
6	P21/SOUT2	21	V_{DD}	36	K01	51	R02/TOUT
7	P22/SCLK2	22	V_{OSC}	37	K02	52	R03/FOUT
8	P23/SRDY2	23	OSC1	38	K03	53	R10
9	P30	24	OSC2	39	K10	54	R11
10	P31	25	V_{D1}	40	K11	55	R12
11	P32	26	OSC3	41	K12	56	R13
12	P33	27	OSC4	42	K13	57	P00
13	P40	28	V_{SS}	43	N.C.	58	P01
14	P41	29	V_{C1}	44	N.C.	59	P02
15	N.C.	30	N.C.	45	V_{DD}	60	P03

N.C. : No Connection

CHAPTER 9 PAD LAYOUT

9.1 Diagram of Pad Layout



Chip thickness: 400 µm
Pad opening: 90 µm

9.2 Pad Coordinates

Unit: mm

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	P42	1.655	1.968	14	V_{C2}	-1.968	1.634	27	V_{SS}	-0.361	-1.968	40	P10/SIN1	1.968	-0.749
2	P43	1.544	1.968	15	V_{C3}	-1.968	1.524	28	R00	-0.213	-1.968	41	P11/SOUT1	1.968	-0.638
3	TEST	1.102	1.968	16	CB	-1.968	1.413	29	R01/BZ	-0.103	-1.968	42	P12/SCLK1	1.968	-0.528
4	RESET	0.992	1.968	17	CA	-1.968	1.300	30	R02/TOUT	0.007	-1.968	43	P13/SRDY1	1.968	-0.418
5	V_{DD}	-0.033	1.968	18	K00	-1.968	0.285	31	R03/FOUT	0.117	-1.968	44	P20/SIN2	1.968	-0.308
6	V_{OSC}	-0.143	1.968	19	K01	-1.968	0.175	32	R10	0.270	-1.968	45	P21/SOUT2	1.968	-0.197
7	OSC1	-0.253	1.968	20	K02	-1.968	0.065	33	R11	0.381	-1.968	46	P22/SCLK2	1.968	-0.087
8	OSC2	-0.364	1.968	21	K03	-1.968	-0.045	34	R12	0.491	-1.968	47	P23/SRDY2	1.968	0.023
9	V_{D1}	-0.474	1.968	22	K10	-1.968	-0.156	35	R13	0.601	-1.968	48	P30	1.968	0.133
10	OSC3	-0.584	1.968	23	K11	-1.968	-0.266	36	P00	1.050	-1.968	49	P31	1.968	0.244
11	OSC4	-0.694	1.968	24	K12	-1.968	-0.376	37	P01	1.160	-1.968	50	P32	1.968	0.354
12	V_{SS}	-0.804	1.968	25	K13	-1.968	-0.486	38	P02	1.270	-1.968	51	P33	1.968	0.464
13	V_{C1}	-0.914	1.968	26	V_{DD}	-1.968	-1.380	39	P03	1.381	-1.968	52	P40	1.968	0.594
–	–	–	–	–	–	–	–	–	–	–	–	53	P41	1.968	0.704

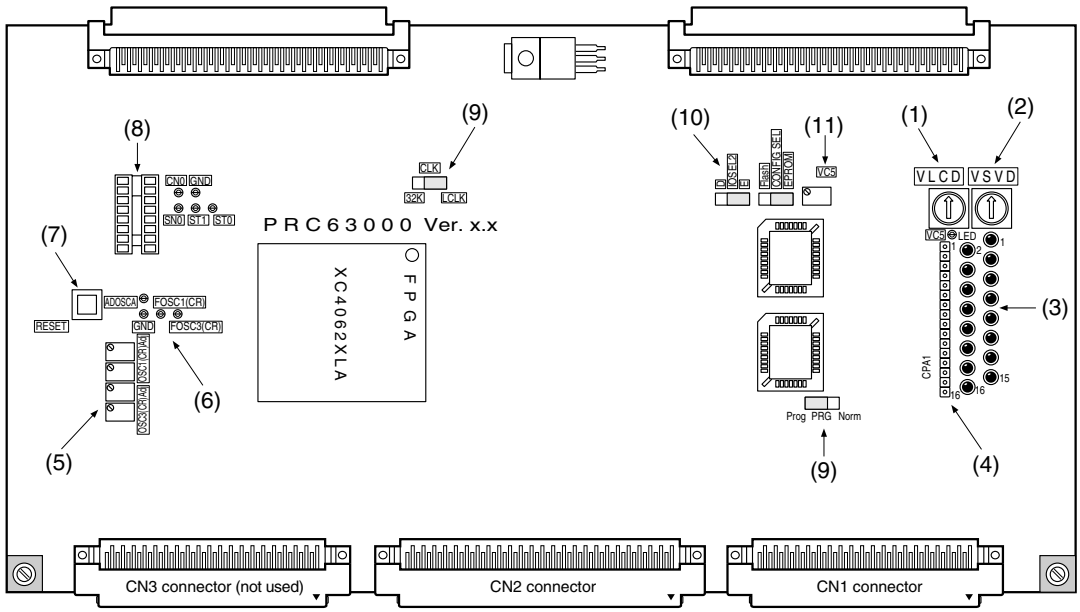
APPENDIX PERIPHERAL CIRCUIT BOARDS FOR S1C63808

This section describes how to use the Peripheral Circuit Boards for the S1C63808 (S5U1C63000P1), which provide emulation functions when mounted on the debugging tool for the S1C63 Family of 4-bit single-chip microcomputers, the ICE (S5U1C63000H1/S5U1C63000H2).

This description of the S1C63 Family Peripheral Circuit Board (S5U1C63000P1) provided in this document assumes that circuit data for the S1C63808 has already been downloaded to the board. For information on downloading various circuit data, please see Section A.3. Please refer to the user's manual provided with your ICE for detailed information on its functions and method of use.

A.1 Names and Functions of Each Part

The S5U1C63000P1 board provides peripheral circuit functions of S1C63 Family microcomputers other than the core CPU. The following explains the names and functions of each part of the S5U1C63000P1 board.



(1) VLCD

Unused

(2) VSVD

This control allows you to vary the power supply voltage artificially in order to verify the operation of the power supply voltage detect function (SVD).

(3) Register monitor LEDs

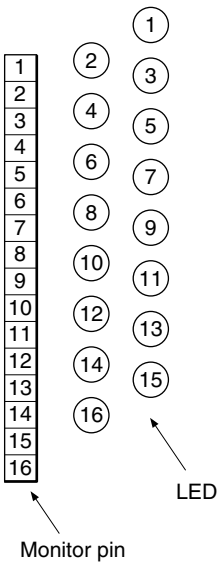
These LEDs correspond one-to-one to the registers listed below. The LED lights when the data is logic "1" and goes out when the data is logic "0".
SVDS0–SVDS2, SVDCHG, SVDON, OSCC, CLKCHG, HVLD, LPWR, LC0–LC2

(4) Register monitor pins

These pins correspond one-to-one to the registers listed below. The pin outputs a high for logic "1" and a low for logic "0".

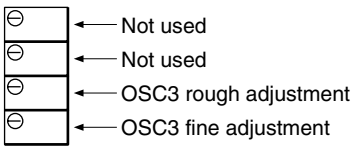
Monitor		LED	
Pin No.	Name	LED No.	Name
1	DONE *	1	DONE *
2	SVDS0	2	SVDS0
3	SVDS1	3	SVDS1
4	SVDS2	4	SVDS2
5	SVDCHG	5	SVDCHG
6	SVDON	6	SVDON
7	OSCC	7	OSCC
8	CLKCHG	8	CLKCHG
9	HVLD	9	HVLD
10	LPWR	10	LPWR
11	LC0	11	LC0
12	LC1	12	LC1
13	LC2	13	LC2
14	–	14	–
15	–	15	–
16	–	16	–

∗ DONE: The monitor pin outputs a high while the LED lights when initialization of this board completes without problems.



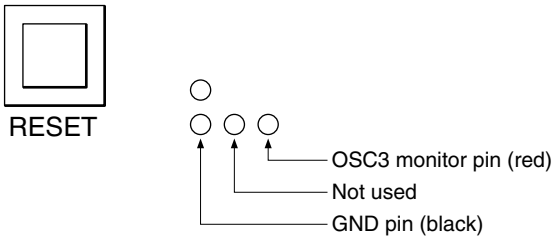
(5) CR oscillation frequency adjusting control

This control allows you to adjust the OSC3 oscillation frequency. This function is effective when ceramic oscillation is selected for the OSC3 oscillation circuit by mask option as well as when CR oscillation is selected. The oscillation frequency can be adjusted in the range of approx. 100 kHz to 8 MHz. Note that the actual IC does not operate with all of these frequencies; refer to Chapter 7, "Electrical Characteristics", to select the appropriate operating frequency.



(6) CR oscillation frequency monitor pins

These pins allow you to monitor the clock waveform from the CR oscillation circuit with an oscilloscope. Note that these pins always output a signal waveform whether or not the oscillation circuit is operating.



(7) RESET switch

This switch initializes the internal circuits of this board and feeds a reset signal to the ICE.

(8) External part connecting socket

Unused

(9) CLK and PRG switch

If power to the ICE is shut down before circuit data downloading is complete, the circuit configuration in this board will remain incomplete, and the debugger may not be able to start when you power on the ICE once again. In this case, temporarily power off the ICE and set CLK to the 32K position and the PRG switch to the Prog position, then switch on power for the ICE once again. This should allow the debugger to start up, allowing you to download circuit data. After downloading the circuit data, temporarily power off the ICE and reset CLK and PRG to the LCLK and the Norm position, respectively. Then power on the ICE once again.

(10) IOSEL2

When downloading circuit data, set IOSEL2 to the "E" position. Otherwise, set to the "D" position.

(11) VC5

This control allows adjustment of the EPD driver voltage values (V_{C1}–V_{C3}).

A.2 Connecting to the Target System

This section explains how to connect the S5U1C63000P1 to the target system.

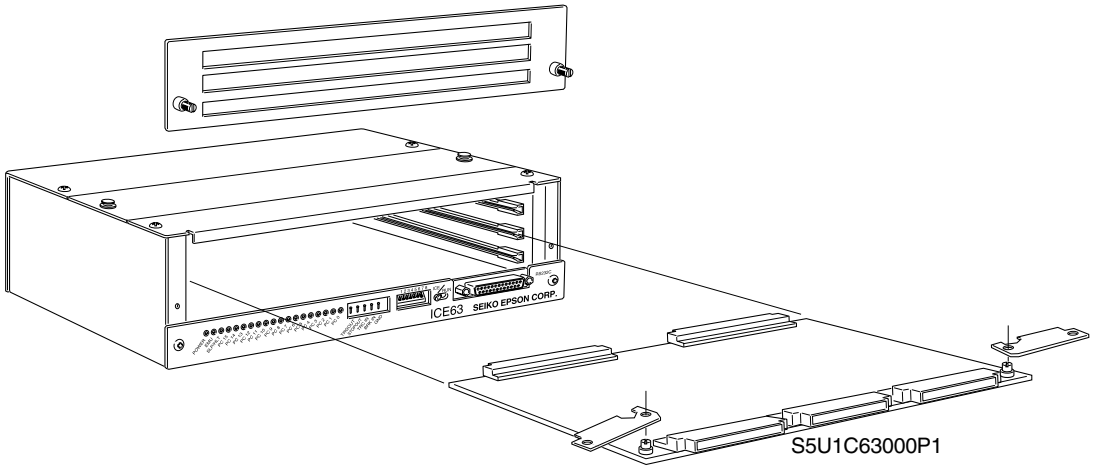


Fig. A.2.1 Installing the peripheral circuit boards to the ICE

- **Installing the S5U1C63000P1 board**

  Set the jig included with the ICE into position as shown in Figure A.2.2. Using this jig as a lever, push it toward the inside of the board evenly on the left and right sides. After confirming that the board has been firmly fitted into the internal slot of the ICE, remove the jig.

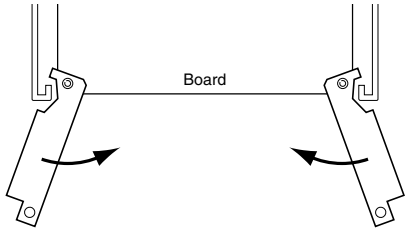


Fig. A.2.2 Installing the board

- **Dismounting the S5U1C63000P1 board**

  Set the jig included with the ICE into position as shown in Figure A.2.3. Using this jig as a lever, push it toward the outside of the board evenly on the left and right sides. After confirming that the board has been dismounted from the backboard connector, pull the board out of the ICE.

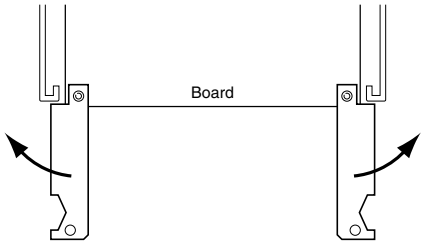


Fig. A.2.3 Dismounting the board

To connect this board (S5U1C63000P1) to the target system, use the I/O connecting cables supplied with the board (80-pin/40-pin × 2, flat type). Take care when handling the connectors, since they conduct electrical power (V_{DD} = +3.3 V).

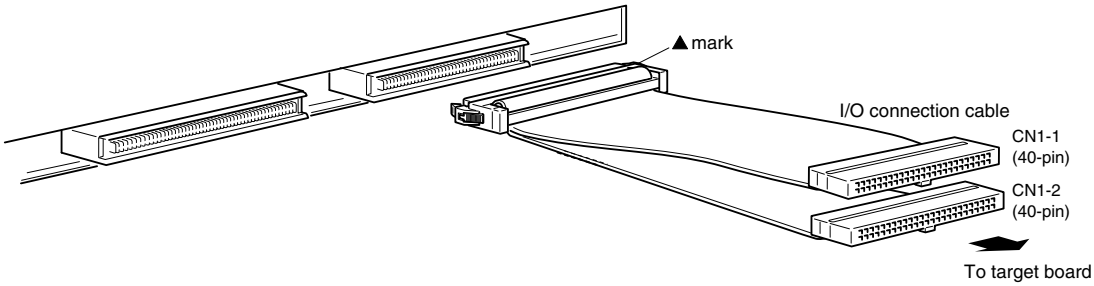


Fig. A.2.4 Connecting the S5U1C63000P1 to the target system

Table A.2.1 I/O connector pin assignment

40-pin CN1-1 connector			40-pin CN1-2 connector		
No.	Pin name	I/O	No.	Pin name	I/O
1	VDD (= 3.3 V)		1	VDD (= 3.3 V)	
2	VDD (= 3.3 V)		2	VDD (= 3.3 V)	
3	K00	I	3	R00	O
4	K01	I	4	R01	O
5	K02	I	5	R02	O
6	K03	I	6	R03	O
7	K10	I	7	R10	O
8	K11	I	8	R11	O
9	K12	I	9	R12	O
10	K13	I	10	R13	O
11	VSS		11	VSS	
12	VSS		12	VSS	
13	P00	I/O	13	Cannot be connected	
14	P01	I/O	14	Cannot be connected	
15	P02	I/O	15	Cannot be connected	
16	P03	I/O	16	Cannot be connected	
17	P10	I/O	17	Cannot be connected	
18	P11	I/O	18	Cannot be connected	
19	P12	I/O	19	Cannot be connected	
20	P13	I/O	20	Cannot be connected	
21	VDD (= 3.3 V)		21	VDD (= 3.3 V)	
22	VDD (= 3.3 V)		22	VDD (= 3.3 V)	
23	P20	I/O	23	Cannot be connected	
24	P21	I/O	24	Cannot be connected	
25	P22	I/O	25	Cannot be connected	
26	P23	I/O	26	Cannot be connected	
27	P30	I/O	27	Cannot be connected	
28	P31	I/O	28	Cannot be connected	
29	P32	I/O	29	Cannot be connected	
30	P33	I/O	30	EXOSC3	
31	Vss		31	VSS	
32	Vss		32	VSS	
33	P40	I/O	33	Cannot be connected	
34	P41	I/O	34	Cannot be connected	
35	P42	I/O	35	VC1	
36	P43	I/O	36	VC2	
37	Cannot be connected		37	VC3	
38	Cannot be connected		38	RESET	
39	Vss		39	VSS	
40	Vss		40	VSS	

A.3 Downloading to S5U1C63000P1

A.3.1 Downloading Circuit Data 1 – when new ICE (S5U1C63000H2) is used

The S5U1C63000P1 board comes with the FPGA that contains factory inspection data, therefore the circuit data for the model to be used should be downloaded. The following explains the downloading procedure.

1) Remove the ICE top cover and then set the DIP switch "IOSEL2" on this board to the "E" position.
2) Connect the ICE to the host PC. Then turn the host PC and ICE on.
3) Invoke the debugger included in the assembler package (ver. 5 or later). For how to use the ICE and debugger, refer to the manuals supplied with the ICE and assembler package.
4) Download the circuit data file (.mot) corresponding to the model by entering the following commands in the command window.

`>XFER`	(erase all)
`>XFWR` *<file name>*	(download the specified file)*
`>XFCP` *<file name>*	(compare the specified file and downloaded data)

   * The downloading takes about 15 minutes.
5) Terminate the debugger and then turn the ICE off.
6) Set the DIP switch "IOSEL2" on this board to the "D" position.
7) Turn the ICE on and invoke the debugger again. Debugging can be started here.

A.3.2 Downloading Circuit Data 2 – when previous ICE (S5U1C63000H1) is used

The standard ICE (S5U1C63000H1, previous model) did not support the circuit data download function for this board. To use the download function, update the ICE firmware according to the following procedure.

1) Set the baud rate of the ICE to 9600 bps. Refer to the manual supplied with the ICE for setting the DIP switch.
2) Connect the ICE to the host PC and then start up the host PC in DOS. When Windows is running, restart in DOS mode.

   Note: Do not use the DOS prompt of Windows.
3) Turn the ICE on.
4) Configure the RS232C parameters for the host PC as follows:

   `C:\>MODE COM1:9600,n,8,1,p` (9600 bps, 8-bit data, 1 stop bit, no parity)
5) Copy the following files included in the assembler package (ver. 5 or later) to a directory on the hard disk.

   `tm63.exe, ice63.com, i63com.o, i63par`
6) Move to the directory in Step 5, run the TM63. TM63 enters command ready status after invocation, enter a command as follows:

```
C:\>tm63 xat↵
TM63 start on IBM PC
TM63 start V01.01
>dlf ice63.com i63com.o i63par 0b↵
                ...
>q↵
```

7) Enter "q" to terminate TM63 after the prompt mark is displayed.
8) The ICE firmware is now updated. Turn the ICE off and then download the circuit data by the procedure described in Section A.3.1.

A.4 Usage Precautions

To ensure correct use of the peripheral circuit board, please observe the following precautions.

A.4.1 Operational precautions

(1) Before inserting or removing cables, turn off power to all pieces of connected equipment.
(2) Do not turn on power or load mask option data if all of the input ports (K00–K03) are held low. Doing so may activate the multiple key entry reset function.
(3) Before debugging, always be sure to load mask option data.

A.4.2 Differences with the actual IC

(1) Differences in I/O

<Interface power supply>

S5U1C63000P1 and target system interface voltage is set to +3.3 V. To obtain the same interface voltage as in the actual IC, attach a level shifter circuit, etc. on the target system side to accommodate the required interface voltage.

<Each output port's drive capability>

The drive capability of each output port on S5U1C63000P1 is higher than that of the actual IC. When designing application system and software, refer to Chapter 7, "Electrical Characteristics", to confirm each output port's drive capability.

<Each port's protective diode>

All I/O ports incorporate a protective diode for VDD and VSS, and the interface signals between S5U1C63000P1 and the target system are set to +3.3 V. Therefore, S5U1C63000P1 and the target system cannot be interfaced with voltages exceeding VDD by setting the output ports for open-drain mode.

<Pull-down resistance value>

The pull-down resistance values on S5U1C63000P1 are set to 220 kΩ which differ from those for the actual IC. For the resistance values on the actual IC, refer to Chapter 7, "Electrical Characteristics". Note that when using pull-down resistors to pull the input pins low, the input pins may require a certain period to reach a valid low level. Exercise caution if a key matrix circuit is configured using a combination of output and input ports, since fall delay times on these input ports differ from those of the actual IC.

(2) Differences in current consumption

The amount of current consumed by the peripheral circuit boards differ significantly from that of the actual IC. Inspecting the LEDs on S5U1C63000P1 may help you keep track of approximate current consumption. The following factors/components greatly affect device current consumption:

<Those which can be verified by LEDs and monitor pins>

a) Run and Halt execution ratio (verified by LEDs and monitor pins on the ICE)
b) OSC3 oscillation on/off (OSCC)
c) CPU clock select (CLKCHG)
d) SVD circuit on/off (SVDON)
e) EPD system voltage circuit on/off (LPWR)

<Those that can only be counteracted by system or software>

f) Current consumed by the internal pull-down resistors
g) Input ports in a floating state

(3) Functional precautions

<SVD circuit>

- The SVD function is realized by artificially varying the power supply voltage using the VSVD control on S5U1C63000P1.
- There is a finite delay time from when the power to the SVD circuit turns on until actual detection of the voltage. On S5U1C63000P1, this delay is set to approx. 500 µsec, which differs from that of the actual IC. Refer to Chapter 7, "Electrical Characteristics", when setting the appropriate wait time for the actual IC.

<Oscillation circuit>

- A wait time is required before oscillation stabilizes after the OSC3 oscillation control circuit (OSCC) is turned on. On S5U1C63000P1, even when OSC3 oscillation is changed (CLKCHG) without a wait time, OSC3 will function normally. Refer to Chapter 7, "Electrical Characteristics", when setting the appropriate wait time for the actual IC.
- Use separate instructions to switch the clock from OSC3 to OSC1 and to turn off the OSC3 oscillation circuit. If executed simultaneously with a single instruction, these operations, although good with S5U1C63000P1, may not function properly well with the actual IC.
- Because the logic level of the oscillation circuit is high, the timing at which the oscillation starts on S5U1C63000P1 differs from that of the actual IC.
- S5U1C63000P1 contains oscillation circuits for OSC1 and OSC3. Keep in mind that even though the actual IC may not have a resonator connected to its OSC3, its emulator can operate with the OSC3 circuit.
- S5U1C63000P1 generates the OSC3 clock using the onboard CR oscillation circuit even if ceramic oscillation is selected for the OSC3 oscillation circuit by mask option.

<Power supply for EPD driver IC>

The characteristics of the power supply for the EPD driver IC, such as voltage values (V_{C1}–V_{C3}) output from the I/O connector and drive capability are different from those of the actual IC. Furthermore, note that the output voltage may oscillate if an element such as a capacitor is connected to the output terminal.
The voltage values can be adjusted manually using the VC5 control.

<Access to undefined address space>

If any undefined space in the S1C63808's internal ROM/RAM or I/O is accessed for data read or write operations, the read/written value is indeterminate. Additionally, it is important to remain aware that indeterminate state differs between S5U1C63000P1 and the actual IC. Note that the ICE (S5U1C63000H1/S5U1C63000H2) incorporates the program break function caused by accessing to an undefined address space.

<Reset circuit>

Keep in mind that the operation sequence from when the ICE and the peripheral circuit board are powered on until the time at which the program starts running differs from the sequence from when the actual IC is powered on till the program starts running. This is because S5U1C63000P1 becomes capable of operating as a debugging system after the user program and optional data are downloaded. When operating the ICE after placing it in free-running mode, always apply a system reset. A system reset can be performed by pressing the reset switch on S5U1C63000P1, by a reset pin input, or by holding the input ports high simultaneously.

A.5 Product Specifications

S5U1C63000P1

Dimension:	254 mm (wide) × 144.8 mm (depth) × 13 mm (height)	(including screws)
Weight:	Approx. 300 g	
Power supply:	DC 5 V ± 5%, less than 1 A	(supplied from ICE main unit)

I/O connection cable (80-pin)

S5U1C63000P1 connector:	KEL8830E-080-170L	
Cable connector (80-pin):	KEL8822E-080-171	
Cable connector (40-pin):	3M7940-6500SC	1 pair
Cable:	40-pin flat cable	1 pair
Interface:	CMOS interface (3.3 V)	
Length:	Approx. 40 cm	

Accessories

40-pin connector for connecting to target system:
3M3432-6002LCSC × 2

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