

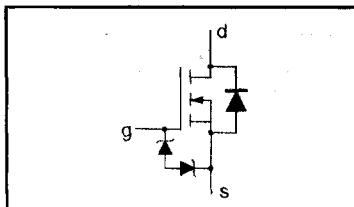
TrenchMOS™ transistor

Logic level FET

PHT6N03LT

FEATURES

- 'Trench' technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Surface mounting package

SYMBOL**QUICK REFERENCE DATA**

$V_{DSS} = 30 \text{ V}$
$I_D = 5.9 \text{ A}$
$R_{DS(ON)} \leq 30 \text{ m}\Omega (V_{GS} = 5 \text{ V})$
$R_{DS(ON)} \leq 28 \text{ m}\Omega (V_{GS} = 10 \text{ V})$

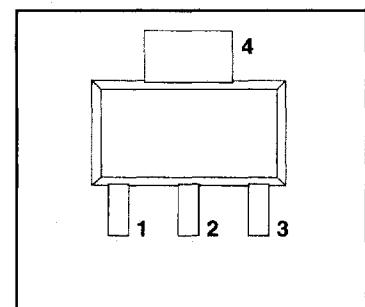
GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor using 'trench' technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHT6N03LT is supplied in the SOT223 surface mounting package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

SOT223**LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	$T_j = 25 \text{ }^\circ\text{C to } 150 \text{ }^\circ\text{C}$	-	30	V
V_{DGR}	Drain-gate voltage	$T_j = 25 \text{ }^\circ\text{C to } 150 \text{ }^\circ\text{C}; R_{GS} = 20 \text{ k}\Omega$	-	30	V
V_{GS}	Gate-source voltage		-	± 13	V
I_D	Continuous drain current	$T_{amb} = 25 \text{ }^\circ\text{C}; V_{GS} = 10 \text{ V}$	-	5.9	A
I_{DM}	Pulsed drain current	$T_{amb} = 100 \text{ }^\circ\text{C}; V_{GS} = 10 \text{ V}$	-	4.1	A
P_D	Total power dissipation		-	23.6	A
T_j, T_{stg}	Operating junction and storage temperature	$T_{amb} = 25 \text{ }^\circ\text{C}$	-55	150	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th(j-sp)}$	Thermal resistance junction to solder point	mounted on any PCB	-	-	15	K/W
$R_{th(j-a)}$	Thermal resistance junction to ambient	mounted on test PCB of fig:17	-	70	-	K/W

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ELECTRICAL CHARACTERISTICS $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 0.25 \text{ mA}$	30	-	-	V
$V_{(\text{BR})\text{GSS}}$	Gate-source breakdown voltage	$I_G = 1 \text{ mA}$	27	-	-	V
$V_{GS(\text{TO})}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 1 \text{ mA}$	10	-	-	V
$R_{DS(\text{ON})}$	Drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 3.2 \text{ A}$ $V_{GS} = 10 \text{ V}; I_D = 3.2 \text{ A}$ $V_{GS} = 5 \text{ V}; I_D = 3.2 \text{ A}; T_j = 150^\circ\text{C}$ $V_{DS} = 25 \text{ V}; I_D = 5.9 \text{ A}$ $V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}$	1 0.6 - - -	1.5 - 24 18 -	2 - 30 28 51	V mΩ mΩ mΩ
g_{ds} I_{oss}	Forward transconductance Zero gate voltage drain current	$T_j = 150^\circ\text{C}$	8	14	-	S
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 5 \text{ V}; V_{DS} = 0 \text{ V}$	-	0.05	10	μA
		$T_j = 150^\circ\text{C}$	-	0.02	500	μA
			-	-	1	μA
			-	-	10	μA
$Q_{g(\text{tot})}$ Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain (Miller) charge	$I_D = 5.9 \text{ A}; V_{DD} = 24 \text{ V}; V_{GS} = 5 \text{ V}$	-	24	-	nC
$t_{d\text{ on}}$ t_r	Turn-on delay time Turn-on rise time	$V_{DD} = 15 \text{ V}; I_D = 5.9 \text{ A}$	-	3	-	nC
$t_{d\text{ off}}$ t_f	Turn-off delay time Turn-off fall time	$V_{GS} = 5 \text{ V}; R_G = 5 \Omega$ Resistive load	- - - -	11 80 95 40	45 130 135 55	ns ns ns ns
L_d L_d L_s	Internal drain inductance Internal drain inductance Internal source inductance	Measured from tab to centre of die Measured from drain lead to centre of die Measured from source lead to source bond pad	- - -	3.5 3.5 7.5	-	nH
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Feedback capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz}$	- - -	1050 270 140	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_s	Continuous source current (body diode)		-	-	5.9	A
I_{SM}	Pulsed source current (body diode)		-	-	10	A
V_{SD}	Diode forward voltage	$I_F = 5.9 \text{ A}; V_{GS} = 0 \text{ V}$	-	0.75	1.2	V
t_{rr} Q_{rr}	Reverse recovery time Reverse recovery charge	$I_F = 5.9 \text{ A}; -dI_F/dt = 100 \text{ A}/\mu\text{s}$ $V_{GS} = -10 \text{ V}; V_R = 25 \text{ V}$	- -	100 0.4	-	ns μC

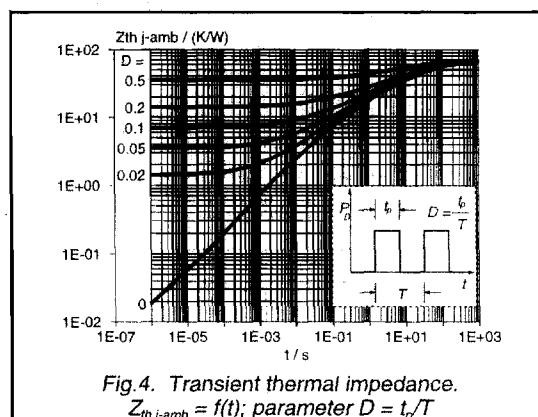
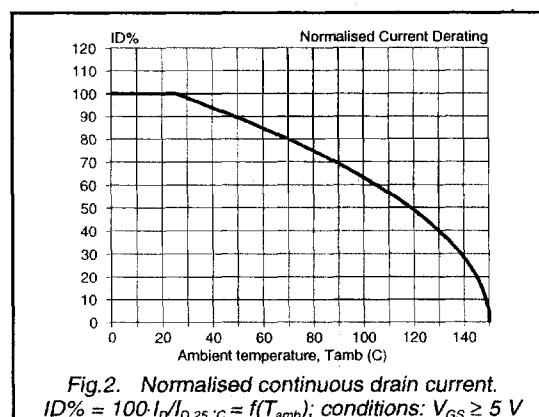
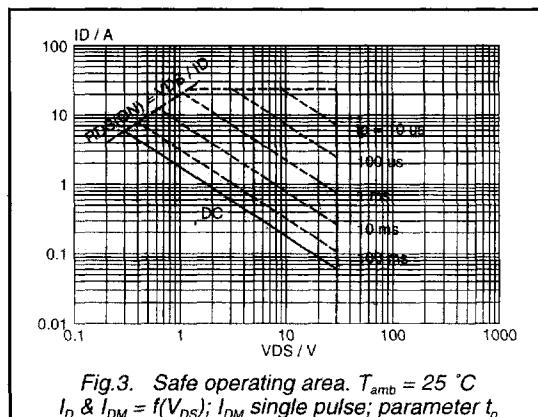
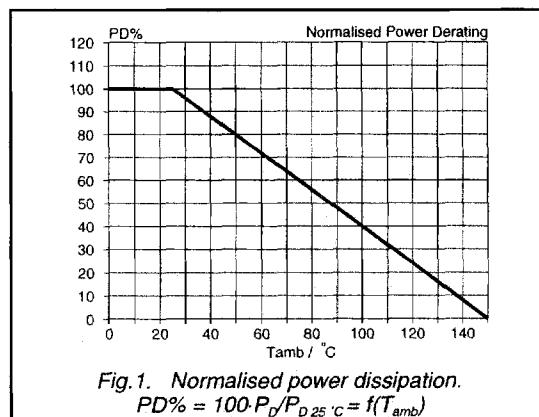
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AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 5.9 \text{ A}$; $V_{DD} \leq 15 \text{ V}$; $V_{GS} = 10 \text{ V}$; $R_{GS} = 50 \Omega$; $T_{amb} = 25^\circ\text{C}$	-	60	mJ



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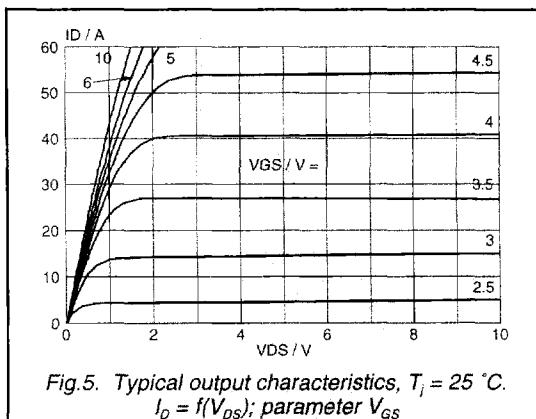


Fig.5. Typical output characteristics, $T_j = 25^\circ\text{C}$.
 $I_D = f(V_{DS})$; parameter V_{GS}

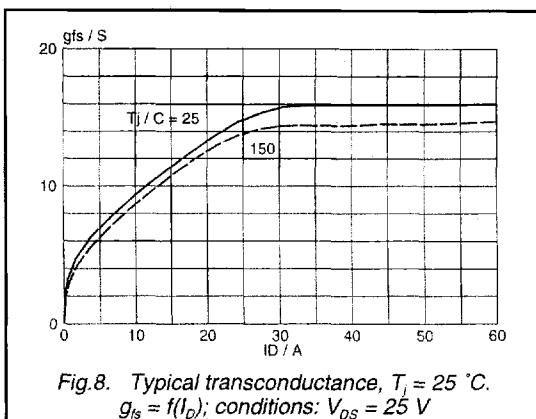


Fig.8. Typical transconductance, $T_j = 25^\circ\text{C}$.
 $g_{fs} = f(I_D)$; conditions: $V_{DS} = 25\text{V}$

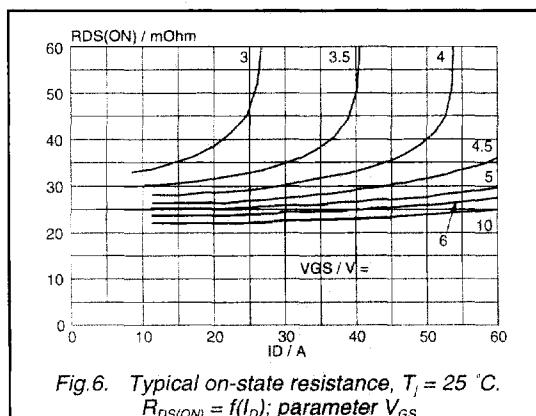


Fig.6. Typical on-state resistance, $T_j = 25^\circ\text{C}$.
 $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

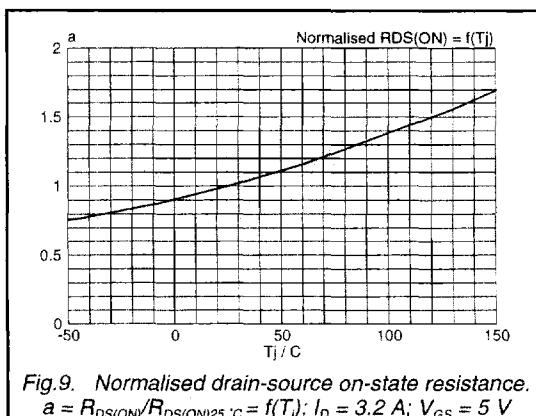


Fig.9. Normalised drain-source on-state resistance.
 $a = R_{DS(ON)}/R_{DS(ON)25^\circ\text{C}} = f(T_j)$; $I_D = 3.2\text{A}$; $V_{GS} = 5\text{V}$

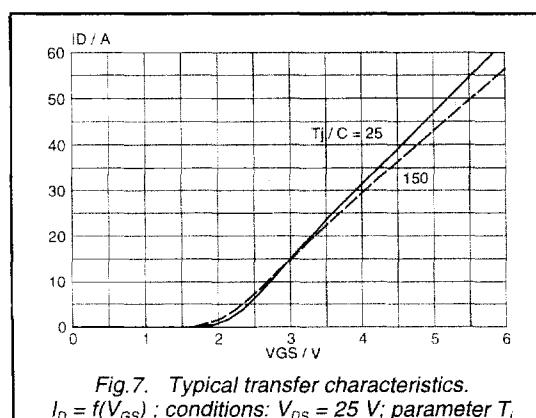


Fig.7. Typical transfer characteristics.
 $I_D = f(V_{GS})$; conditions: $V_{DS} = 25\text{V}$; parameter T_j

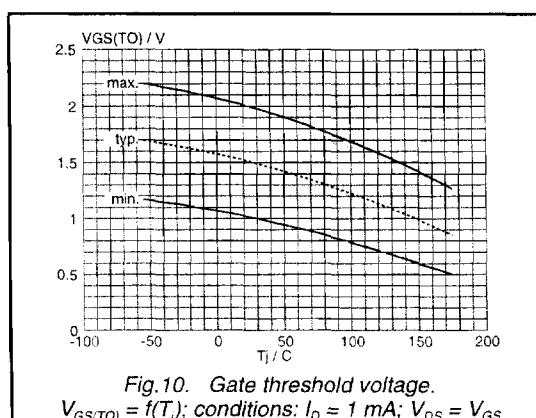


Fig.10. Gate threshold voltage.
 $V_{GS(TH)} = f(T_j)$; conditions: $I_D = 1\text{mA}$; $V_{DS} = V_{GS}$

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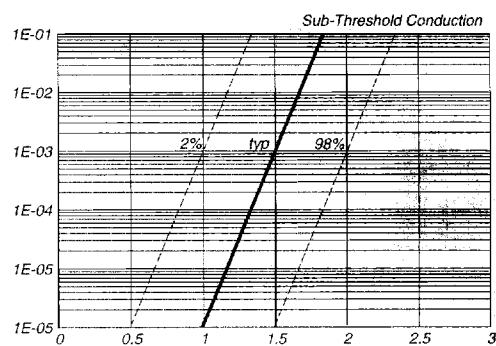


Fig. 11. Sub-threshold drain current.
 $I_D = f(V_{GS})$; conditions: $T_J = 25^\circ\text{C}$; $V_{DS} = V_{GS}$

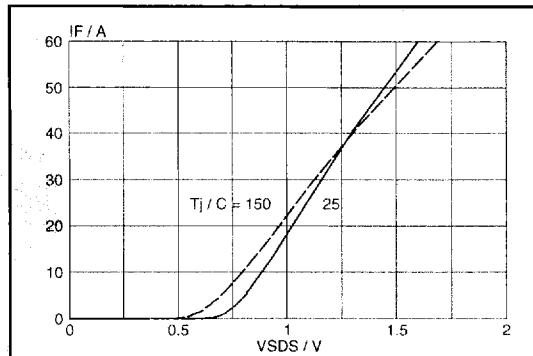


Fig. 14. Typical reverse diode current.
 $I_F = f(V_{DS})$; conditions: $V_{GS} = 0\text{ V}$; parameter T_j

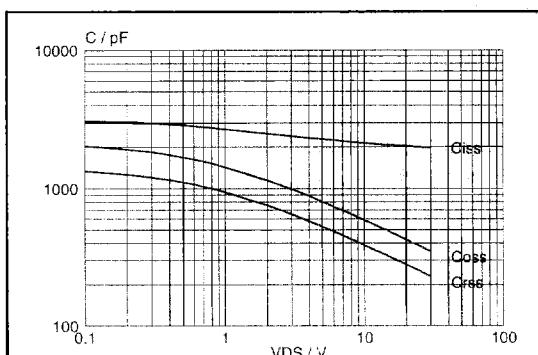


Fig. 12. Typical capacitances, C_{iss} , C_{oss} , C_{rss} .
 $C = f(V_{DS})$; conditions: $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

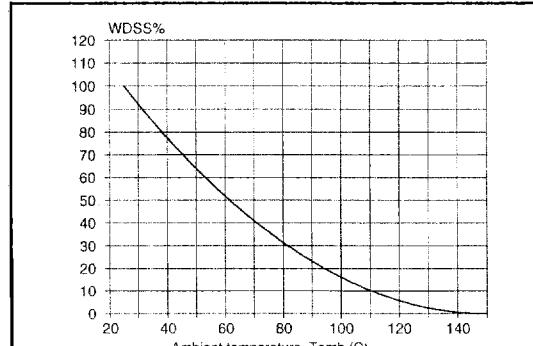


Fig. 15. Normalised avalanche energy rating.
 $W_{DSS}\% = f(T_{amb})$; conditions: $I_D = 5.9\text{ A}$

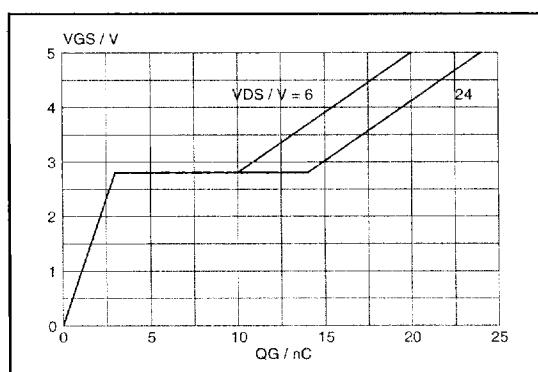


Fig. 13. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$; conditions: $I_D = 5.9\text{ A}$; parameter V_{DS}

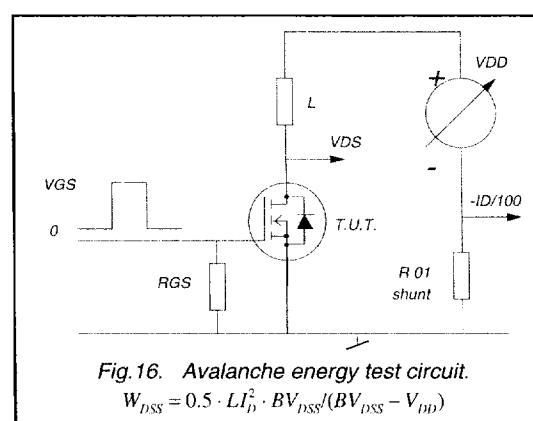
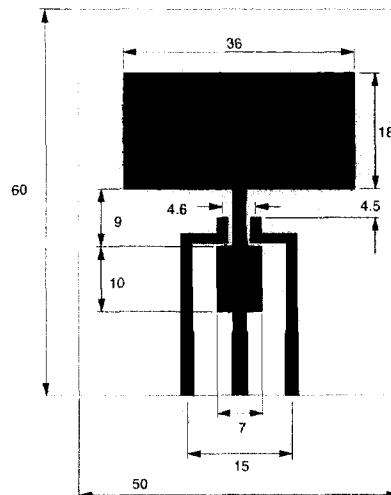


Fig. 16. Avalanche energy test circuit.
 $W_{DSS} = 0.5 \cdot L I_D^2 \cdot BV_{DSS} / (BV_{DSS} - V_{DD})$

**TrenchMOS™ transistor
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*Fig.17. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μ m thick).*