16-bit Programmable LED Dimmer with I²C Interface

FEATURES

- 16 LED drivers with dimming control
- 256 brightness steps
- 16 open drain outputs drive 25 mA each
- 2 selectable programmable blink rates:
  - frequency: 0.593Hz to 152Hz
  - duty cycle: 0% to 99.6%
- I/Os can be used as GPIOs
- 400kHz I²C bus compatible*
- 2.3V to 5.5V operation
- 5V tolerant I/Os
- Active low reset input
- RoHS-compliant 24-Lead SOIC, TSSOP and 24-pad TQFN (4 x 4mm) packages

APPLICATIONS

- Backlighting
- RGB color mixing
- Sensors control
- Power switches, push-buttons
- Alarm systems

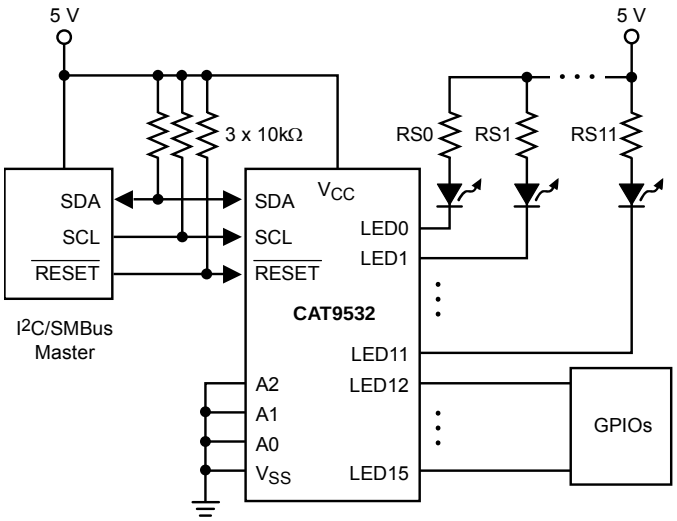
For Ordering Information details, see page 16.

DESCRIPTION

The CAT9532 is a CMOS device that provides 16-bit parallel input/output port expander optimized for LED dimming control. The CAT9532 outputs can drive directly 16 LEDs in parallel. Each individual LED may be turned ON, OFF, or blinking at one of two programmable rates. The device provides a simple solution for dimming LEDs in 256 brightness steps for backlight and color mixing applications. The CAT9532 is suitable in I²C and SMBus compatible applications where it is necessary to limit the bus traffic or free-up the bus master's timer.

The CAT9532 contains an internal oscillator and two PWM signals that drive the LED outputs. The user can program the period and duty cycle for each individual PWM signal. After the initial set-up command to program the Blink Rate 1 and Blink Rate 2 (frequency and duty cycle), only one command from the bus master is required to turn each individual open drain output ON, OFF, or cycle at Blink Rate 1 or Blink Rate 2. Each open drain LED output can provide a maximum output current of 25mA. The total current sunk by all I/Os must not exceed 200mA.

TYPICAL APPLICATION CIRCUIT

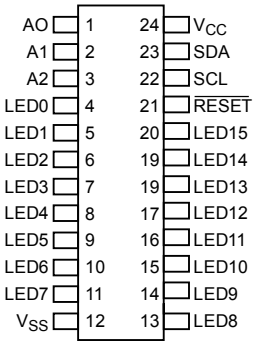


* Catalyst Semiconductor is licensed by Philips Corporation to carry the I²C Protocol.

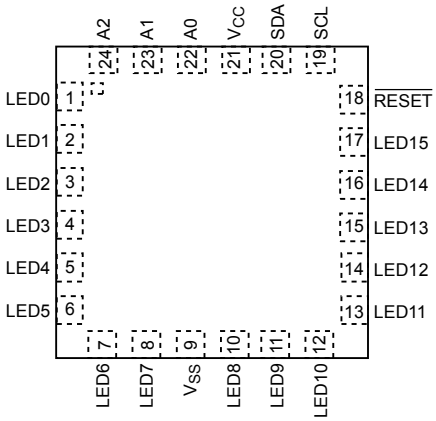
Notes: LED0 to LED11 are used as LED drivers
LED12 to LED15 are used as regular GPIOs

PIN CONFIGURATION

SOIC (W), TSSOP (Y)



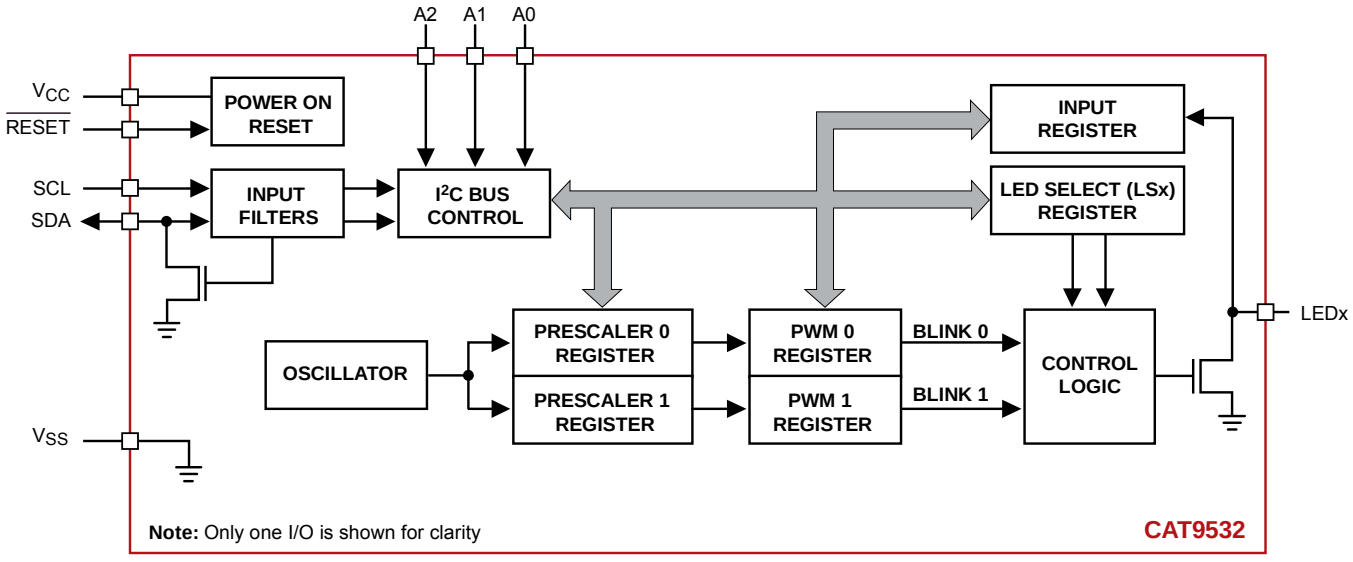
TQFN (HV6)



PIN DESCRIPTION

DIP / SOIC / TSSOP	TQFN	PIN NAME	FUNCTION
1	22	AO	Address Input 0
2	23	A1	Address Input 1
3	24	A2	Address Input 2
4-11	1-8	LED0 - LED7	LED Driver Output 0 to 7, I/O Port 0 to 7
12	9	V_{SS}	Ground
13-20	10-17	LED8 - LED15	LED Driver Output 8 to 15, I/O Port 8 to 15
21	18	$\overline{RESET}$	Reset Input
22	19	SCL	Serial Clock
23	20	SDA	Serial Data
24	21	V_{CC}	Power Supply

BLOCK DIAGRAM



© Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

ABSOLUTE MAXIMUM RATINGS[1]

Parameters	Ratings	Units
V_{CC} with Respect to Ground	-2.0 to +7.0	V
Voltage on Any Pin with Respect to Ground	-0.5 to +5.5	V
DC Current on I/Os	±25	mA
Supply Current	200	mA
Package Power Dissipation Capability (T_A = 25ºC)	1.0	W
Junction Temperature	+150	°C
Storage Temperature	-65 to +150	ºC
Lead Soldering Temperature (10 seconds)	300	ºC
Operating Ambient Temperature	-40 to +85	ºC

Notes:

(1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

© Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

D.C. OPERATING CHARACTERISTICS

V_{CC} = 2.3 to 5.5V, V_{SS} = 0V; T_A = -40ºC to +85ºC, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{CC}	Supply Voltage		2.3	—	5.5	V
I_{CC}	Supply Current	Operating mode; V_{CC} = 5.5V; no load; f_{SCL} = 100kHz	—	250	550	µA
I_{stb}	Standby Current	Standby mode; V_{CC} = 5.5V; no load; $V_I = V_{SS}$ or V_{CC}, f_{SCL} = 0kHz	—	2.1	5.0	µA
ΔI_{stb}	Additional Standby Current	Standby mode; V_{CC} = 5.5V; every LED I/O = V_{IN} = 4.3V, f_{SCL} = 0kHz	—	—	2	mA
V_{POR} (1)	Power-on Reset Voltage	V_{CC} = 3.3V, No load; $V_I = V_{CC}$ or V_{SS}	—	1.5	2.2	V
SCL, SDA, $\overline{\text{RESET}}$						
V_{IL} (2)	Low Level Input Voltage		-0.5	—	0.3 V_{CC}	V
V_{IH} (2)	High Level Input Voltage		0.7 V_{CC}	—	5.5	V
I_{OL}	Low Level Output Current	V_{OL} = 0.4V	3	—	—	mA
I_{IL}	Leakage Current	$V_I = V_{CC} = V_{SS}$	-1	—	+1	µA
C_I (3)	Input Capacitance	$V_I = V_{SS}$	—	—	6	pF
C_O (3)	Output Capacitance	$V_O = V_{SS}$	—	—	8	pF
A0, A1, A2						
V_{IL} (2)	Low Level Input Voltage		-0.5	—	0.8	V
V_{IH} (2)	High Level Input Voltage		2.0	—	5.5	V
I_{IL}	Input Leakage Current		-1	—	1	µA
I/Os						
V_{IL} (2)	Low Level Input Voltage		-0.5	—	0.8	V
V_{IH} (2)	High Level Input Voltage		2.0	—	5.5	V
I_{OL} (4)	Low Level Output Current	V_{OL} = 0.4V; V_{CC} = 2.3V	9	—	—	mA
		V_{OL} = 0.4V; V_{CC} = 3.0V	12	—	—	
		V_{OL} = 0.4V; V_{CC} = 5.0V	15	—	—	
		V_{OL} = 0.7V; V_{CC} = 2.3V	15	—	—	
		V_{OL} = 0.7V; V_{CC} = 3.0V	20	—	—	
		V_{OL} = 0.7V; V_{CC} = 5.0V	25	—	—	
I_{IL}	Input Leakage Current	V_{CC} = 3.6V; $V_I = V_{SS}$ or V_{CC}	-1	—	1	µA
$C_{I/O}$ (3)	Input/Output Capacitance		—	—	8	pF

Notes:

(1) V_{DD} must be lowered to 0.2V in order to reset the device.

(2) V_{IL} min and V_{IH} max are reference values only and are not tested.

(3) This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.

(4) The output current must be limited to a maximum 25mA per each I/O; the total current sunk by all I/O must be limited to 200mA (or 100mA for eight I/Os)

© Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

A.C. CHARACTERISTICS

V_{CC} = 2.3V to 5.5V, T_A = -40ºC to +85ºC, unless otherwise specified[1]

Symbol	Parameter	Min	Typ	Max	Units
f_{SCL}	Clock Frequency			400	kHz
t_{SP}[2]	Input Filter Spike Suppression (SDA, SCL)			50	ns
t_{LOW}	Clock Low Period	1.3			µs
t_{HIGH}	Clock High Period	0.6			µs
t_R[2]	SDA and SCL Rise Time			300	ns
t_F[2]	SDA and SCL Fall Time			300	ns
$t_{HD:STA}$	Start Condition Hold Time	0.6			µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeater Start)	0.6			µs
$t_{HD:DAT}$	Data Input Hold Time	0			ns
$t_{SU:DAT}$	Data in Setup Time	100			ns
$t_{SU:STO}$	Stop Condition Setup Time	0.6			µs
t_{AA}	SCL Low to Data Out Valid			900	ns
t_{DH}	Data Out Hold Time	50			ns
t_{BUF}[2]	Time the Bus must be Free Before a New Transmission Can Start	1.3			µs
Port Timing					
t_{PV}	Output Data Valid			200	ns
t_{PS}	Input Data Setup Time	100			ns
t_{PH}	Input Data Hold Time	1			µs
Reset					
t_W[2]	Reset Pulse Width	10			ns
t_{REC}	Reset Recovery Time	0			ns
t_{RESET}[3]	Time to Reset	400			ns

Notes:

(1) Test conditions according to "AC Test Conditions" table.

(2) This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.

(3) The full delay to reset the part will be the sum of t_{RESET} and the RC time constant of the SDA line.

© Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

AC TEST CONDITIONS

Input Pulse Voltage	$0.2V_{CC}$ to $0.8V_{CC}$
Input Rise and Fall Times	≤5ns
Input Reference Voltage	$0.3V_{CC}$, $0.7V_{CC}$
Output Reference Voltage	$0.5V_{CC}$
Output Load	Current source: I_{OL} = 3mA; 400pF for $f_{SCL(max)}$ = 400kHz

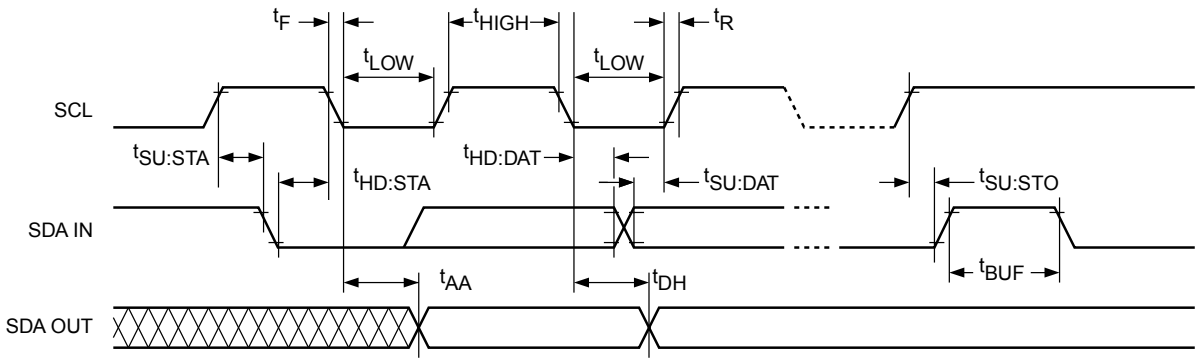


Figure 1. 2-Wire Serial Interface Timing

PIN DESCRIPTION

SCL: Serial Clock
The serial clock input clocks all data transferred into or out of the device. The SCL line requires a pull-up resistor if it is driven by an open drain output.

SDA: Serial Data/Address
The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs. A pull-up resistor must be connected from SDA line to V_{CC}.

LED0 to LED15: LED Driver Outputs / General Purpose I/Os
The pins are open drain outputs used to drive directly LEDs. Any of these pins can be programmed to drive the LED ON, OFF, Blink Rate1 or Blink Rate2. When not used for controlling the LEDs, these pins may be used as general purpose parallel input/output.

$\overline{\text{RESET}}$: External Reset Input
Active low Reset input is used to initialize the CAT9532 internal registers and the I^2C state machine. The internal registers are held in their default state while Reset input is active. An external pull-up resistor of maximum 25kΩ is required when this pin is not actively driven.

© Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

FUNCTIONAL DESCRIPTION

The CAT9532 is a 16-bit I/O bus expander that provides a programmable LED dimmer, controlled through an I^2C compatible serial interface.

The CAT9532 supports the I^2C Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT9532 operates as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

I^2C Bus Protocol

The features of the I^2C bus protocol are defined as follows:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition (Figure 2).

START and STOP Conditions

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT9532 monitors the SDA and SCL lines and will not respond until this condition is met.

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

Device Addressing

After the bus Master sends a START condition, a slave address byte is required to enable the CAT9532 for a read or write operation. The four most significant bits of the slave address are fixed as binary 1100 (Figure 3). The CAT9532 uses the next three bits as address bits.

The address bits A2, A1 and A0 are used to select which device is accessed from maximum eight devices on the same bus. These bits must compare to their hardwired input pins. The 8th bit following the 7-bit slave address is the R/W bit that specifies whether a read or write operation is to be performed. When this bit is set to “1”, a read operation is initiated, and when set to “0”, a write operation is selected.

Following the START condition and the slave address byte, the CAT9532 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT9532 then performs a read or a write operation depending on the state of the R/W bit.

Figure 2. Start/Stop Timing

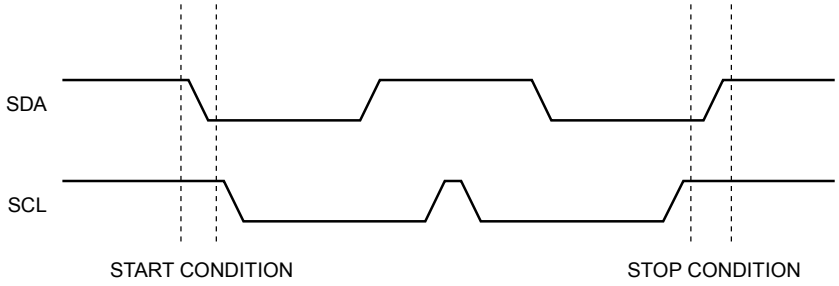
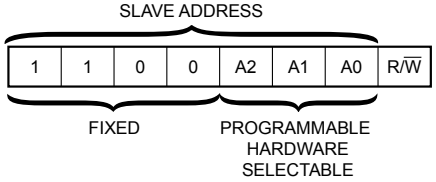


Figure 3. CAT9532 Slave Address



© Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data. The SDA line remains stable LOW during the HIGH period of the acknowledge related clock pulse (Figure 4).

The CAT9532 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8- bit byte.

When the CAT9532 begins a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT9532 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition. The master must then issue a stop condition to return the CAT9532 to the standby power mode and place the device in a known state.

Registers and Bus Transactions

After the successful acknowledgement of the slave address, the bus master will send a command byte to the CAT9532 which will be stored in the Control Register. The format of the Control Register is shown in Figure 5.

The Control Register acts as a pointer to determine which register will be written or read. The four least significant bits, B0, B1, B2, B3, are used to select which internal register is accessed, according to the Table 1.

If the auto increment flag (AI) is set, the four least significant bits of the Control Register are automatically incremented after a read or write operation. This allows the user to access the CAT9532 internal registers sequentially. The content of these bits will rollover to “0000” after the last register is accessed.

Table 1. Internal Registers Selection

B3	B2	B1	B0	Register Name	Type	Register Function
0	0	0	0	INPUT0	READ	Input Register 0
0	0	0	1	INPUT1	READ	Input Register 1
0	0	1	0	PSC0	READ/ WRITE	Frequency Prescaler 0
0	0	1	1	PWM0	READ/ WRITE	PWM Register 0
0	1	0	0	PSC1	READ/ WRITE	Frequency Prescaler 1
0	1	0	1	PWM1	READ/ WRITE	PWM Register 1
0	1	1	0	LS0	READ/ WRITE	LED 0-3 Selector
0	1	1	1	LS1	READ/ WRITE	LED 4-7 Selector
1	0	0	0	LS2	READ/ WRITE	LED 8-11 Selector
1	0	0	1	LS3	READ/ WRITE	LED 12-15 Selector

Figure 4. Acknowledge Timing

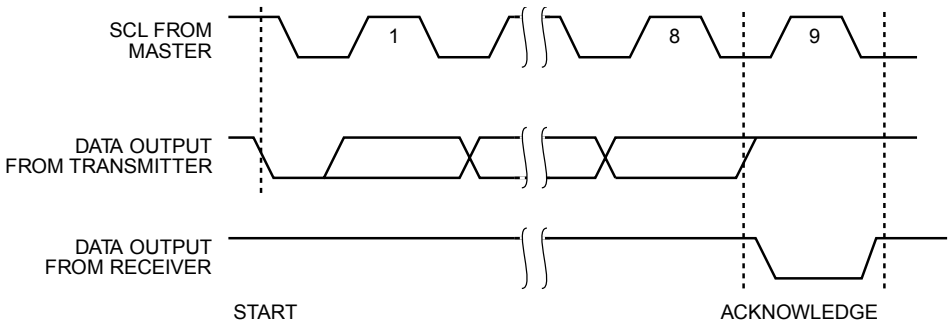
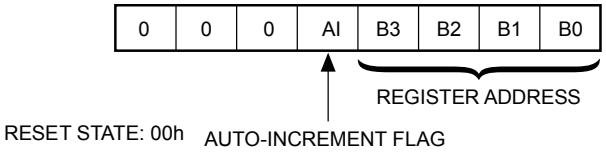


Figure 5. Control Register



© Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

The Input Register 0 and Input Register 1 reflect the incoming logic levels of the I/O pins, regardless of whether the pin is defined as an input or an output. These registers are read only ports. Writes to the input registers will be acknowledged but will have no effect.

Table 2. Input Register 0 and Input Register 1

INPUT0								
	LED 7	LED 6	LED 5	LED 4	LED 3	LED 2	LED 1	LED 0
bit	7	6	5	4	3	2	1	0
default	X	X	X	X	X	X	X	X
INPUT1								
	LED 15	LED 14	LED 13	LED 12	LED 11	LED 10	LED 9	LED 8
bit	7	6	5	4	3	2	1	0
default	X	X	X	X	X	X	X	X

The Frequency Prescaler 0 and Frequency Prescaler 1 registers (PSC0, PSC1) are used to program the period of the pulse width modulated signals BLINK0 and BLINK1 respectively:

T_BLINK0 = (PSC0 + 1) / 152;
T_BLINK1 = (PSC1 + 1) / 152

Table 3. Frequency Prescaler 0 and Frequency Prescaler 1 Registers

PSC0								
bit	7	6	5	4	3	2	1	0
default	0	0	0	0	0	0	0	0
PSC1								
bit	7	6	5	4	3	2	1	0
default	0	0	0	0	0	0	0	0

The PWM Register 0 and PWM Register 1 (PWM0, PWM1) are used to program the duty cycle of BLINK0 and BLINK1 respectively:

Duty Cycle_BLINK0 = PWM0 / 256;
Duty Cycle_BLINK1 = PWM1 / 256

After writing to the PWM0/1 register an 8-bit internal counter starts to count from 0 to 255. The outputs are low (LED on) when the counter value is less than the value programmed into PWM register. The LED is off when the counter value is higher than the value written into PWM register.

Table 4. PWM Register 0 and PWM Register 1

PWM0								
bit	7	6	5	4	3	2	1	0
default	1	0	0	0	0	0	0	0
PWM1								
bit	7	6	5	4	3	2	1	0
default	1	0	0	0	0	0	0	0

Every LED driver output can be programmed to one of four states, LED OFF, LED ON, LED blinks at BLINK0 rate and LED blinks at BLINK1 rate using the LED Selector Registers (Table 5).

Table 5. LED Selector Registers

LS0								
	LED 3		LED 2		LED 1		LED 0	
bit	7	6	5	4	3	2	1	0
default	0	0	0	0	0	0	0	0
LS1								
	LED 7		LED 6		LED 5		LED 4	
bit	7	6	5	4	3	2	1	0
default	0	0	0	0	0	0	0	0
LS2								
	LED 11		LED 10		LED 9		LED 8	
bit	7	6	5	4	3	2	1	0
default	0	0	0	0	0	0	0	0
LS3								
	LED 15		LED 14		LED 13		LED 12	
bit	7	6	5	4	3	2	1	0
default	0	0	0	0	0	0	0	0

The LED output (LED0 to LED15) is set by the 2 bits value from the corresponding LSx Register (x = 0 to 3):

00 = LED Output set Hi-Z (LED Off – Default)
01 = LED Output set LOW (LED On)
10 = LED Output blinks at BLINK0 Rate
11 = LED Output blinks at BLINK1 Rate

Write Operations

Data is transmitted to the CAT9532 registers using the write sequence shown in Figure 6.

If the AI bit from the command byte is set to “1”, the CAT9532 internal registers can be written sequentially. After sending data to one register, the next data byte will be sent to the next register sequentially addressed.

Read Operations

The CAT9532 registers are read according to the timing diagrams shown in Figure 7 and Figure 8. Data from the register, defined by the command byte, will be sent serially on the SDA line.

After the first byte is read, additional data bytes may be read when the auto-increment flag, AI, is set. The additional data byte will reflect the data read from the next register sequentially addressed by the (B3 B2 B1 B0) bits of the command byte.

When reading Input Port Registers (Figure 8), data is clocked into the register on the failing edge of the acknowledge clock pulse. The transfer is stopped when the master will not acknowledge the data byte received and issue the STOP condition.

LED Pins Used as General Purpose I/O

Any LED pins not used to drive LEDs can be used as general purpose input/output, GPIO.

When used as input, the user should program the corresponding LED pin to Hi-Z (“00” for the LSx register bits). The pin state can be read via the Input Register according to the sequence shown in Figure 8.

For use as output, an external pull-up resistor should be connected to the pin. The value of the pull-up resistor is calculated according to the DC operating characteristics. To set the LED output high, the user has to program the output Hi-Z writing “00” into the corresponding LED Selector (LSx) register bits. The output pin is set low when the LED output is programmed low through the LSx register bits (“01” in LSx register bits).

Figure 6. Write to Register Timing Diagram

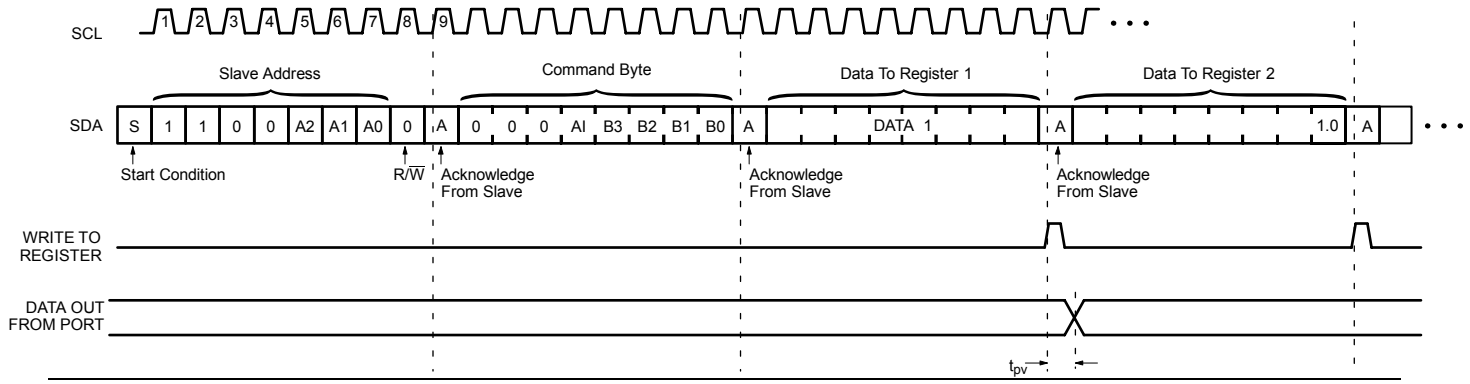
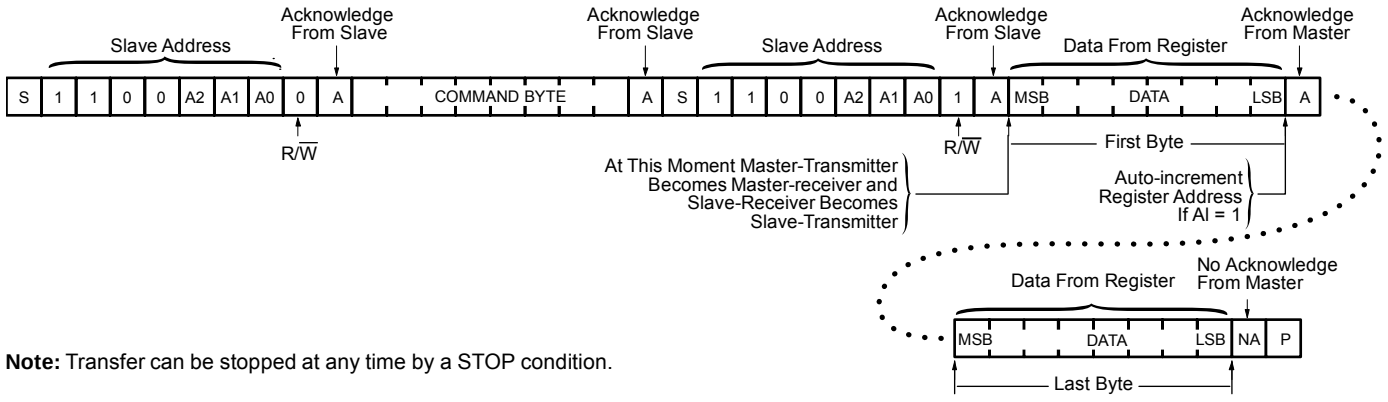


Figure 7. Read from Register Timing Diagram



Note: Transfer can be stopped at any time by a STOP condition.

© Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

External Reset Operation

The CAT9532 registers and the I^2C state machine are initialized to their default state when the RESET input is held low for a minimum of t_W. The external Reset timing is shown in Figure 9.

Power-On Reset Operation

The CAT9532 incorporates Power-On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state. The device is in a reset state for V_{CC} less than the internal POR threshold level (V_{POR}). When V_{CC} exceeds the V_{POR} level, the reset state is released and the CAT9532 internal state machine and registers are initialized to their default state.

Figure 8. Read Input Port Register Timing Diagram

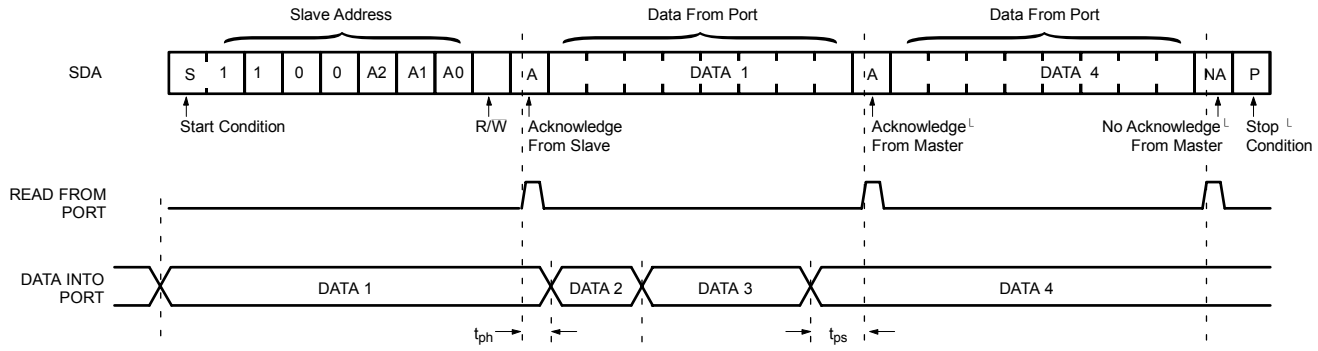
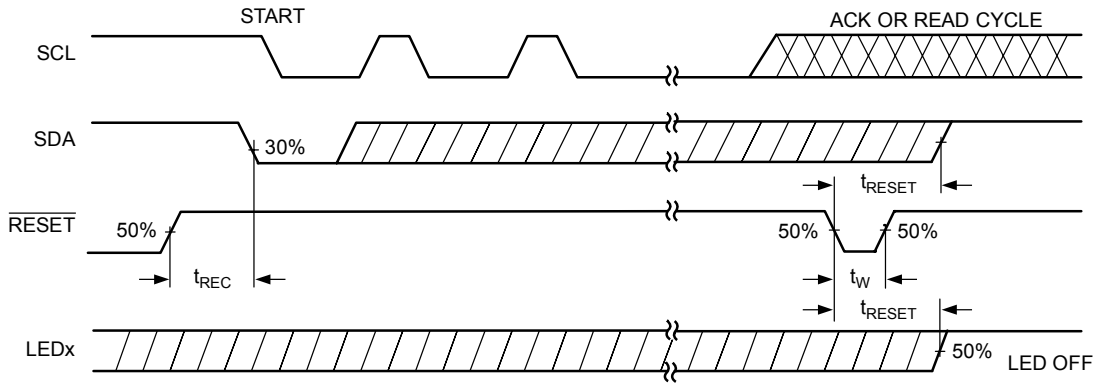


Figure 9. $\overline{\text{RESET}}$ Timing Diagram



APPLICATION INFORMATION

Programming Example

The following programming sequence is an example how to set:

- LED0 to LED3: ON
- LED4 to LED7: Dimming at 30% brightness; Blink 1: 152Hz, duty cycle 30%
- LED8 to LED11: Blink at 2Hz with 50% duty cycle (Blink 2)
- LED12 to LED15: OFF

	Command Description	I²C Data
1	START	
2	Send Slave address, A0-A2 = low	C0h
3	Command Byte: AI="1"; PSC0 Addr	12h
4	Set Blink 1 at 152Hz, T_Blink1 = 1/152 Write PSC0 = 0	00h
5	Set PWM0 duty cycle to 30% PWM0 / 256 = 0.3; Write PWM0=77	4Dh
6	Set Blink 2 at 2Hz, T_Blink1 = 1/2 Write PSC1 = 75	4Bh
7	Set PWM1 duty cycle to 50% PWM1 / 256 = 0.5; Write PWM1=128	80h
8	Write LS0: LED0 to LED3 = ON	55h
9	Write LS1: LED4 to LED7 at Blink1	AAh
10	Write LS2: LED8 to LED11 at Blink2	FFh
11	Write LS3: LED12 to LED15 = OFF	00h
12	STOP	

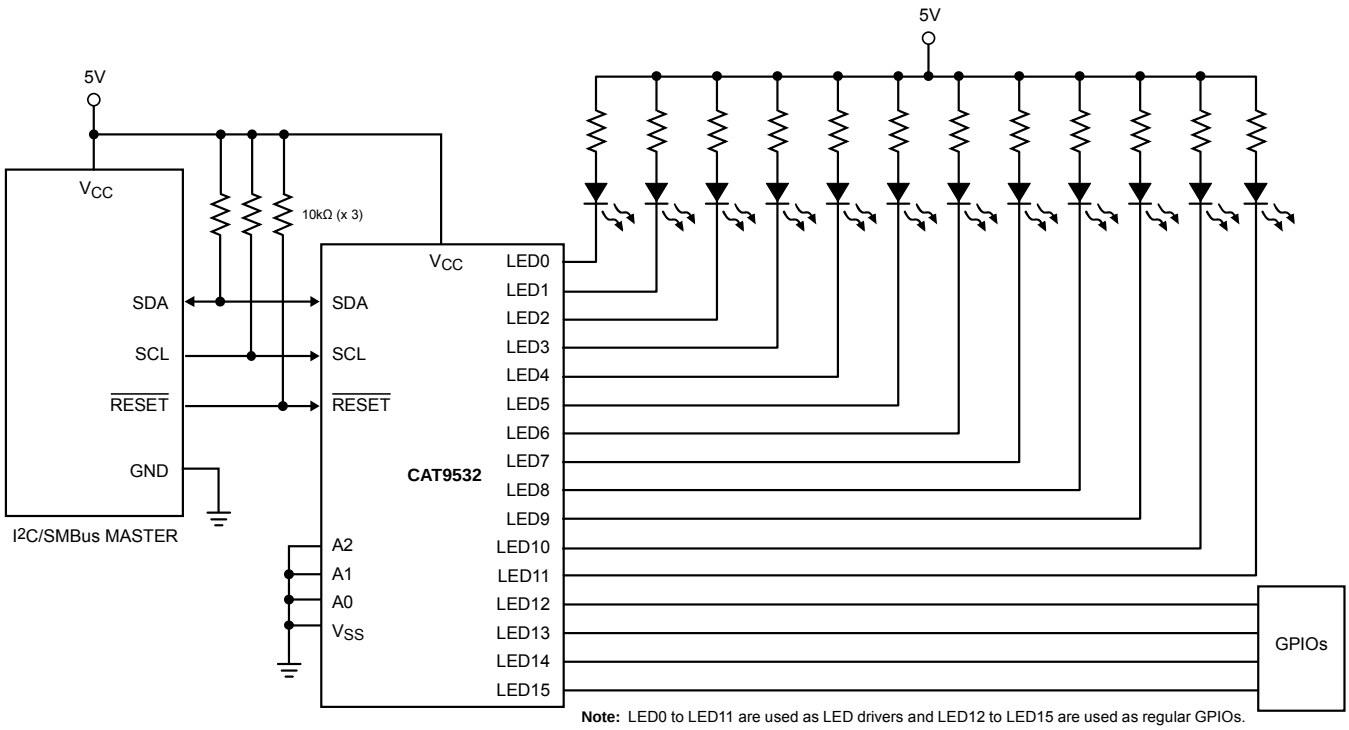
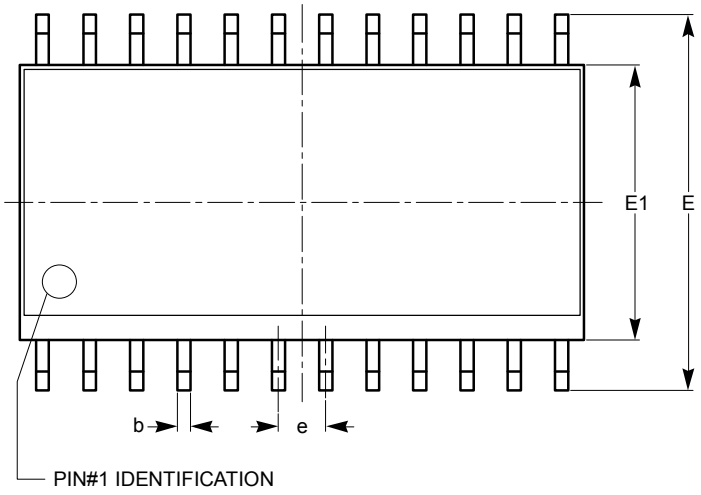


Figure 10. Typical Application

© Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

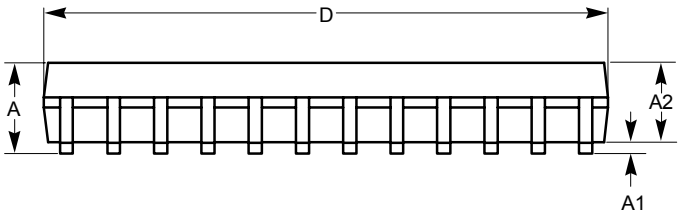
PACKAGE OUTLINE DRAWINGS

SOIC 24-Lead (W)[1][2]

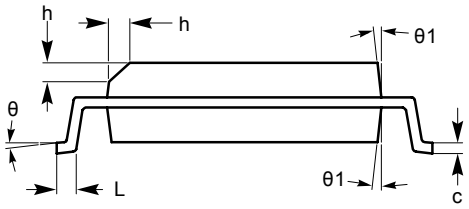


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	2.35		2.65
A1	0.10		0.30
A2	2.05		2.55
b	0.31		0.51
c	0.20		0.33
D	15.20		15.40
E	10.11		10.51
E1	7.34		7.60
e		1.27 BSC	
h	0.25		0.75
L	0.40		1.27
θ	0°		8°
θ1	5°		15°



SIDE VIEW



END VIEW

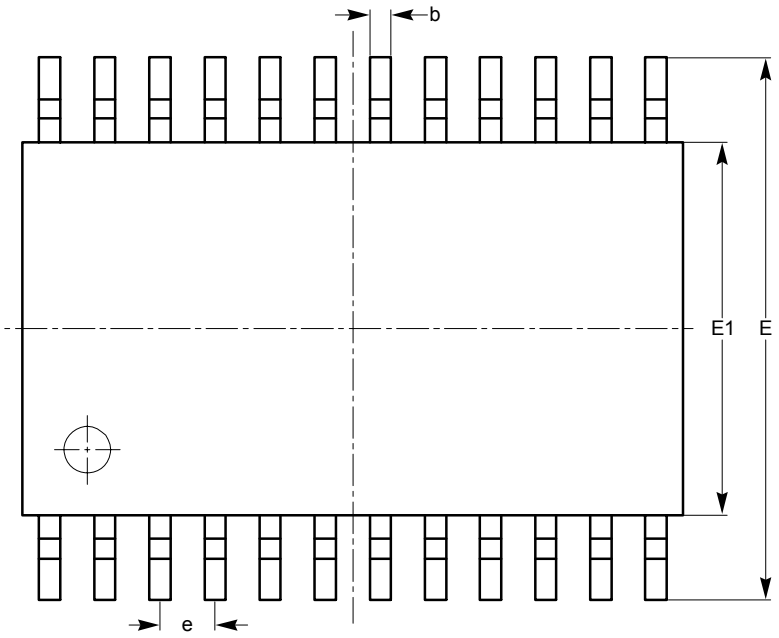
For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:

(1) All dimensions are in millimeters. Angles in degrees.

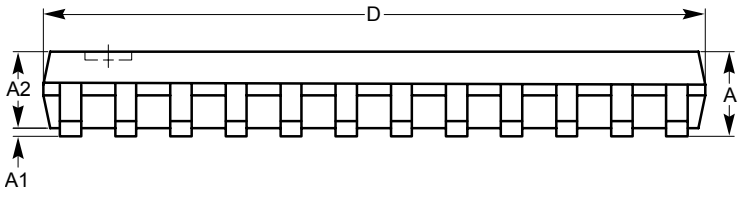
(2) Complies with JEDEC MS-013.

TSSOP 24-Lead 4.4mm (Y)[1][2]

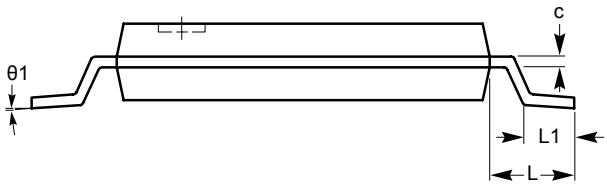


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80		1.05
b	0.19		0.30
c	0.09		0.20
D	7.70	7.80	7.90
E	6.25	6.40	6.55
E1	4.30	4.40	4.50
e		0.65 BSC	
L		1.00 REF	
L1	0.50	0.60	0.70
θ1	0°		8°



SIDE VIEW



END VIEW

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

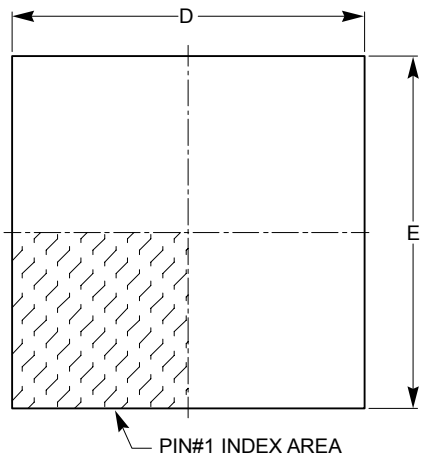
Notes:

(1) All dimensions are in millimeters. Angles in degrees.

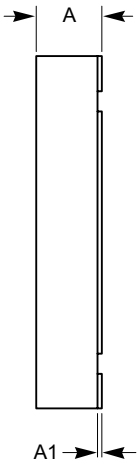
(2) Complies with JEDEC MO-153.

© Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

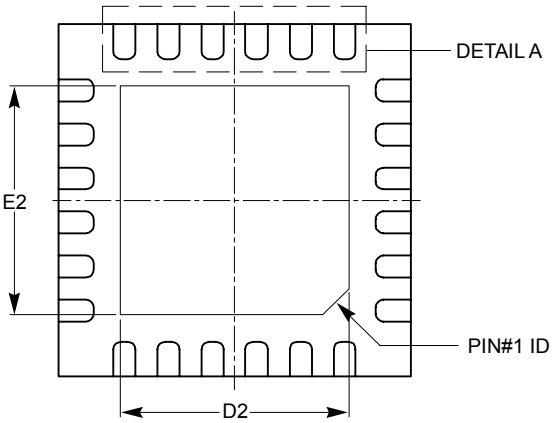
TQFN 24-Lead 4 x 4mm (HV6)[1][2]



TOP VIEW

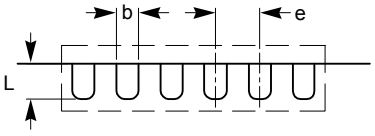


SIDE VIEW

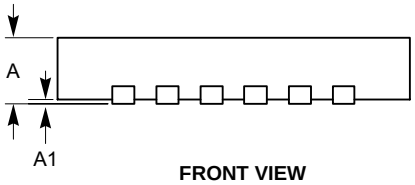


BOTTOM VIEW

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
e		0.50 BSC	
L	0.30	0.40	0.50



DETAIL A



FRONT VIEW

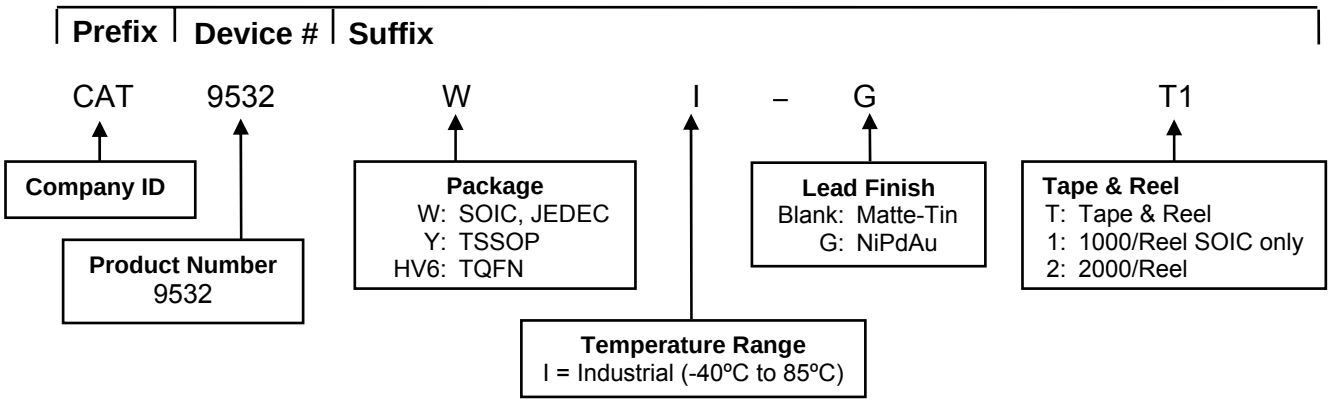
For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:

(1) All dimensions are in millimeters.

(2) Complies with JEDEC MO-220.

EXAMPLE OF ORDERING INFORMATION



ORDERING PART NUMBER

Part Number	Package	Lead Finish
CAT9532WI	SOIC	Matte-Tin
CAT9532WI-T1	SOIC	Matte-Tin
CAT9532YI	TSSOP	Matte-Tin
CAT9532YI-T2	TSSOP	Matte-Tin
CAT9532HV6I	TQFN	Matte-Tin (5)
CAT9532HV6I-T2	TQFN	Matte-Tin (5)
CAT9532HV6I-G	TQFN	NiPdAu
CAT9532HV6I-GT2	TQFN	NiPdAu

Notes:

(1) All packages are RoHS-compliant (Lead-free, Halogen-free).

(2) The standard plated finish is Matte-Tin for SOIC and TSSOP packages. The standard plated finish is NiPdAu for TQFN package.

(3) The device used in the above example is a CAT9532WI-T1 (SOIC, Industrial Temperature, Matte-Tin, Tape & Reel).

(4) For additional temperature options, please contact your nearest Catalyst Semiconductor Sales office.

(5) For package availability, please contact your nearest Catalyst Semiconductor Sales office.

© Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

REVISION HISTORY

Date	Rev.	Reason
10/23/07	A	Initial Issue
12/07/07	B	Update Example of Ordering Information and Ordering Part Number

Copyrights, Trademarks and Patents

© Catalyst Semiconductor, Inc.

Trademarks and registered trademarks of Catalyst Semiconductor include each of the following:
Adaptive Analog™, Beyond Memory™, DPP™, EZDim™, LDD™, MiniPot™, Quad-Mode™ and Quantum Charge Programmable™

Catalyst Semiconductor has been issued U.S. and foreign patents and has patent applications pending that protect its products.

CATALYST SEMICONDUCTOR MAKES NO WARRANTY, REPRESENTATION OR GUARANTEE, EXPRESS OR IMPLIED, REGARDING THE SUITABILITY OF ITS PRODUCTS FOR ANY PARTICULAR PURPOSE, NOR THAT THE USE OF ITS PRODUCTS WILL NOT INFRINGE ITS INTELLECTUAL PROPERTY RIGHTS OR THE RIGHTS OF THIRD PARTIES WITH RESPECT TO ANY PARTICULAR USE OR APPLICATION AND SPECIFICALLY DISCLAIMS ANY AND ALL LIABILITY ARISING OUT OF ANY SUCH USE OR APPLICATION, INCLUDING BUT NOT LIMITED TO, CONSEQUENTIAL OR INCIDENTAL DAMAGES.

Catalyst Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Catalyst Semiconductor product could create a situation where personal injury or death may occur.

Catalyst Semiconductor reserves the right to make changes to or discontinue any product or service described herein without notice. Products with data sheets labeled "Advance Information" or "Preliminary" and other products described herein may not be in production or offered for sale.

Catalyst Semiconductor advises customers to obtain the current version of the relevant product information before placing orders. Circuit diagrams illustrate typical semiconductor applications and may not be complete.

Catalyst Semiconductor, Inc.
Corporate Headquarters
2975 Stender Way
Santa Clara, CA 95054
Phone: 408.542.1000
Fax: 408.542.1200
www.catsemi.com

Document No: MD-9001
Revision: B
Issue date: 12/07/07