S-1009 Series

SUPER-LOW CURRENT CONSUMPTION SUPER HIGH-ACCURACY VOLTAGE DETECTOR WITH DELAY CIRCUIT (EXTERNAL DELAY TIME SETTING)

www.sii-ic.com

Rev.4.2_00

The S-1009 Series is a super high-accuracy voltage detector developed using CMOS process. The detection voltage is fixed internally with an accuracy of ±0.5%. It operates with super low current consumption of 270 nA typ.
The release signal can be delayed by setting a capacitor externally. Delay time accuracy is ±15%. Two output forms Nch open drain and CMOS output are available.
Compared with conventional CMOS voltage detectors, the S-1009 Series is the most suitable for the portable devices due to the super-low current consumption, super high-accuracy and small packages.

■ Features

- Super-low current consumption 270 nA typ. (1.2 V ≤ $-V_{DET}$ < 2.3 V)
- Super high-accuracy detection voltage ±0.5% (2.4 V ≤ $-V_{DET}$ ≤ 4.6 V)
  ±12 mV (0.8 V ≤ $-V_{DET}$ < 2.4 V)
- Operating voltage range 0.6 V to 10.0 V (CMOS output products)
- Hysteresis characteristics 5% ±1%
- Delay time accuracy ±15% (C_D = 4.7 nF)
- Detection voltage 0.8 V to 4.6 V (0.1 V step)
- Output form Nch open drain output (Active “L”)
  CMOS output (Active “L”)
- Lead-free (Sn 100%), halogen-free*1

***1.** Refer to “■ **Product Name Structure**” for details.

■ Applications

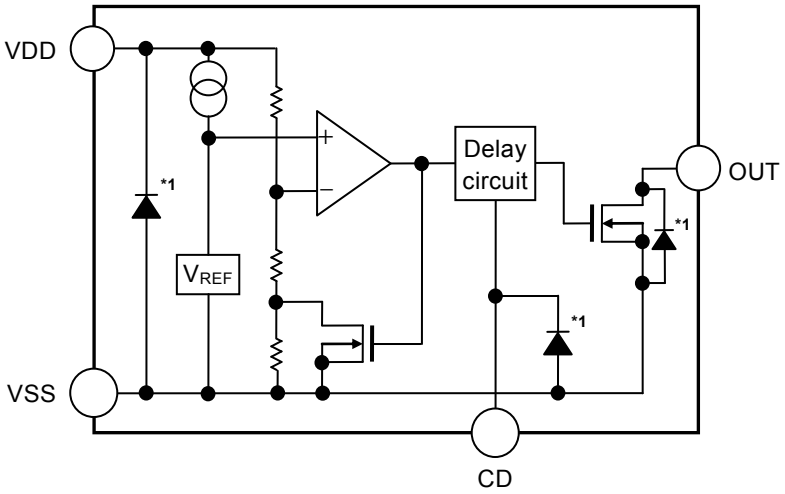
- Power monitor and reset for CPUs and microcomputers
- Constant voltage power monitor for TVs, DVD recorders and home appliances
- Power supply monitor for portable devices such as notebook PCs, digital still cameras and mobile phones

■ Packages

- SC-82AB
- SOT-23-5

■ Block Diagrams

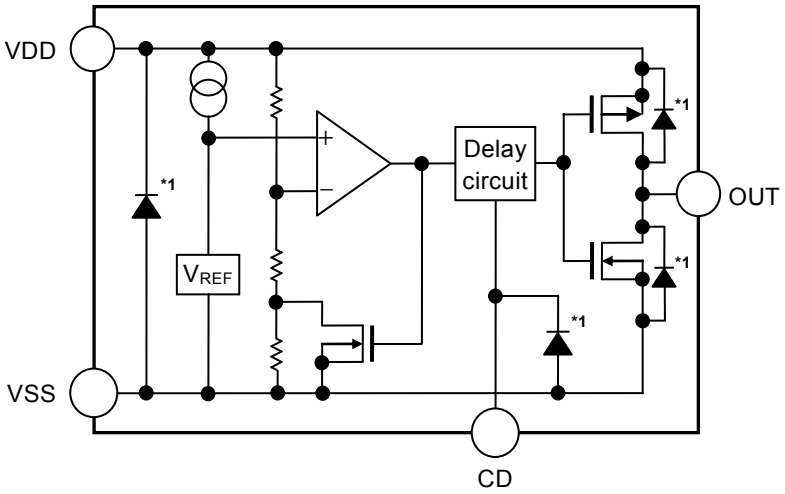
1. Nch open drain output products



***1.** Parasitic diode

Figure 1

2. CMOS output products



***1.** Parasitic diode

Figure 2

■ Product Name Structure

Users can select the detection voltage value, output form, and package type for the S-1009 Series. Refer to "**1. Product name**" regarding the contents of product name, "**2. Packages**" regarding the package drawings and "**3. Product name list**" regarding details of product name.

1. Product name

S-1009 x xx I – xxxx U

Environmental code
- U: Lead-free (Sn 100%), halogen-free

Package abbreviation and IC packing specifications[*1]
- M4T1: SC-82AB, Tape
- M5T1: SOT-23-5, Tape

Detection voltage value
- 08 to 46
- (e.g., when the detection voltage is 1.5 V, it is expressed as 15.)

Output form
- N: Nch open drain output (Active "L")
- C: CMOS output (Active "L")

***1.** Refer to the tape specifications.

2. Packages

Package name	Drawing code		
	Package	Tape	Reel
SC-82AB	NP004-A-P-SD	NP004-A-C-SD NP004-A-C-S1	NP004-A-R-SD
SOT-23-5	MP005-A-P-SD	MP005-A-C-SD	MP005-A-R-SD

3. Product name list

3. 1 Nch open drain output products

Table 1

Detection voltage	SC-82AB	SOT-23-5
0.8 V ± 12 mV	S-1009N08I-N4T1U	S-1009N08I-M5T1U
0.9 V ± 12 mV	S-1009N09I-N4T1U	S-1009N09I-M5T1U
1.0 V ± 12 mV	S-1009N10I-N4T1U	S-1009N10I-M5T1U
1.1 V ± 12 mV	S-1009N11I-N4T1U	S-1009N11I-M5T1U
1.2 V ± 12 mV	S-1009N12I-N4T1U	S-1009N12I-M5T1U
1.3 V ± 12 mV	S-1009N13I-N4T1U	S-1009N13I-M5T1U
1.4 V ± 12 mV	S-1009N14I-N4T1U	S-1009N14I-M5T1U
1.5 V ± 12 mV	S-1009N15I-N4T1U	S-1009N15I-M5T1U
1.6 V ± 12 mV	S-1009N16I-N4T1U	S-1009N16I-M5T1U
1.7 V ± 12 mV	S-1009N17I-N4T1U	S-1009N17I-M5T1U
1.8 V ± 12 mV	S-1009N18I-N4T1U	S-1009N18I-M5T1U
1.9 V ± 12 mV	S-1009N19I-N4T1U	S-1009N19I-M5T1U
2.0 V ± 12 mV	S-1009N20I-N4T1U	S-1009N20I-M5T1U
2.1 V ± 12 mV	S-1009N21I-N4T1U	S-1009N21I-M5T1U
2.2 V ± 12 mV	S-1009N22I-N4T1U	S-1009N22I-M5T1U
2.3 V ± 12 mV	S-1009N23I-N4T1U	S-1009N23I-M5T1U
2.4 V ± 0.5%	S-1009N24I-N4T1U	S-1009N24I-M5T1U
2.5 V ± 0.5%	S-1009N25I-N4T1U	S-1009N25I-M5T1U
2.6 V ± 0.5%	S-1009N26I-N4T1U	S-1009N26I-M5T1U
2.7 V ± 0.5%	S-1009N27I-N4T1U	S-1009N27I-M5T1U
2.8 V ± 0.5%	S-1009N28I-N4T1U	S-1009N28I-M5T1U
2.9 V ± 0.5%	S-1009N29I-N4T1U	S-1009N29I-M5T1U
3.0 V ± 0.5%	S-1009N30I-N4T1U	S-1009N30I-M5T1U
3.1 V ± 0.5%	S-1009N31I-N4T1U	S-1009N31I-M5T1U
3.2 V ± 0.5%	S-1009N32I-N4T1U	S-1009N32I-M5T1U
3.3 V ± 0.5%	S-1009N33I-N4T1U	S-1009N33I-M5T1U
3.4 V ± 0.5%	S-1009N34I-N4T1U	S-1009N34I-M5T1U
3.5 V ± 0.5%	S-1009N35I-N4T1U	S-1009N35I-M5T1U
3.6 V ± 0.5%	S-1009N36I-N4T1U	S-1009N36I-M5T1U
3.7 V ± 0.5%	S-1009N37I-N4T1U	S-1009N37I-M5T1U
3.8 V ± 0.5%	S-1009N38I-N4T1U	S-1009N38I-M5T1U
3.9 V ± 0.5%	S-1009N39I-N4T1U	S-1009N39I-M5T1U
4.0 V ± 0.5%	S-1009N40I-N4T1U	S-1009N40I-M5T1U
4.1 V ± 0.5%	S-1009N41I-N4T1U	S-1009N41I-M5T1U
4.2 V ± 0.5%	S-1009N42I-N4T1U	S-1009N42I-M5T1U
4.3 V ± 0.5%	S-1009N43I-N4T1U	S-1009N43I-M5T1U
4.4 V ± 0.5%	S-1009N44I-N4T1U	S-1009N44I-M5T1U
4.5 V ± 0.5%	S-1009N45I-N4T1U	S-1009N45I-M5T1U
4.6 V ± 0.5%	S-1009N46I-N4T1U	S-1009N46I-M5T1U

3. 2 CMOS output products

Table 2

Detection voltage	SC-82AB	SOT-23-5
0.8 V ± 12 mV	S-1009C08I-N4T1U	S-1009C08I-M5T1U
0.9 V ± 12 mV	S-1009C09I-N4T1U	S-1009C09I-M5T1U
1.0 V ± 12 mV	S-1009C10I-N4T1U	S-1009C10I-M5T1U
1.1 V ± 12 mV	S-1009C11I-N4T1U	S-1009C11I-M5T1U
1.2 V ± 12 mV	S-1009C12I-N4T1U	S-1009C12I-M5T1U
1.3 V ± 12 mV	S-1009C13I-N4T1U	S-1009C13I-M5T1U
1.4 V ± 12 mV	S-1009C14I-N4T1U	S-1009C14I-M5T1U
1.5 V ± 12 mV	S-1009C15I-N4T1U	S-1009C15I-M5T1U
1.6 V ± 12 mV	S-1009C16I-N4T1U	S-1009C16I-M5T1U
1.7 V ± 12 mV	S-1009C17I-N4T1U	S-1009C17I-M5T1U
1.8 V ± 12 mV	S-1009C18I-N4T1U	S-1009C18I-M5T1U
1.9 V ± 12 mV	S-1009C19I-N4T1U	S-1009C19I-M5T1U
2.0 V ± 12 mV	S-1009C20I-N4T1U	S-1009C20I-M5T1U
2.1 V ± 12 mV	S-1009C21I-N4T1U	S-1009C21I-M5T1U
2.2 V ± 12 mV	S-1009C22I-N4T1U	S-1009C22I-M5T1U
2.3 V ± 12 mV	S-1009C23I-N4T1U	S-1009C23I-M5T1U
2.4 V ± 0.5%	S-1009C24I-N4T1U	S-1009C24I-M5T1U
2.5 V ± 0.5%	S-1009C25I-N4T1U	S-1009C25I-M5T1U
2.6 V ± 0.5%	S-1009C26I-N4T1U	S-1009C26I-M5T1U
2.7 V ± 0.5%	S-1009C27I-N4T1U	S-1009C27I-M5T1U
2.8 V ± 0.5%	S-1009C28I-N4T1U	S-1009C28I-M5T1U
2.9 V ± 0.5%	S-1009C29I-N4T1U	S-1009C29I-M5T1U
3.0 V ± 0.5%	S-1009C30I-N4T1U	S-1009C30I-M5T1U
3.1 V ± 0.5%	S-1009C31I-N4T1U	S-1009C31I-M5T1U
3.2 V ± 0.5%	S-1009C32I-N4T1U	S-1009C32I-M5T1U
3.3 V ± 0.5%	S-1009C33I-N4T1U	S-1009C33I-M5T1U
3.4 V ± 0.5%	S-1009C34I-N4T1U	S-1009C34I-M5T1U
3.5 V ± 0.5%	S-1009C35I-N4T1U	S-1009C35I-M5T1U
3.6 V ± 0.5%	S-1009C36I-N4T1U	S-1009C36I-M5T1U
3.7 V ± 0.5%	S-1009C37I-N4T1U	S-1009C37I-M5T1U
3.8 V ± 0.5%	S-1009C38I-N4T1U	S-1009C38I-M5T1U
3.9 V ± 0.5%	S-1009C39I-N4T1U	S-1009C39I-M5T1U
4.0 V ± 0.5%	S-1009C40I-N4T1U	S-1009C40I-M5T1U
4.1 V ± 0.5%	S-1009C41I-N4T1U	S-1009C41I-M5T1U
4.2 V ± 0.5%	S-1009C42I-N4T1U	S-1009C42I-M5T1U
4.3 V ± 0.5%	S-1009C43I-N4T1U	S-1009C43I-M5T1U
4.4 V ± 0.5%	S-1009C44I-N4T1U	S-1009C44I-M5T1U
4.5 V ± 0.5%	S-1009C45I-N4T1U	S-1009C45I-M5T1U
4.6 V ± 0.5%	S-1009C46I-N4T1U	S-1009C46I-M5T1U

■ Pin Configurations

1. SC-82AB

SC-82AB
Top view

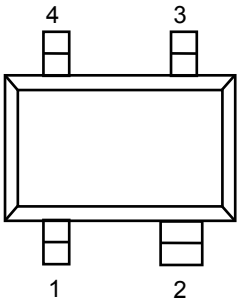


Figure 3

Table 3

Pin No.	Symbol	Description
1	VSS	GND pin
2	VDD	Input voltage pin
3	CD	Connection pin for delay capacitor
4	OUT	Voltage detection output pin

2. SOT-23-5

SOT-23-5
Top view

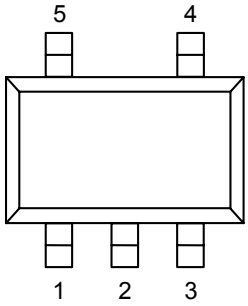


Figure 4

Table 4

Pin No.	Symbol	Description
1	OUT	Voltage detection output pin
2	VDD	Input voltage pin
3	VSS	GND pin
4	NC*1	No connection
5	CD	Connection pin for delay capacitor

***1.** The NC pin is electrically open.
The NC pin can be connected to VDD or VSS.

■ Absolute Maximum Ratings

Table 5

(Ta = +25°C unless otherwise specified)

Item			Symbol	Absolute Maximum Rating	Unit
Power supply voltage			V_{DD}–V_{SS}	12	V
CD pin input voltage			V_{CD}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Output voltage	Nch open drain output products		V_{OUT}	V_{SS} – 0.3 to 12.0	V
	CMOS output products			V_{SS} – 0.3 to V_{DD} + 0.3	V
Output current			I_{OUT}	50	mA
Power dissipation		SC-82AB	P_D	350[*1]	mW
		SOT-23-5		600[*1]	mW
Operating ambient temperature			T_{opr}	–40 to +85	°C
Storage temperature			T_{stg}	–40 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

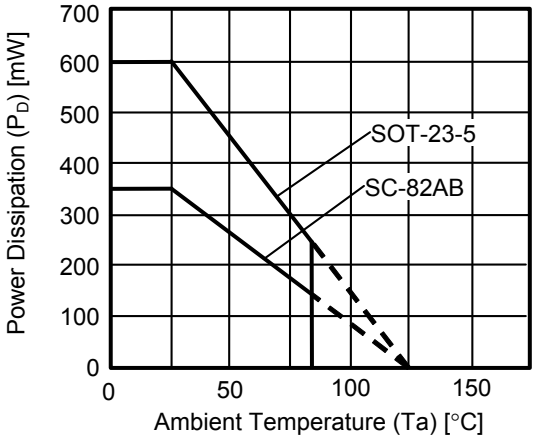


Figure 5 Power Dissipation of Package

■ Electrical Characteristics

1. Nch open drain output products

Table 6

(Ta = +25°C unless otherwise specified)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage[*1]	$-V_{DET}$	0.8 V ≤ $-V_{DET}$ < 2.4 V		$-V_{DET(S)}$ − 0.012	$-V_{DET(S)}$	$-V_{DET(S)}$ + 0.012	V	1
		2.4 V ≤ $-V_{DET}$ ≤ 4.6 V		$-V_{DET(S)}$ × 0.995	$-V_{DET(S)}$	$-V_{DET(S)}$ × 1.005	V	1
Hysteresis width	V_{HYS}	–		$-V_{DET}$ × 0.04	$-V_{DET}$ × 0.05	$-V_{DET}$ × 0.06	V	1
Current consumption	I_{SS}	V_{DD} = +V_{DET} + 0.6 V	0.8 V ≤ $-V_{DET}$ < 1.2 V	–	0.30	0.90	µA	2
			1.2 V ≤ $-V_{DET}$ < 2.3 V	–	0.27	0.90	µA	2
			2.3 V ≤ $-V_{DET}$ < 3.6 V	–	0.42	0.90	µA	2
			3.6 V ≤ $-V_{DET}$ ≤ 4.6 V	–	0.39	0.90	µA	2
Operating voltage	V_{DD}	–		0.7	–	10.0	V	1
Output current	I_{OUT}	Output transistor, Nch, V_{DS} = 0.5 V	V_{DD} = 0.7 V S-1009N08 to 14	0.14	0.40	–	mA	3
			V_{DD} = 1.2 V S-1009N15 to 46	0.73	1.33	–	mA	3
			V_{DD} = 2.4 V S-1009N27 to 46	1.47	2.39	–	mA	3
Leakage current	I_{LEAK}	Output transistor, Nch, V_{DD} = 10.0 V, V_{OUT} = 10.0 V		–	–	0.08	µA	3
Delay time	t_D	C_D = 4.7 nF		22.1	26.0	29.9	ms	4
Detection voltage temperature coefficient[*2]	$\frac{\Delta -V_{DET}}{\Delta Ta \bullet -V_{DET}}$	Ta = –40°C to +85°C	0.8 V ≤ $-V_{DET}$ < 0.9 V	–	±180	±430	ppm/°C	1
			0.9 V ≤ $-V_{DET}$ < 1.2 V	–	±120	±370	ppm/°C	1
			1.2 V ≤ $-V_{DET}$ ≤ 4.6 V	–	±100	±350	ppm/°C	1

***1.** $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Specified detection voltage value (The center value of the detection voltage range in **Table 1**.)

***2.** The temperature change of the detection voltage [mV/°C] is calculated by using the following equation.

$$\frac{\Delta - V_{DET}}{\Delta Ta}[\text{mV/°C}]^{*1} = -V_{DET(S)}(\text{typ.})[\text{V}]^{*2} \times \frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}}[\text{ppm/°C}]^{*3} \div 1000$$

***1.** Temperature change of the detection voltage
***2.** Specified detection voltage
***3.** Detection voltage temperature coefficient

2. CMOS output products

Table 7

(Ta = +25°C unless otherwise specified)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage*1	$-V_{DET}$	0.8 V ≤ $-V_{DET}$ < 2.4 V		$-V_{DET(S)} - 0.012$	$-V_{DET(S)}$	$-V_{DET(S)} + 0.012$	V	1
		2.4 V ≤ $-V_{DET}$ ≤ 4.6 V		$-V_{DET(S)} \times 0.995$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.005$	V	1
Hysteresis width	V_{HYS}	–		$-V_{DET} \times 0.04$	$-V_{DET} \times 0.05$	$-V_{DET} \times 0.06$	V	1
Current consumption	I_{SS}	V_{DD} = $+V_{DET}$ + 0.6 V	0.8 V ≤ $-V_{DET}$ < 1.2 V	–	0.30	0.90	µA	2
			1.2 V ≤ $-V_{DET}$ < 2.3 V	–	0.27	0.90	µA	2
			2.3 V ≤ $-V_{DET}$ < 3.6 V	–	0.42	0.90	µA	2
			3.6 V ≤ $-V_{DET}$ ≤ 4.6 V	–	0.39	0.90	µA	2
Operating voltage	V_{DD}	–		0.6	–	10.0	V	1
Output current	I_{OUT}	Output transistor, Nch, V_{DS} = 0.5 V	V_{DD} = 0.7 V S-1009C08 to 14	0.14	0.40	–	mA	3
			V_{DD} = 1.2 V S-1009C15 to 46	0.73	1.33	–	mA	3
			V_{DD} = 2.4 V S-1009C27 to 46	1.47	2.39	–	mA	3
		Output transistor, Pch, V_{DS} = 0.5 V	V_{DD} = 4.8 V S-1009C08 to 39	1.62	2.60	–	mA	5
			V_{DD} = 6.0 V S-1009C40 to 46	1.78	2.86	–	mA	5
Delay time	t_D	C_D = 4.7 nF		22.1	26.0	29.9	ms	4
Detection voltage temperature coefficient*2	$\frac{\Delta -V_{DET}}{\Delta Ta \bullet -V_{DET}}$	Ta = –40°C to +85°C	0.8 V ≤ $-V_{DET}$ < 0.9 V	–	±180	±430	ppm/°C	1
			0.9 V ≤ $-V_{DET}$ < 1.2 V	–	±120	±370	ppm/°C	1
			1.2 V ≤ $-V_{DET}$ ≤ 4.6 V	–	±100	±350	ppm/°C	1

***1.** $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Specified detection voltage value (The center value of the detection voltage range in **Table 2**.)

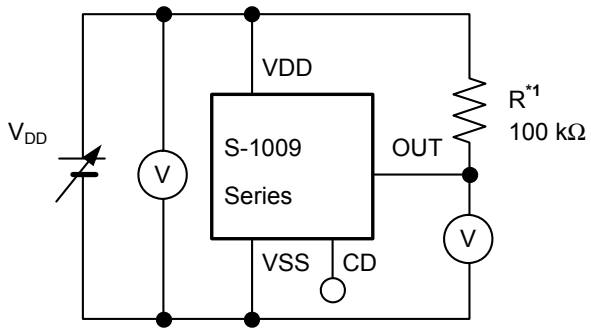
***2.** The temperature change of the detection voltage [mV/°C] is calculated by using the following equation.

$$\frac{\Delta - V_{DET}}{\Delta Ta}[\text{mV/°C}]^{*1} = -V_{DET(S)}(\text{typ.})[\text{V}]^{*2} \times \frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}}[\text{ppm/°C}]^{*3} \div 1000$$

***1.** Temperature change of the detection voltage
***2.** Specified detection voltage
***3.** Detection voltage temperature coefficient

■ Test Circuits

1.



***1.** R is unnecessary for CMOS output products.

Figure 6

2.

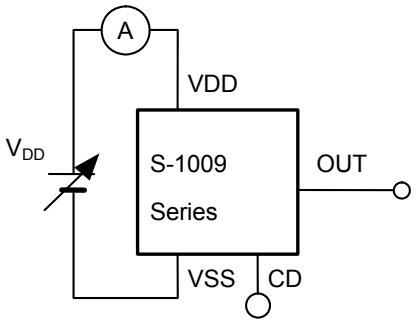
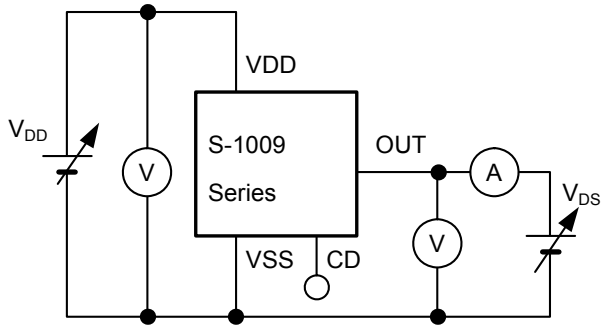


Figure 7

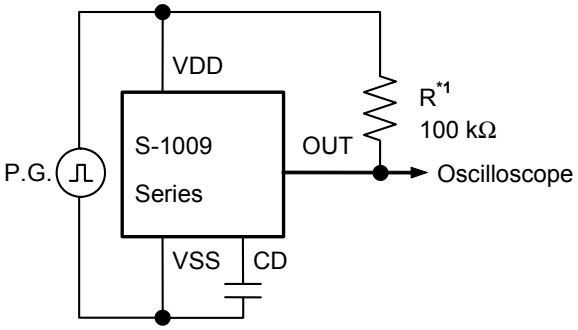
3.



***1.** R is unnecessary for CMOS output products.

Figure 8

4.



***1.** R is unnecessary for CMOS output products.

Figure 9

5.

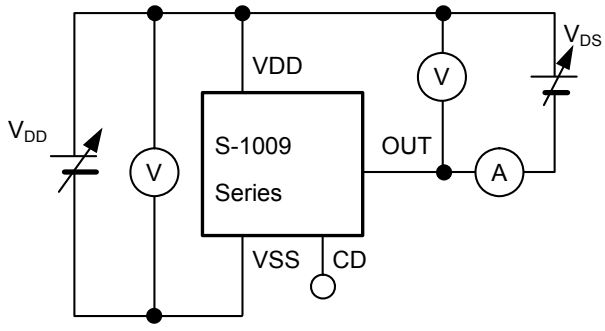


Figure 10

■ Timing Chart

1. Nch open drain output products

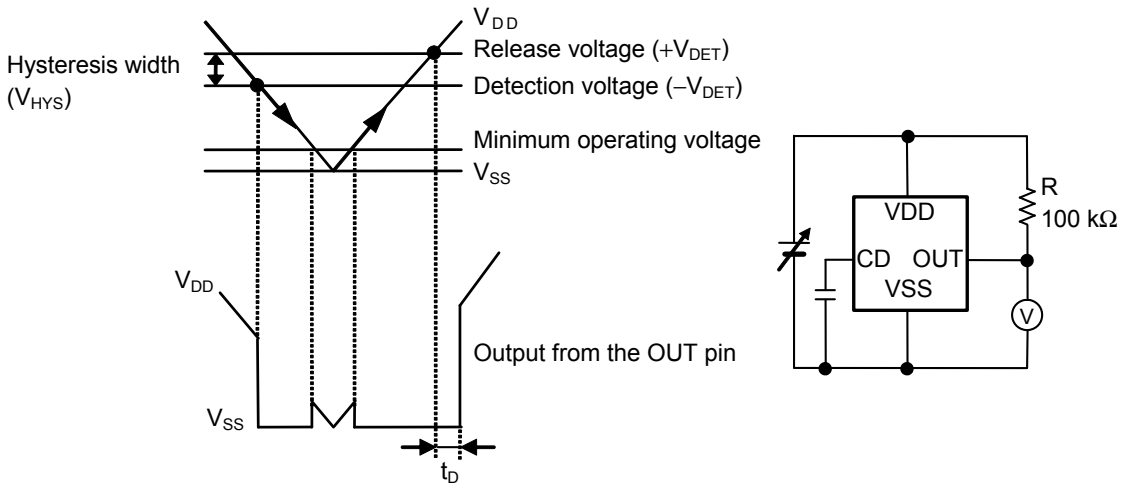
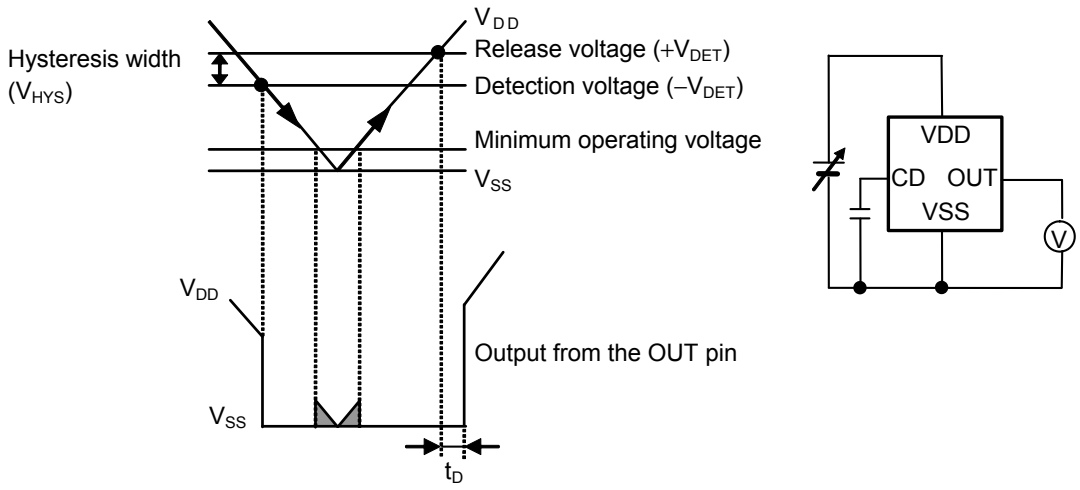


Figure 11

2. CMOS output products



Remark When V_{DD} is the minimum operating voltage or less, the output voltage from the OUT pin is indefinite in the shaded area.

Figure 12

■ Operation

1. Basic operation: CMOS output (Active "L")

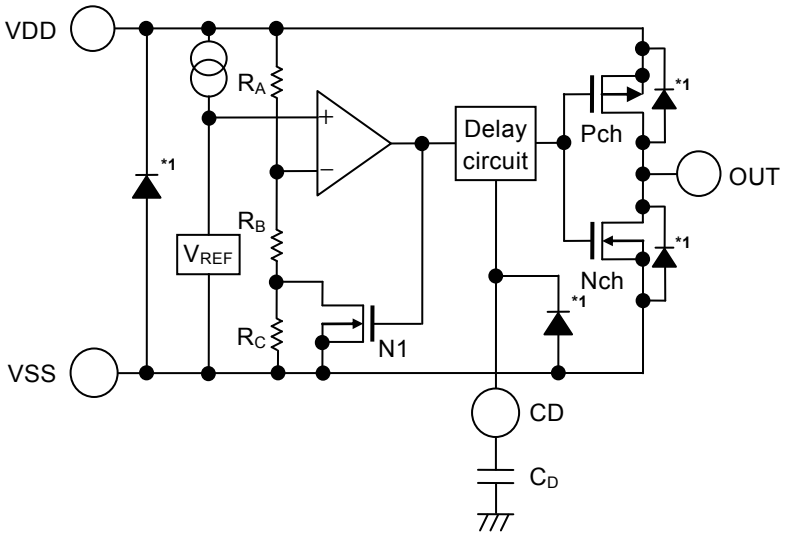
(1) When the power supply voltage (V_{DD}) is the release voltage ($+V_{DET}$) or more, the Nch transistor is OFF and the Pch transistor is ON to output V_{DD} ("H"). Since the Nch transistor N1 in **Figure 13** is OFF, the comparator input voltage is $\frac{(R_B + R_C) \bullet V_{DD}}{R_A + R_B + R_C}$.

(2) Although V_{DD} decreases to $+V_{DET}$ or less, the output is V_{DD} when V_{DD} is the detection voltage ($-V_{DET}$) or more. When V_{DD} decreases to $-V_{DET}$ or less (A in **Figure 14**), the Nch transistor is ON and the Pch transistor is OFF so that V_{SS} is output. The Nch transistor N1 in **Figure 13** is turned on, and the input voltage to the comparator is $\frac{R_B \bullet V_{DD}}{R_A + R_B}$.

(3) The output is indefinite by decreasing V_{DD} to the IC's minimum operating voltage or less. If the output is pulled up, it will be V_{DD}.

(4) V_{SS} is output by increasing V_{DD} to the minimum operating voltage or more. Although V_{DD} exceeds $-V_{DET}$ and V_{DD} is less than $+V_{DET}$, the output is V_{SS}.

(5) When increasing V_{DD} to $+V_{DET}$ or more (B in **Figure 14**), the Nch transistor is OFF and the Pch transistor is ON so that V_{DD} is output. V_{DD} output to the OUT pin delays in t_D by the delay circuit.



***1.** Parasiteic diode

Figure 13 Operation 1

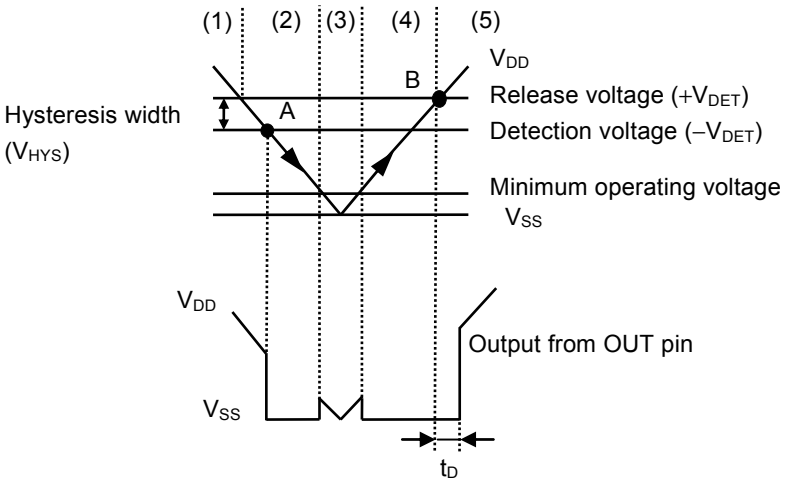


Figure 14 Operation 2

2. Delay Circuit

The delay circuit delays the output signal to the OUT pin from the time at which the power voltage (V_{DD}) exceeds the release voltage ($+V_{DET}$) when V_{DD} is turned on. The output signal is not delayed when V_{DD} decreases to the detection voltage ($-V_{DET}$) or less (Refer to **Figure 14**).

The delay time (t_D) is determined by the time constant of the built-in constant current (approx. 100 nA) and the attached external capacitor (C_D), or the delay time (t_{D0}) when the CD pin is open, and calculated from the following equation.

$$t_D \text{ [ms]} = \text{Delay coefficient} \times C_D \text{ [nF]} + t_{D0} \text{ [ms]}$$

Delay coefficient (+85°C) : Min. 2.82, Typ. 4.20, Max. 5.72
Delay coefficient (+25°C) : Min. 4.70, Typ. 5.47, Max. 6.24
Delay coefficient (–40°C) : Min. 5.64, Typ. 8.40, Max. 12.01

t_{D0} (–40°C to +85°C) : Min. 0.01 ms, Typ. 0.10 ms, Max. 0.24 ms

When the C_D value is sufficiently large, the t_{D0} value can be disregarded.

Caution 1. When the CD pin is open, a double pulse shown in Figure 15 may appear at release. To avoid the double pulse, attach 100 pF or larger capacitor to the CD pin. Do not apply voltage to the CD pin from the exterior.

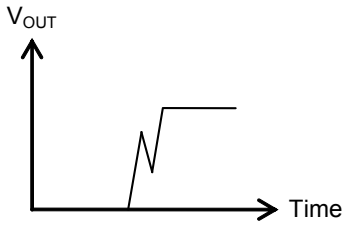


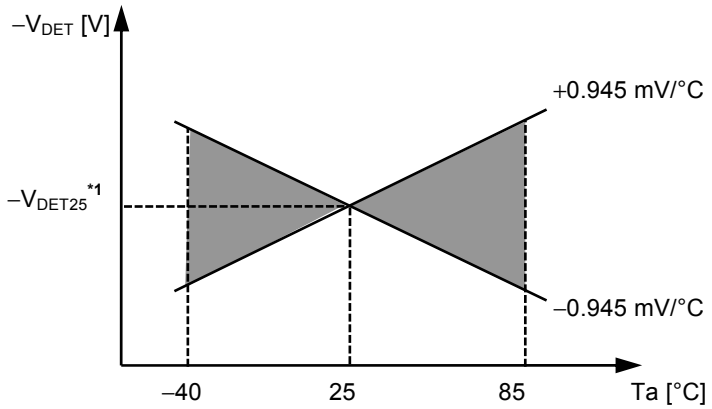
Figure 15

2. **Print circuit board layout should be made in such a way that no current flows into or flows from the CD pin since the impedance of the CD pin is high, otherwise correct delay time cannot be provided.**
3. **There is no limit for the capacitance of the external capacitor (C_D) as long as the leakage current of the capacitor can be ignored against the built-in constant current value. Leakage current causes deviation in delay time. When the leakage current is larger than the built-in constant current, no release takes place.**

3. Other characteristics

3. 1 Temperature characteristics of detection voltage

The shaded area in **Figure 16** shows the temperature characteristics of the detection voltage in the operating temperature range.



***1.** $-V_{DET25}$ is an actual detection voltage value at +25°C.

Figure 16 Temperature characteristics of detection voltage (Example for $-V_{DET}$ = 2.7 V)

3. 2 Temperature characteristics of release voltage

The temperature change $\frac{\Delta + V_{DET}}{\Delta Ta}$ of the release voltage is calculated by using the temperature change $\frac{\Delta - V_{DET}}{\Delta Ta}$ of the detection voltage as follows:

$$\frac{\Delta + V_{DET}}{\Delta Ta} = \frac{+V_{DET}}{-V_{DET}} \times \frac{\Delta - V_{DET}}{\Delta Ta}$$

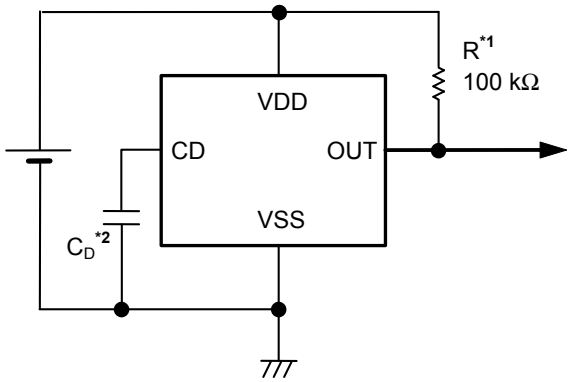
The temperature change of the release voltage and the detection voltage has the same sign consequently.

3. 3 Temperature characteristics of hysteresis voltage

The temperature change of the hysteresis voltage is expressed as $\frac{\Delta + V_{DET}}{\Delta Ta} - \frac{\Delta - V_{DET}}{\Delta Ta}$ and is calculated as follows:

$$\frac{\Delta + V_{DET}}{\Delta Ta} - \frac{\Delta - V_{DET}}{\Delta Ta} = \frac{V_{HYS}}{-V_{DET}} \times \frac{\Delta - V_{DET}}{\Delta Ta}$$

■ Standard Circuit



***1.** R is unnecessary for CMOS output products.

***2.** The delay capacitor (C_D) should be connected directly to the CD pin and to the VSS pin.

Figure 17

Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

■ Explanation of Terms

1. Detection voltage ($-V_{DET}$), release voltage ($+V_{DET}$)

The detection voltage ($-V_{DET}$) is a voltage at which the output turns to "L". The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum ($-V_{DET}$) Min. and the maximum ($-V_{DET}$) Max. is called the detection voltage range (Refer to **Figure 18**).

Example: In the S-1009C15, the detection voltage is either one in the range of $1.488 \leq (-V_{DET}) \leq 1.512$.
This means that some S-1009C15s have $-V_{DET} = 1.488$ V and some have $-V_{DET} = 1.512$ V.

The release voltage is a voltage at which the output turns to "H". The release voltage varies slightly among products of the same specification. The variation of release voltages between the specified minimum ($+V_{DET}$) Min. and the maximum ($+V_{DET}$) Max. is called the release voltage range (Refer to **Figure 19**). The range is calculated from the actual detection voltage ($-V_{DET}$) of a product and is in the range of $-V_{DET} \times 1.04 \leq +V_{DET} \leq -V_{DET} \times 1.06$.

Example: For the S-1009C15, the release voltage is either one in the range of $1.548 \leq (+V_{DET}) \leq 1.602$.
This means that some S-1009C15s have $+V_{DET} = 1.548$ V and some have $+V_{DET} = 1.602$ V.

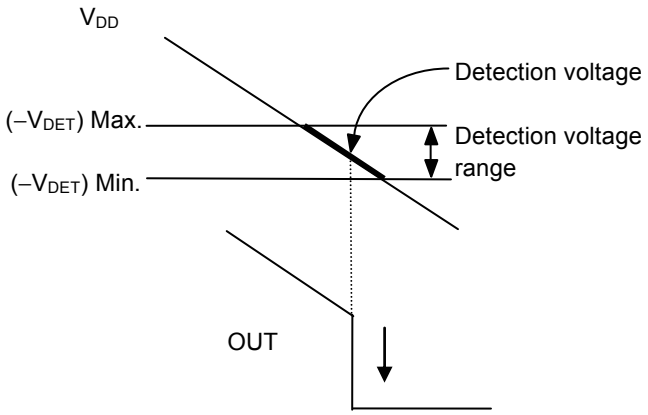


Figure 18 Detection voltage (CMOS output products)

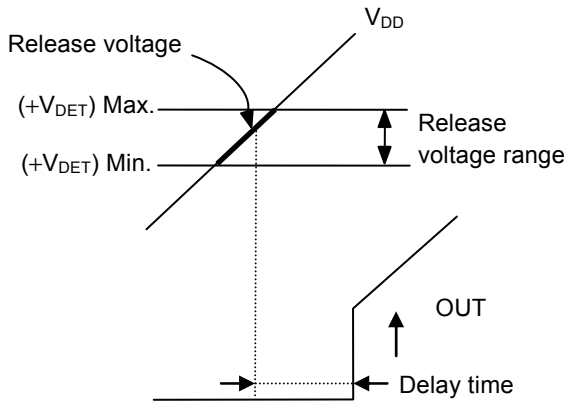


Figure 19 Release voltage (CMOS output products)

2. Hysteresis width (V_{HYS})

The hysteresis width is the voltage difference between the detection voltage and the release voltage (The voltage at point B − The voltage at point A = V_{HYS} in **Figure 14**). Setting the hysteresis width between the detection voltage and the release voltage, prevents malfunction caused by noise on the input voltage.

3. Delay Time (t_D)

The delay time in the S-1009 Series is a period from the input voltage to the V_{DD} pin exceeding the release voltage ($+V_{DET}$) until the output from the OUT pin inverts. The delay time changes according to the external capacitor (C_D).

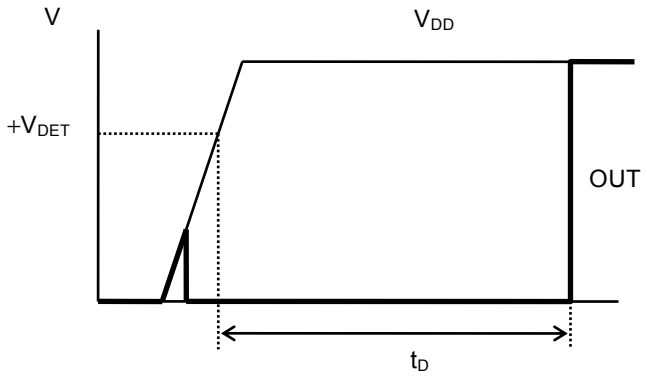


Figure 20 Delay time

4. Through-type current

Through-type current is a current that flows instantaneously at the time of detection and release of a voltage detector. The through-type current is large in CMOS output products, small in Nch open drain output products.

5. Oscillation

In applications where a resistor is connected to the voltage detector input (**Figure 21**), taking a CMOS active "L" product for example, the through-type current which is generated when the output goes from "L" to "H" (release) causes a voltage drop equal to [through-type current] × [input resistance] across the resistor. When the input voltage drops below the detection voltage ($-V_{DET}$) as a result, the output voltage goes to low level. In this state, the through-type current stops and its resultant voltage drop disappears, and the output goes from "L" to "H". The through-type current is then generated again, a voltage drop appears, and repeating the process finally induces oscillation.

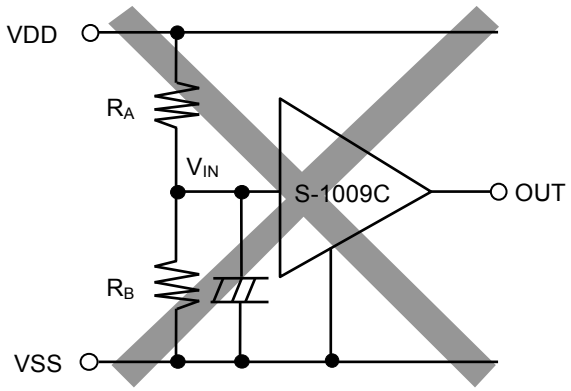


Figure 21 An example for bad implementation due to detection voltage change

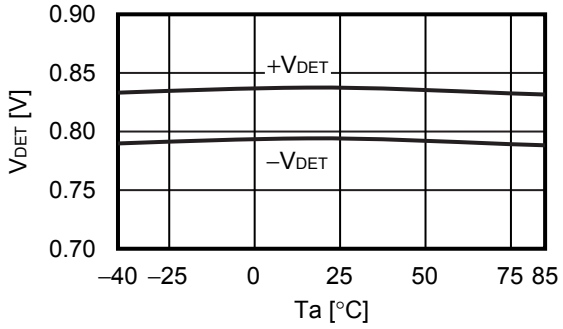
■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- In CMOS output products of the S-1009 Series, the through-type current flows at the detection and the release. If the input impedance is high, oscillation may occur due to the voltage drop by the through-type current during releasing.
- In CMOS output products oscillation may occur when a pull-down resistor is used, and falling speed of the power supply voltage (V_{DD}) is slow near the detection voltage.
- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics of the external parts should be taken into consideration. SII shall not bear any responsibility for patent infringements related to products using the circuits described herein.
- SII claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

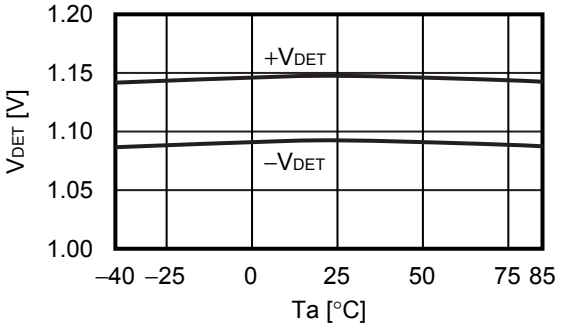
■ Characteristics (Typical Data)

1. Detection voltage (V_{DET}) – temperature (Ta)

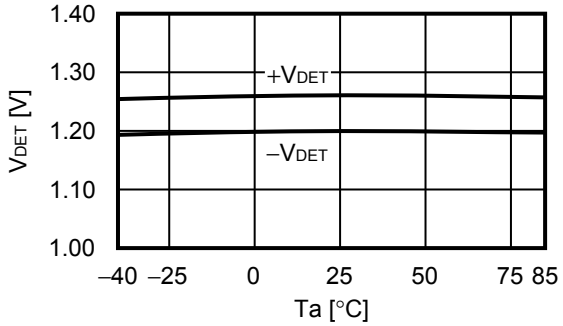
S-1009N08



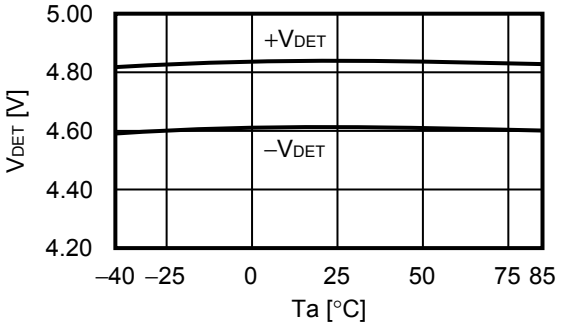
S-1009N11



S-1009N12

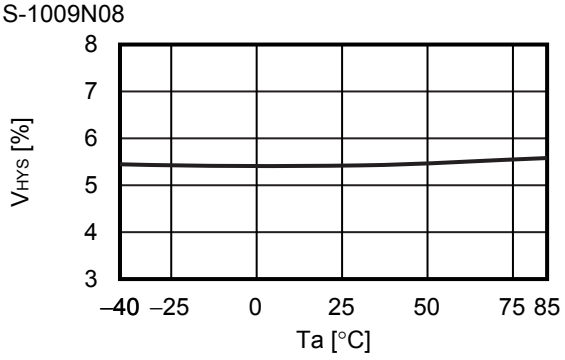


S-1009N46

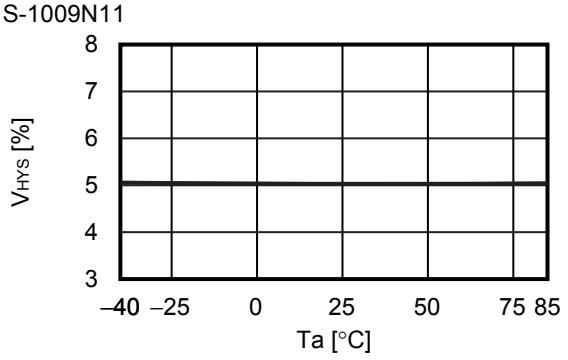


2. Hysteresis voltage width (V_{HYS}) – temperature (Ta)

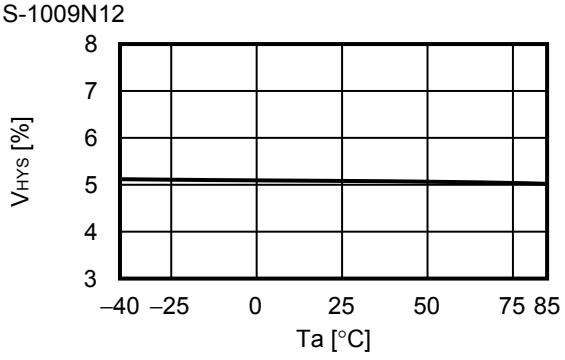
S-1009N08



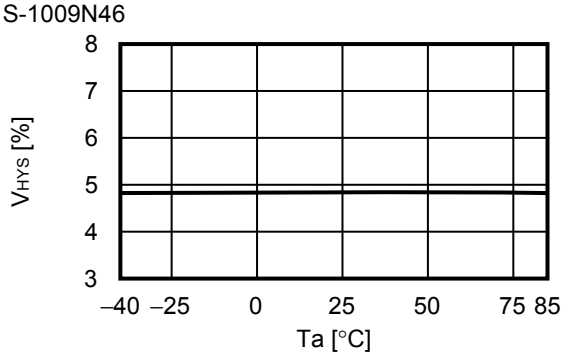
S-1009N11



S-1009N12

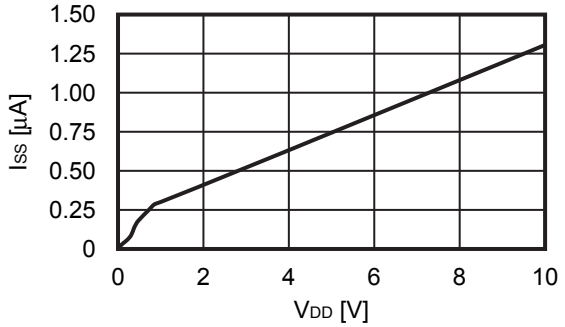


S-1009N46

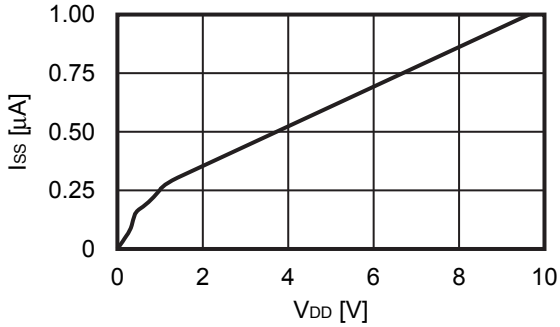


3. Current consumption (I_{SS}) – input voltage (V_{DD})

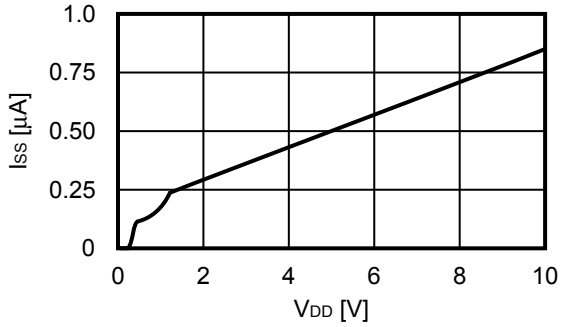
S-1009C08 Ta = +25°C



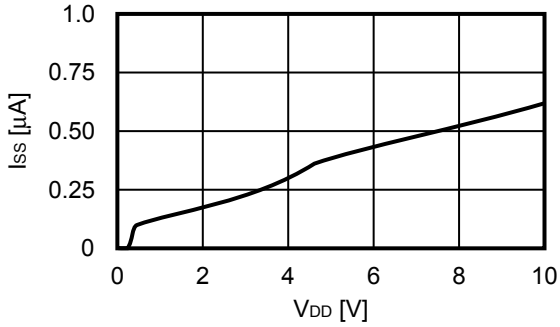
S-1009C11 Ta = +25°C



S-1009C12 Ta = +25°C

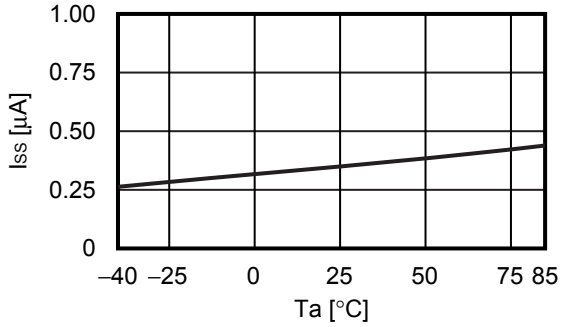


S-1009C46 Ta = +25°C

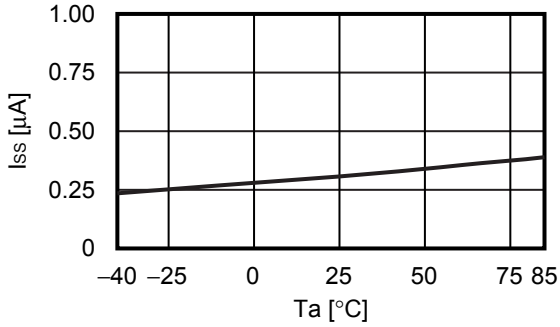


4. Current consumption (I_{SS}) – temperature (Ta)

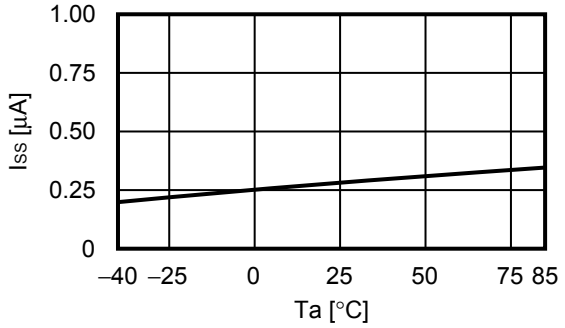
S-1009N08 V_{DD} = +V_{DET} + 0.6 V



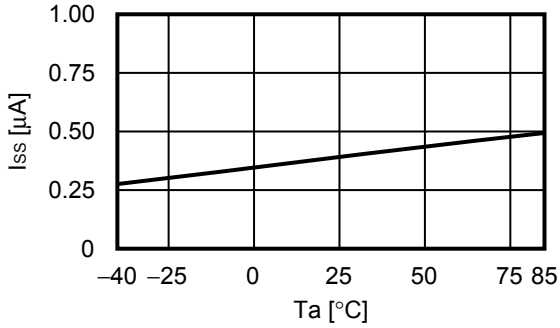
S-1009N11 V_{DD} = +V_{DET} + 0.6 V



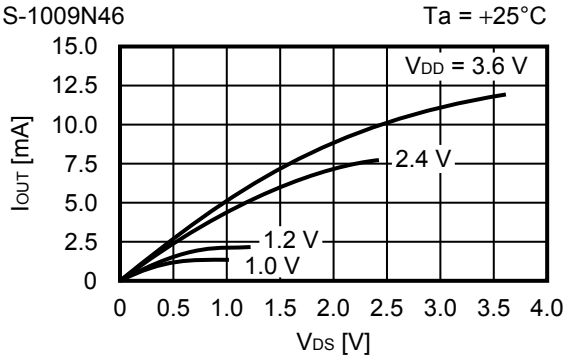
S-1009N12 V_{DD} = +V_{DET} + 0.6 V



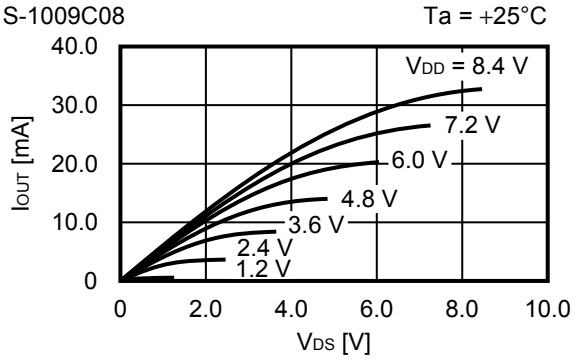
S-1009N46 V_{DD} = +V_{DET} + 0.6 V



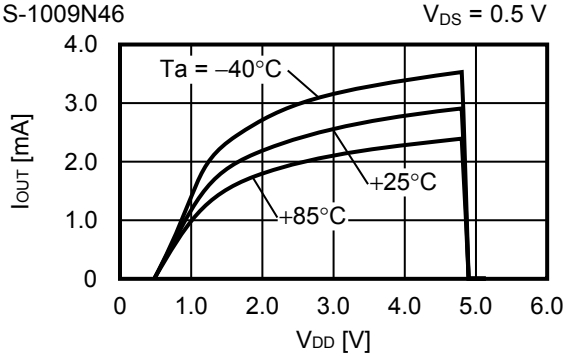
5. Nch transistor output current (I_{OUT}) – V_{DS}



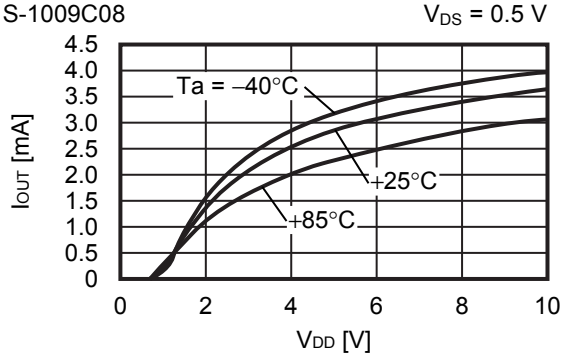
6. Pch transistor output current (I_{OUT}) – V_{DS}



7. Nch transistor output current (I_{OUT}) – input voltage (V_{DD})

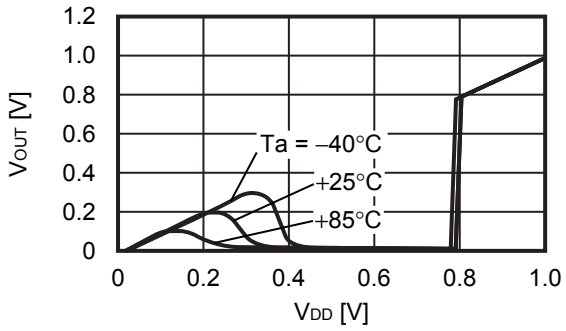


8. Pch transistor output current (I_{OUT}) – input voltage (V_{DD})

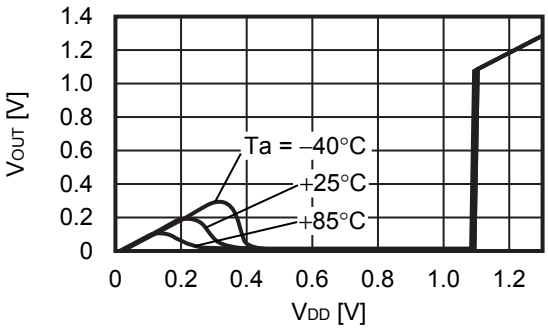


9. Minimum operating voltage – input voltage (V_{DD})

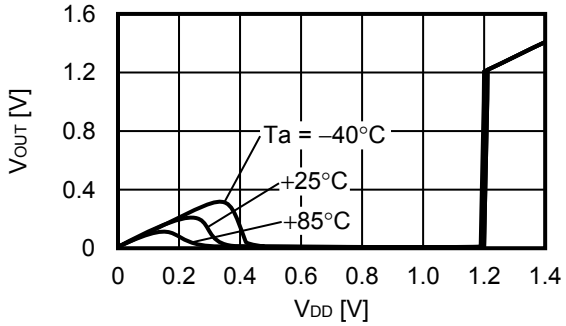
S-1009N08 Pull-up to V_{DD}
Pull-up resistance: 100 kΩ



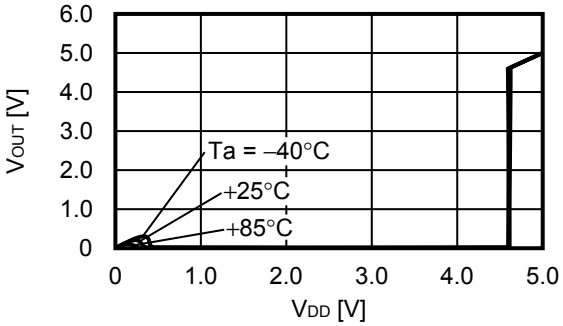
S-1009N11 Pull-up to V_{DD}
Pull-up resistance: 100 kΩ



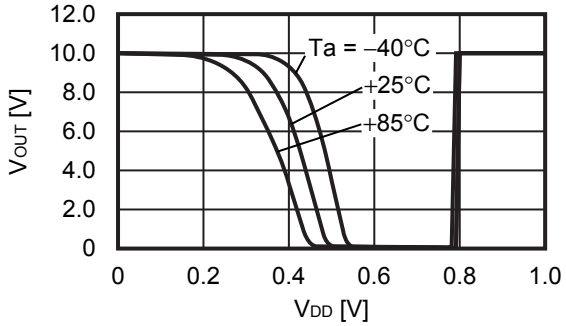
S-1009N12 Pull-up to V_{DD}
Pull-up resistance: 100 kΩ



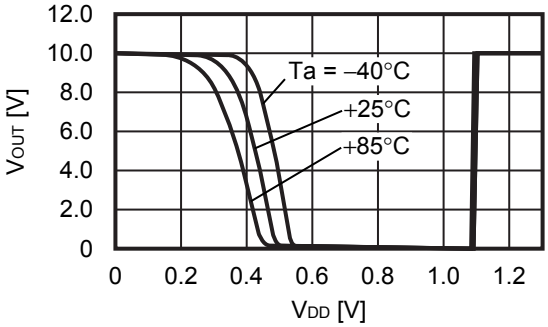
S-1009N46 Pull-up to V_{DD}
Pull-up resistance: 100 kΩ



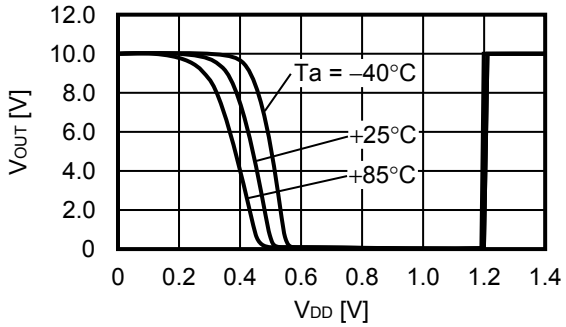
S-1009N08 Pull-up to 10 V
Pull-up resistance: 100 kΩ



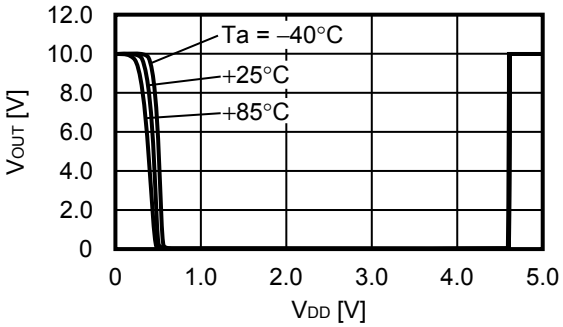
S-1009N11 Pull-up to 10 V
Pull-up resistance: 100 kΩ



S-1009N12 Pull-up to 10 V
Pull-up resistance: 100 kΩ

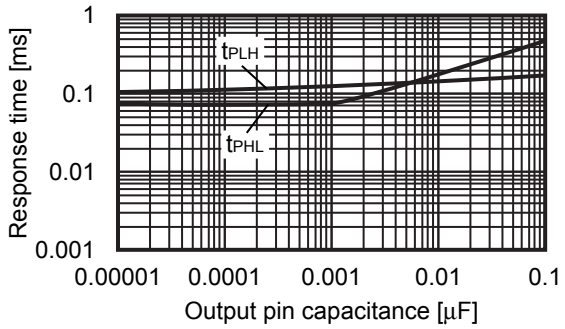


S-1009N46 Pull-up to 10 V
Pull-up resistance: 100 kΩ

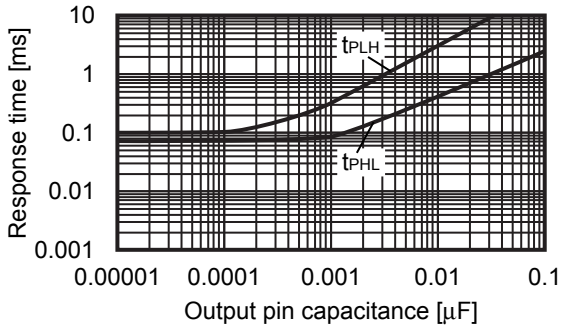


10. Dynamic response – C_{OUT} (CD pin; open)

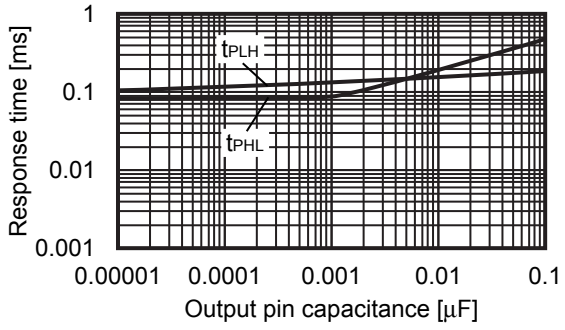
S-1009C08



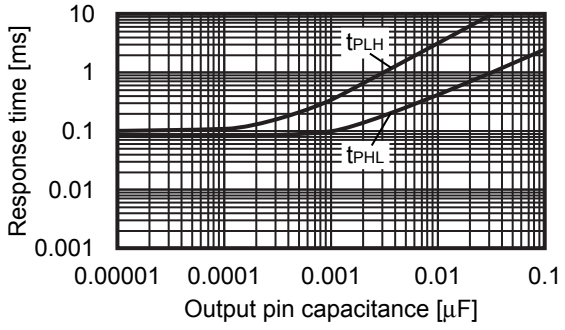
S-1009N08



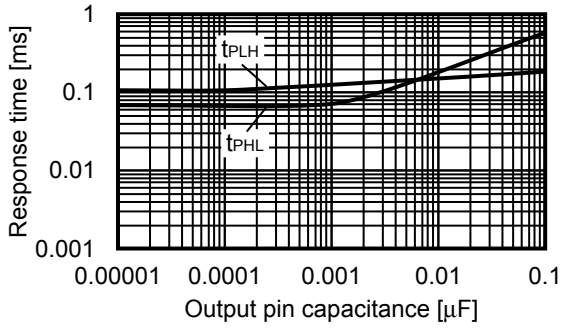
S-1009C11



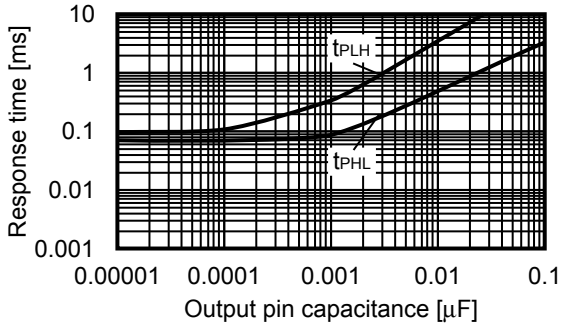
S-1009N11



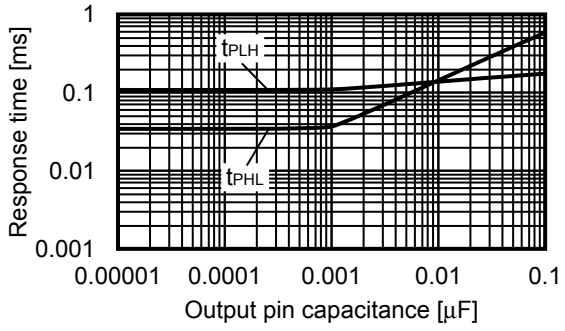
S-1009C12



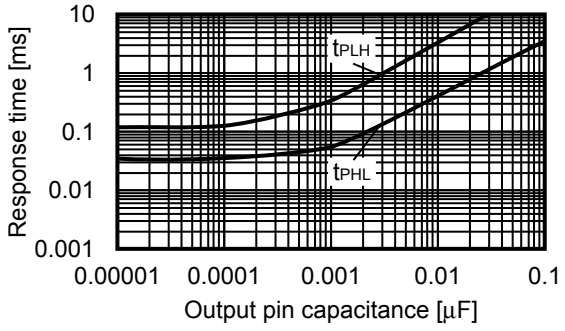
S-1009N12

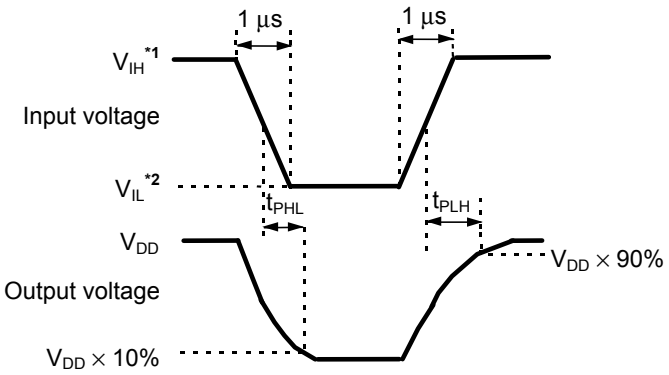


S-1009C46



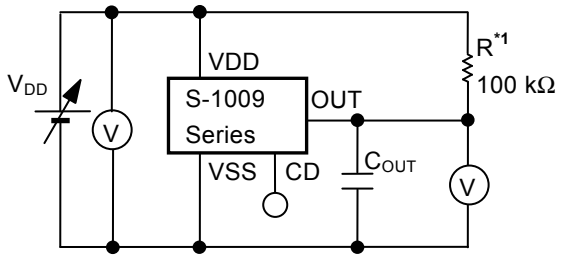
S-1009N46





***1.** V_{IH} = 10 V
***2.** V_{IL} = 0.7 V

Figure 22 Measurement Condition for Response Time

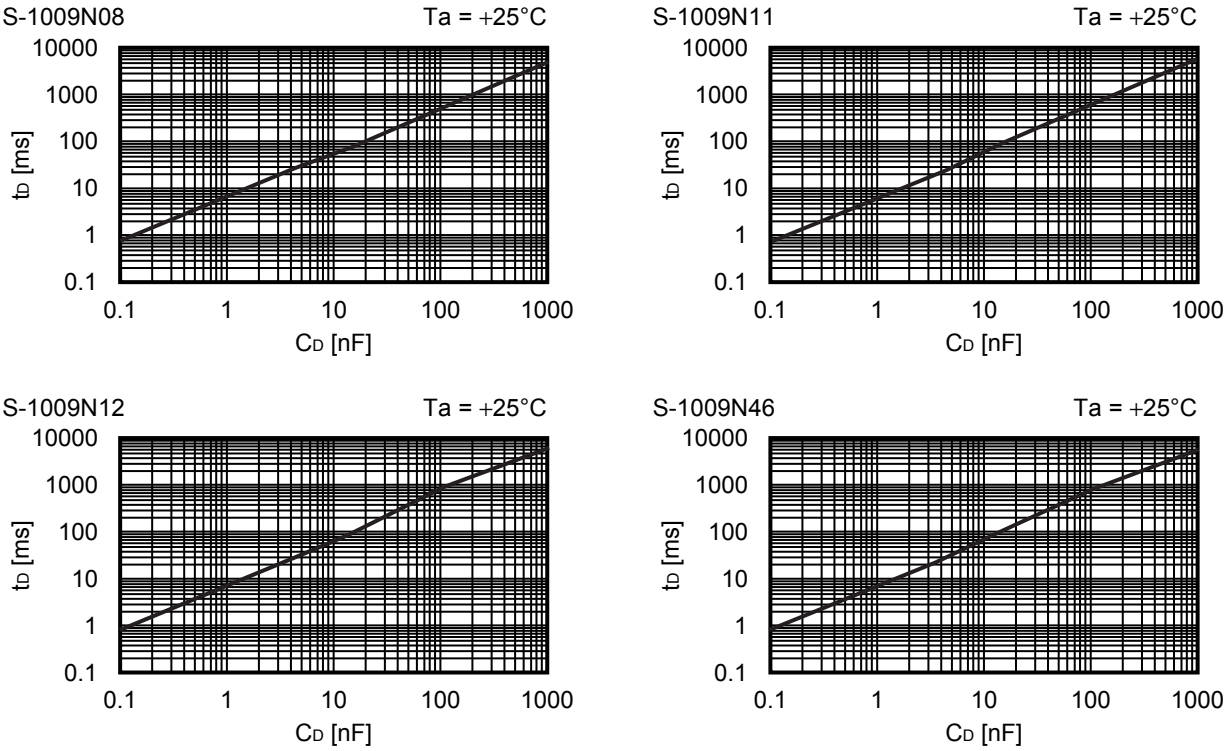


***1.** R is unnecessary for CMOS output products.

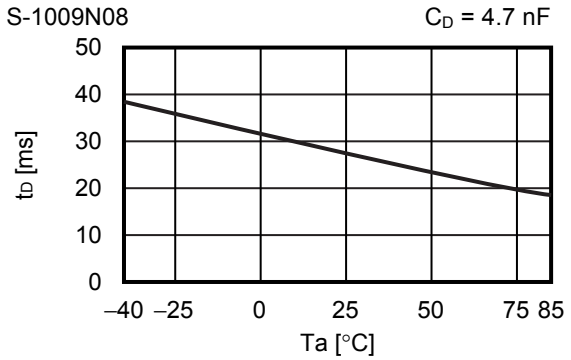
Figure 23 Measurement Circuit for Response Time

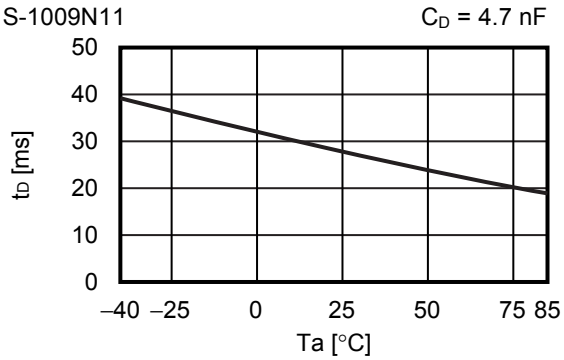
Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

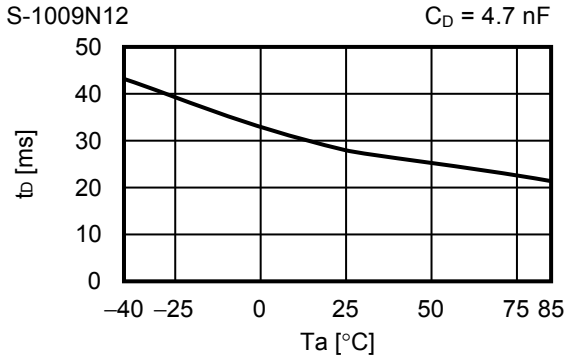
11. Delay Time – CD Pin Capacitance (C_D) (No output pin capacitance)

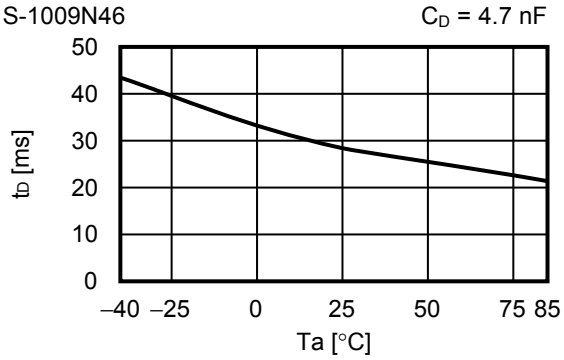


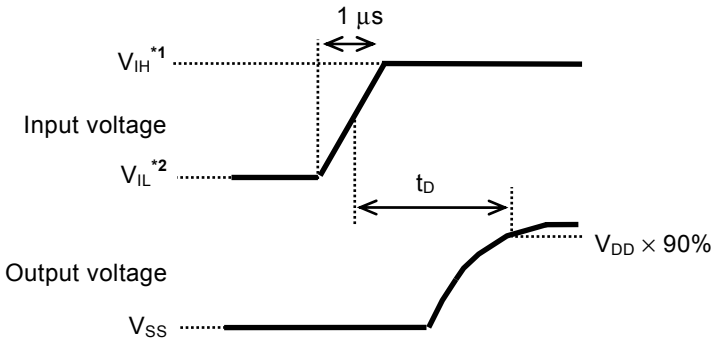
12. Delay Time – Temperature (Ta)





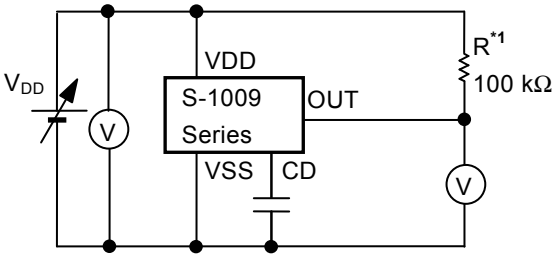






***1.** V_{IH} = 10 V
***2.** V_{IL} = 0.7 V

Figure 24 Measurement condition for delay time



***1.** R is unnecessary for CMOS output products.

Figure 25 Measurement circuit for delay time

Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

■ Application Circuit Examples

1. Microcomputer reset circuits

In microcomputers, when the power supply voltage is lower than the guaranteed operating voltage, an unspecified operation may be performed or the contents of the memory register may be lost. When power supply voltage returns to the normal level, the microcomputer needs to be initialized. Otherwise, the S-1009 Series may malfunction after that.

Reset circuits to protect microcomputer in the event of current being momentarily switched off or lowered.

Using the S-1009 Series which has the low operating voltage, a high accuracy detection voltage and hysteresis, reset circuits can be easily constructed as seen in **Figure 26** and **27**.

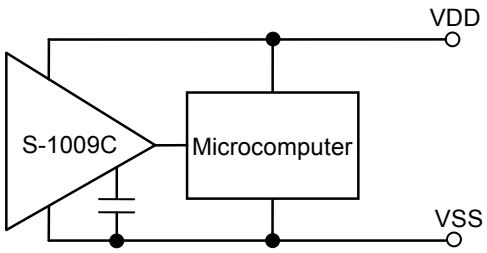
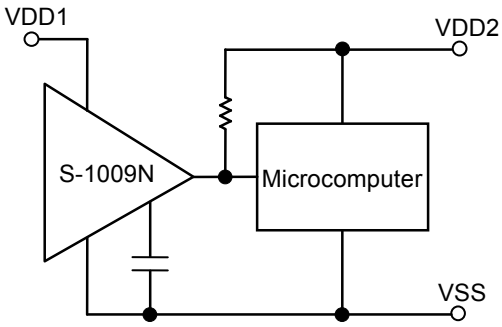


Figure 26 Example of reset circuit (S-1009C)



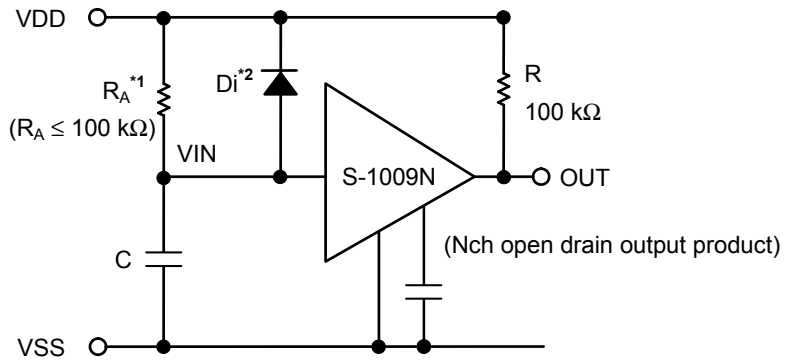
(Only for Nch open drain output products)

Figure 27 Example of reset circuit (S-1009N)

Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

2. Power-on reset circuit

A power-on reset circuit can be constructed using the S-1009 Series (Nch open drain output products only).



***1.** R should be 100 kΩ or less to prevent oscillation.

***2.** Diode Di instantaneously discharges the charge stored in the capacitor (C) at the power falling, Di can be removed when the delay of the falling time is not important.

Figure 28

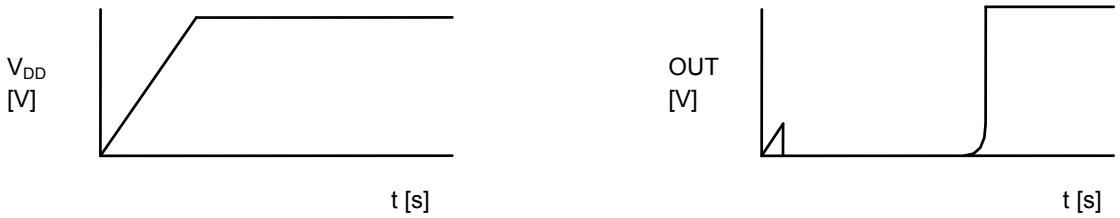


Figure 29

Remark When the power rises sharply, the output may instantaneously be set to the "H" level due to the IC's indefinite area (the output voltage is indefinite when it is the IC's minimum operating voltage or less), as seen in **Figure 30.**

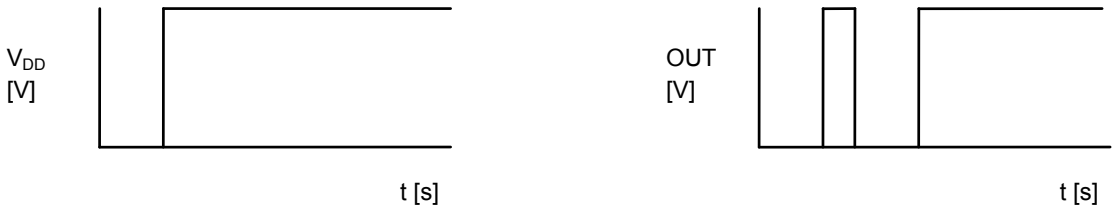


Figure 30

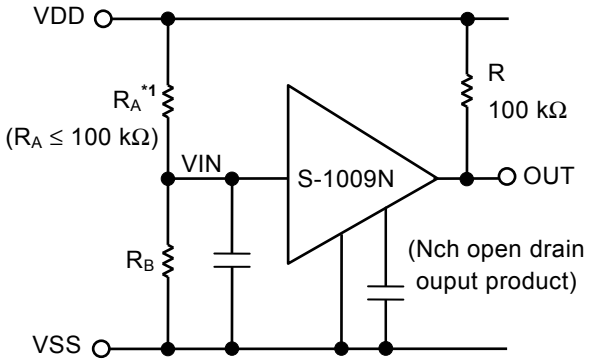
Caution 1. The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

2. Note that the hysteresis width may be larger as the following equation shows when using the above connection. Perform thorough evaluation using the actual application to set the constant.

Maximum hysteresis width = $V_{HYS} + R_A \bullet 20\ \mu A$

3. Change of detection voltage

In the Nch open drain output products of S-1009 Series, users do not need a specific value of detection voltage, the detection voltage can be changed by using a resistance divider or a diode, as seen in **Figure 31** and **32**.
In **Figure 31**, hysteresis width also changes.



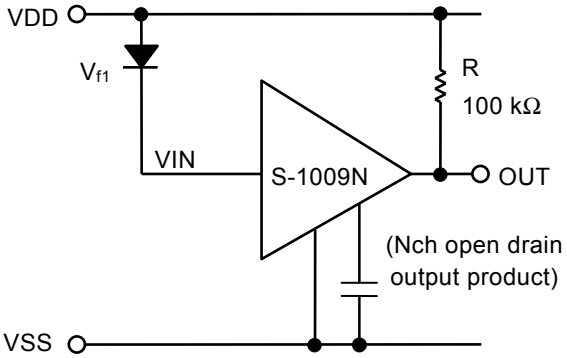
$$\text{Detection voltage} = \frac{R_A + R_B}{R_B} \bullet -V_{DET}$$

$$\text{Hysteresis width} = \frac{R_A + R_B}{R_B} \bullet V_{HYS}$$

***1.** R_A should be 100 kΩ or less to prevent oscillation.

Caution **If R_A and R_B are large, the hysteresis width may also be larger than the value given by the above equation due to the through-type current (which flows slightly in an Nch open drain product).**

Figure 31



Detection voltage = $V_{f1} + (-V_{DET})$

Figure 32

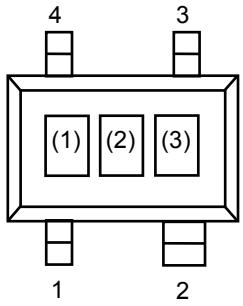
Caution **1. The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.**
2. Note that the hysteresis width may be larger as the following equation shows when using the above connections. Perform thorough evaluation using the actual application to set the constant.

$$\textbf{Maximum hysteresis width} = \frac{R_A + R_B}{R_B} \bullet V_{HYS} + R_A \bullet 20\ \mu A$$

■ Marking Specifications

1. SC-82AB

SC-82AB
Top view



(1) to (3) : Product code (refer to **Product name vs. Product code**)

Product name vs. Product code

1. 1 Nch open drain output products

Product Name	Product Code		
	(1)	(2)	(3)
S-1009N08I-N4T1U	T	8	A
S-1009N09I-N4T1U	T	8	B
S-1009N10I-N4T1U	T	8	C
S-1009N11I-N4T1U	T	8	D
S-1009N12I-N4T1U	T	8	E
S-1009N13I-N4T1U	T	8	F
S-1009N14I-N4T1U	T	8	G
S-1009N15I-N4T1U	T	8	H
S-1009N16I-N4T1U	T	8	I
S-1009N17I-N4T1U	T	8	J
S-1009N18I-N4T1U	T	8	K
S-1009N19I-N4T1U	T	8	L
S-1009N20I-N4T1U	T	8	M
S-1009N21I-N4T1U	T	8	N
S-1009N22I-N4T1U	T	8	O
S-1009N23I-N4T1U	T	8	P
S-1009N24I-N4T1U	T	8	Q
S-1009N25I-N4T1U	T	8	R
S-1009N26I-N4T1U	T	8	S
S-1009N27I-N4T1U	T	8	T
S-1009N28I-N4T1U	T	8	U
S-1009N29I-N4T1U	T	8	V
S-1009N30I-N4T1U	T	8	W
S-1009N31I-N4T1U	T	8	X
S-1009N32I-N4T1U	T	8	Y
S-1009N33I-N4T1U	T	8	Z
S-1009N34I-N4T1U	T	9	A
S-1009N35I-N4T1U	T	9	B
S-1009N36I-N4T1U	T	9	C
S-1009N37I-N4T1U	T	9	D
S-1009N38I-N4T1U	T	9	E
S-1009N39I-N4T1U	T	9	F
S-1009N40I-N4T1U	T	9	G
S-1009N41I-N4T1U	T	9	H
S-1009N42I-N4T1U	T	9	I
S-1009N43I-N4T1U	T	9	J
S-1009N44I-N4T1U	T	9	K
S-1009N45I-N4T1U	T	9	L
S-1009N46I-N4T1U	T	9	M

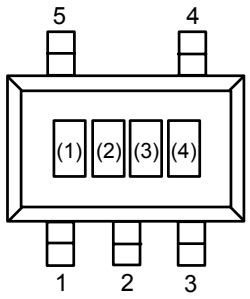
1. 2 CMOS output products

Product Name	Product Code		
	(1)	(2)	(3)
S-1009C08I-N4T1U	T	6	A
S-1009C09I-N4T1U	T	6	B
S-1009C10I-N4T1U	T	6	C
S-1009C11I-N4T1U	T	6	D
S-1009C12I-N4T1U	T	6	E
S-1009C13I-N4T1U	T	6	F
S-1009C14I-N4T1U	T	6	G
S-1009C15I-N4T1U	T	6	H
S-1009C16I-N4T1U	T	6	I
S-1009C17I-N4T1U	T	6	J
S-1009C18I-N4T1U	T	6	K
S-1009C19I-N4T1U	T	6	L
S-1009C20I-N4T1U	T	6	M
S-1009C21I-N4T1U	T	6	N
S-1009C22I-N4T1U	T	6	O
S-1009C23I-N4T1U	T	6	P
S-1009C24I-N4T1U	T	6	Q
S-1009C25I-N4T1U	T	6	R
S-1009C26I-N4T1U	T	6	S
S-1009C27I-N4T1U	T	6	T
S-1009C28I-N4T1U	T	6	U
S-1009C29I-N4T1U	T	6	V
S-1009C30I-N4T1U	T	6	W
S-1009C31I-N4T1U	T	6	X
S-1009C32I-N4T1U	T	6	Y
S-1009C33I-N4T1U	T	6	Z
S-1009C34I-N4T1U	T	7	A
S-1009C35I-N4T1U	T	7	B
S-1009C36I-N4T1U	T	7	C
S-1009C37I-N4T1U	T	7	D
S-1009C38I-N4T1U	T	7	E
S-1009C39I-N4T1U	T	7	F
S-1009C40I-N4T1U	T	7	G
S-1009C41I-N4T1U	T	7	H
S-1009C42I-N4T1U	T	7	I
S-1009C43I-N4T1U	T	7	J
S-1009C44I-N4T1U	T	7	K
S-1009C45I-N4T1U	T	7	L
S-1009C46I-N4T1U	T	7	M

Remark Please contact our sales office for products with specifications other than the above.

2. SOT-23-5

SOT-23-5
Top view



(1) to (3) : Product code (refer to **Product name vs. Product code**)
(4) : Lot number

Product name vs. Product code

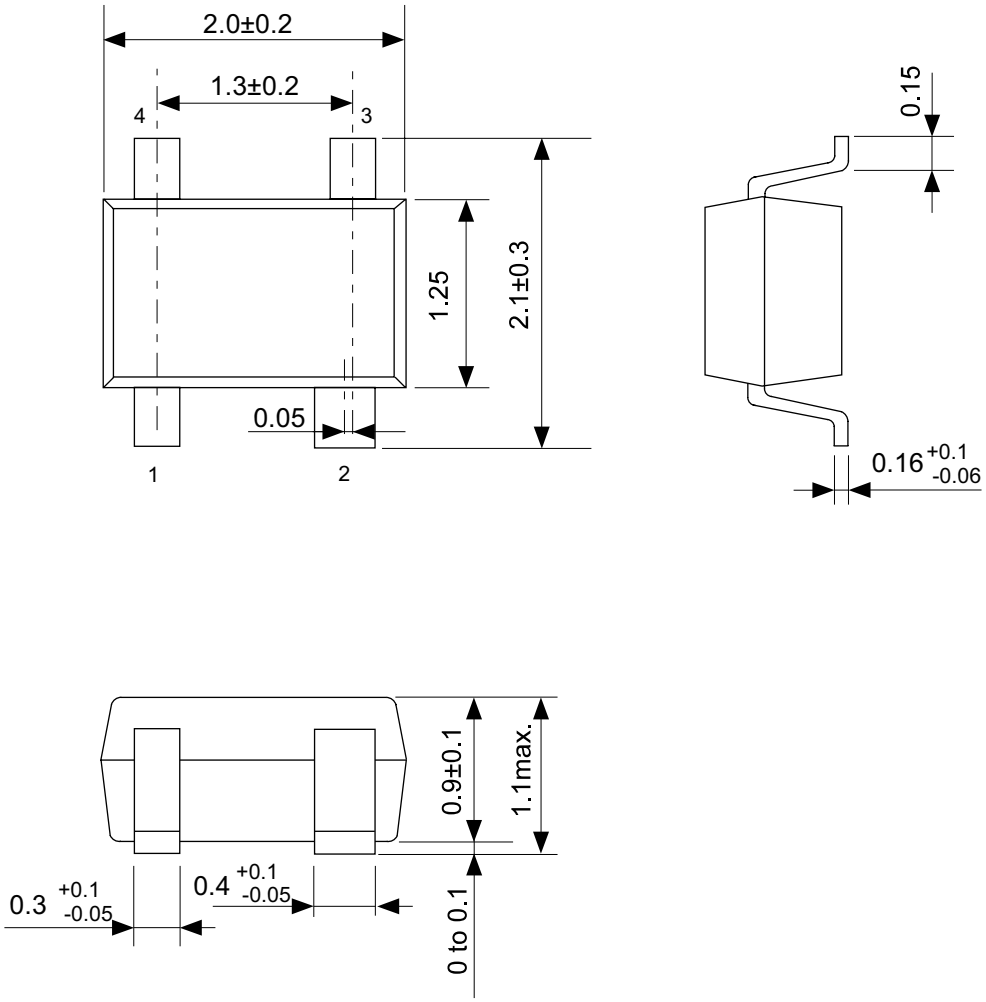
2. 1 Nch open drain output products

Product Name	Product Code		
	(1)	(2)	(3)
S-1009N08I-M5T1U	T	8	A
S-1009N09I-M5T1U	T	8	B
S-1009N10I-M5T1U	T	8	C
S-1009N11I-M5T1U	T	8	D
S-1009N12I-M5T1U	T	8	E
S-1009N13I-M5T1U	T	8	F
S-1009N14I-M5T1U	T	8	G
S-1009N15I-M5T1U	T	8	H
S-1009N16I-M5T1U	T	8	I
S-1009N17I-M5T1U	T	8	J
S-1009N18I-M5T1U	T	8	K
S-1009N19I-M5T1U	T	8	L
S-1009N20I-M5T1U	T	8	M
S-1009N21I-M5T1U	T	8	N
S-1009N22I-M5T1U	T	8	O
S-1009N23I-M5T1U	T	8	P
S-1009N24I-M5T1U	T	8	Q
S-1009N25I-M5T1U	T	8	R
S-1009N26I-M5T1U	T	8	S
S-1009N27I-M5T1U	T	8	T
S-1009N28I-M5T1U	T	8	U
S-1009N29I-M5T1U	T	8	V
S-1009N30I-M5T1U	T	8	W
S-1009N31I-M5T1U	T	8	X
S-1009N32I-M5T1U	T	8	Y
S-1009N33I-M5T1U	T	8	Z
S-1009N34I-M5T1U	T	9	A
S-1009N35I-M5T1U	T	9	B
S-1009N36I-M5T1U	T	9	C
S-1009N37I-M5T1U	T	9	D
S-1009N38I-M5T1U	T	9	E
S-1009N39I-M5T1U	T	9	F
S-1009N40I-M5T1U	T	9	G
S-1009N41I-M5T1U	T	9	H
S-1009N42I-M5T1U	T	9	I
S-1009N43I-M5T1U	T	9	J
S-1009N44I-M5T1U	T	9	K
S-1009N45I-M5T1U	T	9	L
S-1009N46I-M5T1U	T	9	M

2. 2 CMOS output products

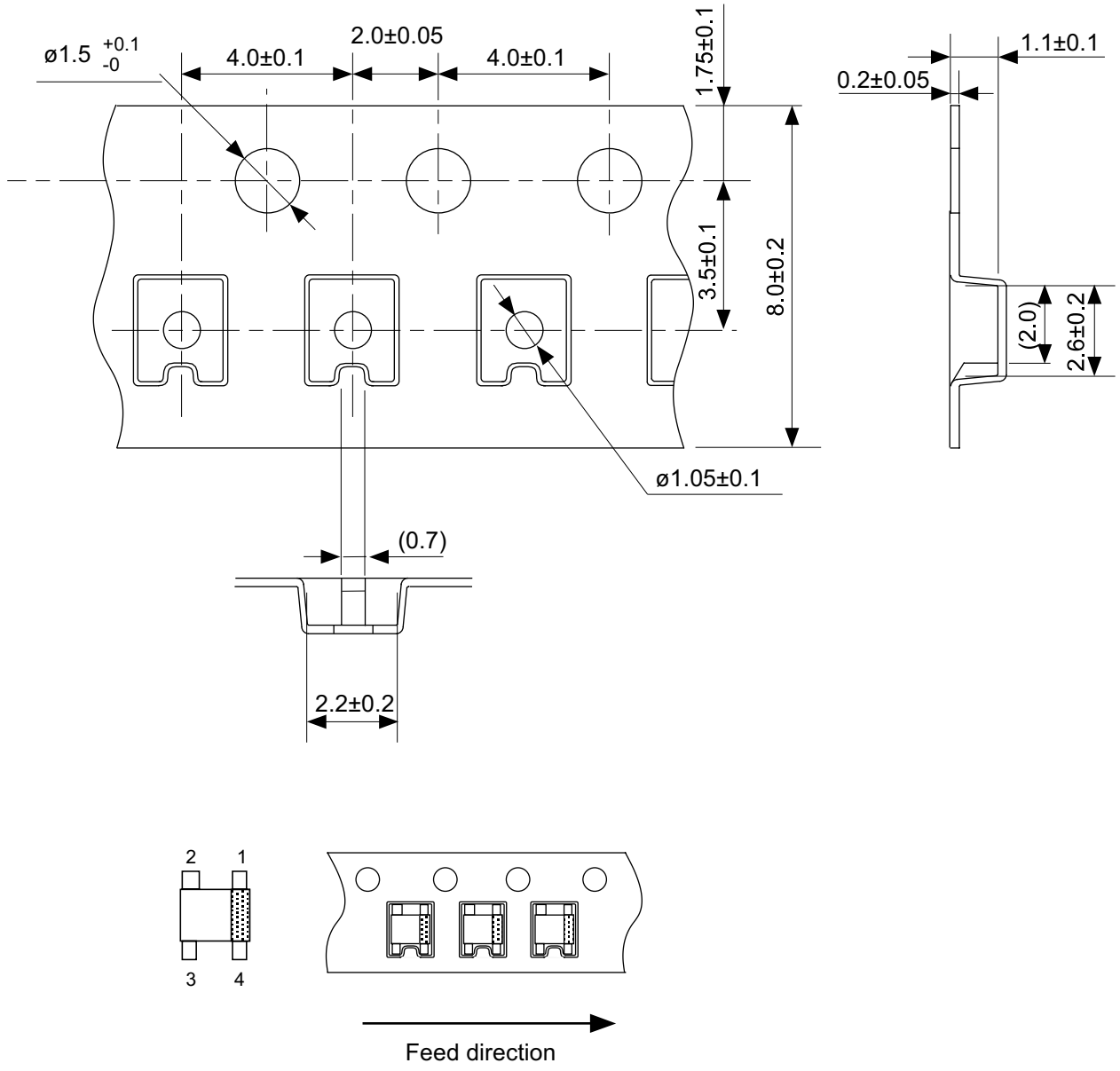
Product Name	Product Code		
	(1)	(2)	(3)
S-1009C08I-M5T1U	T	6	A
S-1009C09I-M5T1U	T	6	B
S-1009C10I-M5T1U	T	6	C
S-1009C11I-M5T1U	T	6	D
S-1009C12I-M5T1U	T	6	E
S-1009C13I-M5T1U	T	6	F
S-1009C14I-M5T1U	T	6	G
S-1009C15I-M5T1U	T	6	H
S-1009C16I-M5T1U	T	6	I
S-1009C17I-M5T1U	T	6	J
S-1009C18I-M5T1U	T	6	K
S-1009C19I-M5T1U	T	6	L
S-1009C20I-M5T1U	T	6	M
S-1009C21I-M5T1U	T	6	N
S-1009C22I-M5T1U	T	6	O
S-1009C23I-M5T1U	T	6	P
S-1009C24I-M5T1U	T	6	Q
S-1009C25I-M5T1U	T	6	R
S-1009C26I-M5T1U	T	6	S
S-1009C27I-M5T1U	T	6	T
S-1009C28I-M5T1U	T	6	U
S-1009C29I-M5T1U	T	6	V
S-1009C30I-M5T1U	T	6	W
S-1009C31I-M5T1U	T	6	X
S-1009C32I-M5T1U	T	6	Y
S-1009C33I-M5T1U	T	6	Z
S-1009C34I-M5T1U	T	7	A
S-1009C35I-M5T1U	T	7	B
S-1009C36I-M5T1U	T	7	C
S-1009C37I-M5T1U	T	7	D
S-1009C38I-M5T1U	T	7	E
S-1009C39I-M5T1U	T	7	F
S-1009C40I-M5T1U	T	7	G
S-1009C41I-M5T1U	T	7	H
S-1009C42I-M5T1U	T	7	I
S-1009C43I-M5T1U	T	7	J
S-1009C44I-M5T1U	T	7	K
S-1009C45I-M5T1U	T	7	L
S-1009C46I-M5T1U	T	7	M

Remark Please contact our sales office for products with specifications other than the above.



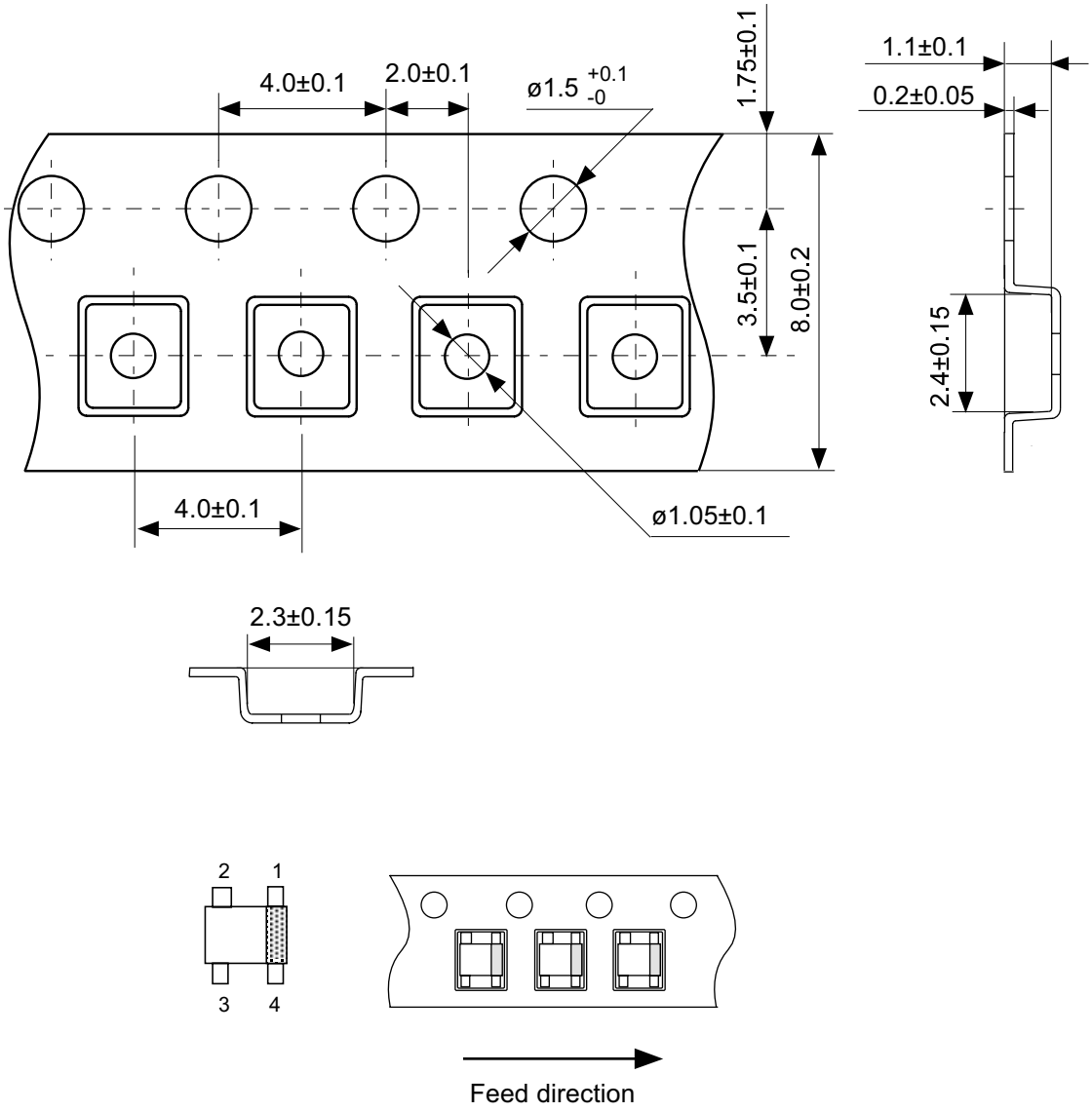
No. NP004-A-P-SD-1.1

TITLE	SC82AB-A-PKG Dimensions
No.	NP004-A-P-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	



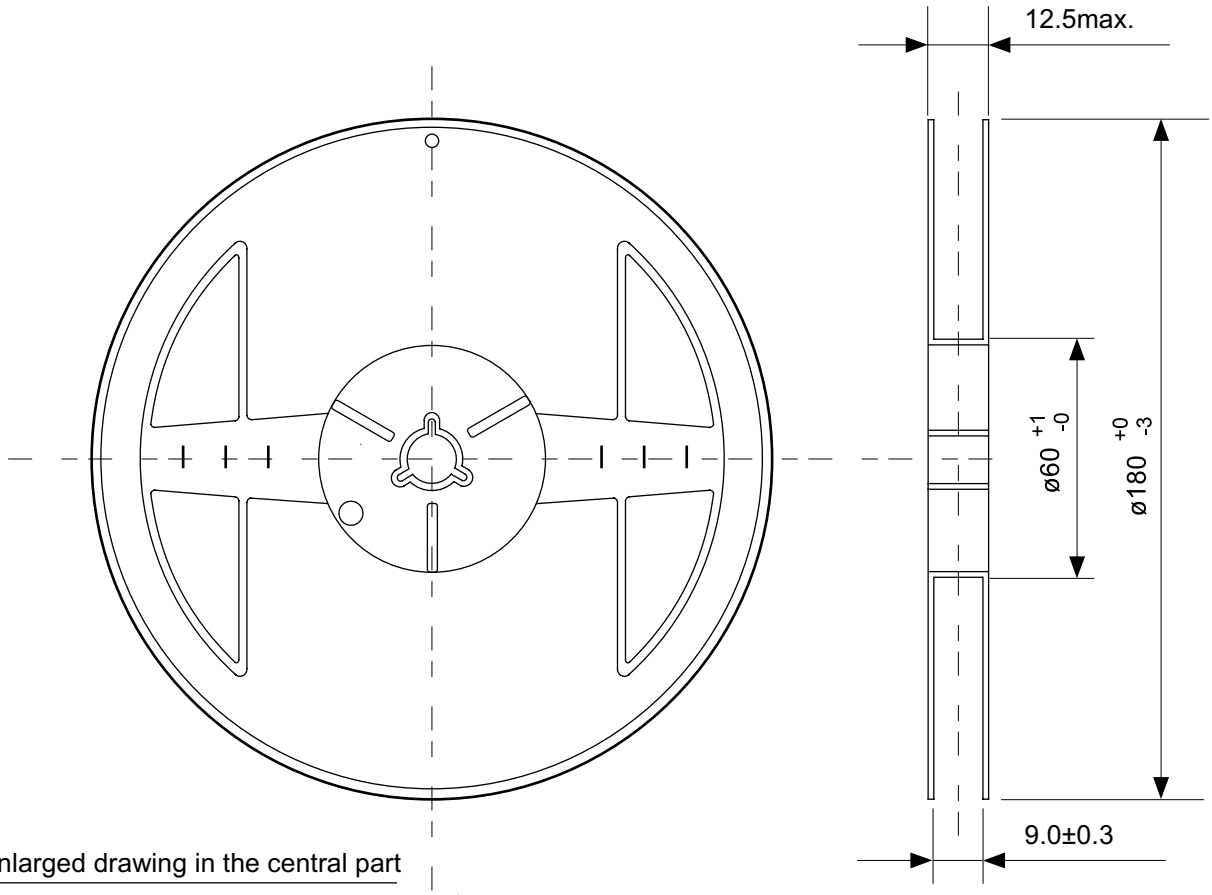
No. NP004-A-C-SD-3.0

TITLE	SC82AB-A-Carrier Tape
No.	NP004-A-C-SD-3.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	

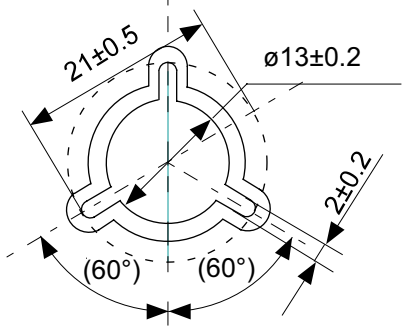


No. NP004-A-C-S1-2.0

TITLE	SC82AB-A-Carrier Tape
No.	NP004-A-C-S1-2.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	

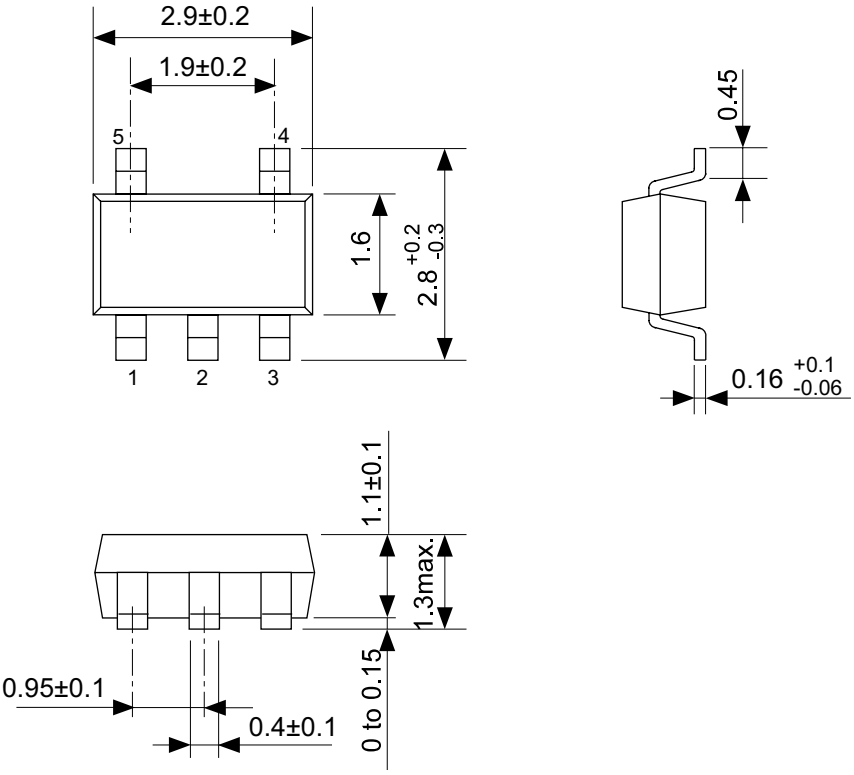


Enlarged drawing in the central part



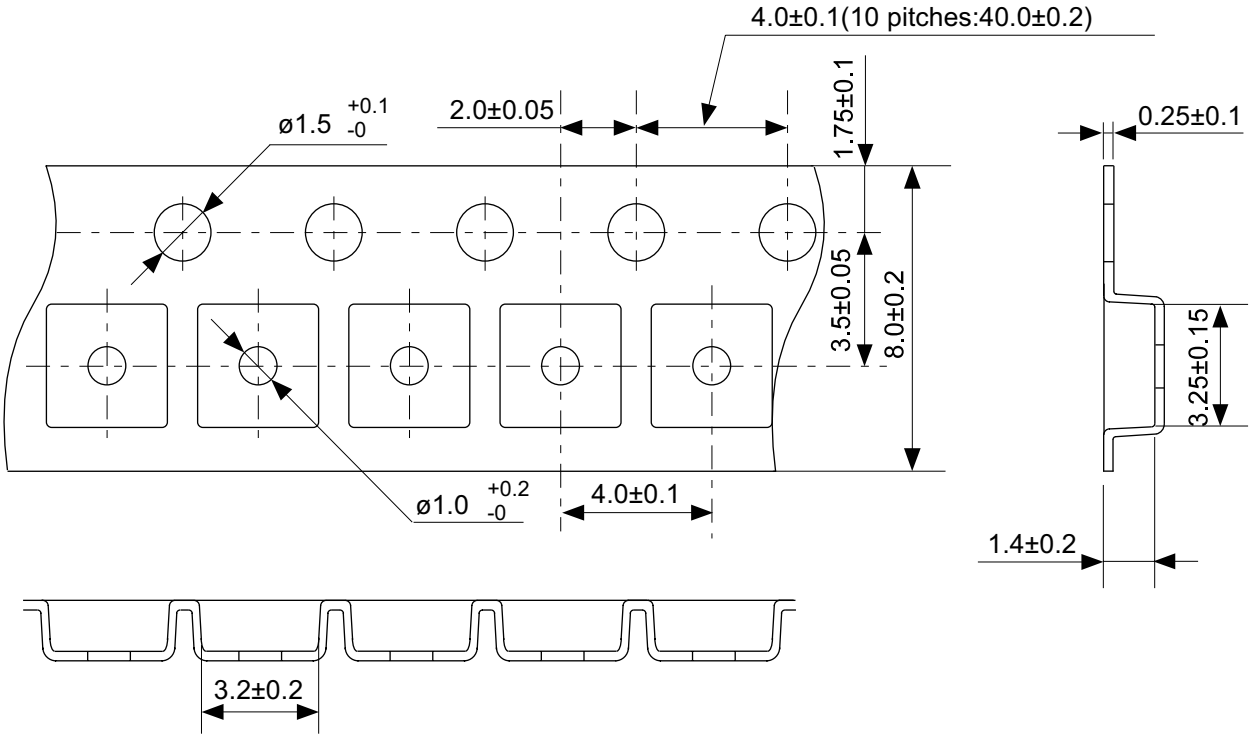
No. NP004-A-R-SD-1.1

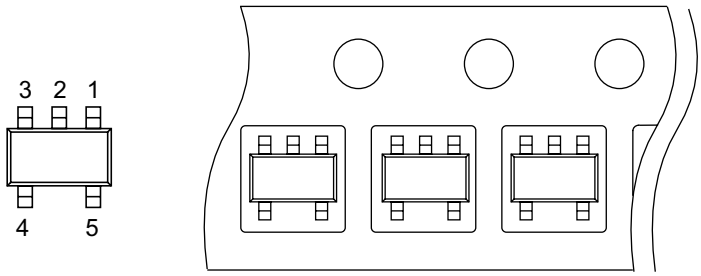
TITLE	SC82AB-A-Reel		
No.	NP004-A-R-SD-1.1		
SCALE		QTY.	3,000
UNIT	mm		
Seiko Instruments Inc.			



No. MP005-A-P-SD-1.2

TITLE	SOT235-A-PKG Dimensions
No.	MP005-A-P-SD-1.2
SCALE	
UNIT	mm
Seiko Instruments Inc.	

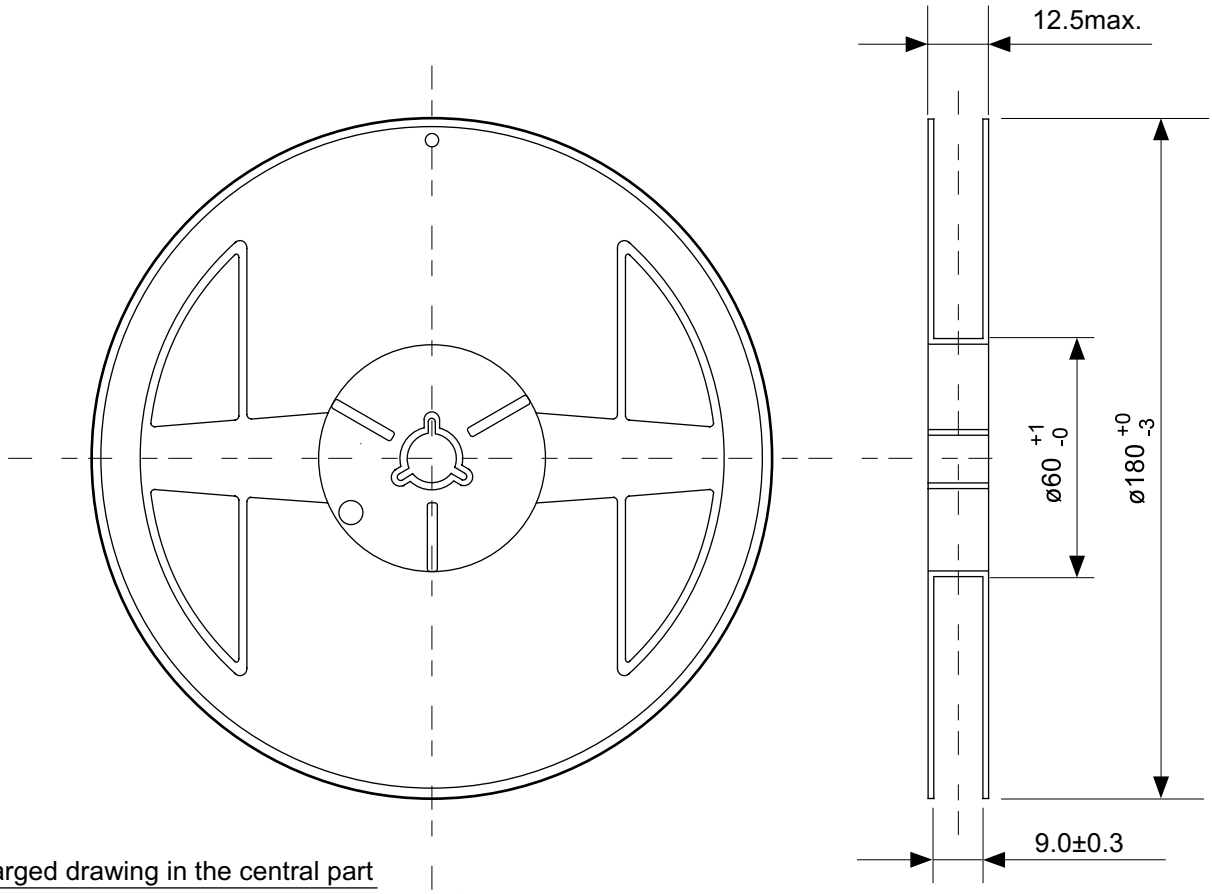




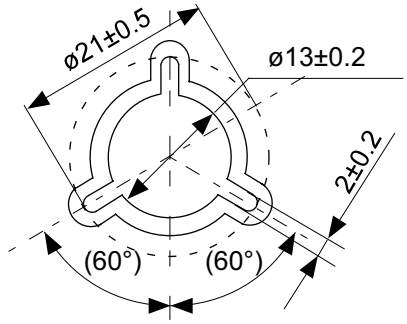
Feed direction

No. MP005-A-C-SD-2.1

TITLE	SOT235-A-Carrier Tape
No.	MP005-A-C-SD-2.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. MP005-A-R-SD-1.1

TITLE	SOT235-A-Reel		
No.	MP005-A-R-SD-1.1		
SCALE		QTY.	3,000
UNIT	mm		
Seiko Instruments Inc.			

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