mosaic

Mosaic
Semiconductor
Inc.

256K X 8 SRAM

MS8256FK-45/55

Issue 1.2 : September 1993

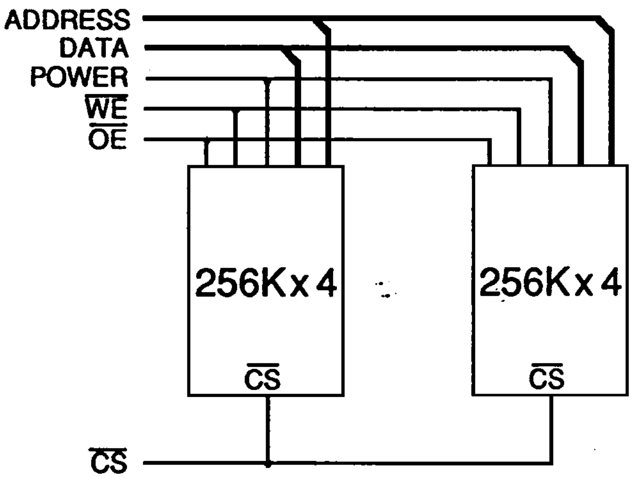
ADVANCE PRODUCT INFORMATION

524,288 x 8 CMOS High Speed Static RAM

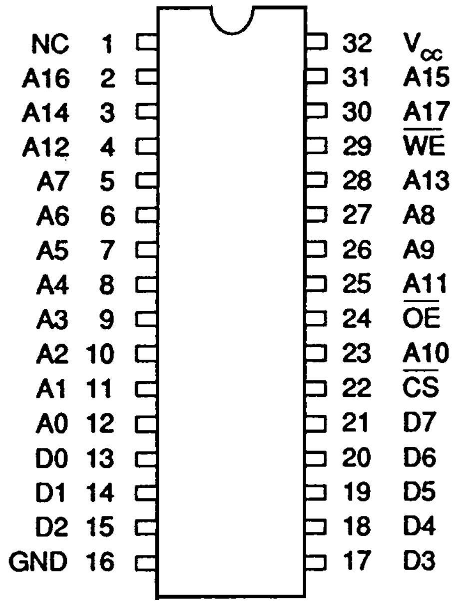
Features

Very Fast Access Times of 45/55 ns
(35 ns under development)
JEDEC Standard 32 pin DIL footprint
Operating Power 350 mW (typ.)
Low Power Standby 200 µW (typ.)
20 µW (typ.) - L
Battery back-up capability
Completely Static Operation
Common data inputs & outputs
Onboard Decoupling Capacitors

Block Diagram



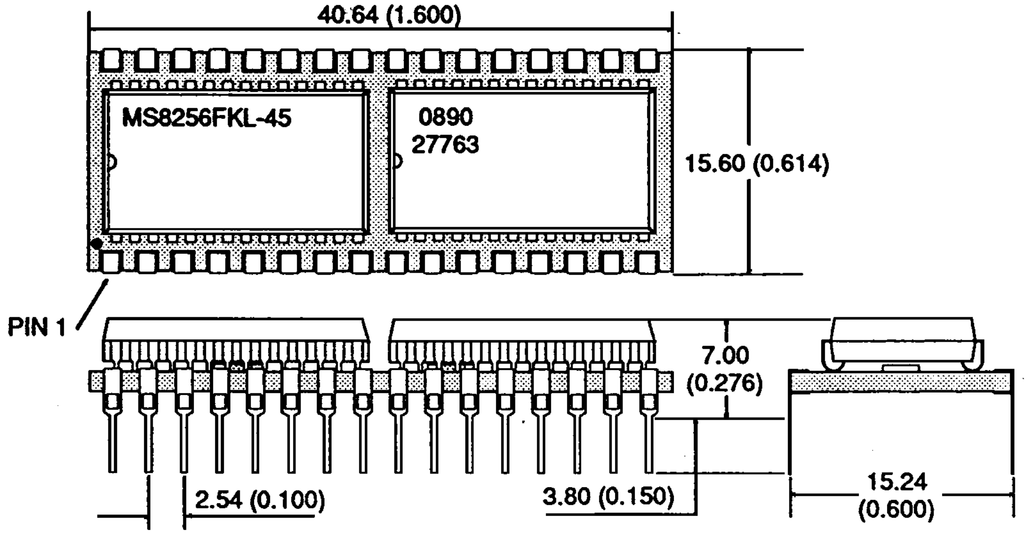
Pin Definition



Pin Functions

A0-A17	Address Inputs
D0-7	Data Input/Output
CS	Chip Select
OE	Output Enable
WE	Write Enable
V_{cc}	Power (+5V)
GND	Ground

Package Details Dimensions in mm (inches).



Absolute Maximum Ratings (1)

Voltage on any pin relative to V_{SS} (2)	V_T	-0.5 to +7	V
Power Dissipation	P_T	1	W
Storage Temperature	T_{STG}	-55 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) V_t can be -2.0V pulse of less than 10ns.

Recommended Operating Conditions

		min	typ	max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	0.6	V
Input Low Voltage	V_{IL}	-0.5	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (85121)

DC Electrical Characteristics (V_{CC}=5V±10%,T_A= -40°C to +85°C)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current	I_{LI1}	$0V \leq V_{IN} \leq V_{CC}$	-	-	4	µA
Output Leakage Current	I_{LO}	$\overline{CS}=V_{IH,}$ $V_{I/O}$=GND to V_{CC}	-	-	4	µA
Operating Supply Current	I_{CC}	$\overline{CS}=V_{IL}, I_{I/O}$=0mA, minimum cycle	-	140	240	mA
Standby SupplyCurrent	I_{SB}	$\overline{CS}=V_{IH}$, minimum cycle	-	60	120	mA
	I_{SB1}	$\overline{CS} \geq V_{CC}$-0.2V, $0.2V \geq V_{IN} \geq V_{CC}$-0.2V	-	0.04	4	mA
-L Part	I_{SB2}	$\overline{CS} \geq V_{CC}$-0.2V, $0.2V \geq V_{IN} \geq V_{CC}$-0.2V	-	4	400	µA
Output Voltage	V_{OL}	I_{OL}=8.0mA	-	-	0.4	V
	V_{OH}	I_{OH}=-4.0mA	2.4	-	-	V

Typical values are at V_{CC}=5.0V,T_A=25°C and specified loading.

Capacitance (V_{CC}=5V±10%,T_A=25°C)

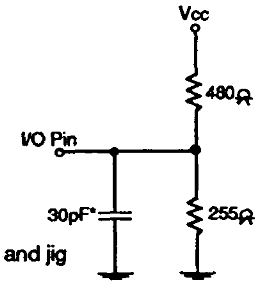
Parameter	*Symbol*	*Test Condition*	*max*	*Unit*
I/P Capacitance	C_{IN1}	V_{IN} = 0V	12	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	11	pF

Note: Capacitance calculated, not measured.

AC Test Conditions

- * Input pulse levels: GND to 3.0V
- * Input rise and fall times: 5ns
- * Input and Output timing reference levels: 1.5V
- * Output load: See Load Diagram
- * V_{cc}=5V±10%

Output Load Circuits

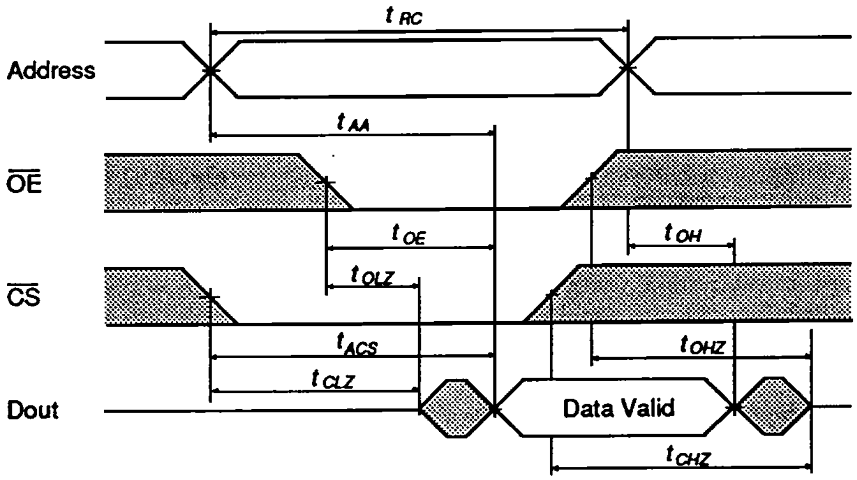


*Including scope and jig

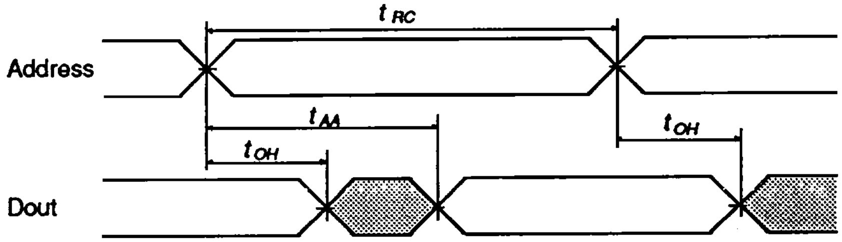
Read Cycle Timing

		-45		-55			
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*Unit*	*Note*
Read Cycle Time	t_{RC}	45	-	55	-	ns	
Address Access Time	t_{AA}	-	45	-	55	ns	
Chip Select Access Time	t_{ACS}	-	45	-	55	ns	
Output Enable to Output Valid	t_{OE}	-	23	-	30	ns	
Output Hold from Address Change	t_{OH}	5	-	5	-	ns	
Chip Selection to Output in Low Z	t_{CLZ}	10	-	10	-	ns	1
Output Enable to Output in Low Z	t_{OLZ}	0	-	0	-	ns	1
Chip Deselection to Output in High Z	t_{CHZ}	0	20	0	20	ns	1
Output Disable to Output in High Z	t_{OHZ}	0	15	0	20	ns	1

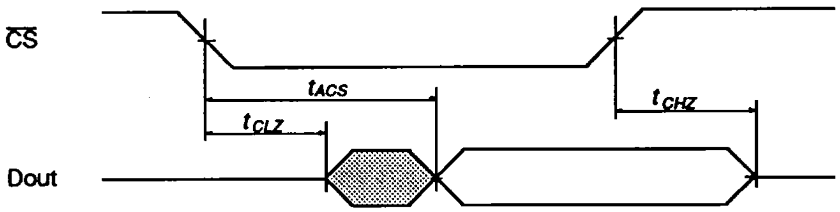
Read Cycle No.1 Timing Waveform (1,2)



Read Cycle No.2Timing Waveform (1,2,3,5)



Read Cycle No. 3Timing Waveform (1,2,4,5)



Notes:

1. Transition is measured ±200mV from steady voltage with Load B. This parameter is sampled and not 100% tested.
2. $\overline{WE}$ is High for Read Cycle.
3. Device is continuously selected, $\overline{CS}=V_{IL}$.
4. Address valid prior to or coincident with $\overline{CS}$ transition Low.
5. $\overline{OE}=V_{IL}$.

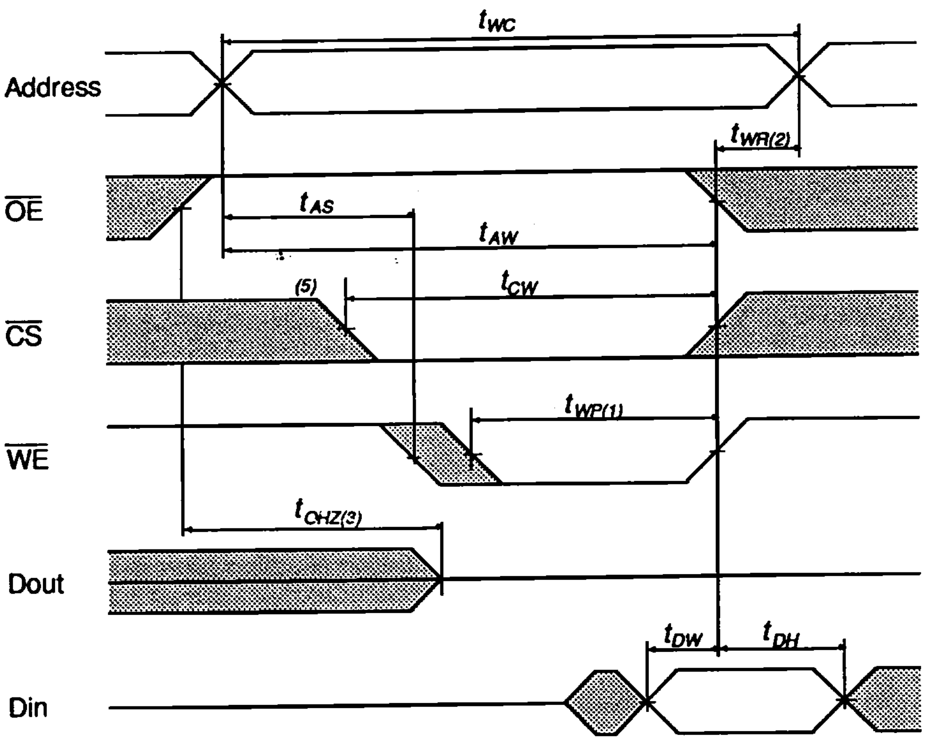
Write Cycle Timing

		-45		-55			
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*Unit*	*Note*
Write Cycle Time	t_{RC}	45	-	55	-	ns	
Chip Selection to End of Write	t_{CW}	40	-	50	-	ns	
Address Valid to End of Write	t_{AW}	40	-	50	-	ns	
Address Setup Time	t_{AS}	0	-	0	-	ns	
Write Pulse Width	t_{WP}	35	-	40	-	ns	
Write Recovery Time	t_{WR}	3	-	3	-	ns	
Write to Output in High Z	t_{WHZ}	0	15	0	20	ns	2
Data to Write Time Overlap	t_{DW}	25	-	30	-	ns	
Data Hold from Write Time	t_{DH}	0	-	0	-	ns	
Output Disable to Output in High Z	t_{OHZ}	0	15	0	20	ns	2
Output Active from End of Write	t_{OW}	0	-	0	-	ns	1

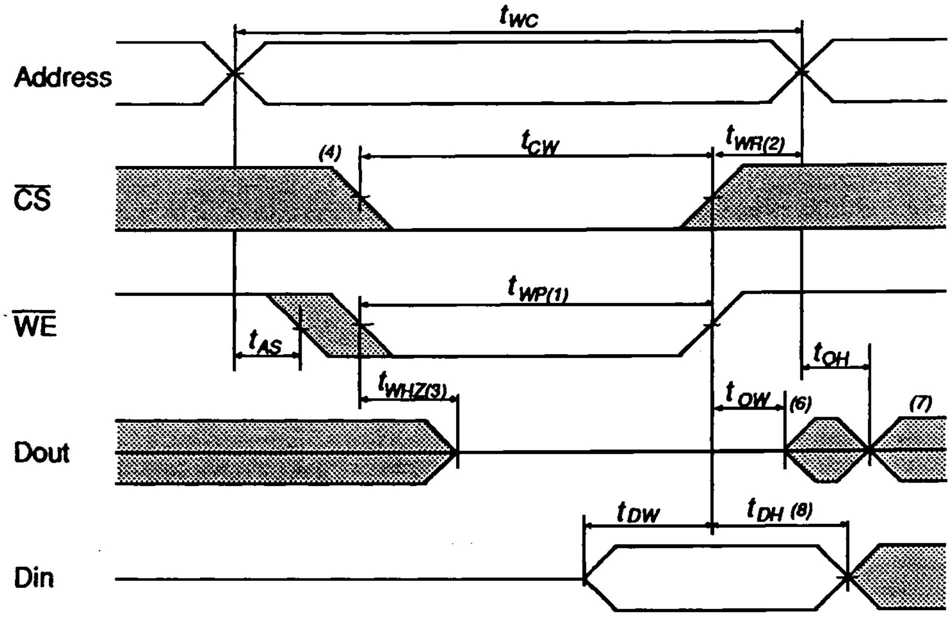
Notes:

1. Transition is measured ±200 mV from steady state voltage. This parameter is sampled and not 100% tested.
2. t_{WHZ} and t_{OHZ} are defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

Write Cycle No. 1 Timing Waveform



Write Cycle No.2 Timing Waveform (5)



Notes:

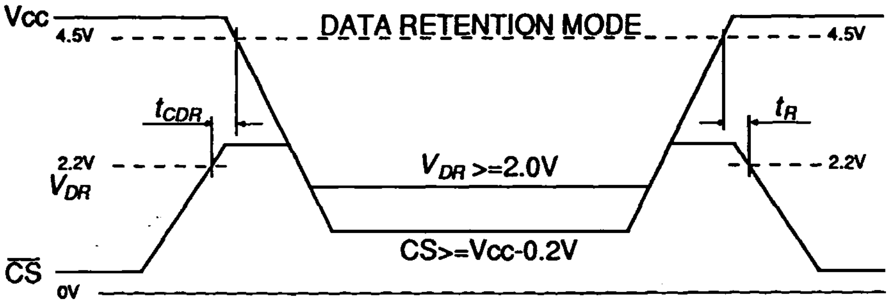
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state. Input signals out of phase must not be applied.
4. If the CS low transition occurs simultaneously with or after the $\overline{WE}$ low transition,O/P's remain in a high impedance state.
5. OE is continuously low. ($\overline{OE}=V_{IL}$)
6. Dout is in the same phase as written data of this write cycle.
7. Dout is the read data of next address.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. I/P signals out of phase must not be applied to I/O pins.

Low V_{cc} Data Retention Characteristics - L Version Only (T_A= 0 to 70°C)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS}>=V_{CC}-0.2V$	2.0	-	-	V
Data Retention Current	I_{CCDR}	$V_{CC}=3.0V$, $\overline{CS}\geq V_{CC}-0.2$	-	4	200[2]	µA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	t_{RC} [1]	-	-	ns

Notes: (1) t_{RC}=Read Cycle Time (2) V_{CC}=3.0V

Low V_{CC} Data Retention Timing Waveform



Ordering Information

MS8256FKLI-45

Speed
45 = 45 ns
55 = 55 ns

Temp. range/screening
Blank = Commercial Temp.
I = Industrial Temp.

Power Consumption
Blank = Standard Part
L = Low Power Part

Package
FK = Plastic 32 pin DIL

Organization
8256 = 256K x 8

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