128 K x 8 CMOS SRAM Module

MS8128FK-10/12/15

Issue 2.2: July 1988

PRELIMINARY INFORMATION

mosaic

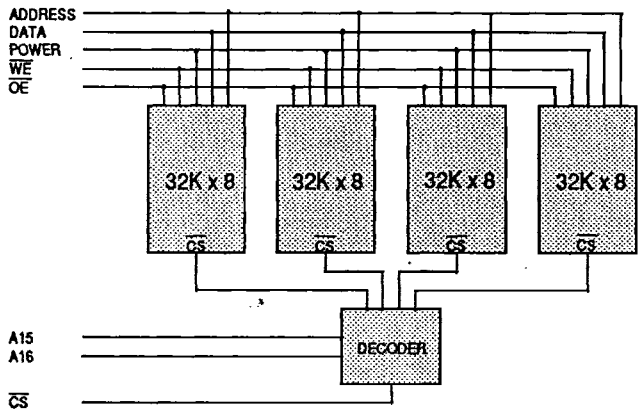
Mosaic Semiconductor Inc.

131,072 x 8 CMOS High Speed Static RAM

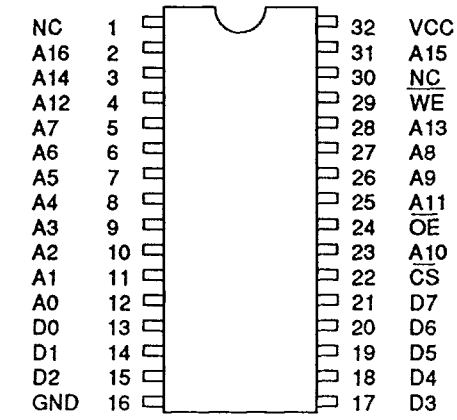
Features

- Fast Access Times of 100/120/150
- JEDEC Standard 32 pin DIL footprint
- Low Power Standby 2mW (typ.)
  40uW (typ.)- L Version
- Low Power Operation 150mW at 1MHz
- Completely Static Operation
- Equal Access and Cycle Times
- Battery back-up capability
- Directly TTL compatible
- Common data inputs & outputs

Block Diagram



Pin Definition

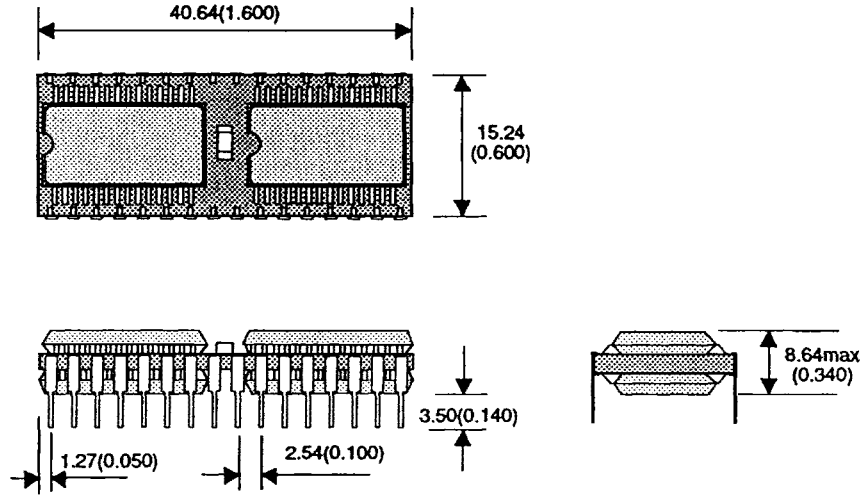


Pin Functions

A0-A16	Address Inputs
D0-7	Data Input/Output
CS	Chip Select
OE	Output Enable
WE	Write Enable
NC	No Connect
Vcc	Power (+5V)
GND	Ground

Package Details

Dimensions in mm (inches).Tolerance on all dimensions +/-0.254(0.010).



Absolute Maximum Ratings

Voltage on any pin relative to V_{ss}	V_t	-0.5V to +7	V
Power Dissipation	P_t	1	W
Storage Temperature	T_{stg}	-65 to +150	°C

Recommended Operating Conditions

		min	typ	max	
Supply Voltage	V_{cc}	4.5	5.0	5.5	V
Input High Voltage	V_{ih}	2.2	-	Vcc+0.3	V
Input Low Voltage	V_{il}	-0.3	-	0.8	V
Operating Temperature	T_a	0	-	70	°C

DC Electrical Characteristics

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current	I_{li}	V_{in}=Gnd to V_{cc}	-	-	8.0	uA
I/O Leakage Current	I_{lio}	$\overline{CS}$=V_{ih}, Vout=Gnd to Vcc	-	-	8.0	uA
Operating Power Supply Current	I_{cc}	$\overline{CS}$=V_{il}, I_{out}=0mA	-	20	45	mA
Average Power Supply Current	I_{cc1}	Min. Cycle,duty=100%,	-	50	100	mA
Standby Power	I_{sb}	$\overline{CS}$=V_{ih}	-	14	18	mA
Supply Current	I_{sb1}	$\overline{CS}$>=V_{cc}-0.2V	-	0.4	10	mA
Standby Current (LP Part)	I_{sb2}	As I_{sb1}	-	8	400	uA
Output Voltage	V_{ol}	I_{ol}=2.1mA	-	-	0.4	V
	V_{oh}	I_{oh}=-1.0mA	2.4	-	-	V

Note 1: Typical values are at V_{cc}=5.0V, T_a=25°C and specified loading.

Capacitance (V_{cc}=5V+/-10%, T_a=25°C)

Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance ($\overline{CS}$):	C_{ics}	Vin=0V	-	6	pF
I/P Capacitance (other):	C_{in}	V_{in}=0V	-	27	pF
I/O Capacitance:	$C_{I/o}$	$V_{I/o}$=0V	-	35	pF

Note: Capacitance calculated, not measured.

AC Test Conditions

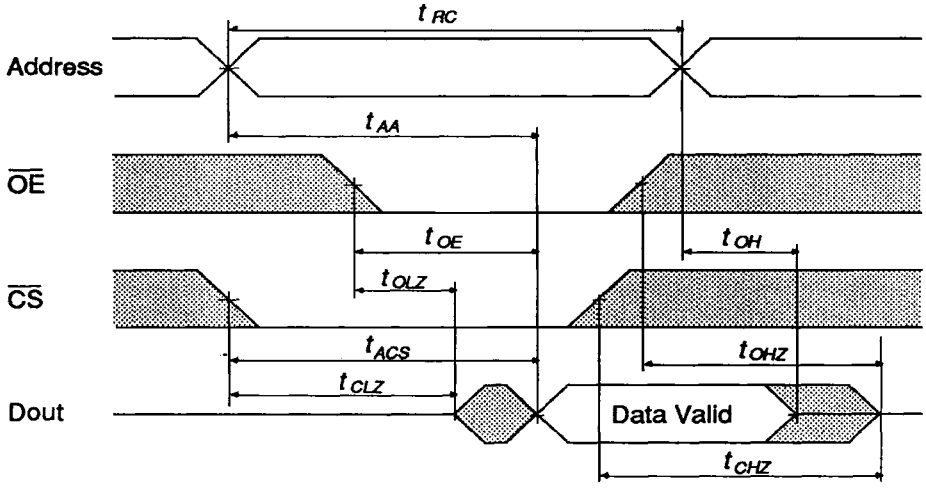
* Input pulse levels: Gnd to 3.0V* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: 1 TTL gate + 100pF
* Vcc=5V+/-10%

Electrical Characteristics & Recommended AC Operating Conditions

Read Cycle

Parameter	Symbol	10 min	10 max	12 min	12 max	15 min	15 max	Unit
Read Cycle Time	t_{RC}	100	-	120	-	150	-	ns
Address Access Time	t_{AA}	-	100	-	120	-	150	ns
Chip Select Access Time	t_{ACS}	-	100	-	120	-	150	ns
Output Enable to Output Valid	t_{OE}	-	50	-	60	-	70	ns
Output Hold from Address Change	t_{OH}	5	-	10	-	10	-	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	-	10	-	10	-	ns
Output Enable to Output in Low Z	t_{OLZ}	5	-	5	-	5	-	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	35	0	40	0	45	ns
Output Disable to Output in High Z	t_{OHZ}	0	30	0	35	0	40	ns

Read Cycle Timing Waveform (1,2)

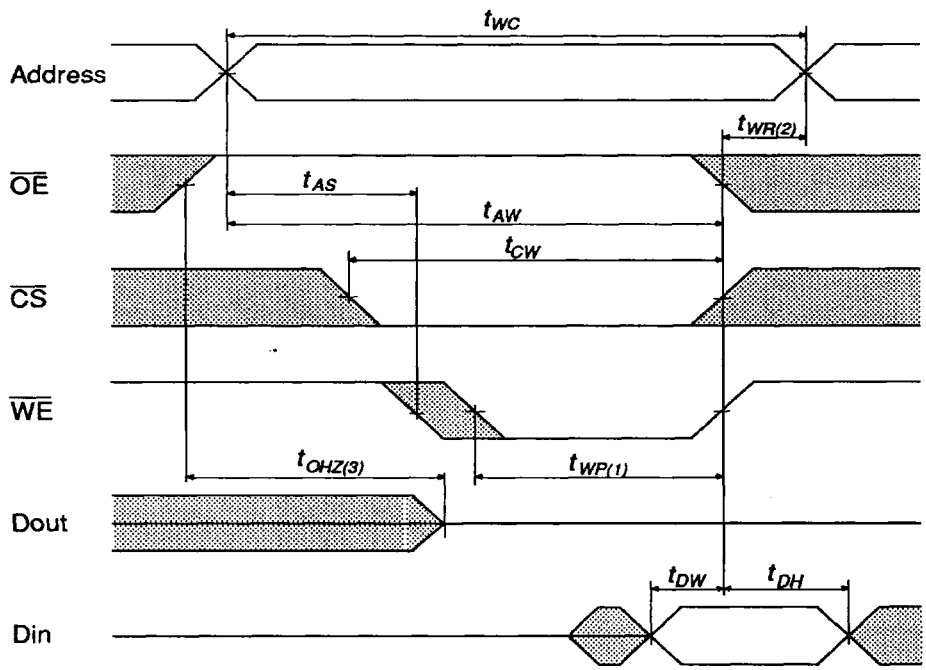


Notes:
1. $\overline{WE}$ is High for Read Cycle.
2. Address valid prior to or coincident with $\overline{CS}$ transition Low.

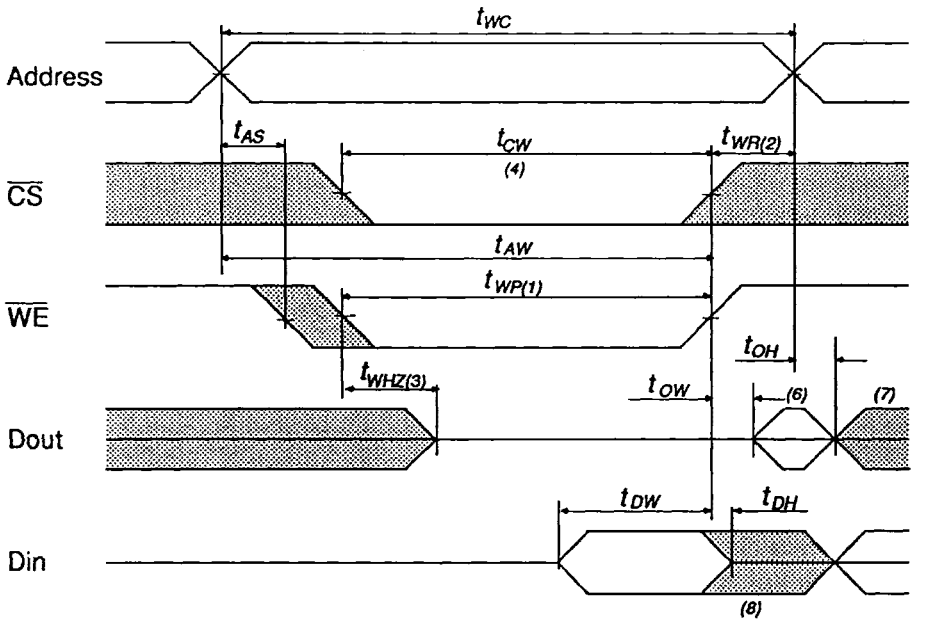
Write Cycle

Parameter	Symbol	10 min	10 max	12 min	12 max	15 min	15 max	Unit
Write Cycle Time	t_{WC}	100	-	120	-	150	-	ns
Chip Selection to End of Write	t_{CW}	90	-	105	-	115	-	ns
Address Valid to End of Write	t_{AW}	90	-	105	-	115	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	75	-	90	-	100	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Write to Output in High Z	t_{WHZ}	0	30	0	35	0	40	ns
Data to Write Time Overlap	t_{DW}	35	-	40	-	50	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Disable to Output in High Z	t_{OHZ}	0	30	0	35	0	40	ns
Output Active from End of Write	t_{OW}	5	-	5	-	5	-	ns

Write Cycle No.1 Timing Waveform



Write Cycle No.2 Timing Waveform (5)



Notes:

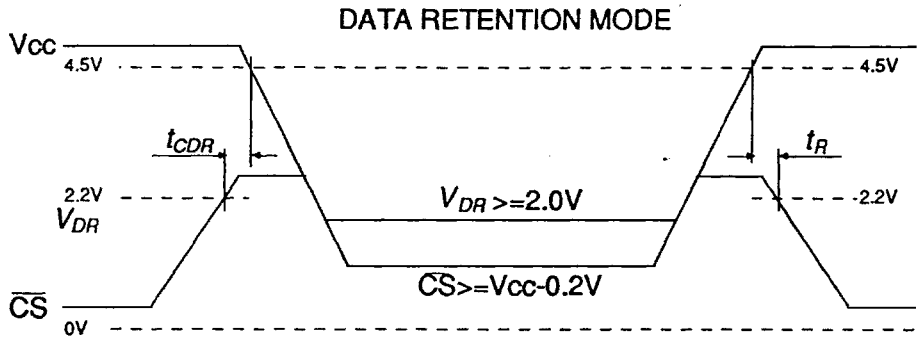
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state. Input signals out of phase must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
5. OE is continuously low. ($\overline{OE}$=Vil)
6. Dout is in the same phase as written data of this write cycle.
7. Dout is the read data of next address.
8. If CS is low during this period, I/O pins are in the output state. Input signals out of phase must not be applied to I/O pins.

Low V_{cc} Data Retention Characteristics - L Version Only (Ta=0 to +70°C)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Vcc for Data Retention	V_{DR}	$\overline{CS}$>=V_{cc}-0.2V	2.0	-	-	V
Data Retention Current	I_{CCDR}	Vcc=3.0V,$\overline{CS}$>=2.8V I/P's<=0.2V or >=2.8V	-	-	200	uA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	t_{RC}*	-	-	ns

* t_{RC}=Read Cycle Time

Low Vcc Retention Timing Diagram - L Version Only



Ordering Information

MS8128FKL-10

Speed	100,120,150 ns
Temp. range/ screening	Blank = Commercial Temp. I = Industrial Temp.
Power Consumption	Blank = Standard Power Part L = Low Power Part
Package	FK = 600 mil 32 pin Plastic DIP

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