mosaic

Mosaic Semiconductor Inc.

128 K x 8 SRAM Module

MS8128FK-35/45/55

Issue 1.0 April 1990

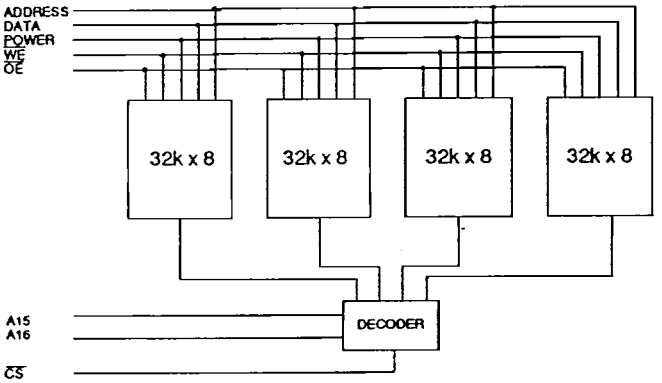
ADVANCE PRODUCT INFORMATION

131,072 x 8 CMOS High Speed Static RAM

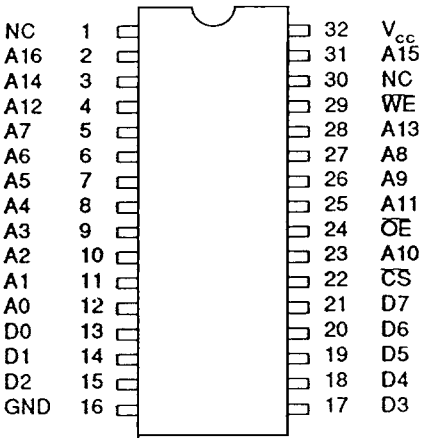
Features

- Fast Access Times of 35,45,55 ns
- JEDEC Standard 32 pin DIL Footprint
- Low Power Standby 8.8mW (max)
- Low Power Operation 150mW (typ.) at 1MHz
- Completely Static Operation
- Equal Access and Cycle Times
- Battery Back-up Capability
- Directly TTL Compatible
- Common Data Inputs & Outputs
- Onboard Decoupling Capacitors

Block Diagram



Pin Definition

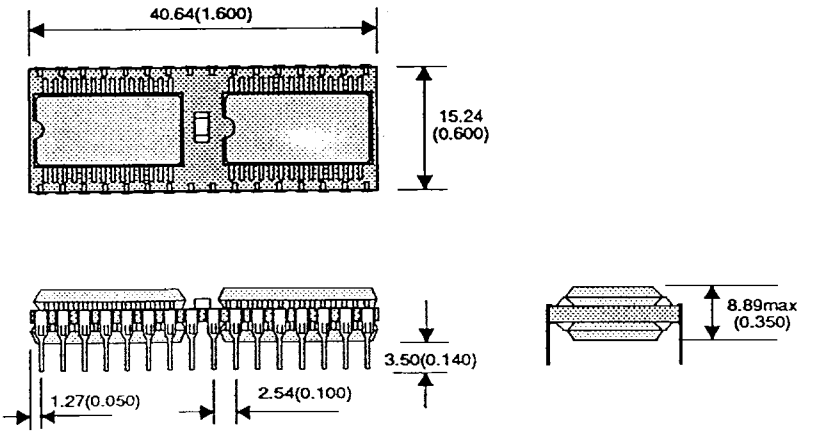


Pin Functions

A0-A16	Address Inputs
D0-7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
NC	No Connect
V_{CC}	Power (+5V)
GND	Ground

Package Details

Dimensions in mm (inches). Tolerance on all dimensions +/-0.254(0.010).



Absolute Maximum Ratings

Voltage on any pin relative to V_{ss}	V_t	-0.5V to +7	V
Power Dissipation	P_t	1	W
Storage Temperature	T_{stg}	-65 to +150	°C

Recommended Operating Conditions

		min	typ	max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5	V
Input Low Voltage	V_{IL}	-0.5	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (8128FKI)

Note: V_t can be -3.0V pulse of less than 20ns.

DC Electrical Characteristics

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current	I_{LI}	V_{IN}=GND to V_{CC}	-	-	8.0	uA
I/O Leakage Current	I_{LIO}	$\overline{CS}$=V_{IH}, V_{OUT}=GND to V_{CC}	-	-	8.0	uA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, I_{OUt}=0mA, f=0Hz	-	30	89	mA
Average Supply Current	I_{CC1}	$\overline{CS}$=V_{IL}, I_{OUT}=0mA f= f_{MAX}	-	-	144	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}	-	-	12	mA
	I_{SB1}	$\overline{CS}$>=V_{cc}-0.2V	-	-	1.6	mA
Output Voltage	V_{OL}	I_{OL}= 8mA	-	-	0.4	V
	V_{OH}	I_{OH}= -4.0mA	2.4	-	-	V

Note 1: Typical values are at V_{cc}=5.0V, T_a=25°C and specified loading.

Capacitance (V_{cc}=5V+/-10%, T_a=25°C)

Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance($\overline{CS}$) :	C_{IN}	V_{in}=0V	-	4.5	pF
Input Capacitance(other):	C_{IN}	V_{IN}=0V	-	44	pF
I/O Capacitance:	$C_{I/O}$	$V_{i/o}$=0V	-	44	pF

Note: Capacitance calculated, not measured.

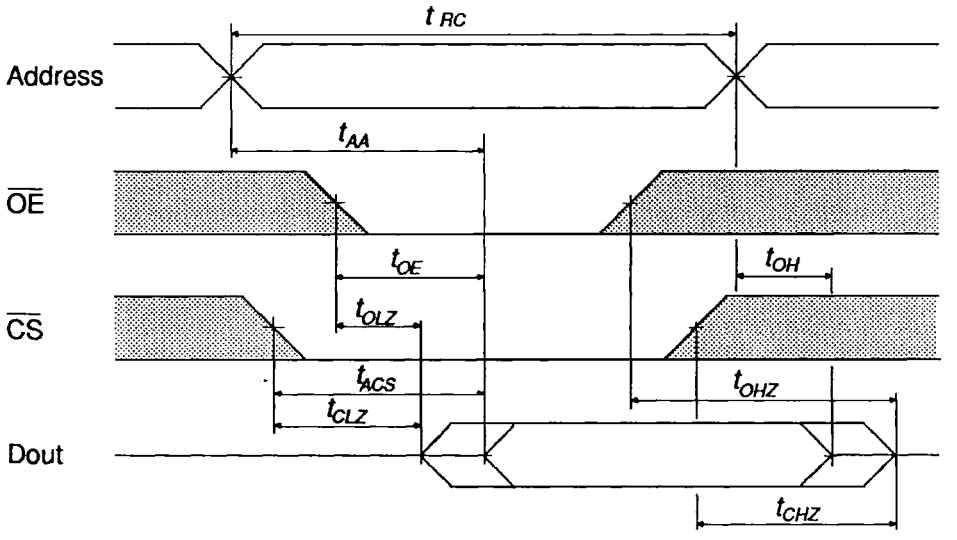
AC Test Conditions

* Input pulse levels: GND to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: 1 TTL gate + 100pF
* Vcc=5V+/-10%

Read Cycle Timing

Parameter	Symbol	-35 min	-35 max	-45 min	-45 max	-55 min	-55 max	Unit
Read Cycle Time	t_{RC}	35	-	45	-	55	-	ns
Address Access Time	t_{AA}	-	35	-	45	-	55	ns
Chip Select Access Time	t_{ACS}	-	35	-	45	-	55	ns
Output Enable to Output Valid	t_{OE}	-	15	-	20	-	25	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	5	-	ns
Chip Selection to Output in Low Z	t_{CLZ}	5	-	5	-	5	-	ns
Output Enable to Output in Low Z	t_{OLZ}	2	-	0	-	0	-	ns
Chip Deselection to Output in High Z	t_{CHZ}	-	15	-	20	-	25	ns
Output Disable to Output in High Z	t_{OHZ}	-	15	-	20	-	25	ns

Read Cycle Timing Waveform (1,2)

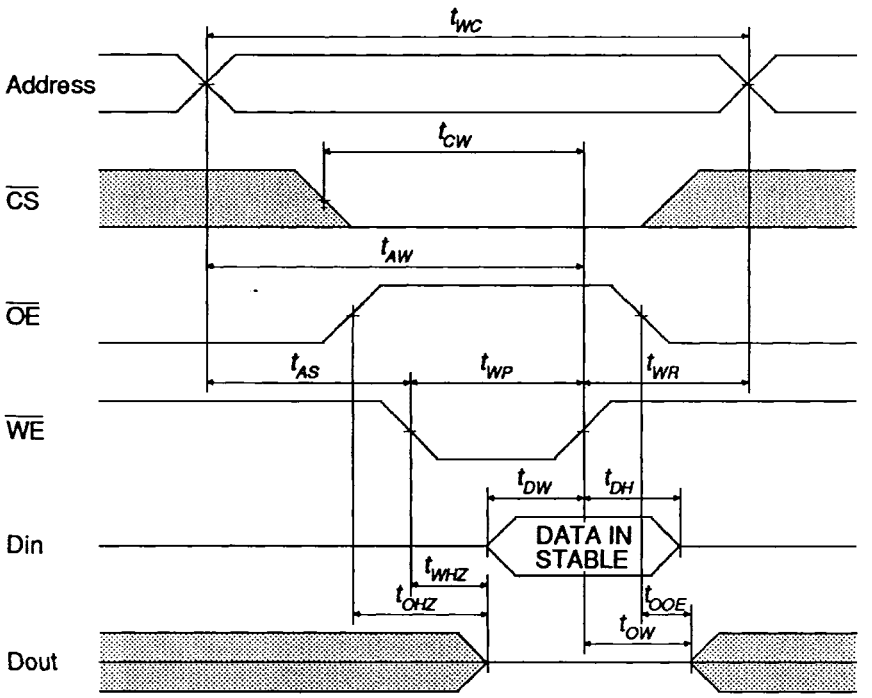


Notes:
1. $\overline{WE}$ is High for Read Cycle.
2. Address valid prior to or coincident with $\overline{CS}$ transition Low.

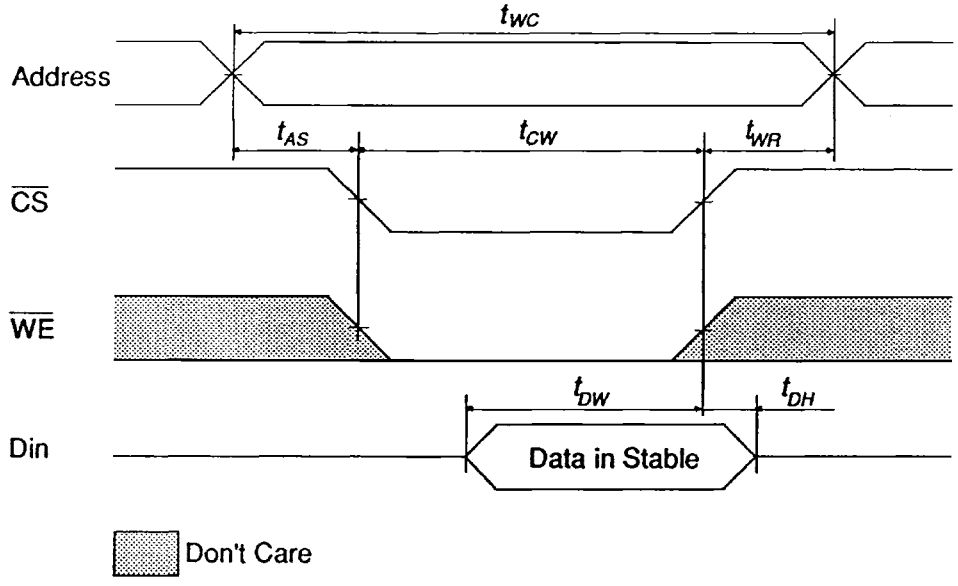
Write Cycle

Parameter	Symbol	-35 min	-35 max	-45 min	-45 max	-55 min	-55 max	Unit
Write Cycle Time	t_{WC}	35	-	45	-	55	-	ns
Chip Selection to End of Write	t_{CW}	30	-	40	-	50	-	ns
Address Valid to End of Write	t_{AW}	30	-	40	-	50	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	30	-	35	-	40	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Write to Output in High Z	t_{WHZ}	-	15	-	20	-	25	ns
Data to Write Time Overlap	t_{DW}	15	-	20	-	25	-	ns
Data Hold from Write Time(WE)	t_{DH}	0	-	0	-	0	-	ns
Output Disable to Output in High Z	t_{OHZ}	-	15	-	20	-	25	ns
Output Active from End of Write	t_{OW}	5	-	5	-	5	-	ns

Write Cycle No.1 Timing Waveform



Write Cycle No.2 Timing Waveform



Notes:

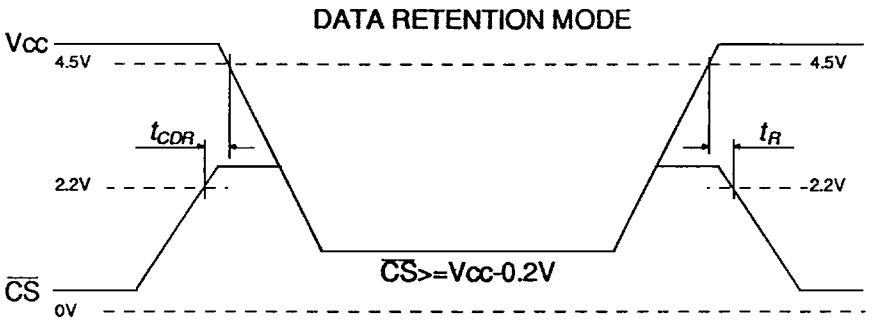
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state. Input signals out of phase must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE}$=Vil)
6. Dout is in the same phase as written data of this write cycle.
7. Dout is the read data of next address.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Input signals out of phase must not be applied to I/O pins.

Low V_{cc} Data Retention Characteristics - L Version Only (Ta=0 to +70°C)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Vcc for Data Retention	V_{DR}	$\overline{CS}$>=V_{cc}-0.2V	2.0	-	-	V
Data Retention Current	I_{CCDR1}	Vcc=3.0V,$\overline{CS}$>=2.8V I/P's<=0.2V or >=2.8V	-	-	800	µA
	I_{CCDR2}	Vcc= 2.0V	-	-	480	µA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	t_{RC}*	-	-	ns

* t_{RC}=Read Cycle Time

Low V_{cc} Data Retention Timing Waveform - L Version Only



Ordering Information

MS8128FKLI-45

Speed	35,45,55 ns	
Temperature Range	Blank	= Commercial Temp.
	I	= Industrial Temp.
Power Consumption	Blank	= Standard Power Part
	L	= Low Power Part
Package	FK	= 32 Pin 600 mil Plastic DIP

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