

ML12015
ML12016
ML12017
Dual Modulus Prescaler

MECL PLL COMPONENTS

SEMICONDUCTOR TECHNICAL DATA

Legacy Device: Motorola MC12015, MC12016, MC12017

The ML12015, ML12016 and ML12017 are dual modulus prescalers which will drive divide by 32 and 33, 40 and 41, and 64 and 65, respectively. An internal regulator is provided to allow these devices to be used over a wide range of power–supply voltages. The devices may be operated by applying a supply voltage of 5.0 Vdc $\pm 10\%$ at Pin 7, or by applying an unregulated voltage source from 5.5 Vdc to 9.5 Vdc to Pin 8.

- 225 MHz Toggle Frequency
- Low-Power 7.5 mA Maximum at 6.8 V
- Control Input and Output Are Compatible With Standard CMOS
- Connecting Pins 2 and 3 Allows Driving One TTL Load
- Supply Voltage 4.5 V to 9.5 V
- Operating Temperature Range $T_A = -40$ to $85^{\circ}C$

P DIP 8 = PP PLASTIC PACKAGE CASE 626–04



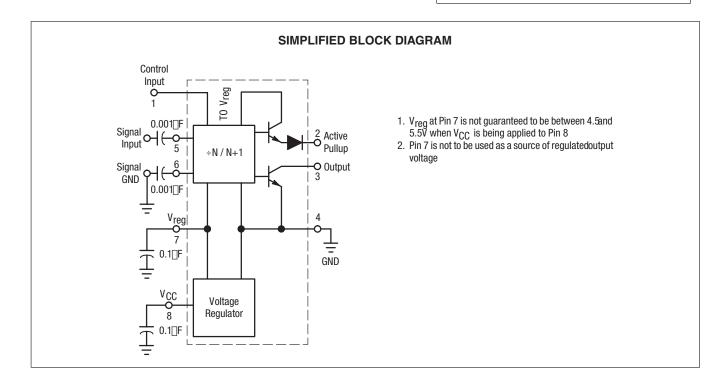


SO 8 = -5P
PLASTIC PACKAGE
CASE 751
(SO-8)

CROSS REFERENCE/ORDERING INFORMATION

PACKAGE	MOTOROLA	LANSDALE
P-DIP 8	MC12015P	ML12015PP
SO8	MC12015D	ML12015-5P
P-DIP 8	MC12016P	ML12016PP
SO 8	MC12016D	ML12016-5P
P-DIP 8	MC12017P	ML12017PP
SO 8	MC12017D	ML12017-5P

Note: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Regulated Voltage, Pin 7	V _{reg}	8.0	Vdc
Power Supply Voltage, Pin 8	VCC	10	Vdc
Operating Temperature Range	T _A	-40 to +85	C
Storage Temperature Range	T _{stg}	T _{stg} -65 to +175	

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.5 \text{ to } 9.5 \text{ V}; V_{req} = 4.5 \text{ to } 5.5 \text{ V}; T_A = -40 \text{ to } 85 \text{ C}, \text{ unless otherwise noted.}$)

Characteristic	Symbol	Min	Тур	Max	Unit
Toggle Frequency (Sine Wave Input)					MHz
	fmax	225	_	-	
	fmin	-	-	35	
Supply Current	ICC	-	6.0	7.8	mA
Control Input HIGH (☐32, 40 or 64)	VIH	2.0	-	-	V
Control Input LOW (□33, 41 or 65)	VIL	-	-	0.8	V
Output Voltage HIGH (I _{SOUrce} = 50∏A) [Nofe 1]	VOH	2.5	-	-	V
Output Voltage LOW (I _{sink} = 2mA) [Note 1]	V _{OL}	_	_	0.5	V
Input Voltage Sensitivity	V _{in}				mVpp
35 MHz		400	_	800	
50 to 225 MHz		200	-	800	
PLL Response Time [Notes 2 and 3]	tpLL	_	_	t _{out} to 70	ns

NOTES: 1. Pin 2 connected to Pin 3.

2. tp_L = the period of time the PLL has from the prescaler rising output tranistion (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection.

3. tout = period of output waveform.

Figure 1. Generic block diagram showing prescaler connection to PLL device

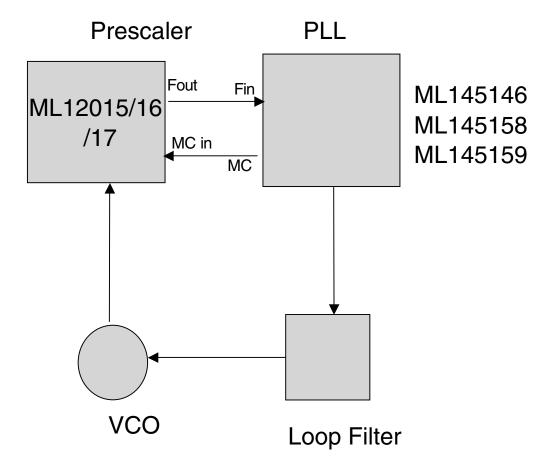
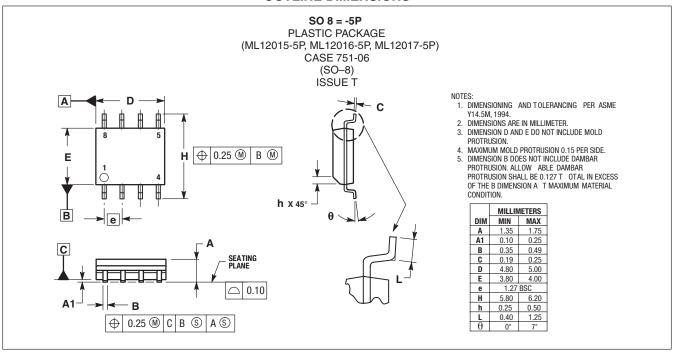
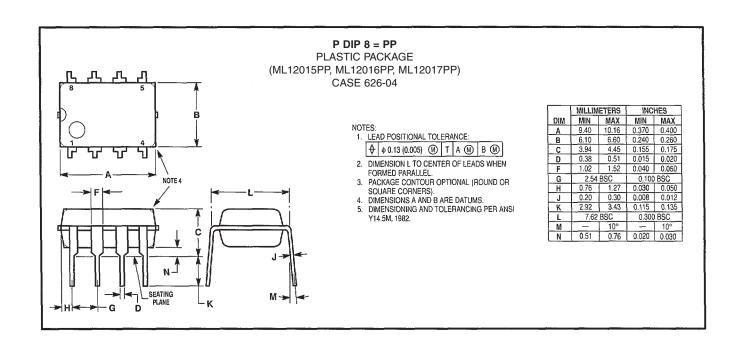


Figure 1. shows a generic block diagram for connecting a prescaler to a PLL device that supports dual modulus control. Application note AN535 decribes using a two-modulus prescaler technique.By using prescaler higher frequencies can be achieve than by a single CMOS PLL device.

OUTLINE DIMENSIONS





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