

General Description

The 932SQ420D is a main clock synthesizer for Romley-generation Intel based server platforms. The 932SQ420D is driven with a 25 MHz crystal for maximum performance. It generates CPU outputs of 100 or 133.33 MHz.

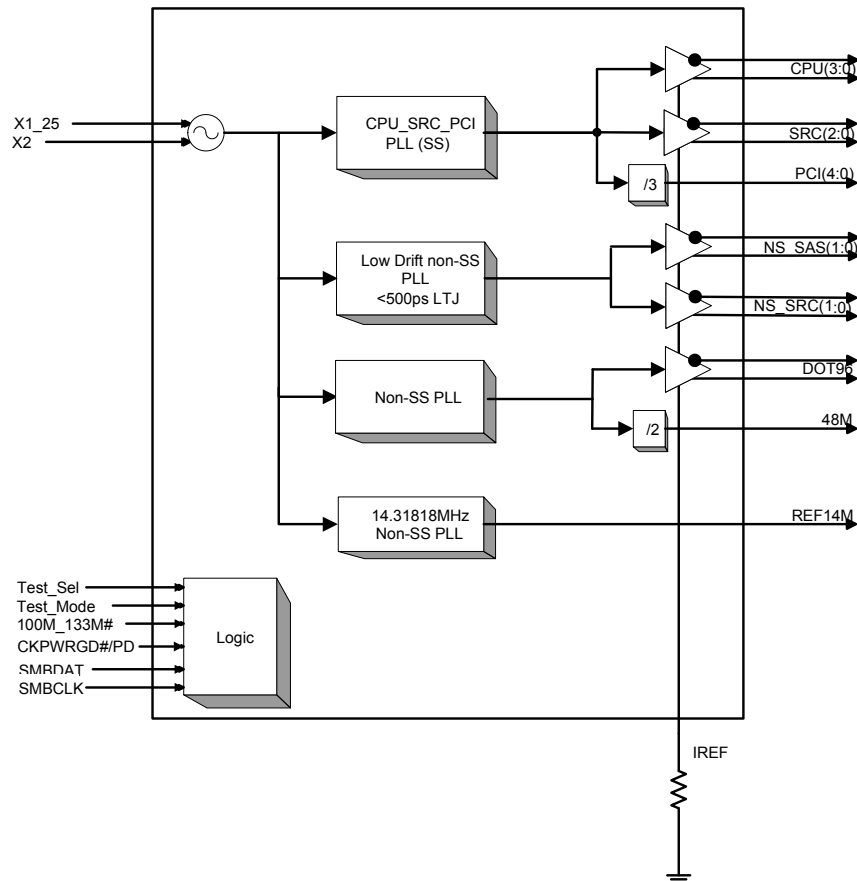
Recommended Application

CK420BQ

Output Features

- 4 - HCSL CPU outputs
- 4 - HCSL Non-Spread SAS/SRC outputs
- 3 - HCSL SRC outputs
- 1 - HCSL DOT96 output
- 1 - 3.3V 48M output
- 5 - 3.3V PCI outputs
- 1- 3.3V REF output

Block Diagram



Features/Benefits

- 0.5% down spread capable on CPU/SRC/PCI outputs/Lower EMI
- 64-pin TSSOP and MLF packages/Space Savings

Key Specifications

- Cycle to cycle jitter: CPU/SRC/NS_SRC/NS_SAS < 50ps.
- Phase jitter: PCIe Gen2 < 3ps rms, Gen3 < 1ps rms
- Phase jitter: QPI 9.6GB/s < 0.2ps rms
- Phase jitter: NS-SAS < 0.4ps rms using raw phase data
- Phase jitter: NS-SAS < 1.3ps rms using Clk Jit Tool 1.6.3

Pin Configuration - 64TSSOP

| | | | | |
|--------------------------------|----|----------|----|-------------|
| SMBCLK | 1 | 932SQ420 | 64 | SMBDAT |
| GND14 | 2 | | 63 | VDDCPU |
| AVDD14 | 3 | | 62 | CPU3T |
| VDD14 | 4 | | 61 | CPU3C |
| ^v REF14_3x/TEST_SEL | 5 | | 60 | CPU2T |
| GND14 | 6 | | 59 | CPU2C |
| GNDXTAL | 7 | | 58 | GNDCPU |
| X1_25 | 8 | | 57 | VDDCPU |
| X2_25 | 9 | | 56 | CPU1T |
| VDDXTAL | 10 | | 55 | CPU1C |
| GNDPCI | 11 | | 54 | CPU0T |
| VDDPCI | 12 | | 53 | CPU0C |
| PCI4_2x | 13 | | 52 | GNDNS |
| PCI3_2x | 14 | | 51 | AVDD_NS_SAS |
| PCI2_2x | 15 | | 50 | NS_SAS1T |
| PCI1_2x | 16 | | 49 | NS_SAS1C |
| PCI0_2x | 17 | | 48 | NS_SAS0T |
| GNDPCI | 18 | | 47 | NS_SAS0C |
| VDDPCI | 19 | | 46 | GNDNS |
| VDD48 | 20 | | 45 | VDDNS |
| [^] 48M_2x/100M_133M# | 21 | | 44 | NS_SRC1T |
| GND48 | 22 | | 43 | NS_SRC1C |
| GND96 | 23 | | 42 | NS_SRC0T |
| DOT96T | 24 | | 41 | NS_SRC0C |
| DOT96C | 25 | | 40 | IREF |
| AVDD96 | 26 | | 39 | GNDSRC |
| TEST_MODE | 27 | | 38 | AVDD_SRC |
| CKPWRGD#/PD | 28 | | 37 | VDDSRC |
| VDDSRC | 29 | | 36 | SRC2T |
| SRC0T | 30 | | 35 | SRC2C |
| SRC0C | 31 | | 34 | SRC1T |
| GNDSRC | 32 | | 33 | SRC1C |

64-TSSOP

Note: Pins with ^ prefix have internal 120K pullup
Pins with v prefix have internal 120K pulldown

Spread Spectrum Control

| SS_Enable (B1b0) | CPU, SRC & PCI |
|---------------------|-------------------|
| 0 | OFF |
| 1 | ON |

932SQ420 Power Down Functionality

| CKPWRGD#/PD | Differential Outputs | Single-ended Outputs | Single ended Outputs w/Latch |
|-------------|-------------------------|-------------------------|---------------------------------|
| 1 | Hi-Z ¹ | Low | Low ² |
| 0 | Running | | |

1. Hi-Z on the differential outputs will result in both True and Complement being low due to the termination network
2. These outputs are Hi-Z after VDD is applied and before the first assertion of CKPWRGD#.

Power Group Pin Numbers

| MLF | | TSSOP | | Description |
|--------|------|--------|--------|--|
| VDD | GND | VDD | GND | |
| 57 | 56 | 3 | 2 | 14MHz PLL Analog |
| 58 | 60 | 4 | 6 | REF14M Output and Logic |
| 64 | 61 | 10 | 7 | 25MHz XTAL |
| 2, 9 | 1, 8 | 12, 19 | 11, 18 | PCI Outputs and Logic |
| 10 | 12 | 20 | 22 | 48MHz Output and Logic |
| 16 | 13 | 26 | 23 | 96MHz PLL Analog, Output and Logic |
| 19, 27 | 22 | 29, 37 | 32 | SRC Outputs and Logic |
| 28 | 29 | 38 | 39 | SRC PLL Analog |
| 35 | 36 | 45 | 46 | Non-Spreading Differential Outputs & Logic |
| 41 | 42 | 51 | 52 | NS-SAS/SRC PLL Analog |
| 47, 53 | 48 | 57,63 | 58 | CPU Outputs and Logic |

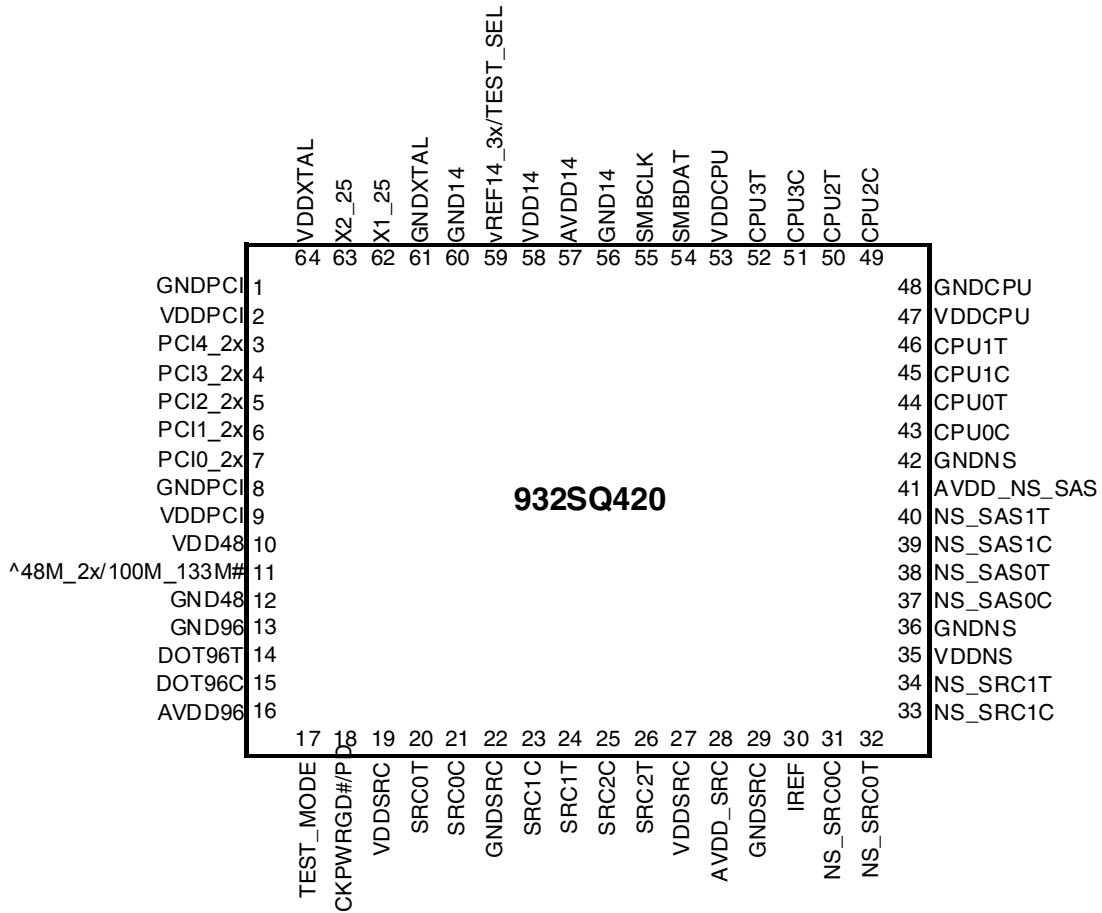
Pin Descriptions - 64 TSSOP

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|--------------------|------|---|
| 1 | SMBCLK | IN | Clock pin of SMBUS circuitry, 5V tolerant |
| 2 | GND14 | PWR | Ground pin for 14MHz output and logic. |
| 3 | AVDD14 | PWR | Analog power pin for 14MHz PLL |
| 4 | VDD14 | PWR | Power pin for 14MHz output and logic |
| 5 | vREF14_3x/TEST_SEL | I/O | 14.318 MHz reference clock. 3X drive strength as default / TEST_SEL latched input to enable test mode. Refer to Test Clarification Table. This pin has a weak (~120Kohm) internal pull down. |
| 6 | GND14 | PWR | Ground pin for 14MHz output and logic. |
| 7 | GNDXTAL | PWR | Ground pin for Crystal Oscillator. |
| 8 | X1_25 | IN | Crystal input, Nominally 25.00MHz. |
| 9 | X2_25 | OUT | Crystal output, Nominally 25.00MHz. |
| 10 | VDDXTAL | PWR | 3.3V power for the crystal oscillator. |
| 11 | GNDPCI | PWR | Ground pin for PCI outputs and logic. |
| 12 | VDDPCI | PWR | 3.3V power for the PCI outputs and logic |
| 13 | PCI4_2x | OUT | 3.3V PCI clock output |
| 14 | PCI3_2x | OUT | 3.3V PCI clock output |
| 15 | PCI2_2x | OUT | 3.3V PCI clock output |
| 16 | PCI1_2x | OUT | 3.3V PCI clock output |
| 17 | PCI0_2x | OUT | 3.3V PCI clock output |
| 18 | GNDPCI | PWR | Ground pin for PCI outputs and logic. |
| 19 | VDDPCI | PWR | 3.3V power for the PCI outputs and logic |
| 20 | VDD48 | PWR | 3.3V power for the 48MHz output and logic |
| 21 | ^48M_2x/100M_133M# | I/O | 3.3V 48MHz output/ 3.3V tolerant CPU frequency select latched input pin. See ViiFS and VihFS values for thresholds. This pin has a weak (~120Kohm) internal pull up. 1 = 100MHz, 0 = 133MHz operating frequency |
| 22 | GND48 | PWR | Ground pin for 48MHz output and logic. |
| 23 | GND96 | PWR | Ground pin for DOT96 output and logic. |
| 24 | DOT96T | OUT | True clock of differential 96MHz output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 25 | DOT96C | OUT | Complementary clock of differential 96MHz output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 26 | AVDD96 | PWR | 3.3V power for the 48/96MHz PLL and the 96MHz output and logic |
| 27 | TEST_MODE | IN | TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table. |
| 28 | CKPWRGD#/PD | IN | CKPWRGD# is an active low input used to sample latched inputs and allow the device to Power Up. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLLs are stopped. |
| 29 | VDDSRC | PWR | 3.3V power for the SRC outputs and logic |
| 30 | SRC0T | OUT | True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 31 | SRC0C | OUT | Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 32 | GNDSRC | PWR | Ground pin for SRC outputs and logic. |
| 33 | SRC1C | OUT | Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 34 | SRC1T | OUT | True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 35 | SRC2C | OUT | Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 36 | SRC2T | OUT | True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 37 | VDDSRC | PWR | 3.3V power for the SRC outputs and logic |
| 38 | AVDD_SRC | PWR | 3.3V power for the SRC PLL analog circuits |
| 39 | GNDSRC | PWR | Ground pin for SRC outputs and logic. |
| 40 | IREF | OUT | This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value. |

Pin Descriptions - 64 TSSOP(cont.)

| | | | |
|----|-------------|-----|---|
| 41 | NS_SRC0C | OUT | Complementary clock of differential non-spreading SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 42 | NS_SRC0T | OUT | True clock of differential non-spreading SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 43 | NS_SRC1C | OUT | Complementary clock of differential non-spreading SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 44 | NS_SRC1T | OUT | True clock of differential non-spreading SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 45 | VDDNS | PWR | 3.3V power for the Non-Spreading differential outputs outputs and logic |
| 46 | GNDNS | PWR | Ground pin for non-spreading differential outputs and logic. |
| 47 | NS_SAS0C | OUT | Complementary clock of differential non-spreading SAS output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 48 | NS_SAS0T | OUT | True clock of differential non-spreading SAS output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 49 | NS_SAS1C | OUT | Complementary clock of differential non-spreading SAS output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 50 | NS_SAS1T | OUT | True clock of differential non-spreading SAS output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 51 | AVDD_NS_SAS | PWR | 3.3V power for the non-spreading SAS/SRC PLL analog circuits. |
| 52 | GNDNS | PWR | Ground pin for non-spreading differential outputs and logic. |
| 53 | CPU0C | OUT | Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 54 | CPU0T | OUT | True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 55 | CPU1C | OUT | Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 56 | CPU1T | OUT | True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 57 | VDDCPU | PWR | 3.3V power for the CPU outputs and logic |
| 58 | GNDCPU | PWR | Ground pin for CPU outputs and logic. |
| 59 | CPU2C | OUT | Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 60 | CPU2T | OUT | True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 61 | CPU3C | OUT | Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 62 | CPU3T | OUT | True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 63 | VDDCPU | PWR | 3.3V power for the CPU outputs and logic |
| 64 | SMBDAT | I/O | Data pin of SMBUS circuitry, 5V tolerant |

Pin Configuration - 64 MLF



Note: Pins with ^ prefix have internal 120K pullup
 Pins with v prefix have internal 120K pulldown

Pin Descriptions - 64 MLF

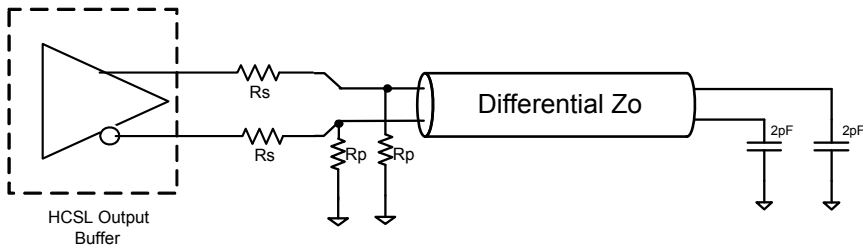
| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|--------------------|------|---|
| 1 | GNDPCI | PWR | Ground pin for PCI outputs and logic. |
| 2 | VDDPCI | PWR | 3.3V power for the PCI outputs and logic |
| 3 | PCI4_2x | OUT | 3.3V PCI clock output |
| 4 | PCI3_2x | OUT | 3.3V PCI clock output |
| 5 | PCI2_2x | OUT | 3.3V PCI clock output |
| 6 | PCI1_2x | OUT | 3.3V PCI clock output |
| 7 | PCI0_2x | OUT | 3.3V PCI clock output |
| 8 | GNDPCI | PWR | Ground pin for PCI outputs and logic. |
| 9 | VDDPCI | PWR | 3.3V power for the PCI outputs and logic |
| 10 | VDD48 | PWR | 3.3V power for the 48MHz output and logic |
| 11 | ^48M_2x/100M_133M# | I/O | 3.3V 48MHz output/ 3.3V tolerant CPU frequency select latched input pin. See ViIFS and VihFS values for thresholds. This pin has a weak (~120Kohm) internal pull up. 1 = 100MHz, 0 = 133MHz operating frequency |
| 12 | GND48 | PWR | Ground pin for 48MHz output and logic. |
| 13 | GND96 | PWR | Ground pin for DOT96 output and logic. |
| 14 | DOT96T | OUT | True clock of differential 96MHz output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 15 | DOT96C | OUT | Complementary clock of differential 96MHz output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 16 | AVDD96 | PWR | 3.3V power for the 48/96MHz PLL and the 96MHz output and logic |
| 17 | TEST_MODE | IN | TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table. |
| 18 | CKPWRGD#/PD | IN | CKPWRGD# is an active low input used to sample latched inputs and allow the device to Power Up. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLLs are stopped. |
| 19 | VDDSRC | PWR | 3.3V power for the SRC outputs and logic |
| 20 | SRC0T | OUT | True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 21 | SRC0C | OUT | Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 22 | GNDSRC | PWR | Ground pin for SRC outputs and logic. |
| 23 | SRC1C | OUT | Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 24 | SRC1T | OUT | True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 25 | SRC2C | OUT | Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 26 | SRC2T | OUT | True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 27 | VDDSRC | PWR | 3.3V power for the SRC outputs and logic |
| 28 | AVDD_SRC | PWR | 3.3V power for the SRC PLL analog circuits |
| 29 | GNDSRC | PWR | Ground pin for SRC outputs and logic. |
| 30 | IREF | OUT | This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value. |
| 31 | NS_SRC0C | OUT | Complementary clock of differential non-spreading SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 32 | NS_SRC0T | OUT | True clock of differential non-spreading SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 33 | NS_SRC1C | OUT | Complementary clock of differential non-spreading SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 34 | NS_SRC1T | OUT | True clock of differential non-spreading SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |

Pin Descriptions - 64 MLF (cont).

| | | | |
|----|--------------------|-----|---|
| 35 | VDDNS | PWR | 3.3V power for the Non-Spreading differential outputs outputs and logic |
| 36 | GNDNS | PWR | Ground pin for non-spreading differential outputs and logic. |
| 37 | NS_SAS0C | OUT | Complementary clock of differential non-spreading SAS output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 38 | NS_SAS0T | OUT | True clock of differential non-spreading SAS output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 39 | NS_SAS1C | OUT | Complementary clock of differential non-spreading SAS output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 40 | NS_SAS1T | OUT | True clock of differential non-spreading SAS output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 41 | AVDD_NS_SAS | PWR | 3.3V power for the non-spreading SAS/SRC PLL analog circuits. |
| 42 | GNDNS | PWR | Ground pin for non-spreading differential outputs and logic. |
| 43 | CPU0C | OUT | Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 44 | CPU0T | OUT | True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 45 | CPU1C | OUT | Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 46 | CPU1T | OUT | True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 47 | VDDCPU | PWR | 3.3V power for the CPU outputs and logic |
| 48 | GNDCPU | PWR | Ground pin for CPU outputs and logic. |
| 49 | CPU2C | OUT | Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 50 | CPU2T | OUT | True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 51 | CPU3C | OUT | Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 52 | CPU3T | OUT | True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 53 | VDDCPU | PWR | 3.3V power for the CPU outputs and logic |
| 54 | SMBDAT | I/O | Data pin of SMBUS circuitry, 5V tolerant |
| 55 | SMBCLK | IN | Clock pin of SMBUS circuitry, 5V tolerant |
| 56 | GND14 | PWR | Ground pin for 14MHz output and logic. |
| 57 | AVDD14 | PWR | Analog power pin for 14MHz PLL |
| 58 | VDD14 | PWR | Power pin for 14MHz output and logic |
| 59 | vREF14_3x/TEST_SEL | I/O | 14.318 MHz reference clock. 3X drive strength as default / TEST_SEL latched input to enable test mode. Refer to Test Clarification Table. This pin has a weak (~120Kohm) internal pull down. |
| 60 | GND14 | PWR | Ground pin for 14MHz output and logic. |
| 61 | GNDXTAL | PWR | Ground pin for Crystal Oscillator. |
| 62 | X1_25 | IN | Crystal input, Nominally 25.00MHz. |
| 63 | X2_25 | OUT | Crystal output, Nominally 25.00MHz. |
| 64 | VDDXTAL | PWR | 3.3V power for the crystal oscillator. |

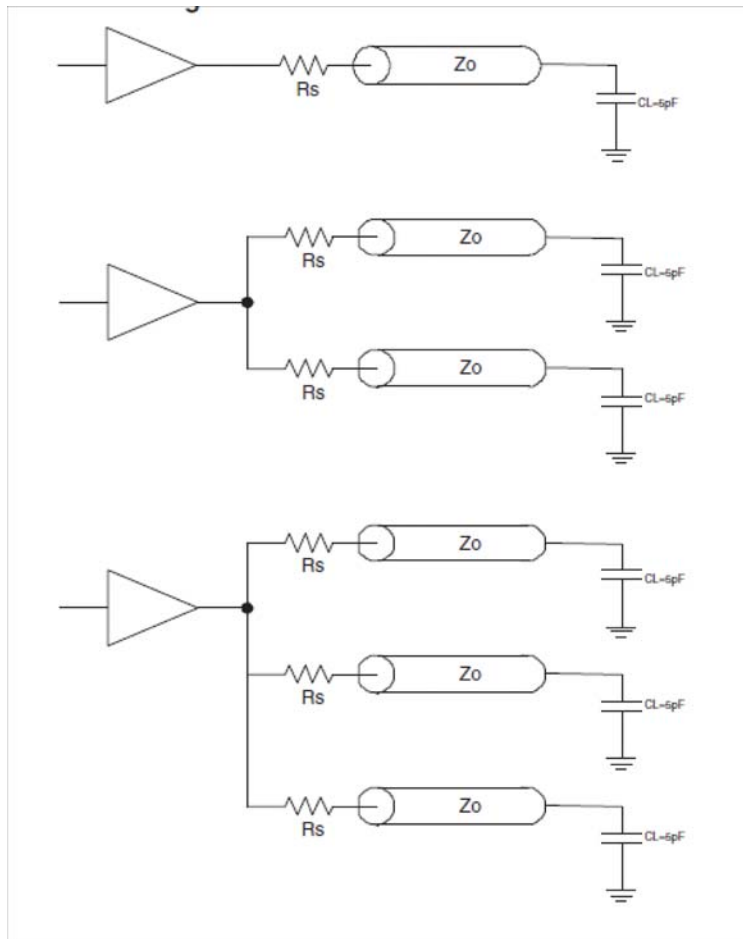
Test Loads and Recommended Terminations

932SQ420 Differential Test Loads



Differential Output Termination Table

| DIF Zo (Ω) | Iref (Ω) | Rs (Ω) | Rp (Ω) |
|---------------------|-------------------|-----------------|-----------------|
| 100 | 475 | 33 | 50 |
| 85 | 412 | 27 | 42.3 or 43.2 |



Single-ended Output Termination Table

| Output | Loads | Rs Value (for each load) | |
|---------|-------|-----------------------------|------------------|
| | | Zo = 50 Ω | Zo = 60 Ω |
| PCI/USB | 1 | 36 | 43 |
| PCI/USB | 2 | 22 | 33 |
| REF | 1 | 39 | 47 |
| REF | 2 | 27 | 36 |
| REF | 3 | 10 | 20 |

Electrical Characteristics - Absolute Maximum Ratings

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---------------------------|--------------------|----------------------------|---------|-----|-----------------------|-------|-------|
| 3.3V Core Supply Voltage | VDDA | | | | 4.6 | V | 1,2 |
| 3.3V Logic Supply Voltage | VDD | | | | 4.6 | V | 1,2 |
| Input Low Voltage | V _{IL} | | GND-0.5 | | | V | 1 |
| Input High Voltage | V _{IH} | Except for SMBus interface | | | V _{DD} +0.5V | V | 1 |
| Input High Voltage | V _{IHSMB} | SMBus clock and data pins | | | 5.5V | V | 1 |
| Storage Temperature | T _s | | -65 | | 150 | °C | 1 |
| Junction Temperature | T _j | | | | 125 | °C | 1 |
| Case Temperature | T _c | | | | 110 | °C | 1 |
| Input ESD protection | ESD prot | Human Body Model | 2000 | | | V | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Operation under these conditions is neither implied nor guaranteed.

DC Electrical Characteristics - Differential Current Mode Outputs

T_A = T_{COM}; Supply Voltage VDD = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|-------------------------|------------------------|---|------|------|------|-------|---------|
| Slew rate | dV/dt | Scope averaging on | 1 | 2.4 | 4 | V/ns | 1, 2, 3 |
| Slew rate matching | ΔdV/dt | Slew rate matching, Scope averaging on | | 9 | 20 | % | 1, 2, 4 |
| Rise/Fall Time Matching | ΔTrf | Rise/fall matching, Scope averaging off | | | 125 | ps | 1, 8, 9 |
| Voltage High | V _{High} | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 660 | 772 | 850 | mV | 1 |
| Voltage Low | V _{Low} | | -150 | 9 | 150 | | 1 |
| Max Voltage | V _{max} | Measurement on single ended signal using absolute value. | | 810 | 1150 | mV | 1, 7 |
| Min Voltage | V _{min} | | -300 | -17 | | | 1, 7 |
| Vswing | V _{swing} | Scope averaging off | 300 | 1446 | | mV | 1, 2 |
| Crossing Voltage (abs) | V _{cross_abs} | Scope averaging off | 250 | 351 | 550 | mV | 1, 5 |
| Crossing Voltage (var) | Δ-V _{cross} | Scope averaging off | | 24 | 140 | mV | 1, 6 |

¹Guaranteed by design and characterization, not 100% tested in production. I_{REF} = VDD/(3xR_R). For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω (100Ω differential impedance).

²Measured from differential waveform

³Slew rate is measured through the V_{swing} voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

⁴Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

⁵V_{cross} is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶The total variation of all V_{cross} measurements in any particular system. Note that this is a subset of V_{cross_min}/max (V_{cross} absolute) allowed. The intent is to limit V_{cross} induced modulation by setting V_{cross_delta} to be smaller than V_{cross} absolute.

⁷Includes overshoot and undershoot.

⁸Measured from single-ended waveform

⁹Measured with scope averaging off, using statistics function. Variation is difference between min and max.

Electrical Characteristics - Input/Supply/Common Parameters

TA = T_{COM}; Supply Voltage VDD = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|----------------------------------|---------------------|---|-----------------------|---------|-----------------------|-------|-------|
| Ambient Operating Temperature | T _{COM} | Commercial range | 0 | | 70 | °C | 1 |
| Input High Voltage | V _{IH} | Single-ended inputs, except SMBus, low threshold and tri-level inputs | 2 | | V _{DD} + 0.3 | V | 1 |
| Input Low Voltage | V _{IL} | Single-ended inputs, except SMBus, low threshold and tri-level inputs | GND - 0.3 | | 0.8 | V | 1 |
| Input Current | I _{IN} | Single-ended inputs, V _{IN} = GND, V _{IN} = VDD | -5 | | 5 | uA | 1 |
| | I _{INP} | Single-ended inputs. V _{IN} = 0 V; Inputs with internal pull up resistors V _{IN} = VDD; Inputs with internal pull-down resistors | -200 | | 200 | uA | 1 |
| Low Threshold Input-High Voltage | V _{IH_FS} | 3.3 V +/-5% | 0.7 | | V _{DD} + 0.3 | V | 1 |
| Low Threshold Input-Low Voltage | V _{IL_FS} | 3.3 V +/-5% | V _{SS} - 0.3 | | 0.35 | V | 1 |
| Input Frequency | F _i | | | 25.00 | | MHz | 2 |
| Pin Inductance | L _{p.in} | | | | 7 | nH | 1 |
| Capacitance | C _{IN} | Logic Inputs | | | 5 | pF | 1 |
| | C _{OUT} | Output pin capacitance | | | 5 | pF | 1 |
| | C _{INX} | X1 & X2 pins | | | 5 | pF | 1 |
| Clk Stabilization | T _{STAB} | From V _{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock | | | 1.8 | ms | 1,2 |
| SS Modulation Frequency | f _{MODIN} | Allowable Frequency (Triangular Modulation) | 30 | 31.500 | 33 | kHz | 1 |
| Tdrive_PD# | t _{DRVPD} | Differential output enable after PD# de-assertion | | 200.000 | 300 | us | 1,3 |
| Tfall | t _F | Fall time of control inputs | | | 5 | ns | 1,2 |
| Trise | t _R | Rise time of control inputs | | | 5 | ns | 1,2 |
| SMBus Input Low Voltage | V _{ILSMB} | | | | 0.8 | V | 1 |
| SMBus Input High Voltage | V _{IHSMB} | | 2.1 | | V _{DDSMB} | V | 1 |
| SMBus Output Low Voltage | V _{OLSMB} | @ I _{PULLUP} | | | 0.4 | V | 1 |
| SMBus Sink Current | I _{PULLUP} | @ V _{OL} | 4 | | | mA | 1 |
| Nominal Bus Voltage | V _{DDSMB} | 3V to 5V +/- 10% | 2.7 | | 5.5 | V | 1 |
| SCLK/SDATA Rise Time | t _{RSMB} | (Max V _{IL} - 0.15) to (Min V _{IH} + 0.15) | | | 1000 | ns | 1 |
| SCLK/SDATA Fall Time | t _{FSMB} | (Min V _{IH} + 0.15) to (Max V _{IL} - 0.15) | | | 300 | ns | 1 |
| SMBus Operating Frequency | f _{MAXSMB} | Maximum SMBus operating frequency | | | 100 | kHz | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Control input must be monotonic from 20% to 80% of input swing.

³Time from deassertion until outputs are >200 mV

AC Electrical Characteristics - Differential Current Mode Outputs

$T_A = T_{COM}$; Supply Voltage $V_{DD} = 3.3\text{ V} \pm 5\%$

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|---------------|--------------------------------------|-----|------|-----|-------|-------|
| Duty Cycle | t_{DC} | Measured differentially, PLL Mode | 45 | 50.1 | 55 | % | 1 |
| Skew, Output to Output | t_{sk3SRC} | Across all SRC outputs, $V_T = 50\%$ | | 13.5 | 50 | ps | 1 |
| Skew, Output to Output | t_{sk3CPU} | Across all CPU outputs, $V_T = 50\%$ | | 43 | 50 | ps | 1 |
| Jitter, Cycle to cycle | $t_{jcc-cyc}$ | CPU, SRC, NS_SAS outputs | | 35 | 50 | ps | 1,3 |
| | | DOT96 output | | 75 | 250 | ps | 1,3 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² $I_{REF} = V_{DD}/(3 \times R_R)$. For $R_R = 475\Omega$ (1%), $I_{REF} = 2.32\text{mA}$. $I_{OH} = 6 \times I_{REF}$ and $V_{OH} = 0.7\text{V} @ Z_O=50\Omega$.

³ Measured from differential waveform

Electrical Characteristics - Phase Jitter Parameters

$T_A = 0 - 70^\circ\text{C}$; Supply Voltage $V_{DD}/V_{DDA} = 3.3\text{ V} \pm 5\%$,

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|--------------|-------------------|--|-----|------|-----|----------|---------|
| Phase Jitter | $t_{jphPCleG1}$ | PCIe Gen 1 | | 28 | 86 | ps (p-p) | 1,2,3,6 |
| | $t_{jphPCleG2}$ | PCIe Gen 2 Lo Band $10\text{kHz} < f < 1.5\text{MHz}$ | | 0.9 | 3 | ps (rms) | 1,2,6 |
| | | PCIe Gen 2 High Band $1.5\text{MHz} < f < \text{Nyquist (50MHz)}$ | | 1.7 | 3.1 | ps (rms) | 1,2,6 |
| | $t_{jphPCleG3}$ | PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz) | | 0.4 | 1 | ps (rms) | 1,2,4,6 |
| | t_{jphQPI_SMI} | QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI) | | 0.15 | 0.5 | ps (rms) | 1,5,7 |
| | | QPI & SMI (100MHz, 8.0Gb/s, 12UI) | | 0.13 | 0.3 | ps (rms) | 1,5,7 |
| | | QPI & SMI (100MHz, 9.6Gb/s, 12UI) | | 0.11 | 0.2 | ps (rms) | 1,5,7 |
| | $t_{jphSAS12G}$ | SAS12G (Filtered REFCLK Jitter 20KHz to 20MHz.) | | 0.34 | 0.4 | ps (rms) | 1,8,9 |
| | $t_{jphSAS12G}$ | SAS 12G | | 0.70 | 1.3 | ps (rms) | 1,5,8 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² See <http://www.pcisig.com> for complete specs

³ Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

⁴ Subject to final radification by PCI SIG.

⁵ Calculated from Intel-supplied Clock Jitter Tool v 1.6.6

⁶ Applied to SRC outputs

⁷ Applies to CPU outputs

⁸ Applies to NS_SAS, NS_SRC outputs, Spread Off

⁹ Intel calculation from raw phase noise data

Electrical Characteristics - PCI

$T_A = 0 - 70^\circ\text{C}$; Supply Voltage $V_{DD}/V_{DDA} = 3.3\text{ V} \pm 5\%$,

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|---------------|---------------------------------|-----|------|------|----------|-------|
| Output Impedance | R_{DSP} | $V_O = V_{DD}^*(0.5)$ | 12 | | 55 | Ω | 1 |
| Output High Voltage | V_{OH} | $I_{OH} = -1\text{ mA}$ | 2.4 | | | V | 1 |
| Output Low Voltage | V_{OL} | $I_{OL} = 1\text{ mA}$ | | | 0.55 | V | 1 |
| Output High Current | I_{OH} | MIN @ $V_{OH} = 1.0\text{ V}$ | -33 | | | mA | 1 |
| | | MAX @ $V_{OH} = 3.135\text{ V}$ | | | -33 | mA | 1 |
| Output Low Current | I_{OL} | MIN @ $V_{OL} = 1.95\text{ V}$ | 30 | | | mA | 1 |
| | | MAX @ $V_{OL} = 0.4\text{ V}$ | | | 38 | mA | 1 |
| Clock High Time | T_{HIGH} | 1.5V | 12 | | | ns | 1 |
| Clock Low Time | T_{LOW} | 1.5V | 12 | | | ns | 1 |
| Edge Rate | $t_{slew/f}$ | Rising/Falling edge rate | 1 | 1.8 | 4 | V/ns | 1,2 |
| Duty Cycle | d_{T1} | $V_T = 1.5\text{ V}$ | 45 | 50.5 | 55 | % | 1 |
| Group Skew | t_{skew} | $V_T = 1.5\text{ V}$ | | 294 | 500 | ps | 1 |
| Jitter, Cycle to cycle | $t_{jcy-cyc}$ | $V_T = 1.5\text{ V}$ | | 108 | 500 | ps | 1 |

See "Single-ended Test Loads Page" for termination circuits

¹Guaranteed by design and characterization, not 100% tested in production.

²Measured between 0.8V and 2.0V

Electrical Characteristics - 48MHz

$T_A = 0 - 70^\circ\text{C}$; Supply Voltage $V_{DD}/V_{DDA} = 3.3\text{ V} \pm 5\%$,

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|-------------------|---------------------------------|-------|-----|--------|----------|-------|
| Output Impedance | R_{DSP} | $V_O = V_{DD}^*(0.5)$ | 20 | | 60 | Ω | 1 |
| Output High Voltage | V_{OH} | $I_{OH} = -1\text{ mA}$ | 2.4 | | | V | 1 |
| Output Low Voltage | V_{OL} | $I_{OL} = 1\text{ mA}$ | | | 0.55 | V | 1 |
| Output High Current | I_{OH} | MIN @ $V_{OH} = 1.0\text{ V}$ | -29 | | | mA | 1 |
| | | MAX @ $V_{OH} = 3.135\text{ V}$ | | | -33 | mA | 1 |
| Output Low Current | I_{OL} | MIN @ $V_{OL} = 1.95\text{ V}$ | 29 | | | mA | 1 |
| | | MAX @ $V_{OL} = 0.4\text{ V}$ | | | 27 | mA | 1 |
| Clock High Time | T_{HIGH} | 1.5V | 8.094 | | 10.036 | ns | 1 |
| Clock Low Time | T_{LOW} | 1.5V | 7.694 | | 9.836 | ns | 1 |
| Edge Rate | t_{slew/f_USB} | Rising/Falling edge rate | 1 | 1.5 | 2 | V/ns | 1,2 |
| Duty Cycle | d_{T1} | $V_T = 1.5\text{ V}$ | 45 | 51 | 55 | % | 1 |
| Jitter, Cycle to cycle | $t_{jcy-cyc}$ | $V_T = 1.5\text{ V}$ | | 109 | 350 | ps | 1 |

See "Single-ended Test Loads Page" for termination circuits

¹Guaranteed by design and characterization, not 100% tested in production.

²Measured between 0.8V and 2.0V

Electrical Characteristics - Current Consumption

$T_A = T_{COM}$; Supply Voltage $V_{DD} = 3.3\text{ V} \pm 5\%$

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|--------------------------|----------------|---|-----|-----|-----|-------|-------|
| Operating Supply Current | $I_{DD3.3OP}$ | All outputs active @100MHz, C_L = Full load; | | 380 | 400 | mA | 1 |
| Powerdown Current | $I_{DD3.3PDZ}$ | All differential pairs tri-stated | | 16 | 20 | mA | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - REF

$T_A = 0 - 70^\circ\text{C}$; Supply Voltage $V_{DD}/V_{DDA} = 3.3\text{ V} \pm 5\%$,

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|------------------------|----------------|---------------------------------|------|------|------|----------|-------|
| Output Impedance | R_{DSP} | $V_O = V_{DD}*(0.5)$ | 12 | | 55 | Ω | 1 |
| Output High Voltage | V_{OH} | $I_{OH} = -1\text{ mA}$ | 2.4 | | | V | 1 |
| Output Low Voltage | V_{OL} | $I_{OL} = 1\text{ mA}$ | | | 0.55 | V | 1 |
| Output High Current | I_{OH} | MIN @ $V_{OH} = 1.0\text{ V}$ | -33 | | | mA | 1 |
| | | MAX @ $V_{OH} = 3.135\text{ V}$ | | | -33 | mA | 1 |
| Output Low Current | I_{OL} | MIN @ $V_{OL} = 1.95\text{ V}$ | 30 | | | mA | 1 |
| | | MAX @ $V_{OL} = 0.4\text{ V}$ | | | 38 | mA | 1 |
| Clock High Time | T_{HIGH} | 1.5V | 27.5 | | | ns | 1 |
| Clock Low Time | T_{LOW} | 1.5V | 27.5 | | | ns | 1 |
| Edge Rate | $t_{sle wr/f}$ | Rising/Falling edge rate | 1 | 1.9 | 4 | V/ns | 1,2 |
| Duty Cycle | d_{t1} | $V_T = 1.5\text{ V}$ | 45 | 50.5 | 55 | % | 1 |
| Jitter, Cycle to cycle | $t_{jyc-cyc}$ | $V_T = 1.5\text{ V}$ | | 75 | 1000 | ps | 1 |

See "Single-ended Test Loads Page" for termination circuits

¹Guaranteed by design and characterization, not 100% tested in production.

²Measured between 0.8V and 2.0V

Clock AC Tolerances

| | CPU | SRC, NS_SAS, NS_SRC | PCI | DOT96 | 48MHz | REF | |
|-----------------------|--------|---------------------------|--------|-------|-------|-------|-----|
| PPM tolerance | 100 | 100 | 100 | 100 | 100 | 100 | ppm |
| Cycle to Cycle Jitter | 50 | 50 | 500 | 250 | 350 | 1000 | ps |
| Spread | -0.50% | -0.50% | -0.50% | 0 | 0.00% | 0.00% | % |

Clock Periods – Outputs with Spread Spectrum Disabled

| SSC ON | Center Freq. MHz | Measurement Window | | | | | | | Units | Notes |
|---------------------------|------------------|------------------------------|--------------------------------------|--------------------------------------|-------------------------|--------------------------------------|--------------------------------------|------------------------------|-------|-------|
| | | 1 Clock | 1 us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | | |
| | | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max | | |
| CPU | 100.00000 | 9.94900 | | 9.99900 | 10.00000 | 10.00100 | | 10.05100 | ns | 1,2 |
| | 133.33333 | 7.44925 | | 7.49925 | 7.50000 | 7.50075 | | 7.55075 | ns | 1,2 |
| SRC, NS_SAS, NS_SRC | 100.00000 | 9.94900 | | 9.99900 | 10.00000 | 10.00100 | | 10.05100 | ns | 1,2 |
| PCI | 33.33333 | 29.49700 | | 29.99700 | 30.00000 | 30.00300 | | 30.50300 | ns | 1,2 |
| DOT96 | 96.00000 | 10.16563 | | 10.41563 | 10.41667 | 10.41771 | | 10.66771 | ns | 1,2 |
| 48MHz | 48.00000 | 20.48125 | | 20.83125 | 20.83333 | 20.83542 | | 21.18542 | ns | 1,2 |
| REF | 14.31818 | 69.78429 | | 69.83429 | 69.84128 | 69.84826 | | 69.89826 | ns | 1,2 |

Clock Periods – Outputs with Spread Spectrum Enabled

| SSC ON | Center Freq. MHz | Measurement Window | | | | | | | Units | Notes |
|--------|------------------|------------------------------|--------------------------------------|--------------------------------------|-------------------------|--------------------------------------|--------------------------------------|------------------------------|-------|-------|
| | | 1 Clock | 1 us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | | |
| | | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max | | |
| CPU | 99.75 | 9.94906 | 9.99906 | 10.02406 | 10.02506 | 10.02607 | 10.05107 | 10.10107 | ns | 1,2 |
| | 133.00 | 7.44930 | 7.49930 | 7.51805 | 7.51880 | 7.51955 | 7.53830 | 7.58830 | ns | 1,2 |
| PCI | 33.25 | 29.49718 | 29.99718 | 30.07218 | 30.07519 | 30.07820 | 30.15320 | 30.65320 | ns | 1,2 |
| SRC | 99.75 | 9.94906 | 9.99906 | 10.02406 | 10.02506 | 10.02607 | 10.05107 | 10.10107 | ns | 1,2 |

¹Guaranteed by design and characterization, not 100% tested in production.

²All Long Term Accuracy specifications are guaranteed with the assumption that the REF output is tuned to exactly 14.31818MHz.

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

| Index Block Write Operation | | |
|-----------------------------|-----------|----------------------|
| Controller (Host) | | IDT (Slave/Receiver) |
| T | starT bit | |
| Slave Address | | |
| WR | WRite | |
| Beginning Byte = N | | ACK |
| | | ACK |
| Data Byte Count = X | | ACK |
| Beginning Byte N | | ACK |
| O | X Byte | O |
| O | | O |
| O | | O |
| Byte N + X - 1 | | ACK |
| P | stoP bit | |

SMBus write address = D2 hex

SMBus read address = D3 hex

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends **Byte 0 through Byte X (if X_(H) was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | |
|----------------------------|-----------------|----------------------|
| Controller (Host) | | IDT (Slave/Receiver) |
| T | starT bit | |
| Slave Address | | |
| WR | WRite | |
| Beginning Byte = N | | ACK |
| | | ACK |
| RT | Repeat starT | |
| Slave Address | | |
| RD | ReaD | |
| | | ACK |
| ACK | | |
| | | Data Byte Count=X |
| | | Beginning Byte N |
| O | X Byte | O |
| O | | O |
| O | | O |
| O | | O |
| | | Byte N + X - 1 |
| N | Not acknowledge | |
| P | stoP bit | |

SMBus Table: Output Enable Register

| Byte 0 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|----------------|------------------|------|--------------|--------|---------|
| Bit 7 | 24/25 | DOT96 Enable | Output Enable | RW | Disable-Hi-Z | Enable | 1 |
| Bit 6 | 50/49 | NS_SAS1 Enable | Output Enable | RW | Disable-Hi-Z | Enable | 1 |
| Bit 5 | 48/47 | NS_SAS0 Enable | Output Enable | RW | Disable-Hi-Z | Enable | 1 |
| Bit 4 | 44/43 | NS_SRC1 Enable | Output Enable | RW | Disable-Hi-Z | Enable | 1 |
| Bit 3 | 42/41 | NS_SRC0 Enable | Output Enable | RW | Disable-Hi-Z | Enable | 1 |
| Bit 2 | 36/35 | SRC2 Enable | Output Enable | RW | Disable-Hi-Z | Enable | 1 |
| Bit 1 | 34/33 | SRC1 Enable | Output Enable | RW | Disable-Hi-Z | Enable | 1 |
| Bit 0 | 30/31 | SRC0 Enable | Output Enable | RW | Disable-Hi-Z | Enable | 1 |

SMBus Table: Output Enable Register

| Byte 1 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-----------------|------------------------|------------------|------|--------------|-----------|---------|
| Bit 7 | 5 | REF14_3x Enable | Output Enable | RW | Disable-Low | Enable | 1 |
| Bit 6 | | | RESERVED | | | | 0 |
| Bit 5 | | | RESERVED | | | | 0 |
| Bit 4 | 62/61 | CPU3 | Output Enable | RW | Disable-Hi-Z | Enable | 1 |
| Bit 3 | 60/59 | CPU2 | Output Enable | RW | Disable-Hi-Z | Enable | 1 |
| Bit 2 | 56/55 | CPU1 | Output Enable | RW | Disable-Hi-Z | Enable | 1 |
| Bit 1 | 54/53 | CPU0 | Output Enable | RW | Disable-Hi-Z | Enable | 1 |
| Bit 0 | CPU/SRC/ PCI | Spread Spectrum Enable | Spread Off/On | RW | Spread Off | Spread On | 0 |

SMBus Table: Output Enable Register

| Byte 2 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|--------------|------------------|------|-------------|--------|---------|
| Bit 7 | | | RESERVED | | | | 0 |
| Bit 6 | | | RESERVED | | | | 0 |
| Bit 5 | 13 | PCI4 Enable | Output Enable | RW | Disable-Low | Enable | 1 |
| Bit 4 | 14 | PCI3 Enable | Output Enable | RW | Disable-Low | Enable | 1 |
| Bit 3 | 15 | PCI2 Enable | Output Enable | RW | Disable-Low | Enable | 1 |
| Bit 2 | 16 | PCI1 Enable | Output Enable | RW | Disable-Low | Enable | 1 |
| Bit 1 | 17 | PCI0 Enable | Output Enable | RW | Disable-Low | Enable | 1 |
| Bit 0 | 21 | 48MHz Enable | Output Enable | RW | Disable-Low | Enable | 1 |

SMBus Table: Reserved

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | | | RESERVED | | | | 0 |
| Bit 6 | | | RESERVED | | | | 0 |
| Bit 5 | | | RESERVED | | | | 0 |
| Bit 4 | | | RESERVED | | | | 0 |
| Bit 3 | | | RESERVED | | | | 0 |
| Bit 2 | | | RESERVED | | | | 0 |
| Bit 1 | | | RESERVED | | | | 0 |
| Bit 0 | | | RESERVED | | | | 0 |

SMBus Table: Reserved

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | | | RESERVED | | | | 0 |
| Bit 6 | | | RESERVED | | | | 0 |
| Bit 5 | | | RESERVED | | | | 0 |
| Bit 4 | | | RESERVED | | | | 0 |
| Bit 3 | | | RESERVED | | | | 0 |
| Bit 2 | | | RESERVED | | | | 0 |
| Bit 1 | | | RESERVED | | | | 0 |
| Bit 0 | | | RESERVED | | | | 0 |

SMBus Table: Reserved

| Byte 5 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---------------------------------------|---|---------|
| Bit 7 | | | RESERVED | | | | 0 |
| Bit 6 | | | RESERVED | | | | 0 |
| Bit 5 | | | RESERVED | | | | 0 |
| Bit 4 | - | FS4 | Freq. Sel 4 | RW | See NS_SAS/NS_SRC Frequency Table. | | 0 |
| Bit 3 | - | FS3 | Freq. Sel 3 | RW | | 1 | |
| Bit 2 | - | FS2 | Freq. Sel 2 | RW | | 1 | |
| Bit 1 | - | FS1 | Freq. Sel 1 | RW | | 1 | |
| Bit 0 | - | FS0 | Freq. Sel 0 | RW | | 1 | |

SMBus Table: Test Mode and CPU/SRC/PCI Frequency Select Register

| Byte 6 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|-----------------------|------------------|------|---|--------|---------|
| Bit 7 | - | Test Mode | Test Mode Type | RW | Hi-Z | REF/N | 0 |
| Bit 6 | - | Test Select | Select Test Mode | RW | Disable | Enable | 0 |
| Bit 5 | - | | RESERVED | | | | 0 |
| Bit 4 | - | 100M_133M# (See note) | Frequency Select | R | 133MHz | 100MHz | Latch |
| Bit 3 | - | FS3 | Freq. Sel 3 | RW | See CPU/SRC/PCI Frequency Select Table | | 1 |
| Bit 2 | - | FS2 | Freq. Sel 2 | RW | | 0 | |
| Bit 1 | - | FS1 | Freq. Sel 1 | RW | | 0 | |
| Bit 0 | - | FS0 | Freq. Sel 0 | RW | | 0 | |

Note: Internal Pull up on 100M_133M# pin will result in default CPU frequency of 100 MHz.

SMBus Table: Vendor & Revision ID Register

| Byte 7 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|------------------|---|---------|
| Bit 7 | - | RID3 | REVISION ID | R | 0011 for D rev | | 0 |
| Bit 6 | - | RID2 | | R | | 0 | |
| Bit 5 | - | RID1 | | R | | 1 | |
| Bit 4 | - | RID0 | | R | | 1 | |
| Bit 3 | - | VID3 | VENDOR ID | R | 0001 for ICS/IDT | | 0 |
| Bit 2 | - | VID2 | | R | | 0 | |
| Bit 1 | - | VID1 | | R | | 0 | |
| Bit 0 | - | VID0 | | R | | 1 | |

SMBus Table: Byte Count Register

| Byte 8 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|----------------------------------|------|--|---|---------|
| Bit 7 | - | BC7 | Byte Count Programming b(7:0) | RW | Writing to this register will configure how many bytes will be read back, default is A bytes. (0 to 9) | | 0 |
| Bit 6 | - | BC6 | | RW | | 0 | |
| Bit 5 | - | BC5 | | RW | | 0 | |
| Bit 4 | - | BC4 | | RW | | 0 | |
| Bit 3 | - | BC3 | | RW | | 1 | |
| Bit 2 | - | BC2 | | RW | | 0 | |
| Bit 1 | - | BC1 | | RW | | 1 | |
| Bit 0 | - | BC0 | | RW | | 0 | |

SMBus Table: Device ID Register

| Byte 9 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|-----------------------|------|---|---|---------|
| Bit 7 | | DID7 | Device ID (17 hex) | R | - | - | 0 |
| Bit 6 | | DID6 | | R | - | - | 0 |
| Bit 5 | | DID5 | | R | - | - | 0 |
| Bit 4 | | DID4 | | R | - | - | 1 |
| Bit 3 | | DID3 | | R | - | - | 0 |
| Bit 2 | | DID2 | | R | - | - | 1 |
| Bit 1 | | DID1 | | R | - | - | 1 |
| Bit 0 | | DID0 | | R | - | - | 1 |

CPU/SRC/PCI Frequency Selection Table

| Line | Byte 1, Bit 0 Spread Enable | Byte6 Bit3 FS3 | Byte6 Bit2 FS2 | Byte6 Bit1 FS1 | Byte6 Bit0 FS0 | CPU Speed for 100MHz | CPU Speed for 133MHz | SRC (MHz) | PCI (MHz) | Spread % |
|------|--------------------------------------|----------------------|----------------------|----------------------|----------------------|-------------------------------|-------------------------------|---------------|--------------|-------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 89.97 | 119.97 | 89.97 | 29.99 | 0% |
| 1 | 0 | 0 | 0 | 0 | 1 | 91.28 | 121.70 | 91.28 | 30.43 | |
| 2 | 0 | 0 | 0 | 1 | 0 | 92.58 | 123.44 | 92.58 | 30.86 | |
| 3 | 0 | 0 | 0 | 1 | 1 | 93.75 | 125.00 | 93.75 | 31.25 | |
| 4 | 0 | 0 | 1 | 0 | 0 | 95.05 | 126.73 | 95.05 | 31.68 | |
| 5 | 0 | 0 | 1 | 0 | 1 | 96.22 | 128.30 | 96.22 | 32.07 | |
| 6 | 0 | 0 | 1 | 1 | 0 | 97.53 | 130.03 | 97.53 | 32.51 | |
| 7 | 0 | 0 | 1 | 1 | 1 | 98.83 | 131.77 | 98.83 | 32.94 | |
| 8 | 0 | 1 | 0 | 0 | 0 | 100.00 | 133.33 | 100.00 | 33.33 | |
| 9 | 0 | 1 | 0 | 0 | 1 | 101.30 | 135.07 | 101.30 | 33.77 | |
| 10 | 0 | 1 | 0 | 1 | 0 | 102.47 | 136.63 | 102.47 | 34.16 | |
| 11 | 0 | 1 | 0 | 1 | 1 | 103.78 | 138.37 | 103.78 | 34.59 | |
| 12 | 0 | 1 | 1 | 0 | 0 | 105.08 | 140.10 | 105.08 | 35.03 | |
| 13 | 0 | 1 | 1 | 0 | 1 | 106.25 | 141.67 | 106.25 | 35.42 | |
| 14 | 0 | 1 | 1 | 1 | 0 | 107.55 | 143.40 | 107.55 | 35.85 | |
| 15 | 0 | 1 | 1 | 1 | 1 | 110.03 | 146.70 | 110.03 | 36.68 | |
| 16 | 1 | 0 | 0 | 0 | 0 | 89.97 | 119.97 | 89.97 | 29.99 | -0.5% |
| 17 | 1 | 0 | 0 | 0 | 1 | 91.28 | 121.70 | 91.28 | 30.43 | |
| 18 | 1 | 0 | 0 | 1 | 0 | 92.58 | 123.44 | 92.58 | 30.86 | |
| 19 | 1 | 0 | 0 | 1 | 1 | 93.75 | 125.00 | 93.75 | 31.25 | |
| 20 | 1 | 0 | 1 | 0 | 0 | 95.05 | 126.73 | 95.05 | 31.68 | |
| 21 | 1 | 0 | 1 | 0 | 1 | 96.22 | 128.30 | 96.22 | 32.07 | |
| 22 | 1 | 0 | 1 | 1 | 0 | 97.53 | 130.03 | 97.53 | 32.51 | |
| 23 | 1 | 0 | 1 | 1 | 1 | 98.83 | 131.77 | 98.83 | 32.94 | |
| 24 | 1 | 1 | 0 | 0 | 0 | 100.00 | 133.33 | 100.00 | 33.33 | |
| 25 | 1 | 1 | 0 | 0 | 1 | 101.30 | 135.07 | 101.30 | 33.77 | |
| 26 | 1 | 1 | 0 | 1 | 0 | 102.47 | 136.63 | 102.47 | 34.16 | |
| 27 | 1 | 1 | 0 | 1 | 1 | 103.78 | 138.37 | 103.78 | 34.59 | |
| 28 | 1 | 1 | 1 | 0 | 0 | 105.08 | 140.10 | 105.08 | 35.03 | |
| 29 | 1 | 1 | 1 | 0 | 1 | 106.25 | 141.67 | 106.25 | 35.42 | |
| 30 | 1 | 1 | 1 | 1 | 0 | 107.55 | 143.40 | 107.55 | 35.85 | |
| 31 | 1 | 1 | 1 | 1 | 1 | 110.03 | 146.70 | 110.03 | 36.68 | |

NS_SAS Margining Table

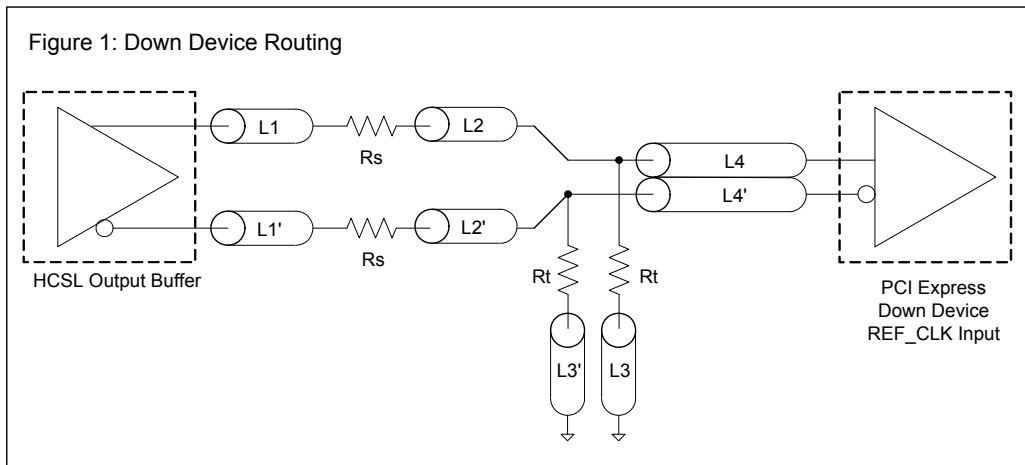
| Line | Byte5 Bit4 FS4 | Byte5 Bit3 FS3 | Byte5 Bit2 FS2 | Byte5 Bit1 FS1 | Byte5 Bit0 FS0 | NS_xxx (MHz) |
|------|----------------------|----------------------|----------------------|----------------------|----------------------|-----------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 58.33 |
| 1 | 0 | 0 | 0 | 0 | 1 | 61.11 |
| 2 | 0 | 0 | 0 | 1 | 0 | 63.89 |
| 3 | 0 | 0 | 0 | 1 | 1 | 66.67 |
| 4 | 0 | 0 | 1 | 0 | 0 | 69.44 |
| 5 | 0 | 0 | 1 | 0 | 1 | 72.22 |
| 6 | 0 | 0 | 1 | 1 | 0 | 75.00 |
| 7 | 0 | 0 | 1 | 1 | 1 | 77.78 |
| 8 | 0 | 1 | 0 | 0 | 0 | 80.56 |
| 9 | 0 | 1 | 0 | 0 | 1 | 83.33 |
| 10 | 0 | 1 | 0 | 1 | 0 | 86.11 |
| 11 | 0 | 1 | 0 | 1 | 1 | 88.89 |
| 12 | 0 | 1 | 1 | 0 | 0 | 91.67 |
| 13 | 0 | 1 | 1 | 0 | 1 | 94.44 |
| 14 | 0 | 1 | 1 | 1 | 0 | 97.22 |
| 15 | 0 | 1 | 1 | 1 | 1 | 100.00 |
| 16 | 1 | 0 | 0 | 0 | 0 | 102.78 |
| 17 | 1 | 0 | 0 | 0 | 1 | 105.56 |
| 18 | 1 | 0 | 0 | 1 | 0 | 108.33 |
| 19 | 1 | 0 | 0 | 1 | 1 | 111.11 |
| 20 | 1 | 0 | 1 | 0 | 0 | 113.89 |
| 21 | 1 | 0 | 1 | 0 | 1 | 116.67 |
| 22 | 1 | 0 | 1 | 1 | 0 | 119.44 |
| 23 | 1 | 0 | 1 | 1 | 1 | 122.22 |
| 24 | 1 | 1 | 0 | 0 | 0 | 125.00 |
| 25 | 1 | 1 | 0 | 0 | 1 | 127.78 |
| 26 | 1 | 1 | 0 | 1 | 0 | 130.56 |
| 27 | 1 | 1 | 0 | 1 | 1 | 133.33 |
| 28 | 1 | 1 | 1 | 0 | 0 | 136.11 |
| 29 | 1 | 1 | 1 | 0 | 1 | 138.89 |
| 30 | 1 | 1 | 1 | 1 | 0 | 141.67 |
| 31 | 1 | 1 | 1 | 1 | 1 | 144.44 |

NOTE: Operation at other than the default entry is not guaranteed. These values are for margining purposes only.

| DIF Reference Clock | | | |
|---|--------------------|------|--------|
| Common Recommendations for Differential Routing | Dimension or Value | Unit | Figure |
| L1 length, route as non-coupled 50ohm trace | 0.5 max | inch | 1 |
| L2 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| L3 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| R_s | 33 | ohm | 1 |
| R_t | 49.9 | ohm | 1 |

| Down Device Differential Routing | | | |
|--|---------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 2 min to 16 max | inch | 1 |
| L4 length, route as coupled stripline 100ohm differential trace | 1.8 min to 14.4 max | inch | 1 |

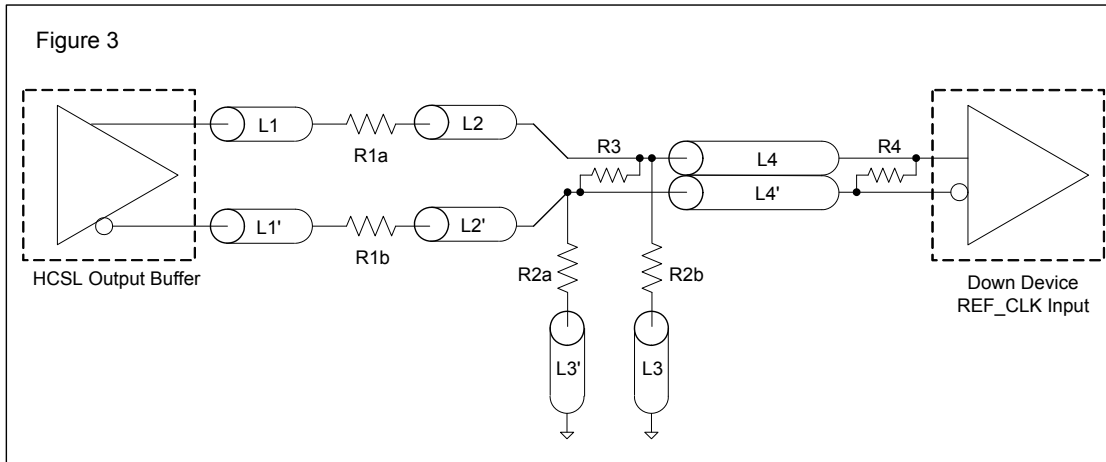
| Differential Routing to PCI Express Connector | | | |
|--|-----------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 0.25 to 14 max | inch | 2 |
| L4 length, route as coupled stripline 100ohm differential trace | 0.225 min to 12.6 max | inch | 2 |



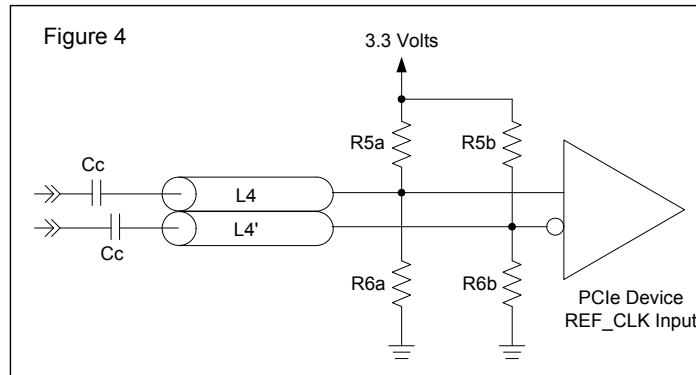
| Alternative Termination for LVDS and other Common Differential Signals (figure 3) | | | | | | | |
|---|-------|------|----|------|------|-----|--------------------------------|
| Vdiff | Vp-p | Vcm | R1 | R2 | R3 | R4 | Note |
| 0.45v | 0.22v | 1.08 | 33 | 150 | 100 | 100 | |
| 0.58 | 0.28 | 0.6 | 33 | 78.7 | 137 | 100 | |
| 0.80 | 0.40 | 0.6 | 33 | 78.7 | none | 100 | ICS874003i-02 input compatible |
| 0.60 | 0.3 | 1.2 | 33 | 174 | 140 | 100 | Standard LVDS |

R1a = R1b = R1

R2a = R2b = R2



| Cable Connected AC Coupled Application (figure 4) | | |
|---|-------------|------|
| Component | Value | Note |
| R5a, R5b | 8.2K 5% | |
| R6a, R6b | 1K 5% | |
| Cc | 0.1 μ F | |
| Vcm | 0.350 volts | |



Test Clarification Table

| Comments | HW | | SW | | OUTPUT |
|---|--------------------|---------------------|---------------------------|--------------------------|--------|
| | TEST_SEL HW PIN | TEST_MODE HW PIN | TEST ENTRY BIT B6b6 | REF/N or HI-Z B6b7 | |
| | 0 | X | 0 | X | NORMAL |
| Power-up w/ TEST_SEL = 1 (>2.0V) to enter test mode. Cycle power to disable test mode. | 1 | 0 | X | 0 | HI-Z |
| | 1 | 0 | X | 1 | REF/N |
| | 1 | 1 | X | 0 | REF/N |
| | 1 | 1 | X | 1 | REF/N |
| If TEST_SEL HW pin is 0 during power-up, test mode can be selected through B6b6. If test mode is selected by B6b6, then B6b7 is used to select HI-Z or REF/N. TEST_Mode pin is not used. Cycle power to disable test mode. | 0 | X | 1 | 0 | HI-Z |
| | 0 | X | 1 | 1 | REF/N |

B6b6: 1= ENTER TEST MODE, Default = 0 (NORMAL OPERATION)

B6b7: 1= REF/N, Default = 0 (HI-Z)

Thermal Characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|---------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still air | | 68.2 | | °C/W |
| | θ_{JA} | 1 m/s air flow | | 63.3 | | °C/W |
| | θ_{JA} | 2 m/s air flow | | 59.6 | | °C/W |
| Thermal Resistance Junction to Case | θ_{JC} | | | 32.5 | | °C/W |
| Thermal Resistance Junction to Board | θ_{JB} | | | 51.5 | | °C/W |

Package Outline and Package Dimensions (64-pin TSSOP)



6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|----------|-------------------------------------|------|--------------------------------|------|
| | MIN | MAX | MIN | MAX |
| A | -- | 1.20 | -- | .047 |
| A1 | 0.05 | 0.15 | .002 | .006 |
| A2 | 0.80 | 1.05 | .032 | .041 |
| b | 0.17 | 0.27 | .007 | .011 |
| c | 0.09 | 0.20 | .0035 | .008 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 8.10 BASIC | | 0.319 BASIC | |
| E1 | 6.00 | 6.20 | .236 | .244 |
| e | 0.50 BASIC | | 0.020 BASIC | |
| L | 0.45 | 0.75 | .018 | .030 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | .004 |

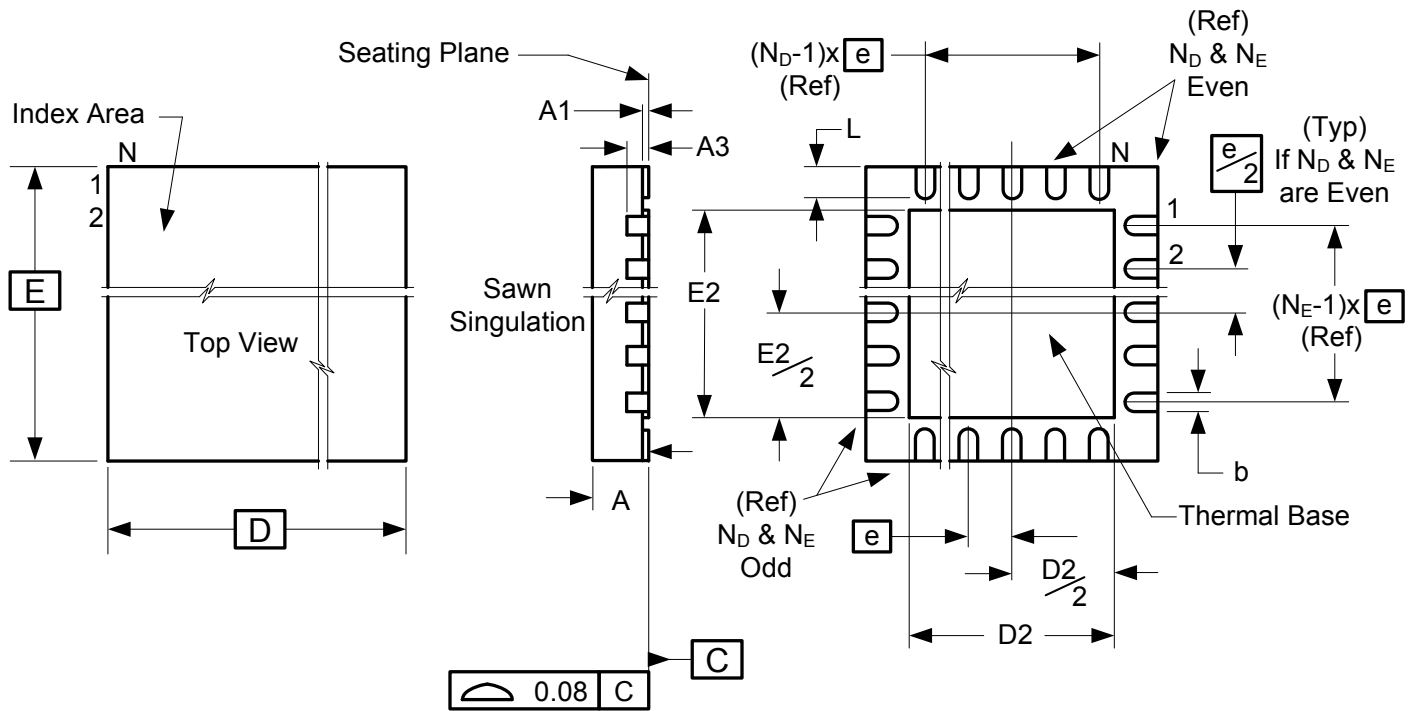
VARIATIONS

| N | D mm. | | D (inch) | |
|----|-------|-------|----------|------|
| | MIN | MAX | MIN | MAX |
| 64 | 16.90 | 17.10 | .665 | .673 |

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

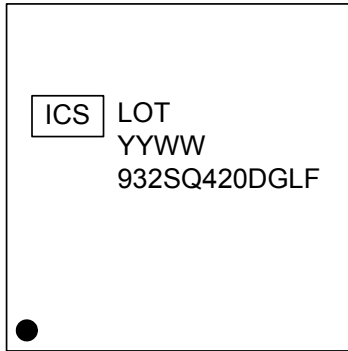
Package Outline and Package Dimensions (64-pin MLF)



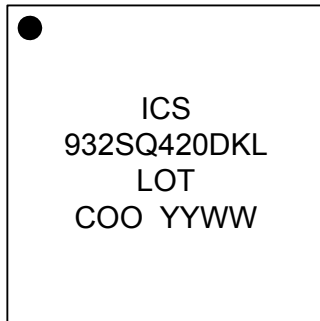
**THERMALLY ENHANCED, VERY THIN, FINE PITCH
QUAD FLAT / NO LEAD PLASTIC PACKAGE**

| DIMENSIONS | | SYMBOL | MIN. | MAX. |
|------------|----|----------------|----------------|------|
| | | A | 0.8 | 1.0 |
| | | A1 | 0 | 0.05 |
| | | A3 | 0.25 Reference | |
| | | b | 0.18 | 0.3 |
| | | e | 0.50 BASIC | |
| | | D x E BASIC | 9.00 x 9.00 | |
| | | D2 MIN. / MAX. | 6.00 | 6.25 |
| | | E2 MIN. / MAX. | 6.00 | 6.25 |
| | | L MIN. / MAX. | 0.30 | 0.50 |
| N | 64 | | | |
| ND | 16 | | | |
| NE | 16 | | | |

Marking Diagram (TSSOP)



Marking Diagram (MLF)



Notes:

1. 'LOT' denotes lot number.
2. 'YYWW' is the date code.
3. 'COO' denotes country of origin.
4. 'L' or 'LF' denotes RoHS compliant package.

Ordering Information

| Part / Order Number | Shipping Packaging | Package | Temperature |
|---------------------|--------------------|--------------|-------------|
| 932SQ420DGLF | Tubes | 64-pin TSSOP | 0 to +70° C |
| 932SQ420DGLFT | Tape and Reel | 64-pin TSSOP | 0 to +70° C |
| 932SQ420DKLF | Tray | 64-pin MLF | 0 to +70° C |
| 932SQ420DKLFT | Tape and Reel | 64-pin MLF | 0 to +70° C |

"LF" suffix to the part number are the Pb-Free configuration, RoHS compliant.

"D" is the device revision designator (will not correlate with the datasheet revision).

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Revision History

| Rev. | Issue Date | Who | Description | Page # |
|------|------------|-----|--|------------|
| 0.9 | 9/16/2010 | RDW | Initial Release | - |
| A | 9/20/2010 | RDW | Minor typo corrections | Various |
| B | 3/1/2011 | RDW | Added rise/fall variation to DC Electrical Characteristics Table | 9 |
| C | 3/9/2011 | RDW | Corrected Line 0 of NS_SAS Margining Table. | 19 |
| D | 4/28/2011 | RDW | Corrected MLF packaging pin description. Pin 37 was missing. | 7 |
| E | 7/26/2011 | RDW | Updated Power Down Functionality table to clarify functionality of single-ended outputs in power down. | 2 |
| F | 9/20/2011 | RDW | 1. Added "Case Temperature" spec to Abs Max ratings 2. Added Thermal Characteristics | Various |
| G | 12/8/2011 | RDW | 1. Updated Phase Jitter Table to correct typo in "Conditions" column for SAS. 2. Mark Spec Added. | 11, 23, 24 |
| H | 4/18/2012 | RDW | 1. Updated Rp values on Output Terminations Table from 43.2 ohms to 42.2 or 43.2 ohms to be consistent with Intel. | 8 |

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