GM76C256BL/BLL-W

32,768 WORDS x 8 BIT
CMOS STATIC RAM

Description

The GM76C256BL/BLL-W is a 262,144 bits static random access memory organized as 32,768 words by 8 bits. Using a 0.8*um* advanced CMOS technology and operated from a single 2.7V to 5.5V supply. Advanced circuit techniques provide both high speed and low power consumption. The GM76C256BL/BLL-W has Chip select $\overline{CS}$, which allows for device selection and data retention control, and output enable ($\overline{OE}$), which provides fast memory access. Thus it is suitable for high speed and low power applications, particularly where battery back-up is required. The GM76C256BL/BLL-W is offered in a 28-pin DIP (600mil), SOP (480mil) and TSOP I (0814).

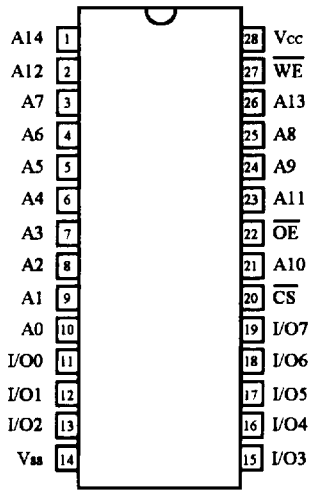
Features

- Fast Speed : 55/70ns at Vcc=5V ± 10%
  120/150ns at Vcc=3V ± 10%
- Low Power Standby and Low Power Operation
  Standby : 110uW (Max) at Vcc=5V ± 10%
  33uW (Max) at Vcc=3V ± 10%
  Operation : 385mW (Max) at Vcc=5V ± 10%
  82.5mW (Max) at Vcc=3V ± 10%
- Completely Static RAM : No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Capability of Battery Back-up Operation
- Single + 2.7 ~ 5.5V Operation
- Standard 28 DIP, SOP and TSOP I

Pin Description

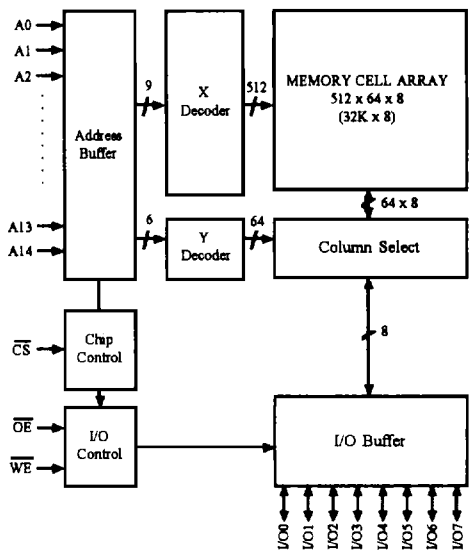
Pin	Function
A0-A14	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{CS}$	Chip Select Input
I/O0-I/O7	Data Input/Output
Vcc	Power Supply
Vss	Ground

Pin Configuration



(Top View)

Block Diagram



Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	℃
T_{STG}	Storage Temperature	-65 ~ 150	℃
V_{SOL}	Soldering Temperature and Time	260, 10 (at lead)	℃, S
V_{CC}	Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Voltage	-0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5 ~ V_{CC} + 0.5	V
P_D	Power Dissipation	1.0	W

*Note: -3.0V at pulse width 50ns Max.

Recommended Operating Conditions (T_A = 0 ~ 70℃)

Symbol	Parameter	Vcc = 5V ± 10%			Vcc = 2.7 ~ 5.5V			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5.0	5.5	2.7	3.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{CC} + 0.3	2.2	-	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	-0.3*	-	0.8	-0.3*	-	0.4	V

*Note: VIL=-0.3V Min for pulse width less than 50ns.

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Ouput	MODE
H	X	X	Hi-Z	Not Selected
L	H	L	Output Data	Read
L	L	X	Input Data	Write
L	H	H	Hi-Z	Output Disable

*Note: X means "don't care".

DC Electrical Characteristics (V_{CC}=5V ± 10%, 3V ± 10%, T_A = 0 ~ 70℃)

Symbol	Parameter	Conditions		Vcc=3V ± 10%			Vcc=5V ± 10%			Unit
				Min	Typ	Max	Min	Typ	Max	
$I_{I(L)}$	Input Leakage Current	V_{IN} = 0 to V_{CC}		-1	-	1	-1	-	1	μA
$I_{O(L)}$	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{SS} \le V_{OUT} \le V_{CC}$		-1	-	1	-1	-	1	μA
V_{OH}	High Level Output Voltage	I_{OH} = -1.0mA		2.2	-	-	2.4	-	-	V
V_{OL}	Low Level Output Voltage	I_{OL} = 2.1mA		-	-	0.4	-	-	0.4	V
I_{CC}	Operating Supply Current	$\overline{CS}$ = V_{IL}, V_{IN} = V_{IH}/V_{IL}, $I_{I/O}$ = 0mA		-	0.6	10	-	7	15	mA
I_{CC1}	Average Operating Current	$\overline{CS}$ = V_{IL}, V_{IN} = V_{IH}/V_{IL}, $I_{I/O}$ = 0mA, tcycle = Min, cycle		-	-	25	-	-	70	mA
I_{CCS1}	Standby Current	$\overline{CS}$ = V_{IH}		-	-	0.5	-	-	1	mA
I_{CCS2}		$\overline{CS}$ ≥ V_{CC}-0.2V	0 ~ 70 ℃	-	-	10	-	-	25	μA
			25 ℃	-	-	1	-	-	2	μA

*TYP. Values are measured at 25. ℃

AC Operating Characteristics (Vcc=5V ± 10%, 3V ± 10%, T_A = 0 ~ 70℃)

Read Cycle

Symbol	Parameter	Conditions	Vcc=3V ± 10%		Vcc=5V ± 10%		Unit
			Min	Max	Min	Max	
t_{RC}	Read Cycle Time	*1	120	-	55	-	ns
t_{AA}	Address Access Time		-	120	-	55	ns
t_{ACS}	Chip Select Access Time		-	120	-	55	ns
t_{OE}	Output Enable Access Time		-	55	-	30	ns
t_{OH}	Output Hold Time		10	-	5	-	ns
t_{CLZ}	Chip Selection to Output in Low-Z	*2	10	-	5	-	ns
t_{OLZ}	Output Disable to Output in Low-Z		10	-	5	-	ns
t_{CHZ}	Chip Deselection to Output in High-Z		0	40	0	20	ns
t_{OHZ}	Output Disable to Output in High-Z		0	40	0	20	ns

Write Cycle

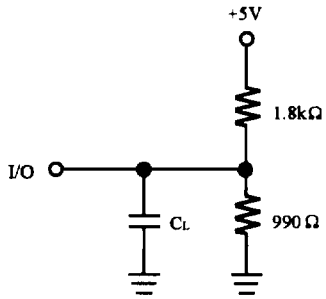
Symbol	Parameter	Conditions	Vcc=3V ± 10%		Vcc=5V ± 10%		Unit
			Min	Max	Min	Max	
t_{WC}	Write Cycle Time	*1	120	-	55	-	ns
t_{CW}	Chip Select to End of Write		100	-	50	-	ns
t_{AW}	Address Set-up Time to End of Write		100	-	50	-	ns
t_{AS}	Address Set-up Time		0	-	0	-	ns
t_{WP}	Write Pulse Width		65	-	45	-	ns
t_{WR}	Write Recovery Time		0	-	0	-	ns
t_{DW}	Data to Write Time Overlap		40	-	25	-	ns
t_{DH}	Data Hold Time		0	-	0	-	ns
t_{WHZ}	Write to Output in High-Z	*2	0	40	0	20	ns
t_{OW}	Output Active from End of Write		10	-	0	-	ns

*1 Test Conditions.

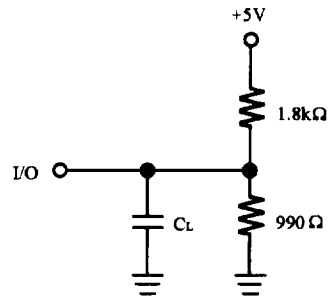
1. Input pulse level : 0.6V to 2.4V
2. $t_r = t_f = 5ns$
3. Input/output timing reference level : 1.5V
4. Output load $C_L = 100pF$

*2 Test Conditions.

1. Input pulse level : 0.6V to 2.4V
2. $t_r = t_f = 5ns$
3. Input timing reference level : 0.8V to 2.2V
4. Output timing reference level :
   ±200mV (the level displacement from stable output voltage level)
5. Output load $C_L = 5pF$



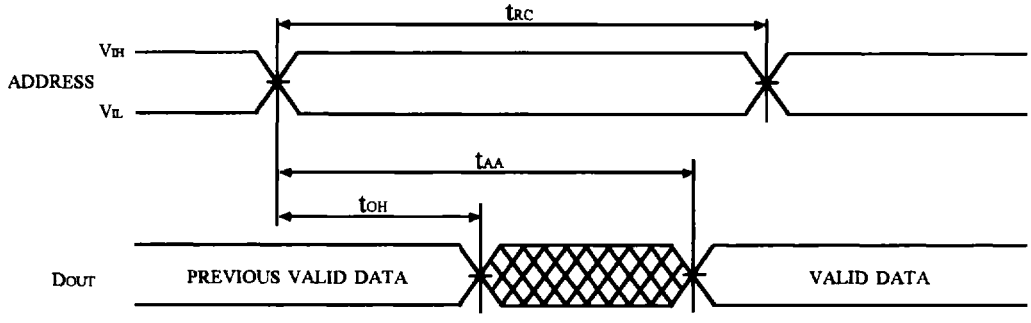
C_L = 100pF (Includes Jig Capacitance)



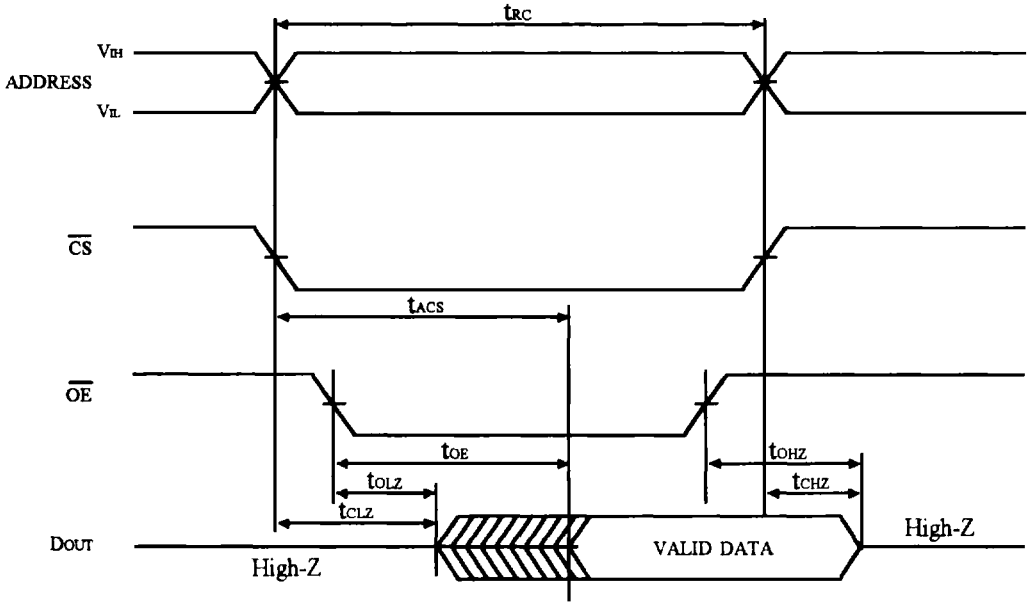
C_L = 5pF (Includes Jig Capacitance)

Timing Waveforms

Read Cycle 1 (Note 1, 3)

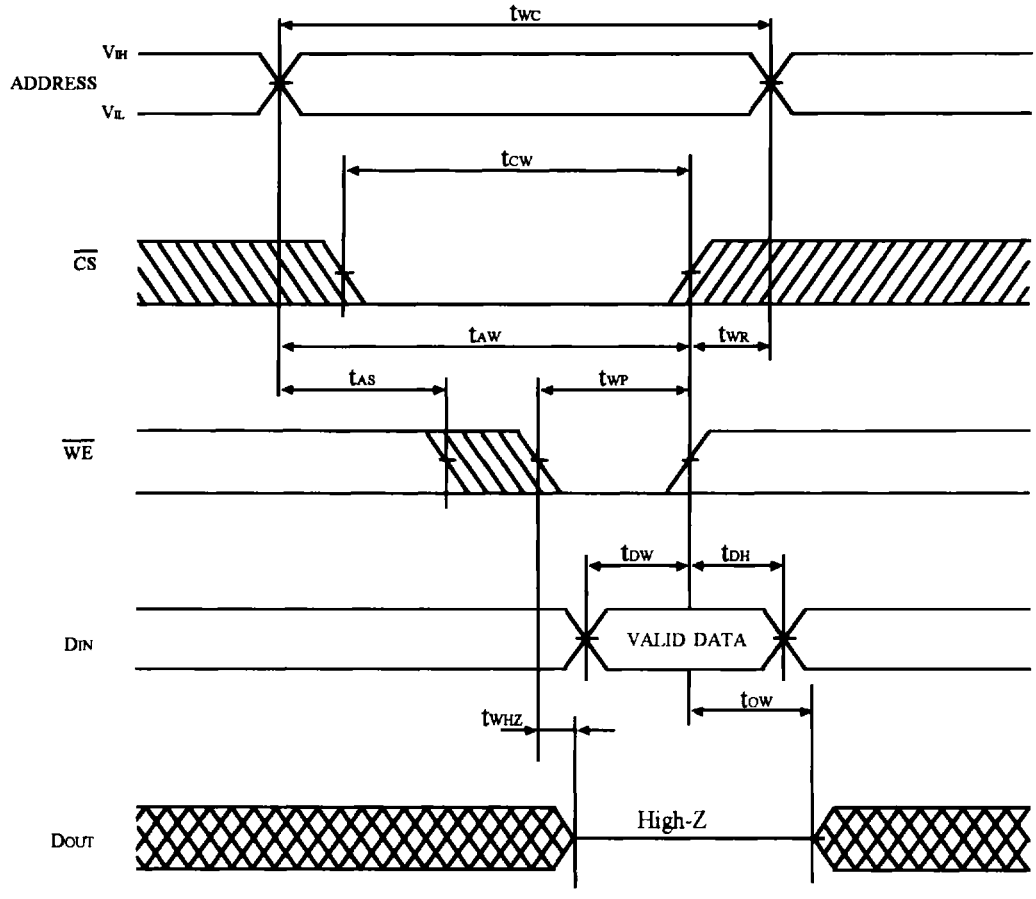


Read Cycle 2 (Note 2, 3)

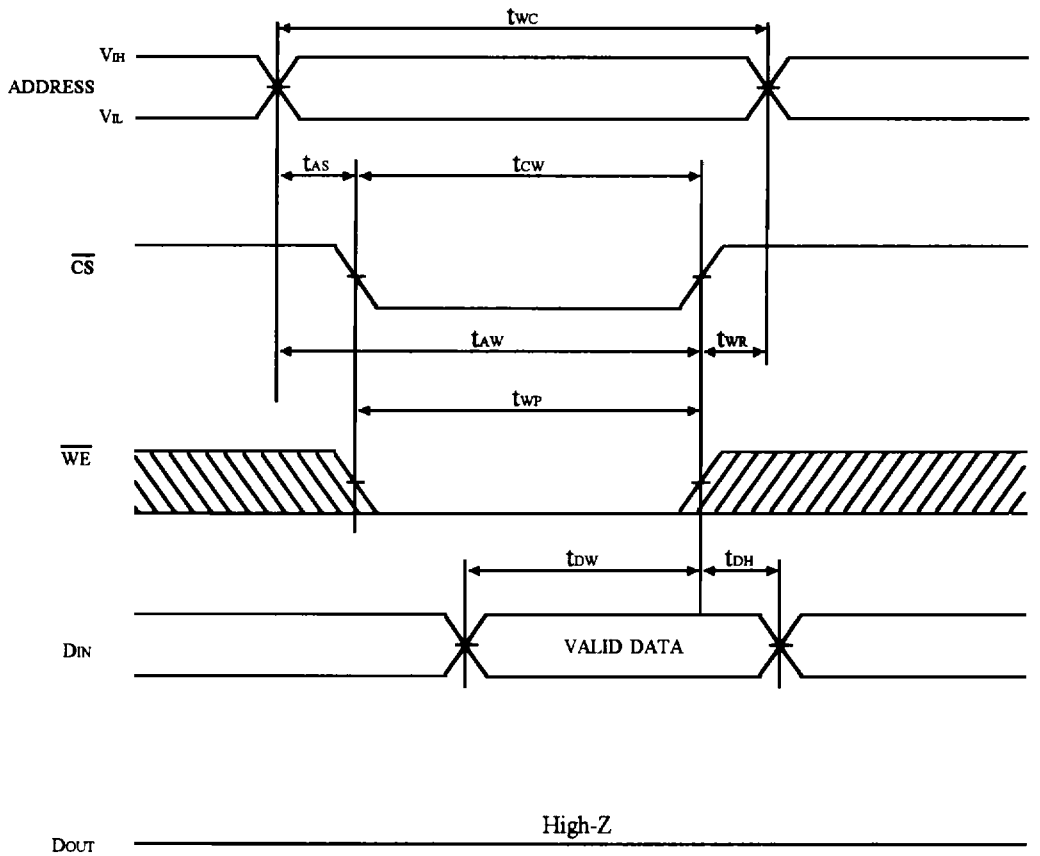


Notes:
1. Device is continuously selected. $\overline{OE}$, $\overline{CS} \leq V_{IL}$.
2. Address valid prior to or coincident with $\overline{CS}$ transition low.
3. $\overline{WE}$ is high for read cycle.

Write Cycle 1 ($\overline{WE}$ Controlled) (Note 1, 2)



Write Cycle 2 ($\overline{CS}$ Controlled) (Note 1, 2, 3)



Notes:
1. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
2. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
3. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

Capacitance

Symbol	Parameter	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	T_A = 25℃, f = 1MHz V_{CC} = 5.0V	-	6	pF
C_{OUT}	Output Capacitance		-	8	pF

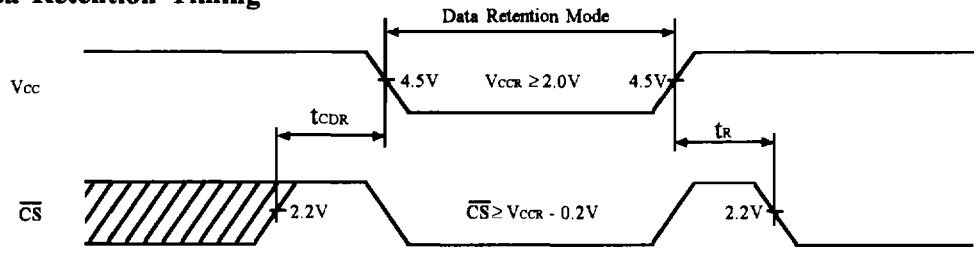
*Note: Tested on a sample basis

Data Retention Characteristics (T_A = 0 ~ 70℃)

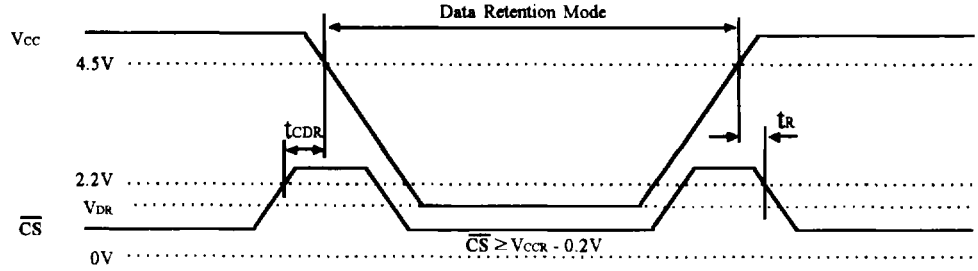
Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_{CCR}	Data Retention Supply Voltage	$\overline{CS} \geq V_{CC}$ - 0.2V		2.0	-	5.5	V
I_{CCR}	Data Retention Current	V_{CC} = 3.0V $\overline{CS} \geq$ 2.8V	BL	-	1*	50	μA
			BLL	-	0.5*	10	
t_{CDR}	Chip Select to Data Retention Time	Refer to the figure below		0	-	-	ns
t_R	Operation Recovery Time			5	-	-	ms

*Note: Typ, Values are measured at 25℃

Data Retention Timing



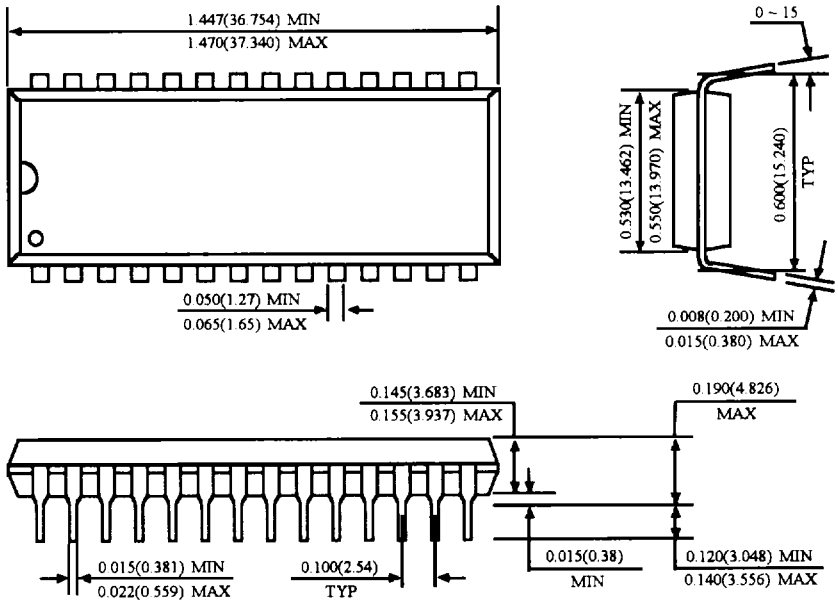
*Note: When retaining data in standby mode, supply voltage can be lowered within a certain range.
Read or write cycle cannot be performed while the supply voltage is low.



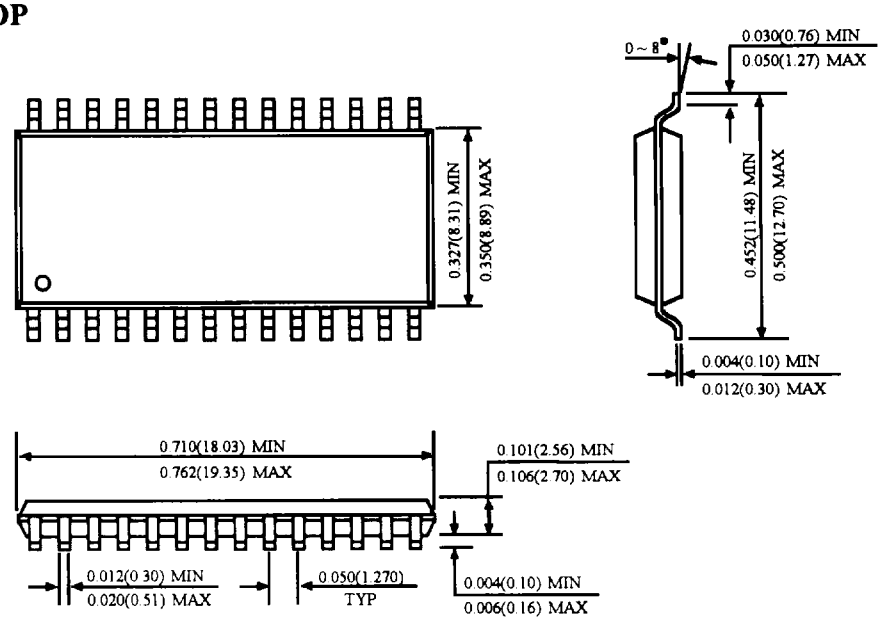
Package Dimensions

Unit: Inches (mm)

28 DIP



28 SOP



Unit: Inches (mm)

28 TSOP