FINAL

Am79512/4

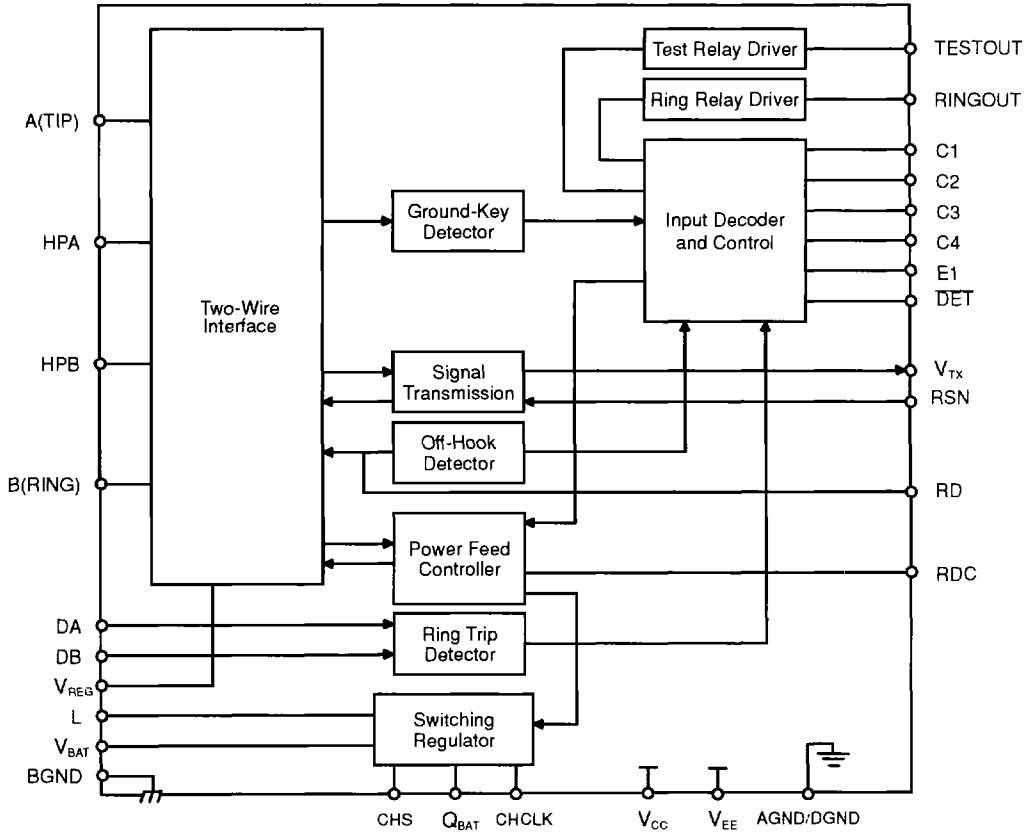
Subscriber Line Interface Circuit

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Programmable constant current feed
- Programmable loop detect threshold
- On-chip switching regulator for low power dissipation
- Polarity reversal feature
- Optimized for –60 V battery
- Line feed characteristics independent of battery variations
- Two-wire impedance set by single external impedance
- Tip open state for ground start lines
- Ring and test relay drivers
- On-hook transmission

BLOCK DIAGRAM



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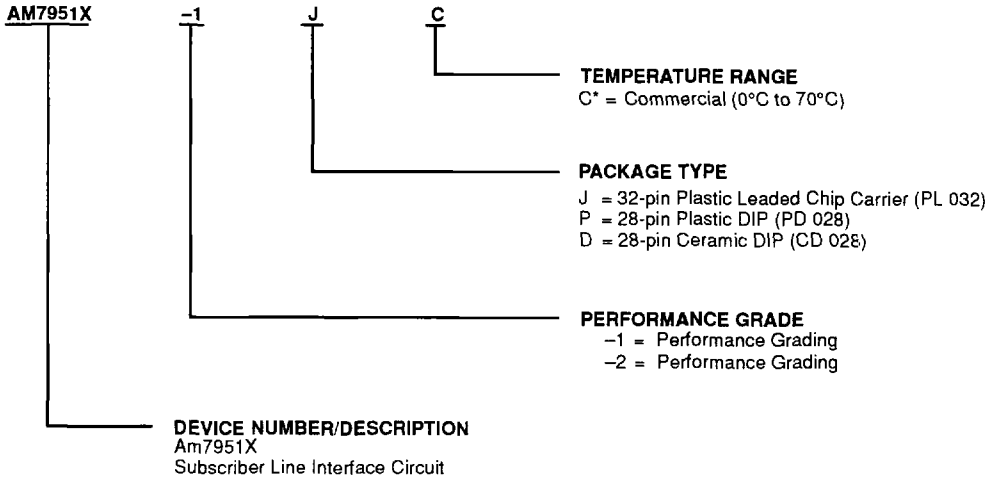
ORDERING INFORMATION

Standard Products

AMD® standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
AM7951X	-1DC, -1JC, -1PC
	-2DC, -2JC, -2PC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

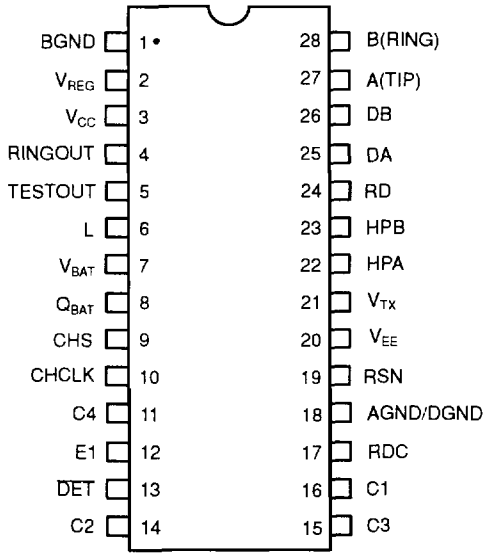
Note:

** Specifications in this data sheet are guaranteed by testing from 0°C to +70°C. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

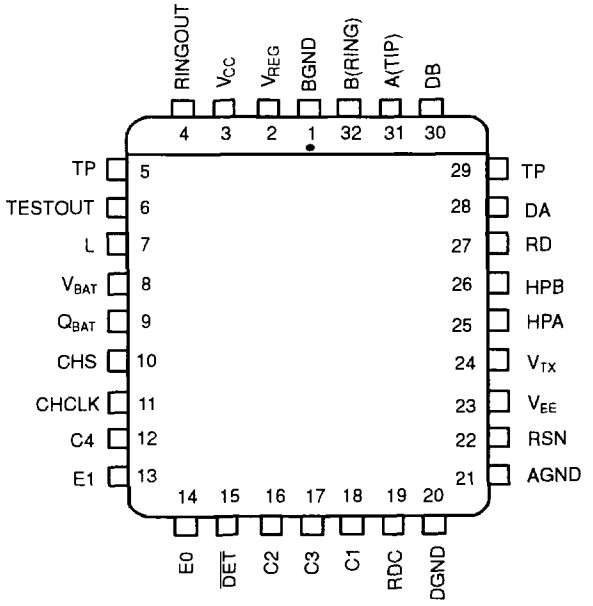
CONNECTION DIAGRAMS

Top View

Am79512



Am79514



Notes:

1. *Pin 1 is marked for orientation.*
2. *TP is a thermal conduction pin tied to substrate.*

PIN DESCRIPTION

AGND
Ground (Am79514)

Analog ground.

DGND
Ground (Am79514)

Digital ground.

AGND/DGND
Ground (Am79512)

Analog and Digital ground are connected internally to a single pin.

A(TIP)
(Output)

Output of A(TIP) power amplifier.

BGND
(Ground)

Battery (power) ground.

B(RING)
(Output)

Output of B(RING) power amplifier.

C3–C1
Decoder (Inputs)

TTL compatible. C3 is MSB and C1 is LSB.

C4
Test Relay Driver Command (Input)

TTL compatible. A logic High enables the driver.

E0
Read Enable (Input)

A logic High enables $\overline{DET}$. A logic Low disables $\overline{DET}$.

E1
Ground Key Enable (Input)

E1 = High connects the ground-key detector to $\overline{DET}$, and E1 = Low connects the off-hook or ring trip detector to $\overline{DET}$.

CHCLK
Chopper Clock (Input)

Input to switching regulator (TTL compatible) Frequency = 256 kHz (Nominal).

CHS
Chopper Stabilization (Input)

Connection for external stabilization components.

DA
Ring Trip Negative (Input)

Negative input to ring trip comparator.

DB
Ring Trip Positive (Input)

Positive input to ring trip comparator.

$\overline{DET}$
Detector (Output)

When enabled, a logic Low indicates that the selected detector is tripped. The detector is selected by the logic inputs (C3–C1, E1). The output is open-collector with a built-in 15K pull-up resistor.

HPA
A(TIP) side of high-pass filter capacitor.

HPB
B(RING) side of high-pass filter capacitor.

L
Switching Regulator Power Transistor (Output)

Connection point for filter inductor and anode of catch diode. This pin will have up to 60 volts of pulse waveform on it and must be isolated from sensitive circuits. Extreme care must be taken to keep the diode connections short because of the high currents and high di/dt.

Q_{BAT}
Quiet Battery

Filtered battery supply for the signal processing circuits. An external 100 Ω, 1/8 W resistor must be connected between Q_{BAT} and V_{BAT} pins.

RD
Detect Resistor Pin

Threshold modification and filter point for the off-hook detector.

RDC
DC Feed Resistor Pin

Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN). The sign of V_{RDC} is minus for normal polarity and plus for reverse polarity.

RINGOUT
Ring Relay Driver (Output)

Sourcing from BGND with internal diode to Q_{BAT}.

RSN

Receive Summing Node (Input)

The metallic current (both AC and DC) between A(TIP) and B(RING) is equal to 1000 times the current into this pin. The networks that program receive gain, two-wire impedance, and feed current all connect to this node. This node is extremely sensitive. Care should be taken to route the 256-kHz chopper clock and switch lines away from the RSN node.

TESTOUT

Test Relay Driver (Output)

Sourcing from BGND with internal diode to Q_{BAT}.

V_{BAT}

Battery supply.

V_{CC}

+5-V power supply.

V_{EE}

–5-V power supply.

V_{REG}

Regulated Voltage (Input)

Provides negative power supply for power amplifiers, connection point for inductor, filter capacitor, and chopper stabilization.

V_{TX}

Transmit Audio (Output)

This output is a unity gain version of the A(TIP) and B(RING) metallic voltage. The other end of the two-wire input impedance programming network connects here.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −55°C to +150°C

V_{CC} with respect to AGND/DGND ... −0.4 V to +7.0 V

V_{EE} with respect to AGND/DGND ... +0.4 V to −7.0 V

V_{BAT} with respect to AGND/DGND ... +0.4 V to −70 V

Note: *Rise time of V_{BAT} (dv/dt) must be limited to 27 V/µs or less when Q_{BAT} bypass = 0.33 µF.*

BGND with respect to
AGND/DGND ..... +1.0 V to −3.0 V

A(TIP) or B(RING) to BGND:

Continuous ..... −70 V to +1.0 V
10 ms (F = 0.1 Hz) ..... −70 V to +5.0 V
1 µs (F = 0.1 Hz) ..... −90 V to +10 V
250 ns (F = 0.1 Hz) ..... −120 V to +15 V

Current from A(TIP) or B(RING) ..... ±150 mA

Voltage on RINGOUT ..... BGND to 70 V above Q_{BAT}

Voltage on TESTOUT ..... BGND to 70 V above Q_{BAT}

Current through relay drivers ..... 60 mA

Voltage on ring trip inputs DA and DB .... V_{BAT} to 0 V

Current into ring trip inputs ..... ±10 mA

Peak current into regulator switch (L pin) .... 150 mA

Switcher transient peak off voltage on L pin ... +1.0 V

C4–C1, E1, CHCLK,
to AGND/DGND ..... −0.4 V to V_{CC} + 0.4 V

Maximum power dissipation, (see note) ... T_A = 70°C

In 28-pin ceramic DIP package ..... 2.58 W

In 28-pin plastic DIP package ..... 1.4 W

In 32-pin PLCC package ..... 1.74 W

Note: *Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never be exposed to this temperature. Operation above 145°C junction temperature may degrade device reliability. See SLIC Packaging Considerations section for more information.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature ..... 0°C to +70°C*

V_{CC} ..... 4.75 V to 5.25 V

V_{EE} ..... −4.75 V to −5.25 V

V_{BAT} ..... −40 V to −63 V

AGND/DGND ..... 0 V

BGND with respect to
AGND/DGND ..... −100 mV to +100 mV

Load resistance on V_{TX} to ground ..... 10 kΩ Min

Operating Ranges define those limits between which the functionality of the device is guaranteed.

** Specifications in this data sheet are guaranteed by testing from 0°C to +70°C. Performance from −40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

ELECTRICAL CHARACTERISTICS (See Note 1)

Description	Test Conditions	P.G.*	Final			Unit	Note
			Min	Typ	Max		
Analog (V_{TX}) output impedance				3	20	Ω	
Analog (V_{TX}) output offset	0°C to +70°C –40°C to +85°C		–35 –40		+35 +40	mV mV	 5
Analog (RSN) input impedance	300 Hz to 3.4 kHz			1	20	Ω	
Longitudinal impedance at A or B					35	Ω	
Overload level Z_{2WIN} = 600 Ω to 900 Ω	4-wire 2-wire		–3.1 –3.1		+3.1 +3.1	Vpk	2
Transmission Performance, 2-Wire Impedance							
2-wire return loss (See Test Circuit D)	300 Hz to 500 Hz 500 Hz to 2500 Hz 2500 Hz to 3400 Hz		26 26 20			dB	5
Longitudinal Balance (2-Wire and 4-Wire, See Test Circuit C)							
Longitudinal to metallic L-T, L-4	200 Hz to 1 kHz normal polarity 0°C to +70°C normal polarity –40°C to +85°C reverse polarity	 –1 –2 –2 –2	 50 63 58 58			 dB	 4
	1 kHz to 3.4 kHz normal polarity 0°C to +70°C normal polarity –40°C to +85°C reverse polarity	 –1 –2 –2 –2	 52 58 54 54			 dB	
Longitudinal sum (L-T) + (T-L)	300 to 3400 Hz		95			dB	
Longitudinal signal generation 4-L or T-L	300 to 800 Hz 800 to 3400 Hz		40 35			dB	
Longitudinal current capability per wire	Active state OHT state				17 8	mArms	
Insertion Loss (2-Wire to 4-Wire and 4-Wire to 2-Wire, See Test Circuits A and B)							
Gain accuracy	0 dBm, 1 kHz, 0°C to +70°C 0 dBm, 1 kHz, –40°C to +85°C 0 dBm, 1 kHz, 0°C to +70°C 0 dBm, 1 kHz, –40°C to +85°C	 –1 –1	–0.15 –0.20 –0.1 –0.15		+0.15 +0.20 +0.1 +0.15	dB dB dB dB	 5 5
Variation with frequency	300 Hz to 3400 Hz Relative to 1 kHz 0°C to +70°C –40°C to +85°C		 –0.1 –0.15		 +0.1 +0.15	 dB dB	 5
Gain tracking	+7 dBm to –55 dBm 0°C to +70°C –40°C to +85°C		 –0.1 –0.15		 +0.1 +0.15	 dB dB	

Note:

** P.G. = Performance Grade*

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions	P.G.*	Final Min	Final Typ	Final Max	Unit	Note
Balance Return Signal (4-Wire to 4-Wire, See Test Circuit B)							
Gain accuracy	0 dBm, 1 kHz, 0°C to +70°C		–0.15		+0.15	dB	
	0 dBm, 1 kHz, –40°C to +85°C		–0.20		+0.20	dB	5
	0 dBm, 1 kHz, 0°C to +70°C	–1	–0.1		+0.1	dB	
	0 dBm, 1 kHz, –40°C to +85°C	–1	–0.15		+0.15	dB	5
Variation with frequency	300 Hz to 3400 Hz Relative to 1 kHz						
	0°C to +70°C		–0.1		+0.1	dB	
	–40°C to +85°C		–0.15		+0.15	dB	5
Gain tracking	+7 dBm to –55 dBm						
	0°C to +70°C		–0.1		+0.1	dB	
	–40°C to +85°C		–0.15		+0.15	dB	
Group delay	F = 1 kHz			5.3		µs	
Total Harmonic Distortion (2-Wire to 4-Wire or 4-Wire to 2-Wire, See Test Circuits A and B)							
Distortion level	0 dBm, 300 Hz to 3400 Hz			–64	–50	dB	
Distortion level	+9 dBm			–55	–40	dB	
Idle Channel Noise							
Psophometric weighted noise	2-wire 0°C to +70°C			–83	–78	dBmp	5, 7
	2-wire –40°C to +85°C			–83	–75		
	4-wire 0°C to +70°C			–83	–78	dBmp	5, 7
	4-wire –40°C to +85°C			–83	–75		
Single Frequency Out-of-Band Noise (See Test Circuit E)							
Metallic	4 kHz to 9 kHz			–76			
	9 kHz to 1 MHz			–76		dBm	4, 5, 9
	256 kHz and harmonics			–57			4, 5
Longitudinal	1 kHz to 15 kHz			–70			
	Above 15 kHz			–85		dBm	4, 5, 9
	256 kHz and harmonics			–57			4, 5
DC Feed Current and Voltage (See Figure 1) Unless otherwise noted, Battery = 60 V (V_{BAT} = –59.3 V)							
Active mode loop current accuracy –1	I_{LOOP} (nominal) = 40 mA		–7.5		+7.5	%	
	R_L = 2000 Ω, Battery = 62 V		23			mA	
–2	R_L = 2080 Ω		22.7			mA	5
On-hook loop voltage	$R_L = \infty$		47.5	49		V	
OHT mode	R_L = 600 Ω		18	20	22	mA	
Tip open mode	R_L = 600 Ω				1.0		
Disconnect mode	R_L = 0				1.0		
Power Dissipation, Battery = –60 V							
On-hook open circuit				50	120		
On-hook OHT mode				175	250		
On-hook active mode				260	400	mW	
Off-hook OHT mode	R_L = 600 Ω			500	750		
Off-hook active mode	R_L = 600 Ω			650	1000		

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions	P.G.*	Final Min	Final Typ	Final Max	Unit	Note
Supply Currents							
V_{CC} On-hook supply current	Open circuit mode OHT mode Active mode			3 6 7.5	4.5 10 12	mA	
V_{EE} On-hook supply current	Open circuit mode OHT mode Active mode			1.0 2.2 2.7	2.3 3.5 6.0	mA	
V_{BAT} On-hook supply current	Open circuit mode OHT mode Active mode			0.4 3.0 4.0	1.0 5.0 6.0	mA	
Power Supply Rejection Ratio (Vripple = 50 mVrms)							
V_{CC}	40 Hz to 3400 Hz 3.4 kHz to 50 kHz		20 20	35 30		dB	6, 7
V_{EE}	40 Hz to 3400 Hz 3.4 kHz to 50 kHz		20 15	30 25		dB	6, 7
V_{BAT}	40 Hz to 3400 Hz 3.4 kHz to 50 kHz		27 20	30 30		dB	6, 7
Off-Hook Detector							
Current threshold	$I_{DET} = 365/R_D$		–20		+20	%	
Ground Key Detector Thresholds Active Mode, Battery = –60 V							
Ground key resistance threshold	B(RING) to GND		2.0	4.2	10.0	kΩ	
Ground key current threshold	B(RING) or midpoint to GND			9		mA	8
Ring Trip Detector Input							
Bias current			–5	–0.05		µA	
Offset voltage	Source resistance = 0 to 200 kΩ		–50	0	+50	mV	
Logic Inputs (C1, C2, C3, C4, E1, and CHCLK)							
Input High voltage			2.0			V	
Input Low voltage					0.8	µA	
Input High current	All inputs except E1		–75		40	µA	
Input High current	Input E1		–75		45	µA	
Input Low current			–0.4			mA	
Logic Output (DET)							
Output Low voltage	$I_{OUT} = 0.8$ mA				0.4	V	
Output High voltage	$I_{OUT} = -0.1$ mA		2.4			V	

Table 1. SLIC Decoding

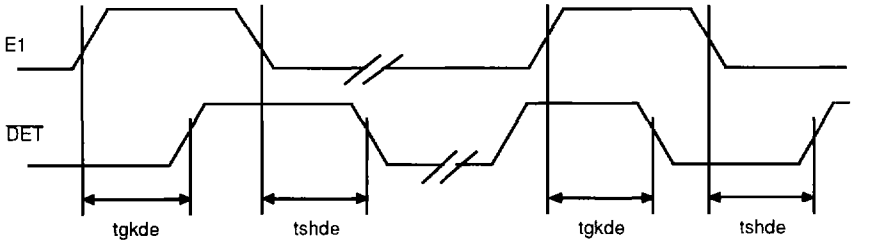
State	C3	C2	C1	Two-Wire Status	DET Output E1 = 0	DET Output E1 = 1
0	0	0	0	Open circuit	Ring trip	Ring trip
1	0	0	1	Ringing	Ring trip	Ring trip
2	0	1	0	Active	Loop det.	Ground key
3	0	1	1	On-hook TX (OHT)	Loop det.	Ground key
4	1	0	0	Tip open	Loop det.	—
5	1	0	1	Reserved	Loop det.	—
6	1	1	0	Active polarity reversal	Loop det.	Ground key
7	1	1	1	OHT polarity reversal	Loop det.	Ground key

SWITCHING CHARACTERISTICS

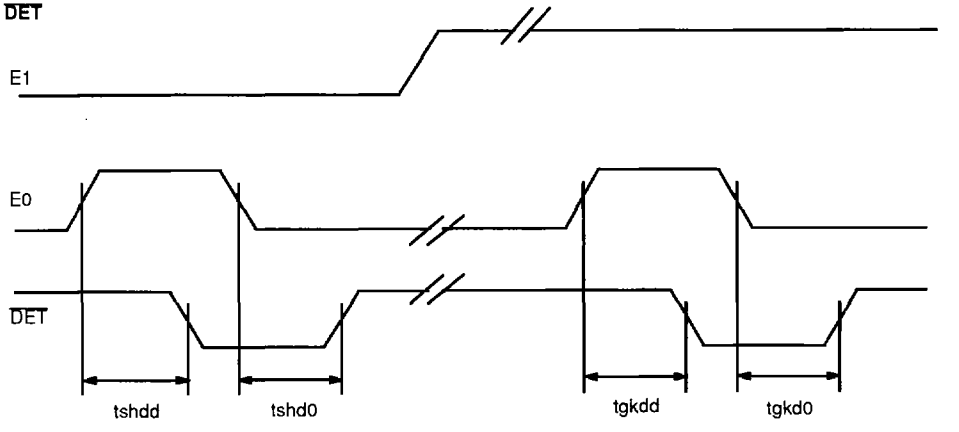
Symbol	Parameter	Test Conditions	Temperature Ranges	Min	Typ	Max	Unit	Note
tgkde	E1 Low to $\overline{DET}$ High (E0 = 1)	Ground key detect mode R_L open, R_G connected (See Figure H)	0°C to +70°C			3.8	µs	5
			−40°C to +85°C			4.0		5
	E1 Low to $\overline{DET}$ Low (E0 = 1)		0°C to +70°C			1.1		5
			−40°C to +85°C			1.6		5
tgkdd	E0 High to $\overline{DET}$ Low (E1 = 0)		0°C to +70°C			1.1		5
			−40°C to +85°C			1.6		5
tgkd0	E0 Low to $\overline{DET}$ High (E1 = 0)		0°C to +70°C			3.8		5
			−40°C to +85°C			4.0		5
tshde	E1 High to $\overline{DET}$ Low (E0 = 1)	Switch hook detect mode R_L = 600 Ω, R_G open (See Figure G)	0°C to +70°C			1.2	µs	5
			−40°C to +85°C			1.7		5
	E1 High to $\overline{DET}$ High (E0 = 1)		0°C to +70°C			3.8		5
			−40°C to +85°C			4.0		5
tshdd	E0 High to $\overline{DET}$ Low (E1 = 1)		0°C to +70°C			1.1		5
			−40°C to +85°C			1.6		5
tshd0	E0 Low to $\overline{DET}$ High (E1 = 1)		0°C to +70°C			3.8		5
			−40°C to +85°C			4.0		5

SWITCHING WAVEFORMS

E1 to $\overline{DET}$



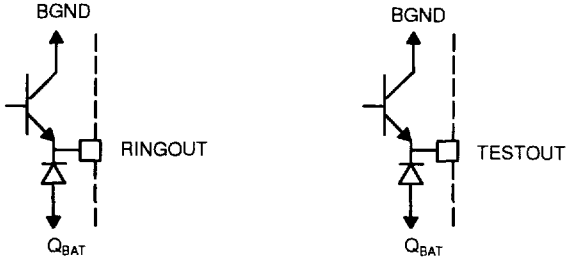
E0 to $\overline{DET}$



Note:

All delays measured at 1.4-V level.

RELAY DRIVER SPECIFICATIONS



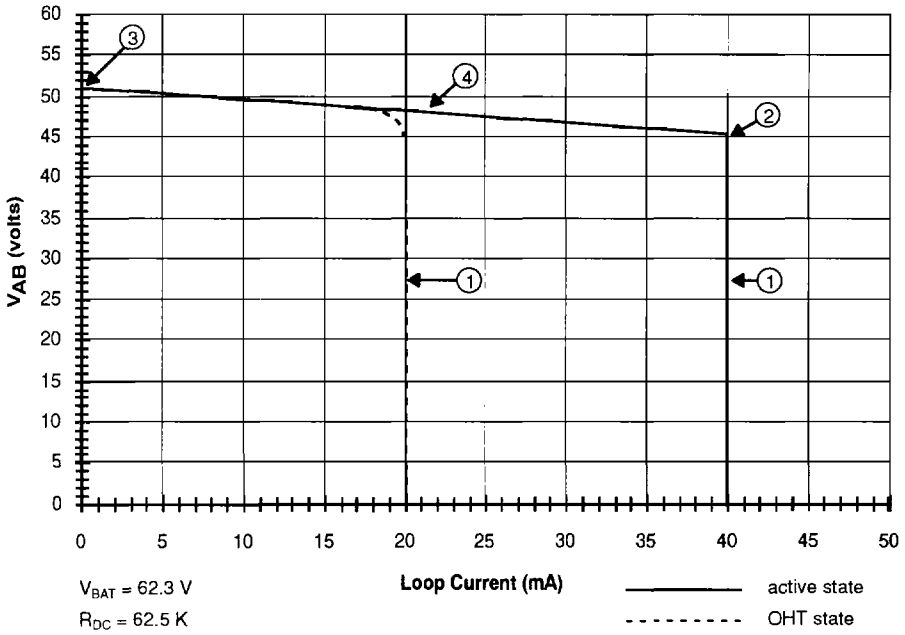
Description	Test Conditions	Min	Typ	Max	Unit	Note
Relay Driver Outputs (RINGOUT, TESTOUT)						
On voltage	50-mA source	B_{GND}–2			V	
Off leakage			0.5	100	µA	
Clamp voltage	50-mA sink	Q_{BAT}–2			V	

Notes:

1. *Unless otherwise noted, test conditions are: V_{BAT} = –60 V, V_{CC} = +5 V, V_{EE} = –5 V, R_L = 600 Ω, C_{HP} = 0.33 µF, R_{DC1} = R_{DC2} = 31.25k, C_{DC} = 0.1 µF, Rd = 51.1k, No fuse resistors, two-wire AC output impedance programming impedance (Z_T) = 600K resistive, Receive input summing impedance (Z_{RX}) = 300k resistive. (See Table 2 for component formulas.)*
2. *Overload level is defined when THD = 1%.*
3. *Balance return signal is the signal generated at V_{TX} by V_{RX}. This spec assumes that the two-wire AC load impedance matches the impedance programmed by Z_T.*
4. *These tests are performed with a longitudinal impedance of 90 Ω and metallic impedance of 300 Ω for frequencies below 12 kHz and 135 Ω for frequencies greater than 12 kHz. These tests are extremely sensitive to circuit board layout. Please refer to application notes for details.*
5. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
6. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*
7. *When the SLIC is in the Anti-Sat 2 operating region, this parameter will be degraded. The exact degradation will depend on system design. The Anti-sat 2 region occurs at high loop resistances when $|V_{BAT}| - |V_{AX} - V_{BX}|$ is less than approximately 15 V.*
8. *"Midpoint" is defined as the connection point between two 300 Ω series resistors connected between A(TIP) and B(RING).*
9. *Fundamental and harmonics from 256-kHz switch regulator chopper are not included.*

Table 2. User-Programmable Components

$Z_T = 1000\ (Z_{2WIN} - 2R_F)$	Where Z_T is connected between the V_{TX} and RSN pins. The fuse resistors are R_F and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between V_{TX} and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G_{42L}} \bullet \frac{1000 \bullet Z_T}{Z_T + 1000\ (Z_L + 2R_F)}$	Where Z_{RX} is connected from V_{RX} to the RSN pin, Z_T is defined above, G_{42L} is the desired receive gain and Z_L is the 2-wire load impedance.
$R_{DC1} + R_{DC2} = \frac{2500}{I_{FEED}}$	Where R_{DC1}, R_{DC2}, and C_{DC} form the network $C_{DC} = (1.5\ ms)(R_{DC1} + R_{DC2})/(R_{DC1} \bullet R_{DC2})$ connected to the RDC pin. R_{DC1} and R_{DC2} are approximately equal.
$R_D = \frac{365}{I_T}, \quad C_D = \frac{0.5\ ms}{R_D}$	Where R_D and C_D form the network connected from RD to –5 V and I_T is the threshold current between on-hook and off-hook.



Notes:

1. *Constant current region:*

   active state, $I_L = \frac{2500}{R_{DC}}$

   OHT state, $I_L = \frac{1}{2} \bullet \frac{2500}{R_{DC}}$

2. *Anti-sat cut-in:*

   $V_{AB} = 46\ V,$ $\quad |V_{BAT}| \geq 58.9\ V$

   $V_{AB} = 1.087\ |V_{BAT}| - 18.017,$ $\quad |V_{BAT}| < 58.9\ V$

3. *Open-circuit voltage:*

   $V_{AB} = 51.23\ V,$ $\quad |V_{BAT}| \geq 61.5\ V$

   $V_{AB} = 1.073\ |V_{BAT}| - 14.72,$ $\quad |V_{BAT}| < 61.5\ V$

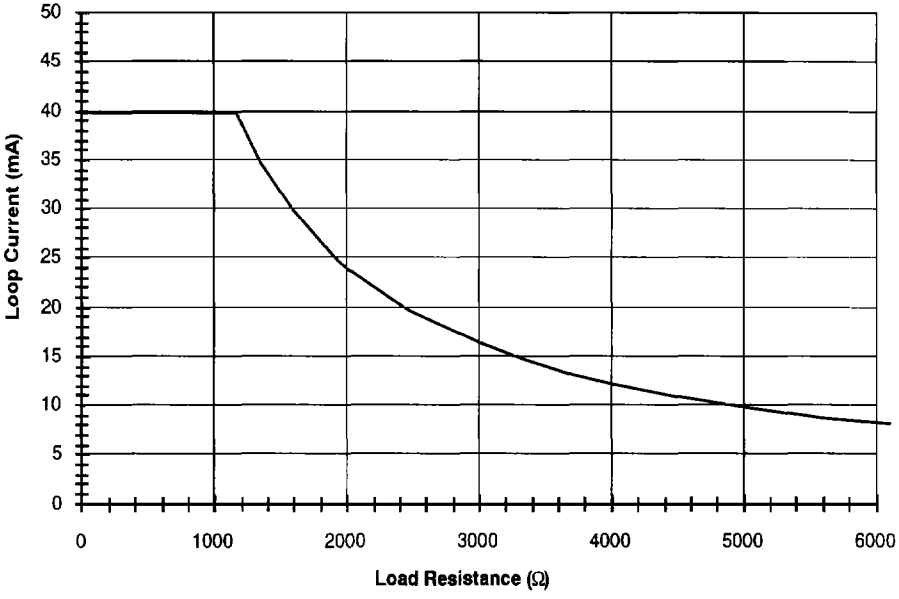
4. *Anti-sat 1 Region:*

   $V_{AB} = 51.23 - I_L \frac{R_{DC}}{488.3}$

5. *Anti-sat 2 Region:*

   $V_{AB} = 1.073\ |V_{BAT}| - 14.72 - I_L \frac{R_{DC}}{1071}$

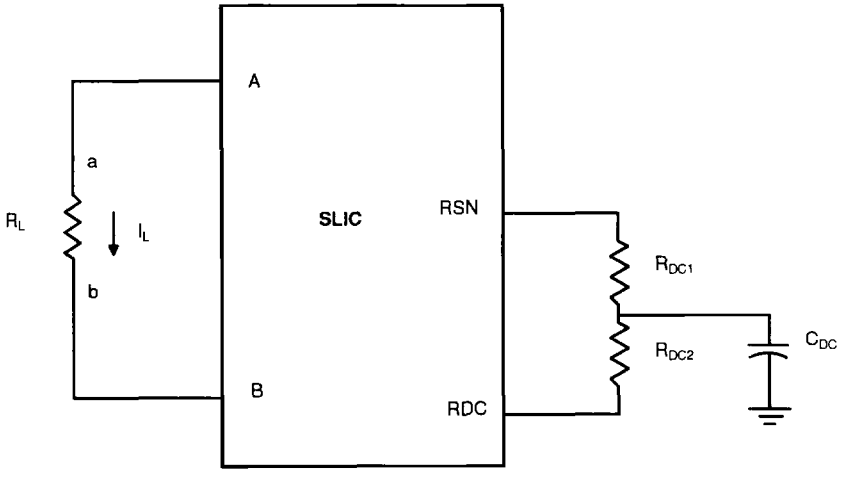
a. V_A–V_B (V_{AB}) Voltage vs Loop Current (Typical)



V_{BAT} = 62.3 V

R_{DC} = 62.5 K

b. Loop Current vs Load Resistance (Typical)



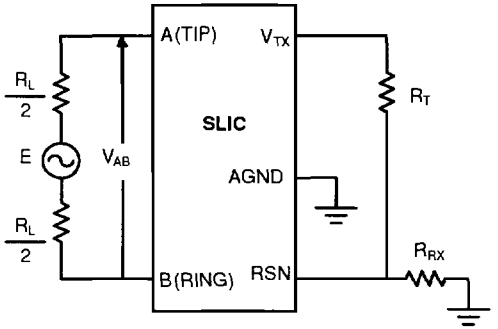
c. Feed Programming

Note:

Feed current programmed by R_{DC1} and R_{DC2}.

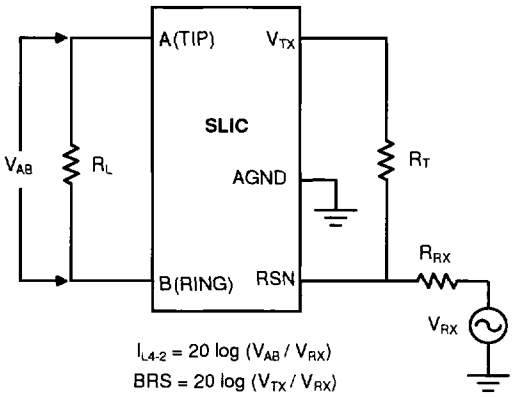
Figure 1. DC Feed Characteristics

TEST CIRCUITS



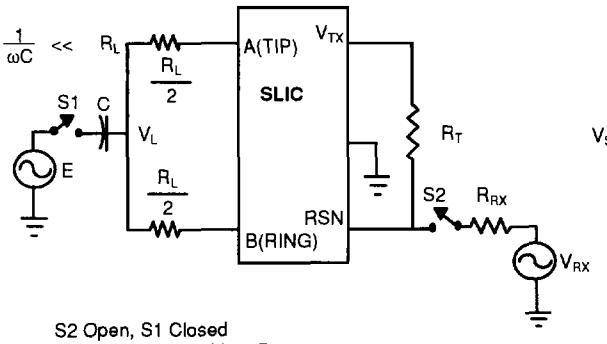
$I_{L2-4} = 20 \log (V_{TX} / V_{AB})$

A. Two-to-Four-Wire Insertion Loss



$I_{L4-2} = 20 \log (V_{AB} / V_{RX})$
$BRS = 20 \log (V_{TX} / V_{RX})$

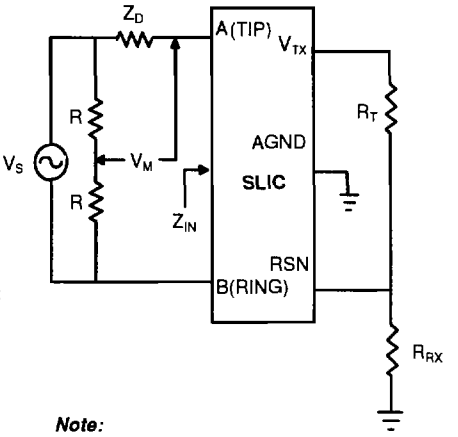
B. Four-to-Two-Wire Insertion Loss and Balance Return Signal



S2 Open, S1 Closed
L-T Long. Bal. = 20 log (V_{AB} / E)
L-T Long. Rej. = 20 log (V_{TX} / E)

S2 Closed, S1 Open
4-L Long. Sig. Gen. = 20 log (V_L / V_{RX})

C. Longitudinal Balance (IEEE)

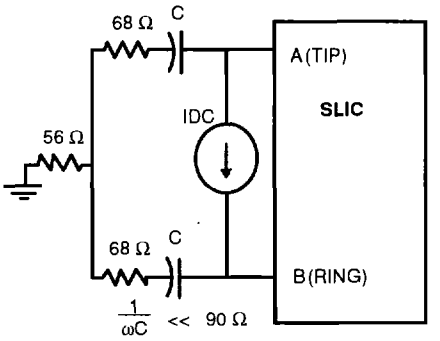


Note:
Z_O is the desired impedance (e.g., the characteristic impedance of the line).

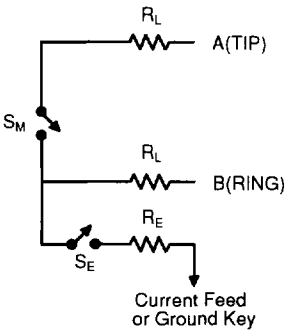
$R_L = \log (2V_M / V_S)$

D. Two-Wire Return Loss Test Circuit

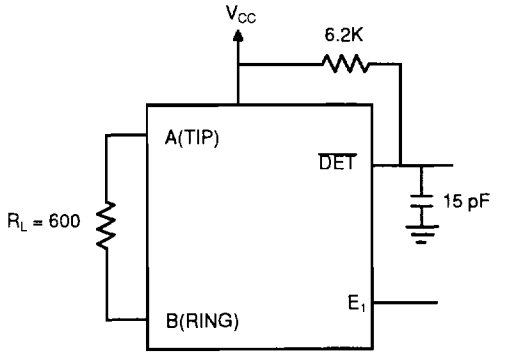
TEST CIRCUITS (continued)



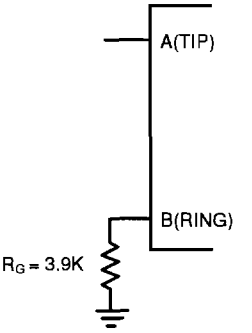
E. Single Frequency Noise



F. Ground-Key Detection



G. Loop Detector Switching



H. Ground-Key Switching