July 1997

Multi-Cache Controller™

DATA SHEET

Integrated Cache Controller for SuperSPARC

DESCRIPTION

The STP1091 is a high-performance external cache controller for the STP1020 (SuperSPARC) and STP1021 (SuperSPARC-II) microprocessors. It is used when a large secondary cache or an interface to a non-MBus system is required. The 2.2 million transistor STP1091 supports up to 2Mbytes of direct-mapped secondary cache (XBusTM) so that effective memory latencies are reduced. The cache controller also integrates 33x8k synchronous tag RAM to reduce system cost. The STP1091 can be configured to interface with two multi-processor system buses: MBus, a circuit-switched MP bus, and XBus, a packet-switched bus. It isolates the SuperSPARC processor from these system buses, allowing faster processor clock operation with a slower system clock.

The STP1091 is a new version of the multi-cache controller STP1090. Like its predecessor this new part is fully SPARC version 8 compliant and is completely upward compatible with the earlier SPARC version 7 implementations running over 8500 SPARC applications and development tools.

The 50 MHz and 60 MHz versions of the STP1091 are for use with the 50 MHz and 60 MHz versions of the STP1020, respectively. The 75 MHz and 90 MHZ version of the STP1091 is usable for either the 75 MHz version of the STP1021 or the 75MHz and 90 MHz version of the STP1021A respectively.

All references to STP1021 in this document also apply to STP1021A.

Features

- High performance cache controller with 75/90 MHz operating frequency
- · Selectable system bus interface
 - SPARC standard MBus or other multiprocessing Buses
- · Cache coherency support for multiprocessing
- Processor bus (VBus) and system bus (MBus or XBus) may be operated at different frequencies
- Integrated cache tags and cache controller with support for several external cache sizes
 - 1 Mbyte (MBus) / 512 KBytes, 1 Mbyte, or 2 MBytes (XBus)
- · Integrated cache hit/miss monitoring registers
- · 8-Bit Boot Bus for ROM and Peripherals (XBus only)
- . Built-In Self Test (BIST) logic
- Full JTAG interface (IEEE1149.1)

Benefits

- Delivers optimum STP1021/STP1021A (SuperSPARC) performance
- Increases reliability by reducing number of devices required in systems
- · Allows a wide range of scalable systems to be built
- Decouples processor from rest of the system to permit ease of frequency scaleability
- Provides flexibility in external cache configurations for a variety of applications
- · Convenient cache performance monitoring support
- · Eliminates slow devices from high speed XBus
- · Provides quick check of device integrity
- · Provides better testability at the board/system level

The STP1091 is intended for use in a broad range of applications from uniprocessor desktop machines to large multiprocessor servers. The STP1091 external cache controller supports multiprocessor configurations using either MBus or XBus interfaces with up to 2 MBytes of secondary cache.

Figure 1 shows an STP1021 based system using the STP1091 external cache controller in an MBus configuration. In this mode, it supports either no external cache or 1MByte external cache.

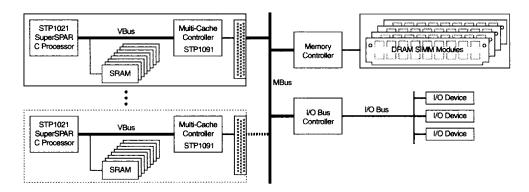


Figure 1. Typical STP1091 Uniprocessor / Multiprocessor System with MBus Interface

Figure 2 shows an STP1021 based system using the STP1091 controller in an XBus configuration. In this mode, it supports cache sizes of 0.5 Mbyte, 1 Mbyte, or 2 MBytes. A maximum of four bus watchers can interface with the STP1091, and each of these can support different system buses.

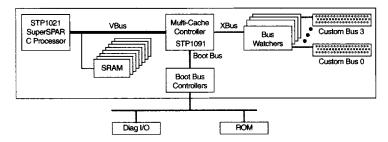


Figure 2. STP1091 System with XBus Interface and External Bus Watchers



TECHNICAL OVERVIEW

Architecture

Figure 3 shows an overview of the STP1091 microarchitecture. The STP1091 can be partitioned into five large functional blocks:

Cache Controller Core: This includes the external cache tag memory, the processor command logic, and the bus command logic. The external cache tag memory keeps track of the usage of the secondary cache. The tag memory is organized as 33 x 8K-bit synchronous memory. In MBus configurations, the tag memory is used for both cache access and bus snooping, whereas in XBus mode, it is used only for cache access. The processor command logic is a group of finite state machines that handle incoming commands from SuperSPARC. They generate bus commands through a request queue. The bus command logic deals with the acknowledgment of these bus requests. The XBus and MBus interfaces place all requests in the input queue, and the bus command logic places corresponding replies in the reply queue.

Processor Interface: The STP1091 interfaces to the SuperSPARC processor through the VBus. The processor interface block shields the bus command logic from VBus arbitration by buffering all VBus accesses. It is also responsible for arbitrating the usage of VBus among the SuperSPARC processor, processor command logic, and the bus command logic.

System Bus Interface: This includes the MBus interface, the XBus interface, and the XBus arbitration logic. The STP1091 operates in the MBus or XBus mode, as selected by the MBSEL pin. When MBSEL is high, the MBus interface is selected.

Queues and Synchronizers: The input queue, request queue, and reply queue are first-in, first-out (FIFO) queues used to communicate between the two clock domains, namely the processor clock and the bus clock. They are implemented with dual-port register files. Control strobes are sent between the two domains through synchronizers, which can be disabled for synchronous operation where both clocks are the same.

Boot Bus Interface: The boot bus interface handles all accesses to the 8-bit boot bus. It implements the address and data multiplexing functions on the bus, as well as the automatic polling of interrupts.

The STP1091 also integrates BIST (Built-In-Self-Test) logic, JTAG interface, and has features that support system and software debugging.

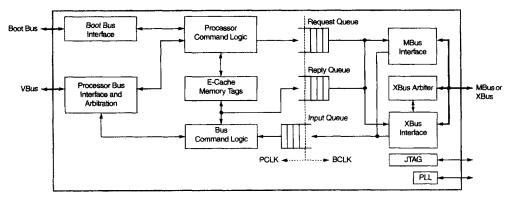


Figure 3. STP1091 Block Diagram

Modes of Operation

The STP1091 allows the system designer to select one of the two modes of operation. This selection is designed-in by statically connecting the MBSEL pin to Ground or V_{CC} . When the MBSEL pin is tied to Ground, the STP1091 operates with XBus interface. When the MBSEL pin is pulled high, the part operates with a MBus interface. Irrespective of the system bus type, the STP1091 always interfaces to the processor through the VBus.

TABLE 1: Configuration Changes with MBSEL Pin

Sub-Block Size	32 bytes	64 bytes
Block Size	128 bytes	256 bytes
Minimum Cache	1 MB	512 KB
Maximum Cache	1 MB	2 MB
Boot-Bus	Not Available	Available
Interrupts	From Pins	From XBus Packets

VBus is a non-multiplexed synchronous bus. It is especially tailored to provide an efficient connection between the STP1021, the STP1091 (the external cache controller), and the external cache memory made up of synchronous SRAMs. It has a 36-bit address bus, and a 64-bit data bus. All transactions on the VBus are synchronized with the STP1021 clock. The arbiter for the VBus transactions is integrated on the STP1091 chip.

In the VBus mode, the STP1021 provides an $\overline{ADDR20}$ signal besides the ADDR20 signal. By contrast, the STP1020N, and STP1020 do not drive this signal. The $\overline{ADDR20}$ is now driven out on a pin that used to be spare3. The $\overline{ADDR20}$ is useful in systems that incorporate 2 MBytes of external cache, and its integration onto the cache controller eliminates an external inverter.

MBus is a SPARC International standard bus designed to function as a processor-independent bus between one or more processors and memory. It is a 64-bit multiplexed high-performance bus. It is fully synchronous with all the transfers controlled by an MBus clock. It supports block transfers in sizes up to 128 bytes with a peak transfer rate of 320 MBytes/s. All transactions on the MBus are arbitrated by an external arbiter. The arbitration algorithm is not included in the MBus definition to allow flexibility in system design. MBus is defined for uniprocessor and multiprocessor systems. The uniprocessor form of MBus is termed "Level1", and the multiprocessor version is called "Level2".

XBus is an extension bus that allows the STP1091 to be connected to one or more system bus interfaces called "Bus Watchers". XBus uses an advanced, synchronous, packet-switched protocol to provide low latency and high bandwidth. It consists of 82 bussed signals, along with three point-to-point arbitration signals per bus watcher. The STP1091 contains a pipelined arbiter that controls accesses to the XBus. In the XBus mode, the STP1091 supports block sizes of 256 bytes.

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SIGNAL DESCRIPTIONS

TABLE 2: Signal Descriptions - MBus Configuration (MBSEL=H)

ADDR[35:0] [1]	1/0	Processor physical address bus.
ADDR20	0	Inverted physical address ADDR20. Eliminates an external inverter for 2MB cache systems.
AERR	0	Indicates either an internal STP1091 error or ERROR is asserted by the processor.
		H = No error.
		L = An internal processor or STP1091 error.
BPLLRC	1	Capacitor for the phase filter of the bus clock PLL. This pin should be connected to an external capacitor to ground. With an internal resistor, this circuit provides the RC time constant for the phase filter of the bus clock domain PLL.
BURST [1]	1	Indicates whether a burst access is in progress. BURST is driven at the same time as ADDR[35:0], and it is asserted during both read bursts and write bursts. BURST is deasserted on the last address of a burst to allow the STP1091 to stop returning RRDY or WRDY with the last data of the burst. H = A burst access is in progress. L = A burst access is not in progress.
CCHBL [1]	-	
COMBL	, ,	This pin indicates the current processor transaction as one that may be cached in an external cache.
		H = Noncacheable access.
		L = Cacheable access.
CMDS [1]	1/0	Command strobe. Indicates the beginning of a bus cycle. The VBus master asserts this signal for one cycle to begin all of its accesses.
		When the STP1091 is a bus master, as indicated by WGRT and RGRT being deasserted, it asserts CMDS to initiate invalidate and demap transactions.
		H = Not a command word
		L = VBus invalidate or demap command word on ADDR[35:0], \overline{DEMAP} , and \overline{WR} .
		When the STP1091 is not a bus master, this signal indicates the first cycle of a VBus transaction.
		H = Not a command word. L = VBus command word on ADDR[35:0], CCHBL, CSA, DEMAP, LDST, SIZE[1:0], SU, RD,
		and WR.
CSA [1]	ı	Control-space access. The processor asserts this pin when performing a read or write to the internal tag RAM, E-cache, or registers of the STP1091.
		H = Normal memory access.
		L = Control-space access.
DATA[63:0] [1]	1/0	Processor data bus.
DEMAP [1]	1	Asserted with CMDS to indicate demap cycle. As an input indicates an external demap cycle.
		H = Non-demap cycle.
		L = Demap cycle from system. The TLB entries matching request will be removed.

TABLE 2: Signal Descriptions - MBus Configuration (MBSEL=H) (Continued)

	•	
DPAR[7:0] ^[1]	1/0	Data bus parity. When parity is enabled, even parity is generated and checked. DPAR0 is parity for bits DATA[63:56]. When parity checking is disabled, odd parity is generated but not checked.
		DPAR0: DPAR4: DATA[63:56] DATA[31:24] DPAR1: DPAR5:
		DATA[55:48] DATA[23:16]
ERROR [1]	1	Processor error. The processor asserts this pin when it has entered an internal error state. The STP1091 initiates an internal reset when ERROR is asserted.
		H = Normal operation. L = Processor internal error.
IRL[3:0]	0	Interrupt request level. This field specifies to the processor the level of the highest priority interrupt request that is currently pending. If IRL[3:0] = 0000, no interrupts are pending. Level 15 (IRL[3:0] = 1111); Nonmaskable interrupt. Level 14: Highest maskable interrupt.
		Level 1: Lowest maskable interrupt. Level 0: No interrupts are pending.
LDST [1]	1	This pin indicates an atomic load/store (LDSTUB, LDSTUBA, SWAP, or SWAPA) operation. It is equivalent to the logical OR of RD and WR signals. H = No LDST.
MAD[63:0]	1/0	L = Atomic load/store (LDST) cycle. Multiplexed command / data bus.
MAS [2]	1/0	MBus address strobe. Asserted by current master when a valid address/command is present on
		MAD[63:0].
		H = A valid address/command is not present on MAD[63:0] L = A valid address/command is present on MAD[63:0]
MBB ^[2]	I/O	MBus busy. Asserted when there is any active transaction on MBus. H = MBus free. L = MBus busy.
MBG	ı	MBus grant. This is a dedicated (not bussed) signal from the MBus arbiter to this bus master. H = Not granted. The STP1021 may not initiate an MBus transaction. L = Granted. The STP1021 may initiate an MBus transaction as soon as MBus is free.
MBR	0	MBus request. This is a dedicated (not bussed) signal from the STP1021 to the MBus arbiter. H = No request. L = Requesting to initiate a transaction on MBus.
MBSEL [2]	ı	MBus select. This pin is used to select the system bus interface. This signal should not be changed during operation of this device. H = MBus system interface
MCLK	 	L = XBus system interface Bus clock.
WICLN	_L '	Dus clock.

TABLE 2: Signal Descriptions - MBus Configuration (MBSEL = H) (Continued)

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MERR	1/0	MBus error error respo		long with N	MRDY and MRTY to indicate acknow	ledgment type (the type of
		MERR	MRDY	MATY	Description	
		Н	н	Н	Idle cycle	
		Н	H	L	Retinquish and retry	
		H H	L	H L	Valid data transfer Reserved	
		L	H	н	Bus error (ERROR1)	
			· H	L H	Timeout error (ERROR2) Uncorrectable error (ERROR3)	
		<u> </u>	L	L	Retry	
MEXC	0		r. Encoded a or response)		RDY/WRDY and RETRY to indicate a	acknowledgment type (the
		MEXC	RADY/WADY	RETRY	Description	
		Н	Н	Н	No reply	İ
	ì	H H	H	L H	Retry Data transfer complete	
		#	L	L.	Undefined error (UD)	
		L	H	H	Bus error (BE) Timeout error (TO)	
		-	L	Н	Reserved	
			L L	L.	Reserved	
MID[3:0]		MBus module ID. The identifier of this MBus device and is usually hardwired by the system. MID3 is the most significant bit (MSB) and MID0 is the least significant bit (LSB).				
····D[0.0]	1	1				•
	1/0	MID3 is the Memory in	e most signil hibit. Assert	ficant bit (N	MSB) and MID0 is the least signification oping cache when it notices a cohe	nt bit (LSB).
MIH ^[2]		MID3 is the Memory in owns. Men	e most signil hibit. Assert nory respond	ficant bit (Ned by a snot ds to this s	MSB) and MID0 is the least significa	nt bit (LSB).
		MID3 is the Memory in owns. Men H = No L = Inhil	e most signil hibit. Assert nory respond memory inhi bit memory.	ficant bit (Ned by a snot ds to this s ibit.	MSB) and MID0 is the least signification oping cache when it notices a cohe	nt bit (LSB). erent read of cache block it
MIH ^[2]	1/0	MID3 is the Memory in owns. Men H = No L = Inhil place of	e most signil hibit. Assert nory respond memory inhi bit memory. f memory.	ficant bit (Ned by a snot ds to this s ibit. The snoop	ASB) and MID0 is the least significal coping cache when it notices a cohe ignal by ignoring the request.	nt bit (LSB). erent read of cache block it espond with the data in
MIH ^[2]		MID3 is the Memory in owns. Men H = No L = Inhit place of	e most signil hibit. Assert nory respond memory inhi bit memory. f memory. equest level.	ficant bit (Ned by a sneds to this sibit. The snoop	ASB) and MID0 is the least significal coping cache when it notices a cohe ignal by ignoring the request.	nt bit (LSB). erent read of cache block it espond with the data in
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	1/0	MID3 is the Memory in owns. Men H = No L = Inhit place of Interrupt re currently p Level 15	e most signil hibit. Assert nory respond memory inhi bit memory. f memory. equest level. ending. If M	ficant bit (Need by a snods to this sibit. The snoop This field s IRL[3:0] = 1111) N	ASB) and MIDO is the least signification oping cache when it notices a cohe ignal by ignoring the request. Sing cache which asserted MIH will respecifies the level of the highest prior the prior opinion on interrupts are pending. IMI (disable all traps).	nt bit (LSB). Prent read of cache block it espond with the data in
MIH ^[2]	1/0	MID3 is the Memory in owns. Men H = No L = Inhii place of Interrupt re currently p Level 18 Level 14	e most signification in the most significant in the most signi	ficant bit (Need by a snot distributed to this sibit. The snoop This field s IRL[3:0] = 11111 Naskable interests	ASB) and MIDO is the least signification oping cache when it notices a cohe ignal by ignoring the request. Sing cache which asserted MIH will respecifies the level of the highest prior the properties of the highest prior opinion interrupts are pending. SIMI (disable all traps).	nt bit (LSB). Prent read of cache block it espond with the data in
MIH ^[2]	1/0	MID3 is the Memory in owns. Men H = No L = Inhit place of Interrupt re currently p Level 18 Level 14 Level 15	e most signification in the most significant signification in the most significant	ficant bit (Need by a snot distributed to this sibit. The snoop This field s IRL[3:0] = 11111 Naskable inte	MSB) and MIDO is the least signification oping cache when it notices a cohe ignal by ignoring the request. Sing cache which asserted MIH will respectifies the level of the highest prior opinion on interrupts are pending. MMI (disable all traps). Iterrupt.	nt bit (LSB). Prent read of cache block it espond with the data in
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MIRL[3:0] MRDY	1/0	MID3 is the Memory in owns. Men H = No L = Inhii place of Interrupt re currently p Level 15 Level 15 Level 0: MBus reac of error res MBus retry error responses	e most signification in this interest and in	ficant bit (Need by a snot distributed by a	MSB) and MID0 is the least significated proping cache when it notices a coherignal by ignoring the request. In grache which asserted MIH will respectifies the level of the highest prior to the proping of the highest prior to the highest pr	ont bit (LSB). Perent read of cache block is espond with the data in rity interrupt request that is powledgment type (the type ovledgment type (the type ovledgment type (the type over the type over
MIH ^[2] MIRL[3:0]	1/0	MID3 is the Memory in owns. Men H = No L = Inhit place of Interrupt re currently p Level 15 Level 15 Level 0: MBus reac of error res MBus retry error responses Memory sl it is cachin H = No	e most signification in this interest and the second i	ficant bit (Need by a snot distributed by a	MSB) and MID0 is the least significated proping cache when it notices a coherignal by ignoring the request. In grache which asserted MIH will respectifies the level of the highest prior to the proping of the highest prior to the highest pr	ont bit (LSB). Perent read of cache block is espond with the data in crity interrupt request that is powledgment type (the type or ledgment type (the type or ledgment type (the type or ledgment type).
MIRL[3:0] MRDY	1/0	MID3 is the Memory in owns. Men H = No L = Inhil place of Interrupt re currently p Level 14 Level 14 Level 05 MBus read of error res Memory sl it is cachin H = No L = Sha SRAM out	e most signification in this interest and a memory inhibit. Assert memory inhibit memory. If memory	ed by a snot sibit. The snoop This field s IRL[3:0] = 1111 N askable inte ts are pend along with N tolle in MEF red by a sr nes will ma	MSB) and MIDO is the least significate proping cache when it notices a coherignal by ignoring the request. Sing cache which asserted MIH will respecifies the level of the highest priorical properties are pending. MMI (disable all traps). MERR and MRTY to indicate acknow MERR and MRDY to indicate acknow MERR acknowledge acknow MERR and MRDY to indicate acknow MERR acknowledge acknow MERR acknowledge	erent read of cache block in espond with the data in crity interrupt request that is considered by the type of the
MIRL[3:0] MRDY MRTY MSH [2] [3]	1/O	MID3 is the Memory in owns. Men H = No L = Inhit place of Interrupt re currently p Level 14 Level 14 Level 15 Level 05 MBus read of error resp Memory sl it is cachin H = No L = Sha SRAM out SRAM. It i	e most signification in this interest and a memory inhibit. Assert memory inhibit memory. If memory	ficant bit (Need by a sned sto this sibit. The snoop This field s IRL[3:0] = 1111) N askable inte ts are pend along with need show in the stable in the	MSB) and MIDO is the least signification oping cache when it notices a coherignal by ignoring the request. Sing cache which asserted MIH will respecifies the level of the highest prior 0000, no interrupts are pending. MMI (disable all traps). Sterrupt. Sterrupt. MERR and MRTY to indicate acknow MERR as a continuous metallic	erent read of cache block in espond with the data in rity interrupt request that in power type (the type of the ty

TABLE 2: Signal Descriptions - MBus Configuration (MBSEL = H) (Continued)

	Carlona est ropu tig	
PCLK	1	Processor clock. Is the same clock as to the processor.
PEND	0	Pending. A store is pending in the STP1091 or on the MBus. This pin is asserted by the STP1091 when it has a store operation pending internally or on the system bus. This signal indicates that at least one outstanding write operation has not completed. H = All write operations issued by processor are completed.
		L = One or more write operations that were issued by processor are not yet complete.
PLLBYP ^[2]	l	PLL bypass. This pin is used to bypass both of the internal phase lock loops. When PLLBYP is asserted, PCLK directly supplies timing for the circuits in the STP1091's processor clock domain, and BCLK directly supplies timing for the circuits of the STP1091's bus clock domain. The normal delay compensation performed by the PLL is defeated. H = PLLs are enabled. Normal operation.
		L = PLLs are disabled. No clock delay compensation.
PPLLRC		Capacitor for the phase filter of the processor clock PLL. This pin should be connected to an external capacitor to ground. With an internal resistor, this circuit provides the RC time constant for the phase filter of the processor clock domain PLL.
RD [1]	-	This pin is asserted when a read address is on ADDR35 - ADDR0. Also asserted with DEMAP to indicate completion of a bus demap operation by the processor. H = No read.
		L = With DEMAP: demap operation requested by the STP1091 is complete. Without DEMAP: a data read request. With LDST and WR: an atomic load/store operation.
RESET	0	Reset. STP1091 output used to reset the processor when the system asserts RSTIN. H = Normal operation. L = Reset to processor.
RETRY	0	Retry. This pin is encoded, along with RRDY or WRDY, and MEXC to indicate the type of acknowledgment. See MEXC description for table. (If this pin is asserted before RRDY or WRDY is asserted for an access, the processor should terminate the current access and restart it once it reacquires the Vbus (if a processor read is pending, a processor write will not be retried until after the read has completed).)
RGRT	0	Read grant. This pin grants the processor read access on the VBus. H = Processor not allowed read access. L = Processor may make read accesses.
RRDY	0	Read ready. This pin indicates that read data is valid. When RRDY is asserted, the processor may reliably sample the incoming data on the same clock edge as RRDY. This signal is used to qualify data specifically for a read access since a write may also be pending. This signal is encoded with MEXC and RETRY. See MEXC description for table.
RSTIN [2]	i	Reset in. Reset from the system to the cache controller. H = Normal operation. L = Hardware reset (see reset section).
SIZE1 ^[1] , SIZE0 ^[1]	0	These bits indicate the transfer size of the current transaction. 00 = Byte 01 = Half word 10 = Word 11 = Doubleword

TABLE 2: Signal Descriptions - MBus Configuration (MBSEL = H) (Configuration

SU [1]	1	Supervisor access. This signal is asserted by the processor with CMDS when the access was initiated in supervisor mode.
	1	H = User (unprivileged) transaction.
		L = Supervisor (privileged) transaction.
SYNC [2]		Synchronous clocks. When this pin is asserted, the synchronizers are bypassed, eliminating their delay but requiring that BCLK and PCLK be identical.
		H = Asynchronous. PCLK and BCLK may have different rates.
		L ≈ Synchronous. PCLK and BCLK must be identical.
TCK ^[2]	ī	JTAG test clock.
TDI ^[2]	1	JTAG test data.
TDO	0	JTAG test data output or PLL output (see TEST below).
TEST	1	Three-state all output drivers and monitor PLL on TDO.
TMS	1	JTAG test mode select.
TRST	ı	JTAG test reset.
WE[7-0] ^[1]	0	SRAM write enables. These signals directly control the write enable signals of synchronous SRAM used as external cache. These pins are driven only when asserted, otherwise they are in the high-impedance state. WEx bit ordering corresponds to the big-endian convention. That is:
		WEO: DATA[63:56] WE4: DATA[31:24]
		WE1: DATA[55:48] WE5: DATA[23:16]
		WE2; DATA[47:40] WE6: DATA[15:8]
		WE3: DATA[39:32] WE7: DATA[7:0]
		H = SRAM read
		L = SRAM write
WEE	0	E-cache write-enable enable. When asserted, the STP1021 may assert its write enables to write E-cache directly. This pin is used to control the assertion of processor's WE[7:0] signals.
		$H = The processor may not drive \overline{WE}[7:0].$
		L = The processor may drive WE[7:0].
WGRT	0	Write grant. This pin grants the processor write access on the VBus.
		H = The processor is not allowed write access.
	1	L = The processor may make write accesses.

TABLE 2: Signal Descriptions - MBus Configuration (MBSEL =H) (Continued)

670 - 670 - 670 -		
WR ^[1]	1/0	As an input, this pin is asserted with a write address on ADDR[35:0] and write data on DATA[63:0]. It is also asserted by the processor with DEMAP to send a demap request to the system bus. H = Not a write cycle. L = Write (or load/store with RD and LDST low or demap) cycle. As an output the STP1091 asserts this pin with an address on ADDR[35:0] to invalidate lines in the processor's internal cache(s) containing that address. H = Normal L = Demap
WRDY	0	Write ready. When WRDY is asserted, the STP1091 has sampled the processor's write data, and so the processor may generate the next access. In the case of burst writes, the processor switches address and data for the next write within the burst on the same clock edge as WRDY was asserted. This pin is used to qualify data specifically for a write access since a read may also be pending. This signal is encoded with MEXC and RETRY. See MEXC description for table.

^{1.} These pins have internal holding drivers.

^{2.} These pins have internal pull-up resistors.

^{3.} These pins have an open drain.

TABLE 3: Signal Descriptions - XBus Configuration (MBSEL = L)

		State of the state
ADDR[35:0] [1]	1/0	Processor physical address bus.
ADDR20	0	Inverted physical address ADDR20. Eliminates an external inverter for 2MB cache systems.
BCLK	1	Bus clock.
BPLLRC	1	Capacitor for the phase filter of the bus clock PLL. This pin should be connected to an external capacitor to ground. With an internal resistor, this circuit provides the RC time constant for the phase filter of the bus clock domain PLL.
BURST [1]	I	Indicates whether a burst access is in progress. BURST is driven at the same time as ADDR[35:0], and it is asserted during both read bursts and write bursts. BURST is deasserted on the last address of a burst to allow the STP1091 to stop returning RRDY or WRDY with the last data of the burst. H = A burst access is in progress. L = A burst access is not in progress.
CCERR	0	Indicates either an internal STP1091 error or ERROR is asserted by the processor H = No error.
		L = An internal processor or STP1091 error.
CCHBL [1]	1	This pin indicates the current processor transaction as one that may be cached in an external cache.
		H = Noncacheable access. L = Cacheable access.
CMDS [1]	1/0	Command strobe. Indicates the beginning of a bus cycle. The VBus master asserts this signal for one cycle to begin all of its accesses. When the STP1091 is a bus master, as indicated by WGRT and RGRT being deasserted, it asserts CMDS to initiate invalidate and demap transactions.
		H = Not a command word.
		L = VBus invalidate or demap command word on ADDR[35:0], \overline{DEMAP} , and \overline{WR} .
		When the STP1091 is not a bus master, this pin indicates the first cycle of a VBus transaction.
		H = Not a command word. L = VBus command word on ADDR[35:0], CCHBL, CSA, DEMAP, LDST, SIZE[1:0],SU, RD, and WR.
CSA [1]	Į.	Control-space access. The processor asserts this pin when performing a read or write to the internal tag RAM, E-cache, or registers of the STP1091.
		H = Normal memory access.
		L = Control space access.
DATA[63:0]	1/0	Processor data bus.
DEMAP [1]	1/0	Asserted with CMDS to indicate demap cycle. As an input indicates an external demap cycle.
	1	When output:
		H = Normal command word.
	1	L = demap cycle system (system should remove TLB entries matching request).
		When input:
		H = Non-demap cycle.
		L = Demap cycle from system. The TLB entries matching request will be removed.

TABLE 3: Signal Descriptions - XBus Configuration (MBSEL = L) (Continued)

DPAR[7:0] ^[1]	1/0					parity is generated and chec g is disabled, odd parity is g	
		DPAR0:		DPAR	**		
		DATA[63 DPAR1:	3:56]	DATA[: DPAR:	•		
		DATA[55	5:48]	DATA[
ERROR [1]	ı	ł				n when it has entered an int	ternal error state. The
			mal operati				
GTLREF	ı	of V _{ref} for G operation o care should	L = Processor internal error. XBus level reference for GTL and GTL/TTL selection. Should be connected to a voltage source of V _{ref} for GTL operation of the XBus interface signals. Should be connected to V _{CC} for TTL operation of the XBus interface signals. Since this pin (and GTLREF1) sets threshold levels, care should be taken to insure that V _{ref} is free of noise. GTLREF and GTLREF1 are connected together internally.				
GTLREF1	ı	XBus level together int		or GTL and	d GTL/TTL se	lection. GTLREF and GTLP	REF1 are connected
IRL[3:0]	0	Interrupt request Level. This field specifies, to the processor, the level of the highest priority interrupt request that is currently pending. If IRL[3:0] = 0000, no interrupts are pending. Level 15: (IRL[3:0] = 1111): Nonmaskable interrupt. Level 14: Highest maskable interrupt. Level 1: Lowest maskable interrupt. Level 0: No interrupts are pending.					
LCMD[2:0]	0	Boot-bus co external Bo			nds are issue	d by the STP1091 and interp	preted by one or more
		LCMD2	LCMD1	LCMD0	Name	Description	7
			************	H L H L H L	ADR-HIGH Interrupt ADR-MED ADR-LOW IDLE-WR READ-VALID WRITE-VALID IDLE	Address bits 23-16 on LDATA Interrupt Status on LDATA Address bits 15-8 on LDATA Address bits 7-0 on LDATA ldle for write Device data on LDATA STP1091 data on LDATA Idle	
LCMDS	0	Boot-bus command strobe. When asserted, this pin indicates that command information on LCMD (and write data on LDATA for WRITE-VALID commands) is valid. Input data is latched on the rising edge.					
	1	1	41				
		H = Inac L = Bus	command	valid.			

TABLE 3: Signal Descriptions - XBus Configuration (MBSEL = L) (Continued)

LDST [1]	1	This pin indicates an atomic load/store (LDSTUB, LDSTUBA, SWAP, or SWAPA) operation. It is equivalent to the logical OR of RD and WR signals. No other transactions may occur while LDST is asserted. H = No LDST. L = Atomic load/store (LDST) cycle.				
MBSEL [2]	1	MBus select. This signal is used to select the system bus interface. This signal should not be changed during operation of this device. H = MBus system interface. L = XBus system interface.				
MEXC	0	VBus error. Encoded along with RDY/WRDY and RETRY to indicate acknowledgment type (the type of error response).				
		MEXC ARDY/WRDY RETRY Description				
		H				
ŌE ^[1]	I/O	SRAM output enable. As an output, this pin controls the pipelined output enable of external cache SRAM. It is used as an input to prevent bus collisions. H = SRAM outputs disabled. L = SRAM outputs enabled.				
PEND	0	Pending. A store is pending in the STP1091 or in the system beyond the STP1091. This signal is asserted by the STP1091 when it has a store operation pending internally or on the system bus. This pin indicates that at least one outstanding write operation has not completed. H = No incomplete write operations outstanding from this processor. L = One or more write operations issued by this processor are not yet complete.				
PCLK	ı	Processor clock. Should be the same as clock to the processor.				
PLLBYP ^[2]	I	PLL bypass. This pin is used to bypass both of the internal phase lock loop. When PLLBYP is asserted PCLK directly supplies timing for the circuits in the STP1091's processor clock domain, and BCLK directly supplies timing for the circuits of the STP1091's bus clock domain. The normal delay compensation performed by the PLL is defeated. H = PLLs are enabled. Normal operation. L = PLLs are disabled. No clock delay compensation.				
PPLLRC		Capacitor for the phase filter of the processor clock PLL. This pin should be connected to an external capacitor to ground. With an internal resistor, this circuit provides the RC time constant for the phase filter of the processor clock domain PLL.				
RD ⁽¹⁾	1	This pin is asserted when a read address is on ADDR[35:0]. Also asserted with DEMAP to indicate completion of a bus demap operation by the processor. H = No read. L = With DEMAP: demap operation requested by the STP1091 is complete. Without DEMA a data read request. With LDST and WR: an atomic load/store operation.				

TABLE 3: Signal Descriptions - XBus Configuration (MBSEL = L) (Continued)

RESET	0	Reset. This STP1091 output is used to reset the processor when the system asserts RSTIN.
		H = Normal operation.
		L = Reset to processor.
RETRY	0	Retry. This pin is encoded, along with RRDY or WRDY, and MEXC to indicate the type of acknowledgment. See MEXC description for table. If this signal is asserted before RRDY or WRDY is asserted for an access, the processor should terminate the current access and restart it once it reacquires the Vbus (if a processor read is pending, a processor write will not be retried until after the read has completed).
RGRT	0	Read grant. This pin grants the processor read access on the VBus.
		H = Processor not allowed read access. L = Processor may make read accesses.
RRDY	0	Read ready. This pin indicates that read data is valid. When RRDY is asserted, the processor may reliably sample the incoming data on the same clock edge as RRDY. This signal is used to qualify data specifically for a read access since a write may also be pending. This signal is encoded with MEXC and RETRY. See MEXC description for table.
RSTIN [2]	1	Reset in. Reset from the system to the cache controller.
		H = Normal operation.
		L = Hardware reset (see reset section).
SIZE1 ^[1] , SIZE0 ^[1]	1	These bits indicate the transfer size of the current transaction. 00 = Byte 01 = Half word 10 = Word 11 = Doubleword
SU [1]	i i	Supervisor access. This pin is asserted by the processor with CMDS when the access was initiated in supervisor mode. H = User (unprivileged) transaction. L = Supervisor (privileged) transaction.
SYNC [2]	 	Synchronous clocks. When this pin is asserted, the synchronizers are bypassed, eliminating their delay, but requiring that BCLK and PCLK be identical. H = Asynchronous. PCLK and BCLK may have different rates. L = Synchronous. PCLK and BCLK must be identical.
TCK [2]	1	JTAG test clock.
TDI [2]	ı	JTAG test data.
TDO	0	JTAG test data output or PLL output (see TEST below).
TEST [2]	1	3-state all output drivers and monitor PLL on TDO.
TMS [2]	1	JTAG test mode select.
TRST [2]	1	JTAG test reset.

TABLE 3: Signal Descriptions - XBus Configuration (MBSEL = L) (Continued)

ARMA		The second secon
WE[7:0] [1]	0	SRAM write enables. These pins directly control the write enable signals of synchronous SRAM used as external cache. These pin are driven only when asserted, otherwise they are in the high-impedance state. WEx bit ordering corresponds to the big-endian convention. That is:
		WE0: DATA[63:56] WE4: DATA[31:24]
		WE1: DATA[55:48] WE5: DATA[23:16]
		WE2: DATA[47:40] WE6: DATA[15:8]
		WE3: DATA[39:32] WE7: DATA[7:0]
		H = SRAM read
	_	L = SRAM write
WGRT	0	Write grant. This pin grants the processor write access on the VBus.
	1	H = The processor not allowed write access.
		L = The processor may make write accesses.
WR [1]	1/0	As an input, this pin is asserted with a write address on ADDR[35:0]and write data on DATA[63:0]. It is also asserted by the processor with DEMAP to send a demap request to the system bus.
		H = Not a write cycle.
		t. = Write (or load/store with RD and LDST low or demap) cycle.
		As an output, the STP1091 asserts this pin with an address on ADDR[35:0] to invalidate lines in the processors's internal cache(s) containing that address.
		H ≈ Normal.
		L = Demap.
WRDY	0	Write ready. When WRDY is asserted, the STP1091 has sampled the processor's write data, and so the processor may generate the next access. In the case of burst writes, the processor switches address and data for the next write within the burst on the same clock edge as WRDY was asserted. This pin is used to qualify data specifically for a write access since a read may also be pending. This pin is encoded with MEXC and RETRY. See MEXC description for table.
XDATA[63:0] [3]	1/0	XBus multiplexed command / data bus.
XREQ0[1] [2] XREQ0[0] [2]	ı	Request field from Bus Watcher 0 (BW0).
XREQ1[1] ^[2] XREQ1[0] ^[2]		Request field from Bus Watcher 1 (BW1).
XREQ2[1] [2] XREQ2[0] [2]	1	Request field from Bus Watcher 2 (BW2).
XREQ3[1] ^[2] XREQ3[0] ^[2]	1	Request field from Bus Watcher 3 (BW3).
XPAR[3:0] [3]	1/0	Parity bits.
		XPAR3 = Parity over XDATA[63:48]
		XPAR2 = Parity over XDATA[47:32]
		XPAR1 = Parity over XDATA[31:16]
		XPAR0 = Parity over XDATA[15:0]
XGNTO [3]	0	XBus Grant to Bus Watcher 0 (BW0).

TABLE 3: Signal Descriptions - XBus Configuration (MBSEL = L) (Continued)

			100 / 100 /
XGNT1 [3]	0	XBus Grant to Bus Watcher 1 (BW1).	
XGNT2 [3]	0	XBus Grant to Bus Watcher 2 (BW2).	
XGNT3 [3]	0	XBus Grant to Bus Watcher 3 (BW3).	

- 1. These pins have internal holding drivers.
- 2. These pins have internal pull-up resistors.
- 3. In GTL operation, the I/O buffer is open drain, while in TTL operation the I/O buffer is 3-state.

TABLE 4: Signal Descriptions - Power Connections

V _{CCC}		Supply voltage (V _{CC}) for internal (core) logic.	
V _{CCСКВ}	1	Supply voltage (V _{CC}) for bus clock and PLL.	
V _{CCCKP}	ı	Supply voltage (V _{CC}) for processor clock and PLL.	
V _{CCPX}	1	Supply voltage (V _{CC}) for bus outputs.	
V _{CCI}	ı	Supply voltage (V _{CC}) for inputs.	
V _{CCP}	1	Supply voltage (V _{CC}) for processor outputs.	
V _{SSC}	1	Ground for internal (core) logic.	
V _{SSCKB}	j	Ground for bus clock and PLL.	
V _{SSCKP}	1	Ground for processor clock and PLL.	
V _{SSI}	1	Ground for inputs.	
V _{SSP}		Ground for processor outputs.	
V _{SSPX}		Ground for bus outputs.	

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings [1]

			And the state of t			
Vcc	Supply voltage range	0 to 6.0	V			
Vı	Input voltage range [2]	-0.5 to V _{CC} + 0.5	V			
Vo	Output voltage range	-0.5 to V _{CC} + 0.5	V			
lik	Input clamp current (V _I < 0 or V _I > V _{CC})	20	mA			
lok	Output clamp current (V _O < 0 or V _O > V _{CC})	50	mA			
	Current into any output in the low state	96	mA			
T _{STG}	Storage temperature	-65 to 150	С			

Operation of the device at values in excess of those listed above will result in degradation or destruction of the device. All voltages are defined
with respect to ground. Functional operation of the device at these or any other conditions beyond those indicated under "recommended
operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Alle um de serveço Cambrilla			T. 1. 1752	100 mm - 100	X-10	
Vcc	Supply Voltage	For SuperSPARC-II Systems	4.95	•	5.05	V
V _{SS}	Ground	<u> </u>	-	0	_	V
V _{IH}	TTL high-level	All except PCLK, BCLK/MCLK	2.0	~	V _{CC} + 0.3	V
	input voltage	PCLK, BCLK/MCLK	2.2	~	V _{CC} + 0.3	٧
V _{IL}	TTL low-level input	ow-level input voltage			0.8	٧
Гон	TTL high-level outp	L high-level output current, all outputs			-370	Α
loL	TTL low-level output current	All outputs except MSH		~	2.0	mA
		MSH	-		8.0	mA
V _{tHG}	GTL high-level inpu	ut voltage	V _{REF} + 0.15	-	_	٧
V _{ILG}	GTL low-level inpu	t voltage			V _{REF} - 0.15	٧
loнg	GTL high-level out	put current		-	10	Α
lolg	GTL low-level outp	ut current	-		36	mA
V _{REF}	GTL reference volt	age	0.7	0.8	0.9	٧
T _A	Operating ambient	temperature	0		[1]	С

^{1.} Maximum ambient temperature is limited by air flow such that the maximum junction temperature does not exceed 80 C

^{2.} Unless otherwise noted, all voltages are with respect at VSS.

DC Characteristics

						er vironas e
Vон	TTL high-level output voltage	V _{CC} = Min, I _{OH} = Max	2.4	_		V
VOL	TTL low-level output voltage	V _{CC} = Max, I _{OL} = Max	_	_	0.4	V
VolG	GTL low-level output voltage	V _{CC} = Max, I _{OLG} = Max		_	0.4	V
VohG	GTL high-level output voltage	V _{CC} = Min, I _{OHG} = Max	1.2	-	_	٧
lcc	Supply current	V _{CC} = Max	T - T	-	1.2	A
Icco	Quiescent supply current	V _{CC} = Max, V _I = V _{SS} or V _{CC}		-	640	mA
loz	High-impedance output current [1]	V _{CC} = Max, V _O = 2.4V		-	20	Α
		V _{CC} = Max, V _O = 0.4V	-	_	-20	Α
lін	Input high current	Inputs with pullups	-	-	-300	Α
		V _{CC} = Max, V _i = Vss to Vcc				
		Inputs with holding drivers [2]		_	-250	Α
		V _{CC} = Max, V _i = V _{CC}	ļ	l		
IIL	Input low current	Inputs with holding drivers [2]	-	-	500	Α
		V _{CC} = Max, V _I = Vss				1
l ₁	Input current	All other inputs	-		50	A
		$V_{CC} = Max$, $V_I = V_{SS}$ to V_{CC}	ľ			
Cı	Input capacitance [2]			5		pF
Co	Output capacitance [2]		-	10		pF

^{1.} Outputs without holding drivers.

^{2.} This specification is provided as an aid to board design. This specification is not assured during manufacturing testing.

VBus Timing - Setup and Hold $^{[1]}$

VBus setup to PCLK	ADDR[35:20], ADDR[2:0]	4.5	-	3.5	_	ns
VBus setup to PCLK	ADDR[19:3]	4.5		3.5	-	ns
VBus setup to PCLK	DATA[63:0], DPAR[7:0]	4.5	_	3.5		ns
VBus setup to PCLK	ERROR, LDST, RD, SIZE1-SIZE0, SU	7.5	-	3.5	-	ns
VBus setup to PCLK	WR, DEMAP	7.5	-	3.5	-	ns
VBus setup to PCLK	BURST, CCHBL, CSA	7.5	-	3.5		ns
VBus setup to PCLK	CMDS	7.5	-	3.5	-	ns
VBus setup to PCLK	ŌĒ	4.5	-	3.5		ns
VBus hold to PCLK	ADDR[35:20], ADDR[2:0]	0.5		0.5	_	ns
VBus hold to PCLK	ADDR[19:3]	0.5		0.5	-	ns
VBus hold to PCLK	DATA[63:0], DPAR[7:0]	0.5	-	0.5	-	ns
VBus hold to PCLK	ERROR, LDST, RD, SIZE1-SIZE0, SU	0.5	_	0.5	_	ns
VBus hold to PCLK	WR, DEMAP	0.5	_	0.5	_	ns
VBus hold to PCLK	BURST, CCHBL, CSA	0.5		0.5		ns
VBus hold to PCLK	CMDS	0.5		0.5		ns
VBus hold to PCLK	ŌĒ	0.5	_	0.5		ns
	VBus setup to PCLK VBus hold to PCLK	VBus setup to PCLK VBus hold to PCLK	VBus setup to PCLK ADDR[19:3] 4.5 VBus setup to PCLK DATA[63:0], DPAR[7:0] 4.5 VBus setup to PCLK ERROR, LDST, RD, SIZE1-SIZE0, SU 7.5 VBus setup to PCLK WR, DEMAP 7.5 VBus setup to PCLK BURST, CCHBL, CSA 7.5 VBus setup to PCLK CMDS 7.5 VBus setup to PCLK OE 4.5 VBus hold to PCLK ADDR[35:20], ADDR[2:0] 0.5 VBus hold to PCLK DATA[63:0], DPAR[7:0] 0.5 VBus hold to PCLK ERROR, LDST, RD, SIZE1-SIZE0, SU 0.5 VBus hold to PCLK WR, DEMAP 0.5 VBus hold to PCLK WR, DEMAP 0.5 VBus hold to PCLK BURST, CCHBL, CSA 0.5 VBus hold to PCLK CMDS 0.5	VBus setup to PCLK ADDR[19:3] 4.5 - VBus setup to PCLK DATA[63:0], DPAR[7:0] 4.5 - VBus setup to PCLK ERROR, LDST, RD, SIZE1-SIZE0, SU 7.5 - VBus setup to PCLK WR, DEMAP 7.5 - VBus setup to PCLK BURST, CCHBL, CSA 7.5 - VBus setup to PCLK CMDS 7.5 - VBus setup to PCLK OE 4.5 - VBus hold to PCLK ADDR[35:20], ADDR[2:0] 0.5 - VBus hold to PCLK DATA[63:0], DPAR[7:0] 0.5 - VBus hold to PCLK ERROR, LDST, RD, SIZE1-SIZE0, SU 0.5 - VBus hold to PCLK WR, DEMAP 0.5 - VBus hold to PCLK WR, DEMAP 0.5 - VBus hold to PCLK BURST, CCHBL, CSA 0.5 - VBus hold to PCLK CMDS 0.5 -	VBus setup to PCLK ADDR[19:3] 4.5 - 3.5 VBus setup to PCLK DATA[63:0], DPAR[7:0] 4.5 - 3.5 VBus setup to PCLK ERROR, LDST, RD, SIZE1-SIZE0, SU 7.5 - 3.5 VBus setup to PCLK WR, DEMAP 7.5 - 3.5 VBus setup to PCLK BURST, CCHBL, CSA 7.5 - 3.5 VBus setup to PCLK CMDS 7.5 - 3.5 VBus setup to PCLK OE 4.5 - 3.5 VBus hold to PCLK ADDR[35:20], ADDR[2:0] 0.5 - 0.5 VBus hold to PCLK DATA[63:0], DPAR[7:0] 0.5 - 0.5 VBus hold to PCLK ERROR, LDST, RD, SIZE1-SIZE0, SU 0.5 - 0.5 VBus hold to PCLK WR, DEMAP 0.5 - 0.5 VBus hold to PCLK WR, DEMAP 0.5 - 0.5 VBus hold to PCLK CMDS 0.5 - 0.5 VBus hold to PCLK CMDS 0.5 - <t< td=""><td>VBus setup to PCLK ADDR[19:3] 4.5 - 3.5 - VBus setup to PCLK DATA[63:0], DPAR[7:0] 4.5 - 3.5 - VBus setup to PCLK ERROR, LDST, RD, SIZE1-SIZE0, SU 7.5 - 3.5 - VBus setup to PCLK WR, DEMAP 7.5 - 3.5 - VBus setup to PCLK BURST, CCHBL, CSA 7.5 - 3.5 - VBus setup to PCLK CMDS 7.5 - 3.5 - VBus setup to PCLK OE 4.5 - 3.5 - VBus hold to PCLK ADDR[35:20], ADDR[2:0] 0.5 - 0.5 - VBus hold to PCLK ADDR[19:3] 0.5 - 0.5 - VBus hold to PCLK DATA[63:0], DPAR[7:0] 0.5 - 0.5 - VBus hold to PCLK ERROR, LDST, RD, SIZE1-SIZE0, SU 0.5 - 0.5 - VBus hold to PCLK WR, DEMAP 0.5 - 0.5 - 0.5 -</td></t<>	VBus setup to PCLK ADDR[19:3] 4.5 - 3.5 - VBus setup to PCLK DATA[63:0], DPAR[7:0] 4.5 - 3.5 - VBus setup to PCLK ERROR, LDST, RD, SIZE1-SIZE0, SU 7.5 - 3.5 - VBus setup to PCLK WR, DEMAP 7.5 - 3.5 - VBus setup to PCLK BURST, CCHBL, CSA 7.5 - 3.5 - VBus setup to PCLK CMDS 7.5 - 3.5 - VBus setup to PCLK OE 4.5 - 3.5 - VBus hold to PCLK ADDR[35:20], ADDR[2:0] 0.5 - 0.5 - VBus hold to PCLK ADDR[19:3] 0.5 - 0.5 - VBus hold to PCLK DATA[63:0], DPAR[7:0] 0.5 - 0.5 - VBus hold to PCLK ERROR, LDST, RD, SIZE1-SIZE0, SU 0.5 - 0.5 - VBus hold to PCLK WR, DEMAP 0.5 - 0.5 - 0.5 -

^{1.} VBus timings are preliminary based on initial specifications and are subject to change.

VBus Timing - Switching Characteristics [1] [2]

t _p (VAO1)	Propagation delay, PCLK to ADDR[35:20], ADDR[2:0]		_	14.0	-	6.0	ns
t _p (VAO2)	Propagation delay, PCLK to ADDR[19:3]		-	14.0		6.0	ns
t _p (VDO)	Propagation delay, PCLK to DATA[63:0], DPAR[7:0]			14.0	_	5.5	ns
t _p (VCO1)	Propagation delay, PCLK to VBus (RGRT, WRGT, RRDY, WRDY, MEXC, WEE, RETRY, PEND)		-	11.5	-	6.0	ns
tp(VCO2)	Propagation delay, PCLK to DEMAP, WR		-	11.5	-	6.0	ns
t _p (CMDS)	Propagation delay, PCLK to CMDS			11.5	-	6.0	ns
t _p (OE)	Propagation delay, PCLK to OE		-	11.5	-	6.0	ns
t _p (WE)	Propagation delay, PCLK to WE[7:0]		-	14.0	-	6.0	ns
tp(RESET)	Propagation delay, PCLK to RESET		_	11.5	-	6.0	ns
t _p (IRL)	Propagation delay (MBus mode), MIRL to IRL	I _{OH} = Max		20.0	-	11.0	ns
	Propagation delay (XBus mode), PCLK to IRL	$I_{OL} = Max$ $V_{load} = 2.25V$	_	15.0	-	11.0	ns
t _{oh} (VAO1)	Output hold, PCLK to ADDR[35:20], ADDR[2:0]	Vload = 2.25V (see Figure 29)	1.0	-	0.5	-	ns
toh(VAO2)	Output hold, PCLK to ADDR[19:3]		1.0	_	0.5		ns
t _{oh} (VDO)	Output hold, PCLK to DATA[63:0], DPAR[7:0]		1.0	-	0.5	-	ns
toh(VCO1)	Output hold, PCLK to VBus (RGRT, WRGT, RRDY, WRDY, MEXC, WEE, RETRY, PEND)		1.0		0.25	-	ns
t _{oh} (VCO2)	Output hold, PCLK to DEMAP, WR		1.0	-	0.25	_	ns
toh(CMDS)	Output hold, PCLK to CMDS		1.0		0.25	-	ns
toh(OE)	Output hold, PCLK to OE		1.0		0.25	-	ns
t _{oh} (WE)	Output hold, PCLK to WE[7:0]		1.0	_	0.25		ns
toh(RESET)	Output hold, PCLK to RESET		1.0		0.25	-	ns
toh(IRL)	Output hold (XBus mode), PCLK to IRL		1.0		0.25	-	ns

^{1.} VBus timings are preliminary based on initial characterization and are subject to change.

^{2.} Switching characteristics are given with maximum number of outputs simultaneously switching.

MBus Timing - Setup and Hold [1]

t _{su} (MAD)	MADnn setup to CLK	MAD[63:0]	5.0		5.0	_	ns
t _{su} (MB)	Bused setup to CLK	MAS, MERR, MRDY, MRTY, MIH, MBB	6.0	_	5.0	-	ns
t _{su} (MPP)	Point-to-point setup to CLK	MBG	8.0	_	6.0	-	ns
t _{su} (MSH)	MSH setup to CLK	MSH	6.0	-	5.0	_	ns
t _h (MAD)	MAD hold time from CLK	MAD[63:0]	1.0		1.0	-	ns
t _h (MB)	Bused hold time from CLK	MAS, MERR, MRDY, MRTY, MIH, MBB	1.0	-	1.0	_	ns
t _h (MPP)	Point-to-point hold time from CLK	MBG	1.0	_	1.0	_	ns
t _h (MSH)	MSH hold time from CLK	MSH	1.0	_	1.0	_	ns

^{1.} The STP1091-50 works with 40 MHz MBUS clock. The STP1091-60 and STP1091-75 work with either 40 or 50 MHz MBUS clock.

MBus Timing - Switching Characteristics [1]

	(1) (1) (1) (1) (1) (1) (1) (1) (1) (1)							
t _p (MAD)	Propagation delay, BCLK to MBus MAD[63:0]			13.5		11.5	ns	
t _p (MC1)	Propagation delay, BCLK to MBus control (MAS, MRDY, MERR, MIH, MBB)	I _{OL} = Max	_	13.5		10.0	ns	
t _p (MRR)	Propagation delay, BCLK to MBus point-to-point MBR			-	12.5	-	12.0	ns
t _p (MSHHL)	Propagation delay, BCLK to MSH (high to low)		-	13.5	_	10.0	ns	
t _p (MSHLH)	Propagation delay, BCLK to MSH (low to high) [2]		_	[2]		[2]	ns	
tp(AERRHL)	Propagation delay, BCLK to AERR (high to low)	I _{OH} = Max	_	13.5		10.0	ns	
tp(AERRLH)	Propagation delay, BCLK to AERR (low to high) [2]	VLOAD =	-	[2]	_	[2]	ns	
t _{oh} (MAD)	Output hold, BCLK to MBus MAD[63:0]	2.25V (See Figure 29)	1.5	_	1.5	_	ns	
t _{oh} (MC1)	Output hold, BCLK to MBus control (MAS, MRDY, MERR, MIH, MBB)	(2.5	-	1.5	-	ns	
t _{oh} (MBR)	Output hold, BCLK to MBus point-to-point MBR		2.5	-	1.5	_	ns	
toh(MSHHL)	Output hold, BCLK to MSH (high to low)		2.5	17.5	1.5	17.5	ns	
toh(MSHLH)	Output hold, BCLK to MSH (low to high)]						
toh(AERR)	Output hold, BCLK to AERR		2.5	-	1.5	-	ns	

^{1.} The STP1091-50 works with 40 MHz MBUS clock. The STP1091-60 and STP1091-75 work with either 40 or 50 MHz MBUS clock.

^{2.} Pins have open-drain implementation. Timing is dependent on external circuits.

XBus Timing - Setup and Hold [1]

t _{su} (XC)	XBus control (GTL) setup to BCLK	XREQn[1], XREQn[0], XGNT3-XGNT0	6.9	-	6.4	-	ns
t _{su} (XD)	XBus XDATA (GTL) setup to BCLK	XD[63:0], XPAR[3:0]	6.9	-	6.4	_	ns
t _h (XC)	XBus control (GTL)	XREQn[1], XREQn[0], XGNT3-XGNT0	0	-	0		ns
t _h (XD)	XBus XDATA (GTL)	XD[63:0], XPAR[3:0]	0	-	0	-	ns

^{1.} The STP1091-50 works with 40 MHz MBUS clock. The STP1091-60 and STP1091-75 work with either 40 or 50 MHz MBUS clock.

XBus Timing (GTL Mode) - Switching Characteristics [1]

t _p (XC)	BCLK to XBus control (XREQn[1]-XREQn[0], XGNT3-XGNT0)			8.9	_	6.4	ns
t _p (XD)	BCLK to XBus XDATA, XPARn		-	8.9	_	6.4	ns
t _p (CCERR)	BCLK to CCERR (high to low)	I _{OL} = Max	~	8.9	-	6.4	ns
t _{oh} (XC)	BCLK to XBus control (XREQn[1]-XREQn[0], XGNT3-XGNT0)	I _{OH} = Max V _{LOAD} = 1.2V	0.6	-	0.6	-	ns
t _{oh} (XD)	BCLK to XBus XDATA, XPARn		0.6	_	0.6	-	ns
toh(CCERR)	CCERR hold time from BCLK (high to low)		0.6	_	0.6	-	ns

^{1.} The STP1091-50 works with 40 MHz MBUS clock. The STP1091-60 and STP1091-75 work with either 40 or 50 MHz MBUS clock.

Clock Timing

									1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
tw(PCLK)	VBus clock cycle pulse duration	PCLK ^[1]	25	-	_	11.1	-	-	ns
	PCLK duty cycle		25	50	75	25	50	75	%
t _w (BCLK)	XBus clock cycle pulse duration	BCLK	25	-		20	-	-	ns
	BCLK duty cycle		25	50	75	25	50	75	%
t _w (MCLK)	MBus clock cycle pulse duration	MCLK	25	-		20	-	-	ns
	MCLK duty cycle		25	50	75	25	50	75	%
t _w (TCK)	JTAG clock cycle pulse duration	TCK	100		-	100	-		ns
	TCK duty cycle		25	50	75	25	50	75	%
t _w (RSTIN)	RSTIN pulse duration [2] [3]	RSTIN	8		_	8		-	PCLK
t _w (TRST)	JTAG RST pulse duration [4]	TRST	50	-	-	50	_	-	ns

- 1. For asynchronous operation, PCLK must be at least 10% faster than BCLK, but must not exceed a ratio of 3: 1.
- 2. RSTIN must be held asserted for 100 ms on power-up.
- 3. Functional minimum parameter; not checked by manufacturing test.
- 4. TRST must be asserted for 50 ns after power is applied.

JTAG and Miscellaneous Timing - Setup and Hold

		Batalanea (p. 2012) Tallian (A. 1.) Recount (B. 2013) Tallian (A. 1.)		
t _{su} (RSTIN)	RSTIN setup to PCLK (synchronous) [1]	15	-	ns
t _{su} (TDI)	TDI to TCK rising edge	10	-	ns
t _{su} (TMS)	TMS to TCK rising edge	10	-	ns
th(RSTIN)	RSTIN hold time from PCLK (synchronous) [1]	15	-	ns
t _h (TDI)	TDI hold time from rising edge	20		ns
t _h (TMS)	TMS hold time from rising edge	20		ns

^{1.} RSTIN can occur anytime during a clock cycle. Time given is minimum to ensure synchronous operation.

JTAG Timing - Switching Characteristics

t _p (TDO)	TCK (falling edge) to TDO	I _{OL} = Max, I _{OH} = Max	-	25	ns	
t _{oh} (TDO)	TCK (falling edge) to TDO	V _{LOAD} = 2.25V	5		ns	
		(See Figure 29)				

Boot Bus Timing - Setup and Hold

t _{su} (B)	LDATA setup to CLK	2	-	ns
t _h (B)	LDATA hold from CLK [1]	2	-	ns

^{1.} This value is characterized but not tested. This value is the earliest that the STP1091 will drive data following a read cycle.

Boot Bus Timing - Switching Characteristics

		m - ++		.7	
t _p (LDATA)	BCLK to LDATA		-	15	ns
t _p (LCMD)	BCLK to LCMD]		15	ns
t _p (LCMDS)	BCLK to LCMDS		_	15	ns
tp(LCMDLCMOS)	LCMD valid to LCMDS [1]	1	1 BCLK	-	
t _p (LDCML)	LDATA valid to LCMDS [1]	I _{OL} = Max I _{OH} = Max V _{LOAD} = 2.25V	1 BCLK	-	
t _{oh} (LDATA)	LDATA hold from BCLK		0	_	ns
t _{oh} (LCMD)	LCMD hold from BCLK		0	_	ns
toh(LCMDS)	LCMDS hold from BCLK		0	_	ns
toh(LCMDLCMH)	LCMD hold from LCMDS high [1]		1 BCLK	_	
toh(LDLCMH)	LCMD hold from LCMDS high [1]		1 BCLK	-	
t _w (LCMDS)	LCMDS pulse width [1]		3 BCLK		ns

^{1.} Functional minimum parameter; not checked by manufacturing test.

Holding Drivers and Pull-Ups

Some pins on the STP1091 have holding drivers. Holding drivers are high-impedance buffers that keep the bus at its previous level until a strong driver changes the level. Holding drivers prevent bus signals from drifting near the threshold at low transition rates as can happen on 3-state buses. Holding drivers will source up to 250 A (pull-up) or sink up to 500 A (pull-down).

TABLE 5: Pins with Holding Drivers

			e figure	
4.				
ADDR[35:0]	WR	ŌĒ	CSA	
DATA[63:0]	RD	WE(7-0)	LDST	
DPAR[7:0]	CMDS	SIZE1, SIZE0	CCHBL	
BURST	DEMAP	ERROR	รับ	

Pins listed in *Table 6* have internal pull-up resistors. These pull-up resistors result in loads that need to be comprehended in system design. The worst-case loading for these inputs is 300 A at V_L of 0.40 volts.

TABLE 6: Pins with Internal Pull-up Resistors

	Aurilla Aurille (1995), Aufle Sa La 1811 (1994)			yeartal an operation was properties.
PLLBYP SYNC	TCK TMS	XREQ3 - XREQ1	XREQ3 - XREQ0	MSH MAS
RSTIN	TDI	XREQ2 - XREQ1	XREQ2 - XREQ0	MIH
LDATA[3:0] MBSEL	TEST	XREQ1 -	XREQ1 -	MBB
		XREQ1 XREQ0 -	XREQ0 XREQ0 -	
		XREQ1	XREQ0	

External Passive Components

There are power-supply decoupling capacitors mounted directly on the PGA package of the STP1091. These are eight $0.1\,$ F capacitors, two each between V_{CCI} and V_{SSI} , V_{CCP} and V_{SSP} , V_{CCC} and V_{SSP} , and between V_{CCPX} and V_{SSPX} .

The PLLRC and BPLLRC pins require and external capacitor. This capacitor forms part of the RC filter for the phase-lock loop control signal. Each of these pins should have a 0.1 F capacitor to ground for proper operation.

Unused inputs should be pulled high or low. Configuration pins (such as MBSEL) also need to be pulled high or low. A 1 k to 5 k esistor to +5V is recommended for pulling signals high.

TIMING CONSIDERATIONS

VBus Timing

The VBus read, write and invalidate operations are explained in the following section.

Cache Disabled/Non-Cacheable Single Read

Figure 4 shows a single read with the cache disabled. The external cache controller (STP1091) goes to the system bus to accomplish this operation. It deasserts \overline{RGRT} to allow the STP1021 to complete pending write operations. When the data is available, the STP1090 negates grant, drives the data, and asserts \overline{RRDY} .

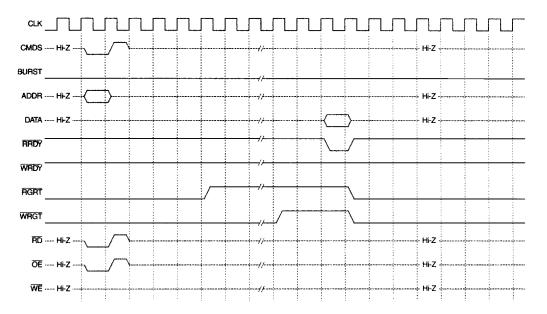


Figure 4. VBus Cache Disabled/Non-Cacheable Single Read

Cache Disabled Write (or Non-Cacheable) Write

Figure 5 shows a cache disabled write. The external cache controller (STP1091) terminates the VBus cycle by issuing a WRDY without asserting WEE. A non-cacheable write would be identical.

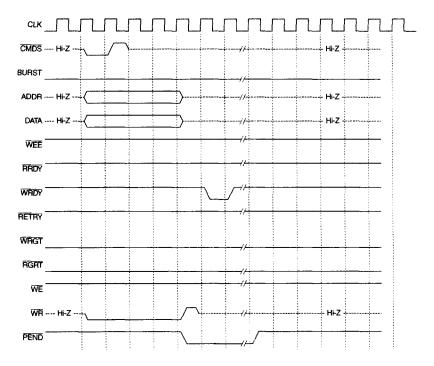


Figure 5. VBus Cache Disabled/Non-Cacheable Single Write

Cacheable Single Read Hit

Figure 6 shows a read by the STP1021 of a single cacheable word with an external cache hit. STP1021 asserts the address, cycle qualifiers, and the \overline{OE} to SRAM. The STP1091 detects a tag match and issues a \overline{RRDY} at the same time that the SRAMs drive data to STP1021. The \overline{OE} from STP1021 is delayed in the registers internal to the synchronous SRAMs, and the data is enabled two cycles after the \overline{OE} is issued to the chip. Note that the partially bussed (not driven by the STP1021 for the entire cycle) VBus control signals are actively deasserted for 1/2 cycle before being released to the bus keepers.

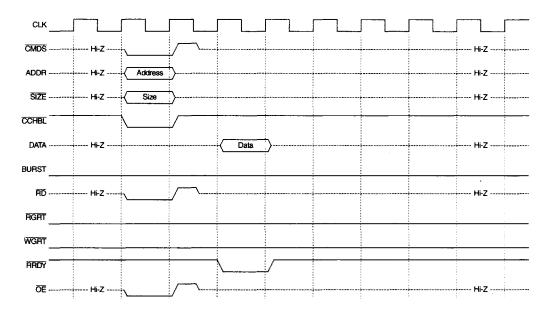


Figure 6. VBus Cacheable Single Read Hit

Cacheable Single Read Miss

Figure 7 shows a cacheable single-read miss. The STP1091 detects that a tag mismatch occurs and issues a cycle to the system bus to obtain data to fill the external cache. It removes \overline{RGRT} to allow STP1021 to proceed with any write operation it may have had pending. When the system bus returns the requested data block, the STP1091 removes the bus grant to STP1021 (negates \overline{WGRT}) to obtain access to the SRAMs. The STP1091 writes the data into the SRAMs. The STP1091 issues a \overline{RRDY} to STP1021, as the data word requested (by STP1021 read) is driven on the DATA lines (while the data is being written into SRAMs).

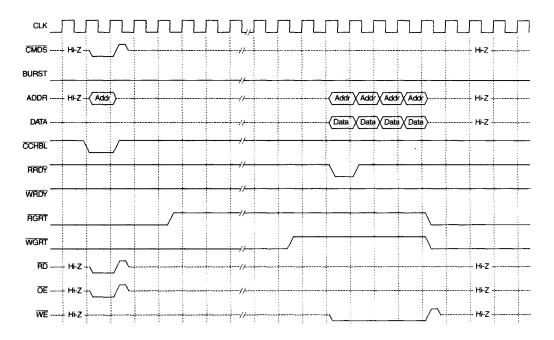


Figure 7. VBus Cacheable Single Read Miss

Burst Read Hit

Figure 8 shows a burst-read hit. As with a cacheable single-read hit, the STP1091 functions mainly to time the cycle by asserting RRDY as the SRAM provides the data.

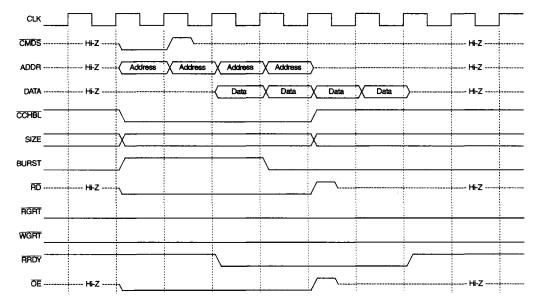


Figure 8. VBus Burst Read Hit

Burst Read Miss

Figure 9 shows a burst read miss. The external cache controller (STP1091) removes RRGT to indicate that the cycle is in progress and that STP1021 can proceed with an outstanding write if one is pending. When the data returns from the system bus, the STP1021 writes it into the SRAM and asserts RRDY when the requested data is on the VBus. Note that, in Figure 9, the STP1091 is in XBus configuration, and consequently the block size is 64 bytes. Only 32 bytes are sent to STP1021, while all 64 bytes are stored in SRAM. Also note that with critical word first ordering, the data returned starts from the index into the block for the requested doubleword, continues to the last index, and then wraps from index 0 to the starting index minus 1.

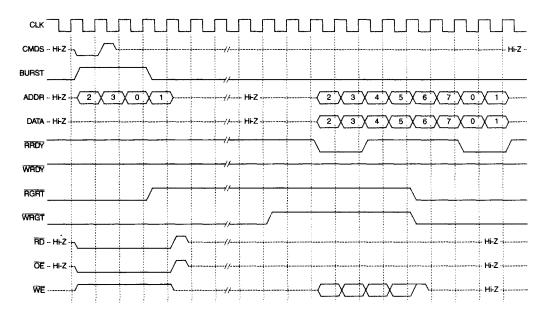


Figure 9. VBus Burst Read Miss

Cacheable Single Write Hit

Figure 10 shows a cacheable single-write hit. The STP1091 asserts $\overline{\text{WEE}}$ at the CMD + 2 cycle (i.e., two cycles after $\overline{\text{CMDS}}$) to allow the assertion of the write data (DATA, DPAR) and the write strobes ($\overline{\text{WE7-WE0}}$). The STP1091 asserts the $\overline{\text{WRDY}}$ in the following cycle ($\overline{\text{CMDS}}$ + 3).

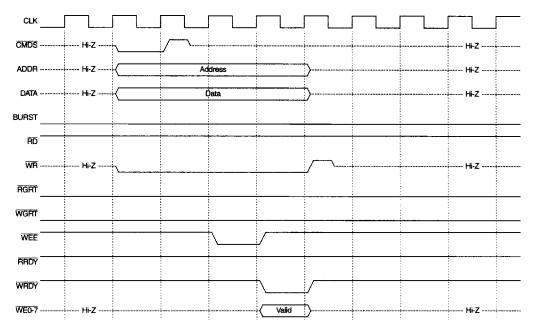


Figure 10. VBus Cacheable Single Write Hit

Cacheable Burst Write Hit

Figure 11 shows a burst write hit. It is basically the same except that WRDY is asserted for each data double-word written in the burst. The STP1021 deasserts BURST one cycle before the last write. Each of the individual writes in the burst from the STP1021 may be from one to eight bytes and may be at any address within the cache block. The number of consecutive writes may be of arbitrary length. If the external cache controller (STP1091) needs the VBus while a burst write cycle is occurring, it can deassert the WRGT signal to terminate the burst cycle prematurely. When the STP1021 reacquires the VBus, it continues the burst write from where it was interrupted.

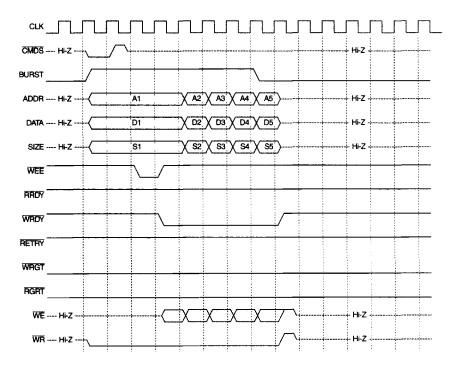


Figure 11. VBus Cacheable Burst Write Hit

Cache Invalidate

Figure 12 shows an invalidate. The external cache controller (STP1091) first removes the STP1021 from the VBus by revoking the \overline{RGRT} and \overline{WGRT} bus grants; it then asserts the address, \overline{WR} and \overline{CMDS} . Multiple invalidates may occur consecutively. Invalidates may also occur when the STP1091 has obtained the VBus for SRAM reads or writes.

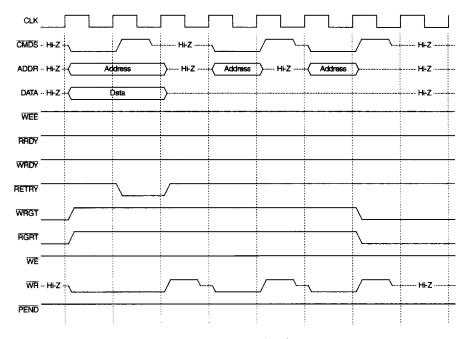


Figure 12. VBus Invalidation

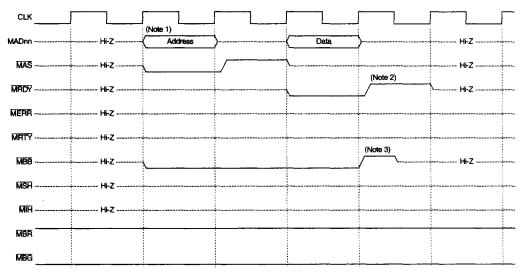


MBus Timing

The MBus read, write and invalidate operations are explained in the following section.

MBus Single Read

The single read cycle transfers a byte, half-word, word, or a double-word. Big-endian word ordering is used (the least significant bytes in a word appear on the high bits of the bus according to SPARC standard). Figure 13 shows an MBus single read operation.

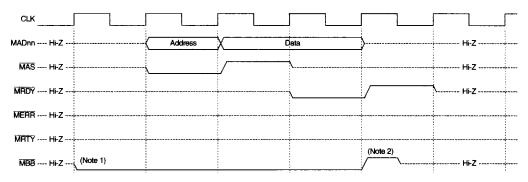


- Notes: 1. MADnn lines are held to their previously driven state by system bus holders.
 - 2. Control lines (MAS, MRDY, MERR, MRTY) are driven inactive for one clock before being released.
 - 3. MBB is driven high for 1/2 clock cycle before being released.

Figure 13. MBus Single Read

MBus Single Write

Single write operations are queued in the STP1021 store buffer. As soon as the STP1021 receives a bus grant, the transactions will be issued on the bus. The processor will not wait during this time, unless the buffer fills. Bytes, half-words, words, and double words may all be stored, with big-endian ordering. Any errors are reported as deferred data store errors. *Figure 14* shows an MBus single write operation.



Notes: 1. MBB is driven active one cycle before MAS during write and Cl cycles.

MBB is driven inactive for 1/2 clock cycle before being released.

Figure 14. MBus Single Write

MBus Burst Read

Figure 15 shows a 32-byte burst read operation. A read operation can be performed on any size of data transfer that is specified by the SIZE bits. Read transactions support wrapping (critical word first ordering). Transactions involving fewer than eight bytes will have undefined data on the unused bytes.

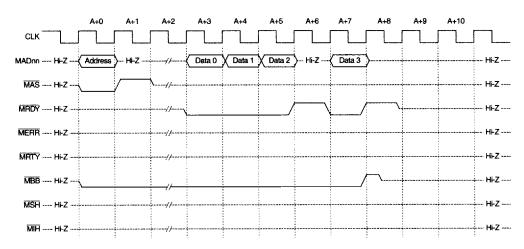
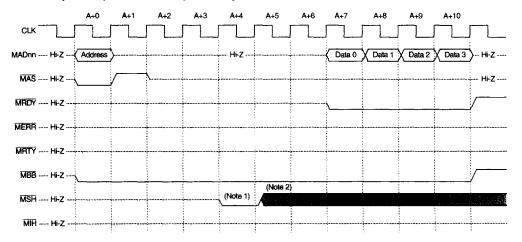


Figure 15. MBus Burst Read

MBus Coherent Read

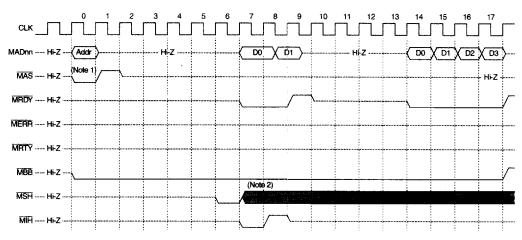
Coherent Read (CR) transactions are used to read data from the current owner. The owner may be memory or another cache. CR will be used for all on-board data cache load misses and all on-board instruction cache misses. If another cache owns the data, it will respond by asserting the MIH signal and providing the data. All CR transactions use critical-word-first ordering. The double-word that is needed first will be the starting address of the transaction. Double-words from memory must be returned in modulo 32-byte address order. Once the needed data arrives, the processor will use it immediately. Figure 16 shows an MBus coherent read of shared data. Any processor that has a valid cached copy of data referenced by CR transactions must assert the MSH signal to indicate that the information is shared. The STP1091 can accept the assertion of MSH at any time until receipt of the first data word. If the data is owned by another cache, the STP1091 will ignore any data ready responses until four cycles beyond the assertion of MIH. This allows memory controllers to begin transmitting data sooner. Memory controllers must not respond with data until a time equal to the maximum MIH assertion delay for any cache in the system. Figure 17 shows an MBus coherent read of owned data.



Notes: 1, MSH may occur from A+2 to A+7.

2. MSH is an open drain signal, it is not driven inactive. The system pull-up resistor returns it to an inactive level.

Figure 16. MBUS Coherent Read of Shared Data



Notes: 1. Device is not the Master.

2. MSH is an open drain signal. It is not driven inactive. The system pull-up resistor returns it to an inactive level.

Figure 17. MBUS Coherent Read of Owned Data

MBus Coherent Invalidate

A Coherent Invalidate (CI) operation can only be performed on a block (32 bytes). All CI operations will be snooped by all snooping caches. If a Coherent Invalidate operation hits in a cache, that copy will be invalidated immediately, regardless of its state. Memory is responsible for the acknowledgment of the CI transaction. *Figure 18* shows a CI operation.

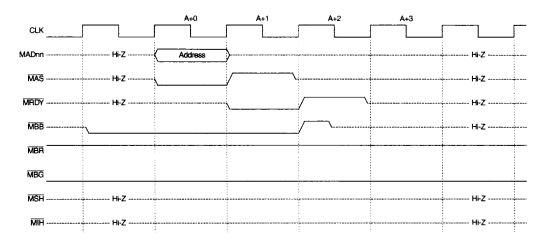


Figure 18. MBus Coherent Invalidate

Coherent Read and Invalidate

Since the MBus supports a write-invalidate type of cache-consistency protocol, a special Coherent Read and Invalidate (CRI) transaction that combines a CR transaction with the CI transaction was included to reduce the number of MBus Coherent transactions,. Caches that are performing CR transactions with the knowledge that they intend to immediately modify the data can issue this transaction.

Each CRI transaction will be snooped by all system caches. If the address hits and the cache does not own the block, that cache immediately invalidate its copy of this block, no matter what state the data was in. If the address hits and the cache owns the block, the block will assert $\overline{\text{MIH}}$ and supply the data. When the data has been successfully supplied, the cache will then invalidate its copy of this block.

MSH is not driven during the CRI transaction.

Coherent Write and Invalidate

A Coherent Write and Invalidate transaction combines a block write transaction with a CI transaction.

Each Coherent Write and Invalidate transaction will be snooped by all system caches. If the address hits, caches will invalidate their copies of this block, no matter what state the data was in. Neither $\overline{\text{MIH}}$ nor $\overline{\text{MSH}}$ is asserted for Coherent Write and Invalidate transactions. *Figure 19* shows a Coherent Write and Invalidate operation.

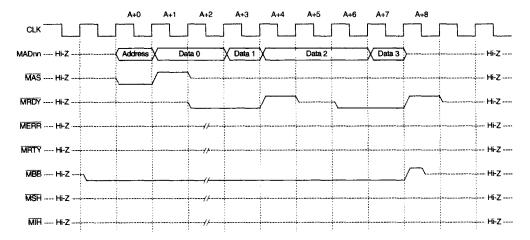
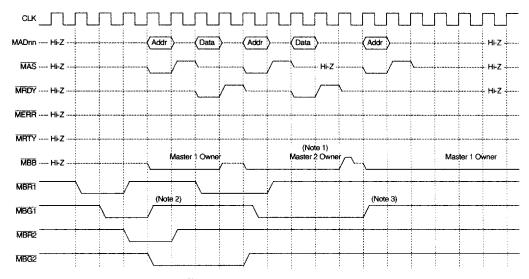


Figure 19. MBus Coherent Write and Invalidate

Arbitration

MBus arbitration is accomplished by an external arbiter. The actual arbitration algorithm is implementation dependent. The STP1091 asserts $\overline{\text{MBR}}$ when it determines that it requires the MBus. It releases $\overline{\text{MBR}}$ immediately after receiving $\overline{\text{MBG}}$. $\overline{\text{MBG}}$ should remain asserted until $\overline{\text{MBB}}$ is negated. The STP1091 normally releases the $\overline{\text{MBB}}$ signal at the termination of the cycle (final acknowledgment); however, after an error acknowledgment, $\overline{\text{BB}}$ will remain asserted for a number of cycles while the finite state machines complete their error response transitions. A generic example of MBus arbitration is shown in *Figure 20*.



- Notes: 1. Master 2 holds the bus by keeping MBB asserted.
 - 2. The arbiter releases MBG at the earliest possible time. If Master 1 had not asserted MBB, it would have lost the bus.
 - 3. Arbiter releases MBG1 when it detects MBB deasserted.

Figure 20. MBUS Arbitration



XBus Operation

The XBus is a packet-switched (message) bus. Packet-switched busses differ from conventional circuit-switched busses in that the bus is not held busy for the total transaction. In a circuit-switched bus, a bus master (for example, a processor), that needs a resource (such as memory) arbitrates for the bus and obtains ownership. It supplies a slave address and waits for a response. The slave either accepts or supplies data and signals the master when it finishes. The master then releases the bus.

Bus Protocol

Cycles

A bus cycle is one period of the bus clock; it forms the unit of time and one-way information transfer.

All cycles on the XBus fall into one of four categories: HEADER, DATA, MEMFAULT, and IDLE. A header cycle is always the first cycle of a packet; data cycles normally constitute the remaining cycles; MEMFAULT cycles are used to indicate an error in one of the data cycles of a packet; IDLE cycles are those during which no packet is being transmitted on the bus.

HEADER and MEMFAULT cycles are indicated by all-even encoding of parity. A given cycle with all-even encoding is a HEADER cycle if it is the first cycle of a packet: otherwise it is a MEMFAULT cycle.

DATA and IDLE cycles are indicated by the all odd encoding of parity. A given cycle with all-odd encoding is a DATA cycle if it is known to be inside some packet; otherwise, it is an IDLE cycle.

When the parity encoding is neither all-even nor all-odd an error is indicated.

Packets

A packet is a contiguous sequence of cycles that constitutes the next higher unit of transfer. The first cycle (header) of a packet carries address and control information, while subsequent cycles carry data. Packets are in two sizes: 2 cycles and 9 cycles.

An XBus device sends a packet after arbitrating for the XBus and getting grant. Packet transmission by a device is uninterruptible once the header cycle has been sent.

A 5-bit DCmd field in each packet encodes the packet type. One of these bits encodes whether the packet is a request or a reply; the other four encode the transmission type.

Transactions

A transaction consists of a pair of packets (request, reply) that together performs some logical function.

Packets usually come in pairs, but there are exceptions to this. For the FLUSH LINE transaction, several reply packets may be generated for one request. For a transaction that times out, no reply packet will be generated.

Packet detection

Header cycles are indicated by even parity encoding on each of the four parity bits XPAR3-XPAR0. The XBus device uses this information as well as its current XBus state information to recognize a header cycle. Once the header cycle has been recognized, the XBus device expects data. The number of data cycles is determined by the length bit in the message header. Data and idle cycles have the same parity encodings: therefore, the parity cannot be used to distinguish between them.

Bus Watchers

Bus watchers interface XBus to application-specific system busses or devices. Their function is to translate XBus transactions to system-bus or device operations and translate system-bus or device requests to XBus transactions.

At the lowest operational level, bus watchers:

- Receive XBus packets, which request system-bus resources or system bus actions.
- Receive system-bus responses or replies to these requests and map them to XBus reply messages.
- Receive system-bus commands directed to the XBus and convert them to appropriate XBus command packets.
- Receive XBus replies and map them to corresponding system-bus replies.
- Snoop system0-bus operations for references to locally cached data and send messages to the STP1091 to perform coherency operations.

Bus watchers request use of XBus on dedicated lines to the STP1091, which contains the XBus arbiter. The meaning of the XREQn[1]-XREQn[0] signals depends on the sequence of values on the two lines. The sequences used and their meanings are described in *Table 7*.

TABLE 7: Arbitration and Flow Control Encoding

НН	-	Idle
HL		Block STP1091 request packets for nine cycles.
HL	HL	Block STP1091 request and reply packets for nine cycles.
LH	нн	Request XBus for low-priority two-cycle packet.
LH	LH	Request XBus for low-priority nine-cycle packet.
LH	HL	Request XBus for low-priority two-cycle packet and block STP1091 packets for nine cycles.
LH	LĹ	Request XBus for low-priority nine-cycle packet and block STP1091 packets for nine cycles.
LL	нн	Not valid.
LL	LH	Request XBus for High-priority nine-cycle packet.
LL	HL	Not valid.
Ш	LL	Request XBus for high-priority nine-cycle packet and block TMX390X55 packets for nine cycles.

Arbitration Priorities

The Xbus arbiter in STP1091 supports four priorities. Listed in descending priority order, they are:

- **BW HIGH:** XBus arbitration requests from bus watcher to send block read reply packets to STP1091.
- CC HIGH: XBus arbitration requests from STP1091 to send reply packets to a bus watcher (Highest priority).

- BW LOW: XBus arbitration requests from bus watcher to send system request packets and most system bus reply packets to STP1091.
- CC LOW: XBus arbitration requests from STP1091 to send requests packets to a bus watcher (lowest priority).

XBus Timing Waveforms

Figure 21 shows a simple 2-cycle packet. The bus watcher request the use of the bus by asserting "01" binary followed by "11" binary on the $\overline{\text{XREQn0}}$ lines. The STP1091 grants the BW the bus for two cycles and the BW sends a 2-cycle packet.

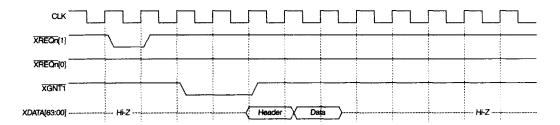


Figure 21. XBus 2-Cycle Packet

Figure 22 shows a 9-cycle packet transmitted by a bus watcher. The $\overline{\text{XREQn}}$ lines are driven "01" binary, followed by another "01" binary. This is a request for a low-priority 9-cycle packet. The STP1091 grants the bus to the BW for nine cycles.

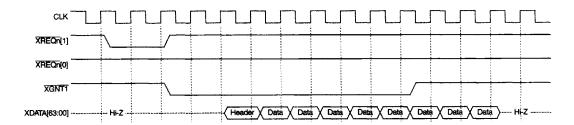


Figure 22. XBus 9-Cycle Packet

Figure 23 shows a STP1091 2-cycle request packet followed by a reply packet from the bus watcher. Note the XREQn arbitration request is for a low-priority 2-cycle packet.

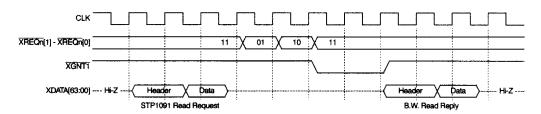


Figure 23. 2-Cycle Request and 2-Cycle Reply

Figure 24 shows a STP1091 9-cycle packet (block write) and a corresponding 2-cycle reply packet.

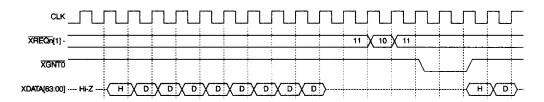


Figure 24. 9-Cycle Request and 2-Cycle Reply

Boot Bus

The boot bus is a simple synchronous 12-pin interface provided by the STP1091 for accessing an EPROM for bootstrap loading and for accessing other low-speed peripherals. The boot bus supports an address space of 16M bytes. Provisions are made for reading or writing from 1 to 8 bytes from/to boot-bus devices and for polling the devices for interrupts. Boot bus is available only in the XBus configuration (when MBSEL is low). Boot bus is accessible from both the VBus and the XBus.

TABLE 8: Boot-Bus Address Decoding

t. -1	
VBus	Noncacheable Space ADDR35-ADDR28= 0xFF ADDR27-ADDR24 = 0x0 or 0x1 ADDR23-ADDR00 = Boot-bus address
XBus ^[1]	PA35-PA28 = 0xFn PA27-PA24 = 0x0 PA23-PA0 = Boot-bus address

^{1.} PA = Physical Address

TABLE 9: Summary of the Boot Bus Physical Signals

				- mg + 1,5 + 0,5 + 0.5	
Section 1991	 1.000		N	ما دوما خفي ٢ دونځه	- Line Catholic
LDATA7-LDATA0	ADDRES	S/DATA Bu	s		BS
LCMD2-LCMD0	Command	d Bus		i	BS
LCMD5	Command	d Strobe			BS

^{1.} BS Signifies bi-state.

Write Valid

The write valid command instructs the address decoder to write the selected device with the data on LDATA7-LDATA0. See *Figure 25*.

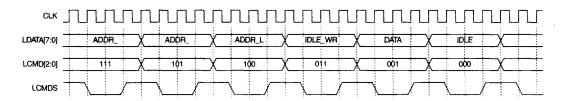


Figure 25. Boot Bus Write

Read Valid

The read valid command instructs the address decoder to drive the selected device data ontoLDATA7-LDATA0. See *Figure 26*.

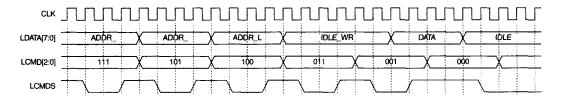


Figure 26. Boot Bus Read

Clocks

In order to reduce system clock skew, a phase-lock loop (PLL) is implemented for each of the clock inputs. For testing and other purposes, a PLL bypass mechanism is provided. When PLLBYP is active, the PLL circuitry of both PCLK and BCLK will be bypassed completely.

Phase-Lock Loop Operation

The PLL operates by constantly measuring internal clock routing and receiver delay and internally generating a clock that is effectively *ahead* of the external clock by an amount equal to the internal routing delay. This ensures that all internal logic sees a clock signal nearly equivalent to that at the external clock pin. All system logic using either PCLK or BCLK is expected to provide acceptable setup and hold times relative to the processor clock input pin.

Prior to normal operation, the PLL must be allowed time to stabilize (i.e., after power up or when PLL has been disabled). During this time, the RESET pin must be asserted. The time required for stabilization is 100 milliseconds.

The input clocks to the STP1091 must never be stopped or changed from normal periodic operation while the PLL is enabled. Doing so will cause PLL instability and unpredictable operation.

To ensure proper operation of the PLL, VCCCKB, VSSCKB, VCCCKP, and VSSCKP should be filtered of system noise. Figure 27 shows a recommended circuit.

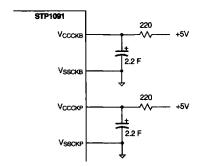


Figure 27. Typical Phase Lock Loop (PLL) Filter Circuit

Note: It is essential that the JTAG TAP controller be reset prior to, or at the same time as RESET in order for the PLL to begin initialization. The TAP controller may be initialized either by asserting the TRST pin or by asserting the TMS pin for five consecutive cycles of TCK (test clock). If this reset does not occur, the PLL clock feedback loop may not be established, and unpredictable operation may result. Whenever the JTAG interface is not in use by a particular system, asserting the TRST signal statically is strongly recommended.

Input Clock Requirements

The STP1091 can tolerate most clean, stable clock sources when the PLL is enabled. With the PLL enabled, the STP1091 uses only the *rising edge* of the input clocks. Internally, the STP1091 doubles the frequency of the input clocks and then halves them to produce stable clocks with 50% duty cycles. The high time of the input clocks must be between 25% and 75%.

When the PLLs are bypassed, care must be taken to provide a 50% duty cycle on each of the clock inputs. Pin timings for operation with the PLLs bypassed are not fully defined.

IMPORTANT NOTE: Operation in a system with the PLLs bypassed is not recommended or fully specified. Use in this manner will generally require reduced operating frequencies and careful system design.

Relationship of PCLK and BCLK

Due to the design of the internal synchronizers, PCLK must be at least 10% faster than BCLK and the ratio of PCLK to BCLK must not exceed 2.8 to 1. These restrictions are true for asynchronous operation (i.e. the $\overline{\text{SYNC}}$ pin is not asserted).

When the SYNC pin is asserted, BCLK and PCLK must be connected to the same clock with a maximum of 150 ps of skew between them.

Reset

Reset can come from the system \overline{RSTIN} (system reset) or from the STP1021. The STP1021 can initiate two different resets; one is watch-dog reset (WD), and the other is software internal reset (SI). Remote processors on the system bus can initiate only software internal resets. The reset register is used to determine the type of reset.

On system reset, the STP1091 will do the following:

- Asynchronously 3-state all DATA/ADDR output drivers on the VBus.
- Asynchronously 3-state all bidirectional output drivers on the MBus/XBus.
- Drive all control strobes on the VBus to high.
- Reset the STP1021 by asserting RESET.
- · Disable E-cache.
- · Reset all finite state machines.
- Reset all internal queues.
- Reset the STP1091 control register, status register, interrupt pending register, and reset register.
- Set Interrupt mask register to 1s.

After system reset, the STP1091 will do the following:

- Continue to reset the STP1021 for eight cycles.
- Configure E-cache tag column redundancy for 150 cycles. During this period of time, bidirectional control strobes are 3-stated, and unidirectional output control strobes are deasserted. After configuring E-cache column tag redundancy, RGRT and WGRT are asserted.

On software internal reset, the STP1091 deasserts RGRT and WGRT, waits for pending operations to complete (E-cache updates will not be completed), then clears store exception pending (SXP) in the status register and the WD bit in the reset register, and resets the STP1021 for eight cycles. On a software internal reset, the parity enable (PE) bit in the STP1091 and the STP1021 may be different. The system software must ensure that both PE bits are identical before issuing the first write after software internal reset.

On watch-dog reset, the STP1091 will do the following:

- In MBus configuration, assert AERR.
- Set the WD bit in the reset register.

Reset Requirements

To ensure the proper operation of the STP1091, the following requirements must be met by the system for reset:

- At power on of the system, system reset RSTIN should be asserted for a minimum of 100 ms after the
 voltage is within the operating tolerance of the chip. If RSTIN is asserted at any other time, it must stay
 asserted for a minimum of eight BCLK cycles. RSTIN can be asynchronous to either or both of BCLK and
 PCLK.
- JTAG reset (TRST) must be asserted at power on for a minimum of 50 ns. TRST can be asynchronous to any or all of BCLK, PCLK and TCK. Two TCLKs elapse after TRST is deasserted before TMS can be asserted.
- After RSTIN is deasserted, there should be no requests from XBus or MBus for a minimum of 150 PCLK cycles in order to allow the E-cache tag memory column redundancy programming to complete. Also, there should be no JTAG operations during this time.
- All the 3-state outputs on the MBus or the XBus (as selected by MBSEL) will be placed in their
 high-impedance state. It is the responsibility of the system logic to assure that these signals remain in their
 appropriate states with pullups as necessary.
- RESET is asserted to the STP1021 asynchronously as soon as RSTIN is asserted. The STP1091 keeps asserting RESET for eight cycles after RSTIN is deasserted. The STP1021 3-states all bidirectional signals on VBus asynchronously when RESET is asserted. During RSTIN the STP1091 drives the bidirectional VBus signals with weak drivers toward V_{CC}. After RSTIN is deasserted, the STP1091 drives all the bidirectional control signals to logic high and then releases them before RESET is deasserted.
- After a boundary/internal scan test, the TRST and RESET should be asserted in the same way as during power on reset for the chip to enter normal operation mode.
- RSTIN should be held deasserted during internal scan.

Error Handling

Errors are handled in four different ways in the STP1091.

- Errors logged to STP1091's error register and reported to the STP1021 through encoding of control strobes <u>MEXC</u>, <u>RRDY</u> (or <u>WRDY</u>), and <u>RETRY</u> are:
 - Errors on a read or a LDST operation.
 - Store exception pending condition of a write miss.
 - Data parity errors on VBus when the STP1091 processor is the master.
 - Errors on a demap initiated by the STP1091 processor.

- Errors are reported to the STP1021 through a level-15 interrupt (for the XBus configuration only). Errors reported in this way are:
 - Asynchronous errors, which include errors of operations that have been acknowledged by STP1091 to the STP1021. These include, for example, stream operations for block copy/zero, shared writes in the XBus configuration, or noncacheable writes, in which errors occur later in the operation.
 - Data parity errors on the VBus when the STP1091 accesses external cache for an incoming bus request.

All these errors are logged into the error register of STP1091. For the MBus configuration, these types of errors are reported to the system by asserting \overline{AERR} .

- Errors are reported to system by asserting CCERR. Errors reported in this way are:
 - XBus errors.
 - Cache consistency errors.
 - VBus parity errors on a flush operation.

These errors are considered catastrophic. They are logged into the error register of the STP1091 before CCERR is asserted.

Errors neither reported or logged. For example, errors on the STP1091 prefetch operation are ignored.

In the MBus configuration, an error on an outgoing request is reported back to the STP1091 with the MBus acknowledgment type by encoding MRDY, MERR, and MRTY.

In the XBus configuration, an error on an outgoing request is reported to the STP1091 in two different ways; the error bit in the header cycle of the reply packet is set, or odd parity is used on a data cycle to indicate a memory fault. In this case, the three least-significant bits of the memory fault data cycle contains the error code.

For MBus and XBus configurations, if a parity error occurs on the VBus when the STP1091 accesses external cache in response to an incoming bus request, a VBus parity error will be reported to the requestor as an uncorrectable error.

Any illegal access from VBus will be reported as a time-out error to STP1091. Illegal accesses from the system bus side are ignored. Atomic load-store to boot bus or the STP1091 registers, out-of-range control space access, and read of interrupt generation register are examples of illegal accesses from VBus.

A parity error on VBus when the STP1021 is the bus master is reported to the STP1021 as an undefined error.

DEBUG SUPPORT

TABLE 10: Boundary Scan Bit Order in MBus Mode

1	Pickers in the second	727	,									4551		· · · · · · · · · · · · · · · · · · ·	Lender on the Company of the	100 00000		Service and Edition
2	1	ļ	MBSEL	53	I	MAD10	105	Ē	oe-merr	157	Ó	MAD41	209		PLLBYP	261	0	DATA54
3	-	i	MIRL1	-	0	MAD10	_		MRDY	158	1	MAD42	-	Ó		_	- - -	DATA53
1	\rightarrow	0		-				0		-	0		_	_		_	0	DATA53
5	4	1	MIRL0	56	0	MAD11	108	E	oe-mrdy	160	1	MAD43	212	0	IRL2	264	T	DATA52
To MIRL2	5	0	MIRLO	57	- 1	MAD12	109	1		161	0		213	0	IFIL3	265	0	DATA52
8 I MIRL2 60 O MAD13 112 O MBSG 164 I MAD45 216 I ADDR2S 268 I DATA 9 O MIRL2 61 I MAD14 113 E O MBSG 166 O MAD45 217 O ADDR2S 269 O DATA 11 O I — 62 O MAD14 114 I I MBB 166 I MAD46 218 I ADDR2S 277 O DATA 11 O — 63 I MAD15 115 O MBB 166 I MAD46 218 I ADDR2S 277 O DATA 11 O — 64 O MAD15 115 O MBB 167 O MAD46 218 I ADDR2S 271 O DATA 13 O — 65 E O MAD15 116 E O MBB 167 O MAD46 218 I ADDR2S 271 O DATA 14 I — 64 O MAD15 116 E O MBB 168 I MAD47 221 O ADDR2S 271 O DATA 15 O — 67 I MAD16 119 E O MBB 168 I MAD47 221 O ADDR2S 272 I DATA 16 I — 68 E O MAD16 119 E O MBS 168 O MAD47 221 O ADDR2S 272 I DATA 17 O — 67 I MAD16 119 E O MBS 168 O MAD47 221 O ADDR2S 275 O DATA 18 I — 68 O MAD16 120 I MBH 172 I MAD8 222 I ADDR2S 274 I DATA 18 E O MAD17 121 O MBH 173 O MAD48 224 I ADDR2D 277 O DATA 18 E O MAD17 121 O MBH 173 O MAD48 224 I ADDR2D 277 O DATA 19 O — 71 I MAD18 122 E O MBH 173 O MAD48 225 I ADDR2D 277 O DATA 19 O — 72 O MAD18 124 O MBH 173 O MAD48 225 I ADDR2D 277 O DATA 20 O — 72 O MAD18 124 O MBS 1 MBH 175 O MAD80 225 I ADDR2D 277 O DATA 21 I MID1 73 I MAD18 125 E O MBH 177 O MAD80 225 I ADDR2D 277 O DATA 22 O MID1 74 O MAD19 126 I DATA 23 I MID2 75 I MAD19 126 I DATA 24 O MID2 75 I MAD19 126 I DATA 25 I MID2 77 I MAD19 128 I MBH 177 O MAD80 229 I ADDR2D 279 O DATA 26 E O MBD 177 I MAD19 128 I DATA 27 I MAD19 77 I MAD19 128 I DATA 28 I MID2 77 I MAD19 128 I DATA 29 I MBD 2 77 I MAD19 128 I DATA 29 I MBD 2 77 I MAD19 128 I DATA 29 I MBD 2 77 I MAD19 128 I DATA 29 I MBD 2 77 I MAD19 128 I DATA 29 I MBD 2 77 I MAD19 128 I DATA 29 I MBD 2 77 I MAD19 128 I DATA 29 I MBD 2 77 I MAD19 128 I DATA 29 I MBD 2 77 I MAD19 128 I DATA 29 I MBD 2 77 I MAD19 128 I DATA 29 I MBD 2 77 I MAD19 128 I DATA 29 I MBD 2 77 I MAD19 128 I DATA 29 I MBD 2 77 I MAD19 128 I DATA 29 I MBD 2 77 I MAD19 128 I DATA 29 I MBD 2 77 I MAD19 129 I DATA 29 I MBD 2 77 I MAD19 128 I DATA 29 I MBD 2 77 I MAD19 129 I DATA 29 I MBD 2 77 I MAD19 129 I DATA 29 I MBD 2 77 I MAD19 129 I DATA 29 I MBD 2 77 I MAD19 129 I DATA 29 I MBD 2 77 I MAD19 129 I DATA 29 I M	6	1	MIRL3	58	o	MAD12	110	0	MATY	162	ı	MAD44	214	1	ADDR24	266	- 1	DATA51
9 O MIRIL2 61 I MAD14 113 E ce-spar 165 O MAD45 217 O ADDR2S 289 C O DATA 11 O — 62 O MAD14 114 I MBB 166 I MAD46 219 I ADDR26 270 I DATA 11 O — 63 I MAD15 115 O MBB 167 O MAD46 219 O ADDR26 270 I DATA 12 I — 64 O MAD15 115 O MBB 167 O MAD46 219 O ADDR26 271 O DATA 13 O — 65 E oe-mxc2 117 I I MS 169 O MAD47 221 O ADDR26 273 O DATA 14 I — 66 E oe-mxc2 117 I I MS 169 O MAD47 221 I ADDR26 273 O DATA 15 O — 67 I MAD16 119 E oe-mas 171 E cemxid 122 I ADDR28 274 I DATA 16 I — 68 C MAD16 120 I MBH 172 I MAD8 222 I ADDR28 275 O DATA 16 I — 68 O MAD16 120 I MBH 172 I MAD8 224 I ADDR28 276 I DATA 17 O — 69 I MAD17 122 E ce-mb 174 I MAD48 224 I ADDR28 276 I DATA 18 E Oe-both 70 O MAD17 122 E ce-mb 174 I MAD48 224 I ADDR28 277 O DATA 19 O — 71 I MAD18 123 I MBH 173 O MAD48 222 I ADDR28 277 O DATA 19 O — 71 I MAD18 123 I MBH 175 O MAD49 222 O ADDR28 277 O DATA 19 O — 71 I MAD18 123 I MBH 175 O MAD49 222 O ADDR28 277 O DATA 19 O — 72 O MAD18 124 O MBH 175 O MAD49 222 O ADDR28 279 O DATA 22 O MBD 1 MAD19 125 E oe-mbh 177 O MAD80 222 I ADDR28 279 O DATA 23 I MBD 1 73 I MAD19 125 E oe-mbh 177 O MAD80 222 I ADDR28 28 I DATA 24 O MID1 74 O MAD18 128 I — 181 O MAD60 222 I ADDR28 28 I DATA 25 O AERR 77 I MAD28 127 I — 179 O MAD61 231 ADDR28 28 I DATA 26 O AERR 77 I MAD28 128 I — 181 O MAD62 229 I ADDR28 28 I DATA 27 I MBD 1 74 O MAD29 128 I — 181 O MAD62 229 I ADDR28 28 I DATA 28 O ABDR28 28 I DATA 29 I MBD 2 76 O MAD29 128 I — 181 O MAD62 229 I ADDR28 28 I DATA 29 I MBD 2 76 I MAD28 128 I — 181 O MAD62 229 I ADDR28 28 I DATA 29 I MBD 2 76 I MAD28 128 I — 181 O MAD62 229 I ADDR28 28 I DATA 29 I MBD 2 76 I MAD29 128 I — 181 O MAD62 229 I ADDR28 28 I DATA 29 I MBD 2 76 I MAD29 128 I — 181 O MAD62 229 I ADDR28 28 I DATA 29 I MBD 2 76 I MAD29 128 I — 181 O MAD62 229 I ADDR28 28 I DATA 29 I MBD 2 76 I MAD29 138 I MBD 2 I DATA 29 I MBD 2 77 I MAD29 138 I MBD 2 I DATA 29 I MBD 2 77 I MAD29 139 I MAD29 139 I MAD29 139 I DATA 29 I MBD 2 77 I MAD29 139 I MAD29 139 I MAD29 139 I DATA 29 I MBD 2 77 I MAD29 29 I MAD29 29 I DATA 29 I MBD 2 77 I	7	0	MIRL3	59	1	MAD13	111		MBG	163	0	MAD44	215	0	ADDR24	267	0	DATA51
10	8	1	MIRL2	60	0	MAD13	112	0	MBG	164		MAD45	216		ADDR25	268	1	DATA50
11	9	0	MIRL2	61		MAD14	113	E	oe-xpar	165	0	MAD45	217	0	ADDR25	269	0	DATA50
12	10			62	0	MAD14	114	1	MBB	166	1	MAD46	218	1	ADDR26	270	Т	DATA49
13	11	0	_	63	1	MAD15	115	0	MBB	167	0	MAD46	219	0	ADDR26	271	0	DATA49
14	12	1		64	0	MAD15	116	E	oe-mbb	168	1	MAD47	220	-	ADDR27	272	1	DATA48
15	13	0	_	65	E	oe-mxd2	117	ı	MAS	169	0	MAD47	221	0	ADDR27	273	0	DATA48
16	14	1	_	66	E	oe-mxd3	118	0	MAS	170	E	oemxd10	222	1	ADDR28	274		DATA47
17	15	0	_	67	1	MAD16	119	E	oe-mas	171	E	oemxd11	223	0	ADDR28	275	0	DATA47
B	16	1	_	68	0	MAD16	120		MIH	172	1	MAD48	224	T	ADDR29	276	1	DATA46
19	17	0		69	i	MAD17	121	0	MIH	173	Ó	MAD48	225	0	ADDR29	277	0	DATA46
20	18	E	oe-bb-dt	70	0	MAD17	122	E	oe-mih	174	1	MAD49	226	- 1	ADDR30	278	-	DATA45
21	19	0		71	ı	MAD18	123	1	MSH	175	0	MAD49	227	0	ADDR30	279	0	DATA45
22 O MIDT 74 O MAD19 126 I 178 I MAD51 230 O ADDR31 282 I DATA 23 I MID2 75 I MAD20 127 I 179 O MAD61 231 I ADDR32 283 O DATA 24 O MID2 76 O MAD20 128 I 180 I MAD52 232 O ADDR32 284 I DATA 25 O AERR 77 I MAD21 129 I 181 O MAD52 233 I ADDR33 285 O DATA 26 E Oe-aerr 78 O MAD21 130 O MBR 182 I MAD53 234 O ADDR33 286 I DATA 26 E Oe-aerr 78 O MAD21 130 O MBR 182 I MAD53 234 O ADDR33 286 I DATA 27 I SPAR-IN 79 I MAD22 131 I MID3 183 O MAD63 255 I ADDR33 286 I DATA 28 O SPAR-OUT 80 O MAD22 131 I MID3 183 O MAD63 255 I ADDR34 287 O DATA 29 I RETIN 81 I MAD22 132 O MID3 184 I MAD54 236 O ADDR34 288 I DATA 29 I RETIN 81 I MAD23 133 I MID0 185 O MAD64 236 O ADDR35 289 O DATA 30 I MAD00 82 O MAD23 134 O MID0 186 I MAD55 239 I PCLK 291 E Oe-dc 31 O MAD00 83 E Oe-mxd4 135 O 187 O MAD55 239 I PCLK 291 E Oe-dc 31 O MAD00 83 E Oe-mxd4 135 O 187 O MAD55 239 I PCLK 291 E Oe-dc 31 O MAD01 85 I MAD24 137 O MAD32 188 E Oemxd12 240 I DATA63 292 I DATA 33 O MAD01 85 I MAD24 137 O MAD32 188 E Oemxd12 240 I DATA63 292 I DATA 34 I MAD01 86 O MAD24 138 I MAD33 190 I MAD66 242 I DATA62 292 I DATA 35 O MAD02 86 O MAD24 138 I MAD33 190 I MAD66 242 I DATA62 295 O DATA 36 I MAD03 88 O MAD25 140 I MAD34 192 I MAD56 243 O DATA62 296 I DATA 37 O MAD03 88 I MAD26 140 I MAD34 192 I MAD56 243 O DATA62 296 I DATA 38 I MAD04 90 O MAD25 140 I MAD34 192 I MAD56 244 I DATA62 296 I DATA 39 O MAD04 91 I MAD26 141 O MAD34 192 I MAD58 246 I DATA60 298 I DATA 40 I MAD05 92 O MAD27 144 I MAD35 196 I MAD58 247 O DATA60 298 I DATA 41 O MAD06 94 O MAD27 144 I MAD36 196 I MAD58 247 O DATA60 298 O DATA 42 I MAD06 94 O MAD28 146 I MAD36 197 O MAD69 250 I DATA61 300 I DATA 44 I MAD06 96 O MAD28 146 I MAD37 198 I MAD60 251 I DATA63 300 I DATA 44 I MAD07 96 O MAD29 148 I MAD36 200 I MAD62 255 I DATA65 300 I DATA 45 O MAD07 97 I MAD30 149 O MAD38 201 O MAD62 255 I DATA65 300 I DATA 46 E Oe-mxd0 98 O MAD31 152 E OE-mxd8 204 I MAD62 255 O DATA63 307 O DATA 47 E OE-mxd0 98 O MAD31 152 E OE-mxd8 204 I MAD62 255 O DATA63 307 O DATA 48 I MAD08 100 O MAD31 1	20	0	_	72	0	MAD18	124	0	MSH	176	1	MAD50	228	E	oeaddr3	280	1	DATA44
23 I MID2 75 I MAD20 127 I — 179 O MAD51 231 I ADDR32 283 O DATA 24 O MID2 76 O MAD20 128 I — 180 I MADS2 232 O ADDR32 284 I DATA 25 O ĀĒRĀ 77 I MAD21 129 I — 181 O MADS2 233 I ADDR33 286 O DATA 26 E oe-aerr 78 O MAD21 130 O ĀĒRĀ 182 I MADS3 234 O ADDR33 286 I DATA 27 I Spare-in 79 I MAD22 131 I MID3 183 O MADS3 235 I ADDR34 287 O DATA 28 O Spare-out 80 O MAD22 132 O MID3 184 I MADS4 236 O ADDR34 288 I DATA 29 I RŠTĪN 81 I MAD23 133 I MID0 185 O MADS4 237 I ADDR35 280 O DATA 30 I MAD00 82 O MAD23 133 I MID0 185 O MADS4 237 I ADDR35 280 O DATA 31 O MAD00 83 E Oe-mxd4 135 O — 187 O MAD55 239 I PCLK 291 E Oe-dz 31 O MAD00 83 E Oe-mxd4 135 O — 187 O MAD55 239 I PCLK 291 E Oe-dz 33 O MAD01 84 E Oe-mxd5 136 I MAD32 188 E Oemxd12 240 I DATA63 292 I DATA 33 O MAD01 85 I MAD24 137 O MAD32 189 E Oemxd12 240 I DATA63 292 I DATA 34 I MAD02 86 O MAD24 138 I MAD33 190 I MAD56 242 I DATA62 294 I DATA 35 O MAD02 87 I MAD25 139 O MAD33 190 I MAD56 242 I DATA62 294 I DATA 36 I MAD03 88 O MAD25 140 I MAD34 192 I MAD57 244 I DATA61 296 I DATA 37 O MAD03 89 I MAD26 141 O MAD35 199 I MAD57 244 I DATA62 296 I DATA 38 I MAD01 90 O MAD26 141 O MAD36 192 I MAD57 244 I DATA62 296 I DATA 38 I MAD04 90 O MAD26 141 O MAD36 199 I MAD59 248 I DATA60 298 I DATA 39 O MAD04 91 I MAD26 141 O MAD36 199 I MAD58 246 I DATA60 299 O DATA 40 I MAD05 92 O MAD27 144 I MAD36 196 I MAD59 248 I DATA60 299 O DATA 41 O MAD06 93 I MAD28 145 O MAD36 197 O MAD69 249 O DATA61 297 O DATA 42 I MAD07 96 O MAD28 146 I MAD37 199 O MAD60 251 O DATA63 300 I DATA 44 I MAD07 96 O MAD28 148 I MAD38 200 I MAD61 252 I DATA55 301 O DATA 45 O MAD06 95 I MAD28 148 I MAD38 200 I MAD61 252 I DATA57 304 I DATA 46 E Oe-mxd1 99 I MAD30 149 O MAD38 201 O MAD61 255 I DATA56 307 O DATA 47 E Oe-mxd1 99 I MAD30 149 O MAD38 201 O MAD61 255 I DATA56 307 O DATA 48 I MAD08 100 O MAD31 150 I MAD39 202 I MAD62 255 I DATA56 307 O DATA 48 I MAD08 100 O MAD31 150 I MAD39 202 I MAD62 255 I DATA56 307 O DATA 48 I MAD08 100 O MAD31 150 I MAD39 202 I MAD62 255 I DATA56 307 O DATA 48 I MAD08 100 O MAD	21	ı	MID1	73	1	MAD19	125	E	oe-msh	177	0	MAD50	229	1	ADDR31	281	0	DATA44
24 O MID2 76 O MAD20 128 i — 180 I MAD52 232 O ADDR32 284 I DATA 25 O ĀĒRR 77 I MAD21 129 I — 181 O MAD52 233 I ADDR33 285 O DATA 26 E Oe-serr 78 O MAD21 130 O MĒR 182 I MAD53 234 O ADDR33 286 I DATA 27 I Spare-ID 79 I MAD22 131 I MID3 183 O MAD53 235 I ADDR33 286 I DATA 28 O Spare-Out 80 O MAD22 132 O MID3 184 I MAD54 236 O ADDR34 287 O DATA 28 O Spare-Out 80 O MAD22 132 O MID3 184 I MAD54 236 O ADDR34 288 I DATA 29 I RSTIN 81 I MAD23 133 I MID0 185 O MAD54 237 I ADDR35 289 O DATA 30 I MAD00 82 O MAD23 134 O MID0 186 I MAD55 238 O ADDR35 289 O DATA 31 O MAD00 83 E Oe-mxd4 135 O — 187 O MAD55 239 I PCLK 291 E Oe-dc 32 I MAD01 84 E Oe-mxd5 136 I MAD32 188 E Oemxd12 240 I DATA63 292 I DATA 33 O MAD01 85 I MAD24 137 O MAD32 189 E OEMXd13 241 O DATA63 293 O DATA 34 I MAD02 86 O MAD24 138 I MAD33 191 O MAD66 242 I DATA62 294 I DATA 35 O MAD02 87 I MAD25 139 O MAD33 191 O MAD66 242 I DATA62 294 I DATA 36 I MAD03 88 O MAD25 140 I MAD34 192 I MAD57 244 I DATA62 295 O DATA 37 O MAD03 88 I MAD26 141 O MAD34 193 O MAD56 249 I DATA62 295 O DATA 38 I MAD04 90 O MAD26 141 O MAD34 193 O MAD57 244 I DATA62 296 I DATA 39 O MAD04 91 I MAD27 143 O MAD35 195 O MAD58 249 O DATA61 297 O DATA 40 I MAD06 93 I MAD26 141 O MAD36 196 I MAD59 248 I DATA60 299 O DATA 41 O MAD06 93 I MAD29 144 I MAD36 196 I MAD69 248 I DATA60 299 O DATA 42 I MAD06 94 O MAD29 148 I MAD37 199 O MAD56 249 O DATA60 299 O DATA 44 I MAD06 95 I MAD29 148 I MAD37 199 O MAD66 251 O DATA60 299 O DATA 44 I MAD06 95 I MAD29 148 I MAD37 199 O MAD66 251 O DATA60 299 O DATA 44 I MAD06 95 I MAD29 148 I MAD37 199 O MAD66 251 O DATA63 300 I DATA 45 O MAD06 95 I MAD29 148 I MAD37 199 O MAD66 255 O DATA65 300 O DATA 46 E O-mxd1 99 I MAD31 150 O MAD38 201 O MAD62 255 O DATA65 300 O DATA 47 E O-mxd1 99 I MAD31 150 O MAD38 201 O MAD62 255 O DATA65 300 O DATA 48 I MAD08 100 O MAD31 152 E O-mxd8 201 I MAD62 256 E O-data7 306 O WES	22	0	MID1	74	0	MAD19	126	1	-	178	- 1	MAD51	230	0	ADDR31	282	1	DATA43
25 O ĀĒRR 77 I MAD21 129 I — 181 O MAD52 233 I ADDR33 285 O DATA 26 E O-earr 78 O MAD21 130 O MBR 182 I MAD53 234 O ADDR33 286 I DATA 27 I Spare-In 79 I MAD22 131 I MID3 183 O MAD63 235 I ADDR34 287 O DATA 28 O Spare-Out 80 O MAD22 132 O MID3 184 I MAD54 236 O ADDR34 288 I DATA 29 I RSTIN 81 I MAD23 133 I MID0 185 O MAD54 237 I ADDR34 288 I DATA 30 I MAD00 82 O MAD23 134 O MID0 185 O MAD55 238 O ADDR35 289 O DATA 30 I MAD00 83 E O-mxd4 135 O — 187 O MAD55 239 I PCLK 291 E O-dc 32 I MAD01 85 I MAD24 137 O MAD03 189 E O-mxd12 240 I DATA63 293 O DATA 31 I MAD02 86 O MAD24 138 I MAD33 190 I MAD66 242 I DATA63 293 O DATA 31 I MAD03 88 O MAD25 139 O MAD03 191 O MAD66 243 O DATA62 294 I DATA 31 O MAD03 88 O MAD25 139 O MAD03 191 O MAD66 243 O DATA62 296 O DATA 31 O MAD03 88 O MAD25 139 O MAD03 191 O MAD66 243 O DATA62 296 O DATA 31 O MAD03 88 O MAD25 139 O MAD03 191 O MAD66 243 O DATA62 296 O DATA 31 O MAD03 88 O MAD25 140 I MAD03 192 I MAD56 244 I DATA61 296 I DATA 31 O MAD03 88 I MAD26 141 O MAD03 192 I MAD56 246 I DATA60 299 O DATA 31 O MAD04 90 O MAD26 142 I MAD03 193 O MAD05 246 I DATA60 299 O DATA 31 O MAD05 92 O MAD27 144 I MAD05 196 I MAD05 246 I DATA60 299 O DATA 32 O MAD04 91 I MAD26 142 I MAD05 196 I MAD05 248 I DATA60 299 O DATA 32 I MAD06 93 I MAD26 144 I MAD06 196 I MAD06 250 I DATA63 300 I DATA 32 I MAD06 94 O MAD29 146 I MAD07 199 O MAD06 251 O DATA61 297 O DATA 34 I MAD06 95 I MAD29 146 I MAD07 199 O MAD06 251 O DATA63 300 I DATA 34 I MAD06 95 I MAD09 148 I MAD09 200 I MAD06 251 O DATA63 300 I DATA 34 I MAD06 96 I MAD07 97 I MAD09 148 I MAD09 200 I MAD06 255 O DATA66 300 I DATA 34 I MAD09 300 I MAD06 350 I MAD06 350 I MAD07 37 I MAD09 200 I MAD06 255 O DATA66 300 I DATA 35 O MAD07 37 I MAD09 200 I MAD06 255 O DATA66 300 I DATA 35 O MAD07 37 I MAD09 200 I MAD09 255 O DATA66 300 O DATA 35 O MAD09 200 I MAD06 255 O DATA66 300 O MAD08 200 I MAD09 200 I MAD06 255 O DATA66 300 O DATA 35 O MAD09 200 I MAD09 200 I MAD0	23	i	MID2	75	1	MAD20	127	1	_	179	0	MAD51	231	1	ADDF132	283	0	DATA43
26 E Oe-serr 78 O MAD21 130 O MBR 182 I MAD53 234 O ADDR33 286 I DATA 27 I spare-out 80 O MAD22 131 I MID3 183 O MAD53 235 I ADDR34 287 O DATA 29 I RSTIN 81 I MAD23 133 I MID0 186 O MAD54 237 I ADDR35 289 O DATA 30 I MAD00 82 O MAD23 134 O MID0 186 I MAD54 237 I ADDR35 290 DATA 31 O MAD00 83 E O-mxd4 135 O — 187 O MAD55 239 I PCLK 291 E O-edc 32 I MAD01 84	24	0	MID2	76	0	MAD20	128	ł		180	1	MAD52	232	0	ADDR32	284	1	DATA42
26 E Ge-aerr 78 O MAD21 130 O MIBR 182 I MAD53 234 O ADDR33 286 I DATA 27 I spare-out 80 O MAD22 131 I MID3 183 O MAD63 235 I ADDR34 287 O DATA 29 I RSTIN 81 I MAD23 133 I MID0 186 I MAD64 237 I ADDR35 289 O DATA 30 I MAD00 82 O MAD23 134 O MID0 186 I MAD55 238 O ADDR35 290 E c-e-dz 31 O MAD01 84 E o-mxd5 136 I MAD32 188 E cemxd112 240 I DATA63 293 O DATA 32 I M	25	0 .	AERR	77	ì	MAD21	129		_	181	0	MAD52	233	ı	ADDR33	285	0	DATA42
27		E	oe-aerr	78	0	MAD21	130	0	MBR	182	1	MAD53	234	0	ADDR33	286	1	DATA41
29 I RSTIN 81 1 MAD23 133 I MIDO 185 O MAD54 237 I ADDR35 289 O DATA 30 I MAD00 82 O MAD23 134 O MIDO 186 I MAD55 238 O ADDR35 290 E Oe-de 31 O MAD00 83 E Oe-mxd4 135 O — 187 O MAD55 239 I PCLK 291 E Oe-de 32 I MAD01 84 E Oe-mxd5 136 I MAD32 188 E Oemxd12 240 I DATA63 292 I DATA 33 O MAD01 85 I MAD24 137 O MAD32 189 E Oemxd12 240 I DATA63 292 I DATA 34 I MAD02 86 O MAD24 137 O MAD32 189 E OEmxd13 241 O DATA63 292 I DATA 35 O MAD02 87 I MAD24 138 I MAD33 190 I MAD66 242 I DATA62 294 I DATA 35 O MAD03 88 O MAD25 140 I MAD34 192 I MAD57 244 I DATA61 296 I DATA 37 O MAD03 89 I MAD26 141 O MAD34 192 I MAD57 244 I DATA61 296 I DATA 39 O MAD03 89 I MAD26 141 O MAD34 193 O MAD57 245 O DATA61 297 O DATA61 2		1	spare-in	79	-	MAD22	131		MID3	183	0	MAD53	235	1	ADDR34	287	0	DATA41
29	28	0	spare-out	80	0	MAD22	132	0	MID3	184	T	MAD54	236	Ö	ADDR34	288		DATA40
31	29	-	RSTIN	81	1	MAD23	133	- 1	MIDO	185	0	MAD54	237	ī	ADDR35	289	0	DATA40
32 1 MAD01	30	1	MAD00	82	0	MAD23	134	0	MIDO	186		MAD55	238	0	ADDR35	290	E	oe-data5
32 I MADO1	31	0	MAD00	83	E	oe-mxd4	135	0		187	0	MAD55	239		PCLK	291	E	oe-data4
34 I MAD02 86 O MAD24 138 I MAD33 190 I MAD56 242 I DATA62 294 I DATA 35 O MAD02 87 I MAD25 139 O MAD33 191 O MAD56 243 O DATA62 296 O DATA 36 I MAD03 88 O MAD26 140 I MAD34 192 I MAD57 244 I DATA61 296 I DATA 37 O MAD03 89 I MAD26 141 O MAD34 193 O MAD56 245 O DATA61 297 O DATA 38 I MAD04 90 O MAD26 142 I MAD35 195 O MAD58 247 O DATA60 298 I DATA 40 I MAD05 <td>$\overline{}$</td> <td>1</td> <td>MAD01</td> <td>84</td> <td>E</td> <td>oe-mxd5</td> <td>136</td> <td>ì</td> <td>MAD32</td> <td>188</td> <td>E</td> <td>oemxd12</td> <td>240</td> <td>ı</td> <td>DATA63</td> <td>292</td> <td>ı</td> <td>DATA39</td>	$\overline{}$	1	MAD01	84	E	oe-mxd5	136	ì	MAD32	188	E	oemxd12	240	ı	DATA63	292	ı	DATA39
35 O MAD02 87 I MAD25 139 O MAD33 191 O MAD66 243 O DATA62 295 O DATA 36 I MAD03 88 O MAD25 140 I MAD34 192 I MAD57 244 I DATA61 296 I DATA 37 O MAD03 89 I MAD26 141 O MAD34 193 O MAD57 245 O DATA61 297 O DATA 38 I MAD04 90 O MAD26 142 I MAD35 194 I MAD58 246 I DATA60 298 I DATA 39 O MAD04 91 I MAD27 143 O MAD35 195 O MAD58 247 O DATA60 298 I DATA 40 I MAD05 <td>33</td> <td>0</td> <td>MAD01</td> <td>85</td> <td>ı</td> <td>MAD24</td> <td>137</td> <td>0</td> <td>MAD32</td> <td>189</td> <td>E</td> <td>oemxd13</td> <td>241</td> <td>0</td> <td>DATA63</td> <td>293</td> <td>0</td> <td>DATA39</td>	33	0	MAD01	85	ı	MAD24	137	0	MAD32	189	E	oemxd13	241	0	DATA63	293	0	DATA39
36 I MAD03 88 O MAD25 140 I MAD34 192 I MAD57 244 I DATA61 296 I DATA 37 O MAD03 89 I MAD26 141 O MAD34 193 O MAD57 245 O DATA61 297 O DATA 38 I MAD04 90 O MAD26 142 I MAD35 194 I MAD58 246 I DATA60 298 I DATA 39 O MAD04 91 I MAD27 143 O MAD35 195 O MAD58 247 O DATA60 299 O DATA 40 I MAD05 92 O MAD27 144 I MAD36 196 I MAD59 248 I DATA59 300 I DATA 41 O MAD05 <td>34</td> <td>i</td> <td>MAD02</td> <td>86</td> <td>0</td> <td>MAD24</td> <td>138</td> <td>1</td> <td>MAD33</td> <td>190</td> <td>-</td> <td>MAD56</td> <td>242</td> <td>1</td> <td>DATA62</td> <td>294</td> <td>-</td> <td>DATA38</td>	34	i	MAD02	86	0	MAD24	138	1	MAD33	190	-	MAD56	242	1	DATA62	294	-	DATA38
37 O MAD03 89 I MAD26 141 O MAD34 193 O MAD57 245 O DATA61 297 O DATA38 38 I MAD04 90 O MAD26 142 I MAD35 194 I MAD58 246 I DATA60 298 I DATA 39 O MAD04 91 I MAD27 143 O MAD35 195 O MAD58 247 O DATA60 299 O DATA 40 I MAD05 92 O MAD27 144 I MAD36 196 I MAD59 248 I DATA59 300 I DATA 41 O MAD05 93 I MAD28 145 O MAD36 197 O MAD59 248 I DATA59 301 O DATA 42 I MAD06 </td <td>35</td> <td>0</td> <td>MAD02</td> <td>87</td> <td>ı</td> <td>MAD25</td> <td>139</td> <td>0</td> <td>MAD33</td> <td>191</td> <td>0</td> <td>MAD56</td> <td>243</td> <td>0</td> <td>DATA62</td> <td>295</td> <td>0</td> <td>DATA38</td>	35	0	MAD02	87	ı	MAD25	139	0	MAD33	191	0	MAD56	243	0	DATA62	295	0	DATA38
38	36	ı	MAD03	88	0	MAD25	140	- 1	MAD34	192	ı	MAD57	244		DATA61	296	i	DATA37
39 O MAD04 91 I MAD27 143 O MAD35 195 O MAD58 247 O DATA60 299 O DATA60 40 I MAD05 92 O MAD27 144 I MAD36 196 I MAD59 248 I DATA59 300 I DATA 41 O MAD06 93 I MAD28 145 O MAD36 197 O MAD59 249 O DATA59 301 O DATA 42 I MAD06 94 O MAD28 146 I MAD37 198 I MAD60 250 I DATA58 302 I DATA 43 O MAD06 95 I MAD29 147 O MAD37 199 O MAD60 251 O DATA58 303 O DATA 44 I MAD07 </td <td>37</td> <td>0</td> <td>MAD03</td> <td>89</td> <td>ı</td> <td>MAD26</td> <td>141</td> <td>0</td> <td>MAD34</td> <td>193</td> <td>0</td> <td>MAD57</td> <td>245</td> <td>0</td> <td>DATA61</td> <td>297</td> <td>0</td> <td>DATA37</td>	37	0	MAD03	89	ı	MAD26	141	0	MAD34	193	0	MAD57	245	0	DATA61	297	0	DATA37
40 I MAD05 92 O MAD27 144 I MAD36 196 I MAD59 248 I DATA59 300 I DATA 41 O MAD05 93 I MAD28 145 O MAD36 197 O MAD59 249 O DATA59 301 O DATA 42 I MAD06 94 O MAD28 146 I MAD37 198 I MAD60 250 I DATA58 302 I DATA 43 O MAD06 95 I MAD29 147 O MAD37 199 O MAD60 251 O DATA58 303 O DATA 44 I MAD07 96 O MAD29 148 I MAD38 200 I MAD60 251 O DATA57 300 I DATA 45 O MAD07 97 I MAD30 149 O MAD38 201 O MAD61 252 I DATA57 300 O DATA 46 E Oe-mxd0 98 O MAD30 150 I MAD39 202 I MAD62 254 I DATA56 306 I DATA 47 E Oe-mxd1 99 I MAD31 151 O MAD39 203 O MAD62 255 O DATA56 307 O DATA 48 I MAD08 100 O MAD31 152 E Oe-mxd8 204 I MAD63 256 E Oe-data7 308 O WES	38	1	MAD04	90	0	MAD26	142	-	MAD35	194	1	MAD58	246	П	DATA60	298	1	DATA36
41 O MAD05 93 I MAD28 145 O MAD36 197 O MAD59 249 O DATA59 301 O DATA59 42 I MAD06 94 O MAD28 146 I MAD37 198 I MAD60 250 I DATA58 302 I DATA54 43 O MAD06 95 I MAD29 147 O MAD37 199 O MAD60 251 O DATA58 303 O DATA54 44 I MAD07 96 O MAD29 148 I MAD38 200 I MAD61 252 I DATA57 304 I DATA54 45 O MAD07 97 I MAD30 149 O MAD38 201 O MAD61 253 O DATA57 305 O DATA54 46 E <td< td=""><td>39</td><td>0</td><td>MAD04</td><td>91</td><td>1</td><td>MAD27</td><td>143</td><td>0</td><td>MAD35</td><td>195</td><td>0</td><td>MAD58</td><td>247</td><td>0</td><td>DATA60</td><td>299</td><td>0</td><td>DATA36</td></td<>	39	0	MAD04	91	1	MAD27	143	0	MAD35	195	0	MAD58	247	0	DATA60	299	0	DATA36
42 I MAD06 94 O MAD28 146 I MAD37 198 I MAD60 250 I DATA58 302 I DATA58 43 O MAD06 95 I MAD29 147 O MAD37 199 O MAD60 251 O DATA58 303 O DATA58 44 I MAD07 96 O MAD29 148 I MAD38 200 I MAD61 252 I DATA57 304 I DATA58 45 O MAD07 97 I MAD30 149 O MAD38 201 O MAD61 253 O DATA57 305 O DATA58 46 E o-mxxd0 98 O MAD30 150 I MAD39 202 I MAD62 254 I DATA56 306 I DATA57 47 E <	40	<u> </u>	MAD05	92	0	MAD27	144	1	MAD36	196	1	MAD59	248	- 1	DATA59	300	1	DATA35
43 O MADO6 95 I MAD29 147 O MAD37 199 O MAD60 251 O DATA58 303 O DATA 44 I MAD07 96 O MAD29 148 I MAD38 200 I MAD61 252 I DATA57 304 I DATA 45 O MAD07 97 I MAD30 149 O MAD38 201 O MAD61 253 O DATA57 305 O DATA 46 E De-mxd0 98 O MAD30 150 I MAD39 202 I MAD62 254 I DATA56 306 I DATA 47 E DE-mxd1 99 I MAD31 151 O MAD39 203 O MAD62 255 O DATA56 307 O DATA 48 I MAD08 100 O MAD31 152 E DE-mxd8 204 I MAD63 256 E DE-data7 308 O WES	41	0	MAD05	93	1	MAD28	145	0	MAD36	197	0	MAD59	249	0	DATA59	301	0	DATA35
44 I MADO7 96 O MAD29 148 I MAD38 200 I MAD61 252 I DATA57 304 I DATA57 45 O MAD07 97 I MAD30 149 O MAD38 201 O MAD61 253 O DATA57 305 O DATA56 46 E oe-mxd0 98 O MAD30 150 I MAD39 202 I MAD62 254 I DATA56 306 I DATA57 47 E oe-mxd1 99 I MAD31 151 O MAD39 203 O MAD62 255 O DATA56 307 O DATA56 48 I MAD08 100 O MAD31 152 E oe-mxd8 204 I MAD63 256 E oe-data7 306 O WE3	42	ı	MAD06	94	٥	MAD28	146	1	MAD37	198	1	MAD60	250	1	DATA58	302	ł	DATA34
45 O MADO7 97 I MAD30 149 O MAD38 201 O MAD61 253 O DATA57 305 O DATA 46 E oe-mxd0 98 O MAD30 150 I MAD39 202 I MAD62 254 I DATA56 306 I DATA 47 E oe-mxd1 99 I MAD31 151 O MAD39 203 O MAD62 255 O DATA56 307 O DATA 48 I MAD08 100 O MAD31 152 E oe-mxd8 204 I MAD63 256 E oe-data7 308 O WES	43	0	MAD06	95	- 1	MAD29	147	0	MAD37	199	0	MAD60	251	0	DATA58	303	0	DATA34
46 E oe-mxd0 98 O MAD30 150 I MAD39 202 I MAD62 254 I DATA56 306 I DATA 47 E oe-mxd1 99 I MAD31 151 O MAD39 203 O MAD62 255 O DATA56 307 O DATA 48 I MAD08 100 O MAD31 152 E oe-mxd8 204 I MAD63 256 E oe-data7 308 O WES	44	ī	MAD07	96	0	MAD29	148	1	MAD38	200	1	MAD61	252	- 1	DATA57	304	1	DATA33
47 E 0e-mxd1 99 I MAD31 151 O MAD39 203 O MAD62 255 O DATA56 307 O DATA 48 I MAD08 100 O MAD31 152 E 0e-mxd8 204 I MAD63 256 E 0e-data7 308 O WE3	45	0	MAD07	97	Ī	MAD30	149	0	MAD38	201	0	MAD61	253	0	DATA57	305	0	DATA33
48 I MAD08 100 O MAD31 152 E oe-mxd8 204 I MAD63 256 E oe-data7 308 O WE3	46	ε	oe-mxd0	98	0	MAD30	150		MAD39	202		MAD62	254	Ī	DATA56	306	1	DATA32
40 I MINESS TO STATE CONTROL TO STATE OF THE	47	Ē	oe-mxd1	99	1	MAD31	151	0	MAD39	203	0	MAD62	255	0	DATA56	307	0	DATA32
49 O MAD08 101 E oe-mxd6 153 E oe-mxd9 205 O MAD63 257 E oe-data6 309 O WE2	48	1	MAD08	100	0	MAD31	152	E	oe-mxd8	204	1	MAD63	256	E	oe-data7	+		WE3
TO C INTEGE TO THE CONTROL OF THE CO	49	0	MAD08	101	E	oe-mxd6	153	Ε	oe-mxd9	205	0	MAD63	257	E	oe-data6	309	0	WE2
50 I MAD09 102 E oe-mxd7 154 I MAD40 206 E oe-mxd14 258 I DATA55 310 O WE1	50	- 1	MAD09	102	E	oe-mxd7	154		MAD40	206	E	oemxd14	258	1	DATA55	310	0	
51 O MAD09 103 I MERR 155 O MAD40 207 E oemxd15 259 O DATA55 311 O WEC	51	0	MAD09	103		MERR	155	0	MAD40	207	E	oemxd15	259	0	DATA55	311	0	WE0
52 I GTLREF1 104 O MERR 156 I MAD41 208 I BCLK 260 I DATA54 312 E 0e-w	52	1	GTLREF1	104	0	MERR	156	ı	MAD41	208	1	BCLK	260	1	DATA54	312	E	oe-we0
313 E oe-dpar1 343 O ADDR18 373 E oe-addr0 403 I CSA 433 O DATA06 462 O DATA	313	E	oe-dpar1	343	0	ADDR18	373	Ε	oe-addr0	403	1	CSA	433	0	DATA06	462	0	DATA20
314 DPAR3 344 ADDR17 374 ADDR03 404 LDST 434 DATA07 464 DATA	314	1	DPAR3	344	I	ADDR17	374	ŀ	ADDR03	404	1	LOST	434		DATA07	464	1	DATA21



TABLE 10: Boundary Scan Bit Order In MBus Mode (Continued)

315	0	DPAR3	345	0	ADDR17	375	0	ADDR03	405	1	CCHBL	435	0	DATA07	465	0	DATA21
316	ı	DPAR2	346		ADDR16	376	. 1	ADDR02	406	Ε	oe-dipar0	436	E	oe-data0	466	1	DATA22
317	0	DPAR2	347	0	ADDR16	377	. 0	ADDR02	407	-	DPAR4	437	E	oe-data i	467	0	DATA22
318	1	DPAR1	348	ŀ	ADDR15	378	- 1	ADDR01	408	0	DPAR4	438	. 1	DATA08	468	1	DATA23
319	0	DPAR1	349	0	ADDR15	379	0	ADDR01	409	1	DPAR5	439	0	DATA08	469	0	DATA23
320	ı	DPAR0	350	-	ADDR14	380	1	ADDR00	410	0	DPAR5	440	1	DATA09	470	E	oe-data2
321	0	DPARO	351	0	ADDR14	381	0	ADDR00	411	1	DPAR6	441	0	DATA09	471	E	oe-data3
322	0	RESET	352	_	ADDR13	382		ŌĒ.	412	0	DPAR6	442	11	DATA10	472	I.	DATA24
323	0	WEE	363	0	ADDR13	383	0	ŎĒ.	413	1	DPAR7	443	0	DATA10	473	٥	DATA24
324	ı	SIZE1	354	1	ADDR12	384	E	oe-oe	414	0	DPAR7	444	ı	DATA11	474		DATA25
325	ı	SIZE0	355	0	ADDR12	385		WR	415	0	WE4	445	0	DATA11	475	0	DATA25
326	1	ERROR	356	E	oe-addri	386	0	WA	416	0	WE5	446	1	DATA12	476	1	DATA26
327	1	SU	357	1	ADDR11	387	E	Qe-Wr	417	0	WE6	447	0	DATA12	477	0	DATA26
328		SYNC	358	0	ADDR11	388	t	RID	418	0	WE7	448	1	DATA13	478	1	DATA27
329	I	ADDR20	359	1	ADDR10	389	1	BURST	419	Ε	oe-we1	449	0	DATA13	479	0	DATA27
330	٥	ADDR20	360	0	ADDR10	390	0	RETRY	420	1	DATA00	450	ı	DATA14	480	- 1	DATA28
331	ı	ADDR23	361	1	ADDR09	391	0	PEND	421	0	DATA00	451	0	DATA14	481	0	DATA28
332	0	ADDR23	362	0	ADDR09	392	0	MEXC	422	1	DATA01	452	1	DATA15	482	1	DATA29
333	ı	ADDR22	363	j.,	ADDR08	393	0	WRDY	423	0	DATA01	453	0	DATA15	483	0	DATA29
334	0	ADDR22	364	٥	ADDR08	394	0	ARDY	424	1.3	DATA02	454	J	DATA16	484	J	DATA30
335	-	ADDR21	365		ADDR07	395	0	WGRT	425	0	DATA02	455	0	DATA16	485	0	DATA30
336	0	ADDR21	366	0	ADDR07	396	0	AGAT	426	1	DATA03	456		DATA17	486	1	DATA31
337	- 1	ADDR20	367		ADDR06	397		CIMIDS	427	0	DATA03	457	0	DATA17	487	0	DATA31
338	0	ADDR20	368	0	ADDR06	398	0	CMDS	428	1	DATA04	458	1	DATA18			
339	ш.	oe-addr2	369	1	ADDR05	399	Ε	oe-cmds	429	0	DATA04	459	0	DATA18			
340	1	ADDR19	370	0	ADDR05	400	ı	DEMAP	430		DATA05	460	1	DATA19			
341	0	ADDR19	371		ADDR04	401	0	DEMAP	431	0	DATA05	461	0	DATA19			
342		ADDR18	372	0	ADDR04	402	E	oe-dmap	432	\Box	DATA06		1	DATA20			

TABLE 11: Boundary Scan Bit Order in XBus Mode

1 MSSES 53 1 XDATALO 106 E Ge-HWAT 157 O XDATALO 209 I PLENTY 281 O DATACA		:						٠										
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7. O LDRAS 59 1 XDRAS 111 1 XPARS 164 1 XDRAS 125 1 ADDRES 557 O DRAS 8 1 DDRAM 60 0 XDRAS 120 XPARS 164 1 XDRAS 164 1 XDRAS 165 0 XDRAS XDRAS 0 XDRAS XDRAS XDRAS 0 XDRAS XDR		ī		_			_											
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9 O LILATAM 61 I I XIATAM 113 E 0-0-ppr 165 O XIATAM 217 O ADDRES 269 O DATAM 111 O I I LILATAM 2 O XIATAM 114 I XIATAM 216 I XIATAM 218 I ADDRES 271 O DATAM 111 O LILATAM 3 63 I XIATAM 114 I XIATAM 216 I XIATAM 219 O ADDRES 271 O DATAM 112 I LILATAM 3 63 I XIATAM 115 I D XIA	$\overline{}$									_			$\overline{}$					
10 LIDATAS 52 O XDATA14 114 11 \$\frac{114}{115} \] 15 O \$\frac{114}{115} \] 16 I XDATA16 218 I ADOPRES 271 O XDATA96 218 O XDATA96 219 O XDATA96 219 O XDATA96 219 O XDATA96 219 O XDATA97 227 I XDATA96 219 O XDATA97 227 I XDATA96 218 O XDATA97 228 I XDATA96 227 I XDATA96 228 I XDA										-	<u> </u>					_		
11 O LDATA3 S3 I XDATA15 115 O XPECDIQ 167 O XDATA46 219 O ADDRES 271 O DATA46 130 O LDATA2 66 E oe-mid2 117 I XPECDIQ 100 O XDATA47 221 O ADDRES 271 O DATA46 141 I LDATA1 66 E oe-mid2 117 I XPECDIQ 170 E oe-mid47 221 O ADDRES 273 O DATA46 141 I LDATA1 66 E oe-mid2 118 O XPECDIQ 170 E oe-mid47 221 O ADDRES 275 O DATA46 141 I LDATA1 67 I XDATA16 130 I XPECDIQ 170 E oe-mid41 223 O ADDRES 275 O DATA46 161 I LDATA0 68 O XDATA16 120 I XPECDIQ 172 I XDATA6 223 O ADDRES 275 O DATA46 161 I LDATA0 68 O XDATA16 120 I XPECDIQ 172 I XDATA66 224 I ADDRES 277 O DATA46 181 I XDATA16 120 I XPECDIQ 172 I XDATA66 225 O ADDRES 277 O DATA46 181 E Oe-bb-dt 70 O XDATA17 122 O XPECDIQ XPE				_													-	
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22 O LCMD1 74 O XDATA19 128 I XRECZ(0) 178 I XDATA51 230 O ADDR31 282 I DATA43 23 I LCMD0 75 I XDATA20 128 I XRECZ(1) 178 I XDATA51 231 I ADDR32 283 O DATA43 24 O LCMD0 76 O XDATA20 128 I XRECZ(1) 180 I XDATA52 322 O ADDR32 284 I DATA42 25 O CČERR 77 I XDATA20 128 I XRECZ(1) 181 O XDATA52 322 O ADDR32 284 I DATA42 26 E G G-BETT 78 O XDATA21 130 O XDATA51 181 O XDATA52 233 I ADDR33 285 O DATA41 27 I Spare-in 79 I XDATA22 131 I XGNTT 183 O XDATA52 231 I ADDR33 285 O DATA41 28 O Spare-out 80 O XDATA21 130 O XGNTT 183 O XDATA53 234 O ADDR34 286 I DATA41 28 O Spare-out 80 O XDATA22 131 XGNTT 183 O XDATA54 236 I ADDR34 287 O DATA41 29 I RSTIN 81 I XDATA22 133 I XGNTT 184 I XDATA54 236 O ADDR34 288 I DATA40 30 I XDATA00 82 O XDATA23 134 O XGNTS 186 I XDATA55 238 O ADDR35 280 O DATA41 31 O XDATA00 83 E G-EMS4 135 O XGNTS 187 O XDATA55 239 I PCLK 291 E G-Edata5 31 O XDATA01 86 I XDATA24 137 O XDATA32 188 E G-EMS4 1 DATA55 230 I DATA63 32 I XDATA01 86 I XDATA24 137 O XDATA32 189 E G-EMS4 1 DATA62 291 I DATA36 33 O XDATA01 86 I XDATA25 140 I XDATA25 189 E G-EMS4 1 DATA62 295 I DATA36 34 I XDATA03 88 I XDATA25 140 I XDATA25 140 I XDATA55 240 I DATA36 280 I DATA36 35 O XDATA03 88 I XDATA26 140 I XDATA26 140 I XDATA55 240 I DATA62 295 O DATA36 36 I XDATA03 88 I XDATA26 140 I XDATA26 140 I XDATA56 241 I DATA36 280 I DATA36 37 O XDATA03 88 I XDATA26 140 I XDATA36 190 I XDATA56 241 I DATA62 295 O DATA36 38 I XDATA06 90 O XDATA26 140 I XDATA36 190 I XDATA56 241 I DATA61 296 I DATA36 39 O XDATA01 86 I XDATA26 140 I XDATA36 190 I XDATA56 241 I DATA66 290 I DATA36 30 I XDATA00 80 I XDATA26 140 I XDATA36 190 I XDATA56 241 I DATA66 290 I DATA36 31 I XDATA06 90 O XDATA26 140 I XDATA36 190 I XDATA56 241 I DATA66 290 I DATA36 31 I XDATA06 90 O XDATA26 140 I XDATA36 190 I XDATA56 241 I DATA66 290 I DATA36 31 I XDATA06 90 O XDATA26 140 I XDATA36 190 I XDATA56 241 I DATA56 300 I DATA36 31 I XDATA06 90 O XDATA26 140 I XDATA36 190 O XDATA56 241 I DATA56 300 I DATA36 31 I XDATA06 90 O XDATA27 144 I XDATA38 190 O XDATA56 240 I DATA56 300 I DAT							_			_								
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24 O LCMOD 76 O XDATA20 128 I XREGSIO 180 I XDATAS2 232 O ADDR32 284 I DATA42 25 O CÖERR 77 I XDATA21 129 I XREGSI 181 O XDATAS2 233 I ADDR33 285 O DATA42 26 E o-e-earr 78 O XDATA21 139 O XREGSI 181 O XDATAS2 233 I ADDR33 286 I DATA41 27 I SQUEEN 79 I XDATA22 131 I XGATTA 183 O XDATAS3 234 O ADDR33 286 I DATA41 28 O squee-out 80 O XDATA22 131 I XGATTA 183 O XDATAS3 235 I ADDR34 287 O DATA41 28 O SQUEE-OUT 80 O XDATA22 132 O XGATT 184 I XDATAS3 235 I ADDR34 287 O DATA41 28 I RSTIN 81 I XDATA22 133 I XGATT 184 I XDATA54 236 O ADDR34 287 O DATA40 30 I XDATA00 82 O XDATA22 131 I XGATT 185 O XDATA54 237 I ADDR35 289 O DATA40 30 I XDATA00 82 O XDATA23 134 O XGATT 185 O XDATA55 238 O ADDR35 280 E O-clusted 31 O XDATA01 84 E O-e-mod 136 O XGATA22 188 E O-emod 12 240 I DATA63 292 I DATA63 33 O XDATA01 85 I XDATA02 136 I XDATA22 188 E O-emod 13 24 I DATA63 292 I DATA63 34 I XDATA00 85 I XDATA24 137 O XDATA32 188 E O-emod 13 241 O DATA63 293 I DATA63 35 O XDATA01 85 I XDATA24 138 I XDATA33 190 I XDATA56 242 I DATA62 295 O DATA38 36 I XDATA03 88 O XDATA24 138 I XDATA34 192 I XDATA57 244 I DATA62 296 O DATA38 37 O XDATA04 90 O XDATA25 140 I XDATA34 192 I XDATA57 244 I DATA61 296 I DATA63 38 I XDATA04 90 O XDATA26 141 O XDATA35 194 I XDATA57 244 I DATA61 296 I DATA63 39 O XDATA04 91 I XDATA26 144 I XDATA34 192 I XDATA57 244 I DATA61 296 I DATA63 39 O XDATA04 91 I XDATA26 144 I XDATA36 194 I XDATA57 244 I DATA61 296 I DATA63 39 O XDATA04 91 I XDATA26 144 I XDATA36 195 I XDATA58 249 O DATA69 299 O DATA36 40 I XDATA06 93 I XDATA27 144 I XDATA36 196 I XDATA57 244 I DATA61 296 I DATA63 39 O XDATA06 91 I XDATA27 143 O XDATA36 197 O XDATA58 249 O DATA69 299 O DATA36 40 I XDATA06 93 I XDATA26 144 I XDATA36 196 I XDATA57 244 I DATA61 296 I DATA63 39 O XDATA06 91 I XDATA27 144 I XDATA36 196 I XDATA58 246 I DATA66 296 I DATA67 40 I XDATA06 93 I XDATA28 145 O XDATA36 197 O XDATA58 249 O DATA68 30 O I DATA68 40 I XDATA06 93 I XDATA28 145 O XDATA36 197 O XDATA58 249 O DATA66 30 O I DATA66 30 O I DATA65 41 I XDATA06 90 O XDATA28 146 I XDAT	_									_								
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44 I XDATA07 96 O XDATA29 148 I XDATA38 200 I XDATA61 252 I DATA57 304 I DATA33 45 O XDATA07 97 I XDATA30 149 O XDATA38 201 O XDATA61 253 O DATA57 306 O DATA33 46 E oe-mxd0 98 O XDATA30 150 I XDATA39 202 I XDATA62 254 I DATA56 306 I DATA32 47 E oe-mxd1 99 I XDATA31 151 O XDATA39 203 O XDATA62 255 O DATA56 307 O DATA32 48 I XDATA08 100 O XDATA31 152 E oe-mxd8 204 I XDATA63 256 E oe-deta63 309 O WE3 <					0					_				-				
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48 I XIDATA08 100 O XIDATA31 152 E oe-mxd8 204 I XIDATA63 256 E oe-data6 309 O WE3 49 O XIDATA08 101 E oe-mxd6 153 E oe-mxd9 205 O XIDATA63 257 E oe-data6 309 O WE2 50 I XIDATA09 102 E oe-mxd7 154 I XIDATA40 206 E oemxd14 258 I DATA55 310 O WE1 51 O XIDATA09 103 I XIPARO 155 O XIDATA40 207 E oemxd15 259 O DATA55 311 O WE1 52 I GTLREF1 104 O XPARO 156 I XDATA41 208 I BCLK 260 I DATA55 311 O WE0 3				 		 			+								1	
49 O XDATA08 101 E 0e-mxd6 153 E 0e-mxd9 205 O XDATA63 257 E 0e-data6 309 O WE2 50 I XDATA09 102 E 0e-mxd7 154 I XDATA40 206 E 0emxd14 258 I DATA55 310 O WE1 51 O XDATA09 103 I XPAR0 155 O XDATA40 207 E 0emxd15 259 O DATA55 311 O WE0 52 I GTLREF1 104 O XPAR0 156 I XDATA41 208 I BCLK 260 I DATA54 312 E 0e-we0 313 E 0e-dpar1 343 O ADDR18 373 E 0e-addr0 403 I CSA 433 O DATA06 462 O DATA20 314 I DPAR3 344 I ADDR17 374 I ADDR03 404 I LDST 434 I DATA07 464 I DATA21 315 O DPAR3 345 O ADDR17 375 O ADDR03 405 I CCHBL 435 O DATA07 465 O DATA21		E		-	<u> </u>										 			
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52 GTLREF1 104 O XPARO 156 XDATA41 208 BCLK 260 DATA54 312 E oe-we0 313 E oe-dper1 343 O ADDR18 373 E oe-addr0 403 CSA 433 O DATA06 462 O DATA20 314 DATA3 344 ADDR17 374 ADDR03 404 LDST 434 DATA07 464 DATA21 315 O DATA3 345 O ADDR17 375 O ADDR03 405 CCHBL 435 O DATA07 465 O DATA21	50	1			E	oe-mxd7	154					oemxd14			DATA55			
313 E 0e-dpar1 343 O ADDR18 373 E 0e-addr0 403 I ČSĀ 433 O DATA06 462 O DATA20 314 I DPAR3 344 I ADDR17 374 I ADDR03 404 I LDST 434 I DATA07 464 I DATA21 315 O DPAR3 345 O ADDR17 375 O ADDR03 405 I ČCHBL 435 O DATA07 465 O DATA21	51	0	XDATA09	103	- 1	XPAR0	155	0	XDATA40	207	E	oemxd15	259	0	DATA55	311	0	WEO
314 ! DPAR3 344 ! ADDR17 374 ! ADDR03 404 ! LDST 434 ! DATA07 464 ! DATA21 315 O DPAR3 345 O ADDR17 375 O ADDR03 405 ! CCHBL 435 O DATA07 465 O DATA21	52	1	GTLREF1	104	0	XPARO	156		XDATA41	208	I		260	l I	DATA54	312	E	oe-we0
315 O DPAR3 345 O ADDR17 375 O ADDR03 405 I CCHBL 435 O DATA07 465 O DATA21	313	E	oe-dpar1	343	0	ADDR18	373	E	oe-addr0	403	Ī		433	0	DATA06	462	0	DATA20
	314		DPAR3	344		ADDR17	374	1	ADDR03	404	1	LDST	434	Ī	DATA07	464		DATA21
316 I DPAR2 346 I ADDR16 376 I ADDR02 406 E oe-dipar0 436 E oe-data0 466 I DATA22	315	0	DPAR3	345	0	ADDR17	375	0	ADDR03	405	1	CCHBL	435	0	DATA07	46 5	O	DATA21
	316	Ĩ.	DPAR2	346		ADDR16	376	1	ADDR02	406	Е	oe-dipar0	436	E	oe-data0	466		DATA22



TABLE 11: Boundary Scan Bit Order in XBus Mode (Continued)

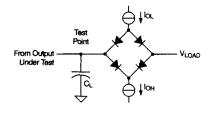
317	0	DPAR2	347	0	ADDR16	377	0	ADDR02	407	1	DPAR4	437	E	oe-data1	467	0	DATA22
318	. 1	DPAR1	348	1	ADDR15	378	I	ADDR01	408	0	DPAR4	438	ı	DATA08	468	I	DATA23
319	0	DPAR1	349	0	ADDR15	379	0	ADDR01	409	-	DPAR5	439	0	DATA08	469	0	DATA23
320	i	DPAR0	350	-	ADDR14	380	Ξ.	ADDR00	410	0	DPAR5	440	Ī	DATA09	470	E	oe-data2
321	0	DPAR0	351	0	ADDR14	381	0	ADDR00	411	ı	DPAR6	441	0	DATA09	471	E	oe-data3
322	0	RESET	352	1	ADDR13	382	1	ŌĒ	412	0	DPAR6	442	. 1	DATA10	472	ı	DATA24
323	0	WEE	353	0	ADDR13	383	0	OE	413		DPAR7	443	0	DATA10	473	0	DATA24
324	1	SIZE1	354	#	ADDR12	384	E	00-00	414	0	DPAR7	444	į	DATA11	474		DATA25
325	- 1	SIZE0	355	0	ADDR12	365	:	WR	415	0	WE4	445	0	DATA11	475	0	DATA25
326	1	ERROR	356	ш	oe-addr1	386	0	WA	416	0	WE5	446		DATA12	476	1	DATA26
327	J	SU	357	-	ADDR11	387	ш	O C-W T	417	0	WE6	447	0	DATA12	477	0	DATA26
328	ı	SYNC	358	0	ADDR11	388	-	RD	418	0	WE7	448	1	DATA13	478		DATA27
329	Ţ.	ADDR20	359		ADDR10	389	_	BURST	419	ш	oe-we1	449	0	DATA13	479	0	DATA27
330	0	ADDR20	360	0	ADDR10	390	0	RETRY	420	1	DATA00	450		DATA14	480	1	DATA28
331	ı	ADDR23	361		ADDR09	391	0	PEND	421	0	DATA00	451	0	DATA14	481	0	DATA28
332	0	ADDR23	362	0	ADDR09	392	0	MEXC	422	-	DATA01	452	1	DATA15	482		DATA29
333	1	ADDR22	363	ļ	ADDR08	393	0	WADY	423	0	DATA01	453	0	DATA15	483	0	DATA29
334	0	ADDR22	364	0	ADDR08	394	0	RRDY	424	1	DATA02	454	1	DATA16	484		DATA30
335	ı	ADDR21	365	1	ADDR07	395	0	WGRT	425	0	DATA02	455	0	DATA16	485	0	DATA30
336	0	ADDR21	366	0	ADOR07	396	0	RGRT	426	1	DATA03	456	1	DATA17	486	I	DATA31
337	ł	ADDR20	367	1	ADDR06	397	-	CMDS	427	0	DATA03	457	0	DATA17	487	0	DATA31
338	0	ADDR20	368	0	ADDR06	398	0	CMDS	428	- 1	DATA04	458	- 1	DATA18	L		
339	E	oe-addr2	369	_	ADDR05	399	E	oe-cmds	429	0	DATA04	459	0	DATA18			
340	ı	ADDR19	370	0	ADDR05	400	1	DEMAP	430	Ī	DATA05	460	1	DATA19			
341	0	ADDR19	371	1	ADDR04	401	0	DEMAP	431	0	DATA05	461	0	DATA19			
342	1	ADDR18	372		ADDR04	402	F	oe-dmac	432	1	DATA06		Ī	DATA20			

PARAMETER MEASUREMENT

TTL Parameters

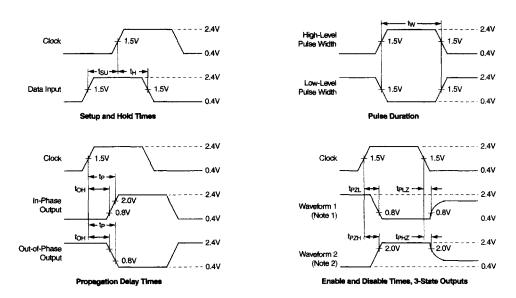
Load Circuit Parameters

t _{en}	tpzH	35	2.0	-370	2.25
	₹PZ1.				
t _{otis}	PHZ	35	2.0	-370	2.25
	t PLZ				
t _{PO}		35	2.2	-2.0	2.25
tpo(MSH)		35	8.0	-2.0	2.25



1. CLOAD includes probes and test fixture capacitance.

Figure 28. TTL Load Circuit and Parameters



- 1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
- Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. For t_{PLZ} and t_{PHZ}, V_{OL} and V_{OH} are specified values.

Figure 29. TTL Voltage Waveforms



GTL Parameters

Load Circuit Parameters

• •					
t _{en}	tеzн	35	36	10	1.2
	tPZL.				
t _{dis}	tpHZ	35	36	10	1.2
	t _{PLZ}].			
tPD		_	36	10	1.2

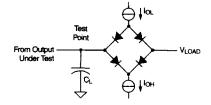
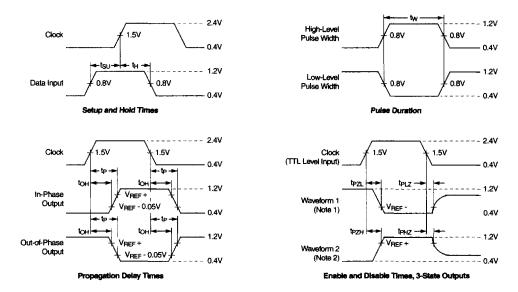


Figure 30. GTL Load Circuit and Parameters



- 1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
- Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. For t_{PLZ} and t_{PHZ}, V_{OL} and V_{OH} are specified values.

Figure 31. GTL Voltage Waveforms

^{1.} CLOAD includes probes and test fixture capacitance.

PIN ASSIGNMENTS

MBus Pinouts

				•									- 1000 - 1000	a ness. Meter	in analoses
A9	RETRY	E5	WE7	H6	VCCI	N1	DATA18	V34	ADDR28	AD32	ADDR29	AJ11	MAD19	AM12	MAD28
111	VCCP	E7	WE5	Н8	WE	N3	DATA24	W1	LIDATA1	AD34	VCCPX	AJ13	MAD24	AM14	VSSC
113	ŌĒ	E9	DPAR7	H10	VSSP	N5	DATA14	wз	DATA29	AE1	VSSPX	AJ15	MAD30	AM16	MAS
4 15	VSSP	E11	DEMAP	H12	CCHBL	N7	DATA11	W5	DATA31	AE3	SPARE	AJ17	MIH	AM18	VSSPX
A17	ADDR05	E13	WRDY	H14	VSSC	N29	DATA49	W7	MX	AE5	TCK	AJ19	N.C.	AM20	MIDO
A19	ADDR09	E15	WA	H16	ADDR00	N31	DATA47	W29	VSSCKP	AE7	MAD01	AJ21	GTLREF1	AM22	VSSC
A21	VSSP	E17	ADDR03	H18	VCCP	N33	DATA48	W31	VCCI	AE29	VCCCKB	AJ23	MAD42	AM24	MAD40
A23	ADDR15	E19	ADDR11	H20	ADDR18	N35	DATA	W33	ADDR27	AE31	IRL0	AJ25	MAD47	AM26	vccc
A25	VCCP	E21	ADDR16	H22	VSSC	P2	DATA22	W35	VCCP	AE33	ADDR26	AJ27	MAD52	AM28	MAD51
A27	SYNC	E23	ADDR22	H24	DPAR01	P4	VSSC	Y2	VSSPX	AE35	ADDR30	AJ29	MAD56	AM30	VSSPX
B8	VSSC	E25	SIZE1	H26	VSSP	P6	DATA16	Y4	MIRLO	AF2	TMS	AJ31	MAD60	AM32	IRL1
B10	CMDS	E27	DPAR2	H28	DATA33	P8	VSSP	Y6	vccc	AF4	vccc	AJ33	MAD61	AN5	TDIODE
B12	VSSP	E29	WEO	H30	VCCI	P28	VSSP	Y8	N.C.	AF6	MAD02	AK4	VSSC	AN7	MAD14
B14	AD	E31	DATA32	H32	DATA36	P30	DATA50	Y28	VCCCKP	AF8	vssc	AK6	MAD06	AN9	MAD21
B16	VCCP	F4	VSSC	H34	VSSP	P32	VSSC	Y30	VCCP	AF28	MAD58	AK8	VSSI	AN11	MAD26
B18	ADDR08	F6	VCCP	J1	DATA08	P34	DATA52	Y32	PLLBYP	AF30	MAD59	AK10	MAD20	AN13	MERR
B20	VCCP	F8	VSSI	JЗ	DATA15	RI	VCCP	Y34	VCCC	AF32	vccc	AK12	VCCPX	AN15	MBB
B22	ADDR17	F10	DPAR06	J5	DATA03	FI3	DATA30	AA1	VCCPX	AF34	ADDR25	AK14	MAD29	AN17	N.C.
B24	VSSP	F12	VSSP	J7	DATA01	R5	DATA20	AA3	MIRL2	AG1	TDI	AK16	vccc	AN19	MID3
B26	ADDR20	F14	MEXC	J29	DATA35	R7	DATA17	AA5	LDATA2	AG3	ASTIN	AK18	N.C.	AN21	N.C.
B28	VSSC	F16	vccc	J31	DATA37	R29	DATA54	AA7	LCMD2	AG5	MAD00	AK20	VCCC	AN23	MAD36
C7	DPAR4	F18	ADDR07	J33	DATA38	R31	DATA53	AA29	BPLLRC	AG7	MAD05	AK22	MAD37	AN25	MAD41
C9	CSA	F20	vccc	J35	DATA42	R33	DATA56	AA31	ADDR34	AG29	VSSC	AK24	VCCPX	AN27	MAD45
C11	WGRT	F22	ADDR21	К2	DATA12	R35	VCCP	AA33	DATA63	AG31	MAD63	AK26	MAD49	AN29	MAD53
C13	PEND	F24	VSSP	K4	vccc	T2	VSSP	AA35	DATA61	AG33	IRL3	AK28	VSSI	AP8	PMC2
C15	ADDR01	F26	RESET	К6	DATA7	T4	DATA23	AB2	N.C.	AG35	ADDR24	AK30	MAD55	AP10	MAD25
C17	ADDR06	F28	VSSI	К8	vssc	Т6	vccc	AB4	VSSC	AH2	VSSPX	AK32	VSSC	AP12	VSSPX
C19	ADDR10	F30	VCCP	K28	VSSC	Т8	DATA21	AB6	MID1	AH4	MAD03	AL3	TEST	AP14	MAD23
C21	ADDR14	F32	VSSC	K30	DATA39	T28	DATA55	AB8	VSSPX	AH6	VCCI	AL5	MAD10	AP16	VCCPX
C23	ADDR19	G3	DATA02	K32	VCCC	T30	VCCP	AB28	VCCC	AH8	MAD09	AL7	MAD12	AP18	РМС3
C25	SŪ	G5	DATA05	K34	DATA43	T32	DATA57	AB30	ADDR31	AH10	VSSPX	AL9	MAD17	AP20	VCCPX
C27	ERROR	G7	DATA00	L1	VSSP	T34	VSSP	AB32	VSSC	AH12	MAD18	AL11	MAD11	AP22	MAD34
C29	DPAR3	G9	WE4	L3	DATA19	U1	MIRL1	AB34	ADDR35	AH14	VSSC	AL13	MAD13	AP24	VSSPX
D4	N.C.	G11	DPAR5	L5	DATA10	UЗ	DATA25	AC1	AERA	AH16	MRDY	AL15	MRTY	AP26	MAD44
D6	VSSP	G13	RGRT	L7	DATA04	U5	DATA27	AC3	N.C.	AH18	VCCPX	AL17	PMC0	AP28	vssc
D8	LDST	G15	BURST	L29	DATA40	U7	DATA26	AC5	MID2	AH20	MAD32	AL19	MBR	AP30	PMC1
D10	vccc	G17	ADDR04	L31	DATA44	U29	PCLK	AC7	TRST	AH22	VSSC	AL21	MAD33	AR9	MAD22
D12	RRDY	G19	ADDR13	L33	DATA45	U31	DATA60	AC29	MCLK	AH24	MAD46	AL23	MAD38	AR11	VCCPX
D14	VSSC	G21	ADDR20	L35	VSSP	U33	DATA59	AC31	ADDR32	AH26	VSSPX	AL25	MAD39	AR13	MAD15
D16	ADDR02	G23	SIZE0	M2	VCCP	U35	DATA58	AC33	ADDR33	AH28	MAD54	AL27	MAD50	AR15	MAD27
D18	VSSP	G25	DPAR0	M4	DATA13	V2	MIRL3	AC35	VSSPX	AH30	VCCI	AL29	MAD48	AR17	MBG
D20	ADDR12	G27	WE1	M6	VSSP	V4	VSSI	AD2	VCCPX	AH32	MAD62	AL31	MAD57	AR19	MSH
D22	VSSC	G29	WE2	M8	DATA06	V6	DATA28	AD4	TDO	AH34	VSSPX	AL33	IRL2	AR21	N.C.
D24	ADDR23	G31	WE3	M2B	DATA41	V8	VCCI	AD6	VSSPX	AJ3	MAD07	AM4	TDIODE0	AR23	MAD35
D26	vccc	G33	DATA34	M30	VSSP	V28	PPLLEC	AD8	GTLREF	AJ5	MAD04	AM6	VSSPX	AR25	VCCPX
D28	WEE	H2	VSSP	M32	DATA46	V30	DATA62	AD28	VSSCKB	AJ7	MAD08	AM8	MAD16	AR27	MAD43
D30	VSSP	H4	DATA09	M34	VCCP	V32	VSSI	AD30	VSSPX	AJ9	MAD13	AM10	VCCC		

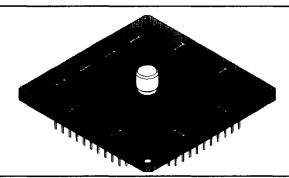


XBus Pinouts

Marine Access	Constitution of the Consti	A941/060	office from a control	. Ser from consti	Le Seu Sédérdo attadés.	22 - 3.2* copy :	S. S. Berger, C. Christeres L. C.	anner namer	125 Table 18 Annual Superior Control of the Land	. 12 [March 46]	100000000000000000000000000000000000000				
M-5-10-10	1988	1.74 Full No. 15	10 mm		o market a		7777		- San						
A9	RETRY	E5	WE7	H6	VCCI	N1	DATA18	V34	ADDR28	AD32	ADDR29	AJ11	XD19	AM12	XD28
A11	VCCP	E7	WE5	H8	WE	N3	DATA24	W1	LDATA1	AD34	VCCPX	AJ13	XD24	AM14	VSSC
A13	ŌĒ	E9	DPAR7	H10	VSSP	N5	DATA14	W3	DATA29	AE1	VSSPX	AJ15	XD30	AM16	XREQ01
A15	VSSP	E11	DEMAP	H12	CCHBL	N7	DATA11	W5	DATA31	AE3	SPARE	AJ17	XREQ10	AM18	VSSPX
A17	ADDR05	E13	WRDY	H14	VSSC	N29	DATA49	W7	MX	AE5	TCK	AJ19	XREQ30	AM20	XGNT2
A19	ADDR09	E15	WR	H16	ADDR00	N31	DATA47	W29	VSSCKP	AE7	XD01	AJ21	GTLREF1	AM22	VSSC
A21	VSSP	E17	ADDR03	H18	VCCP	N33	DATA48	W31	VCCI	AE29	VCCCKB	AJ23	XD42	AM24	XD40
A23	ADDR15	E19	ADDR11	H20	ADDR18	N35	DATA	W33	ADDR27	AE31	IRLO	AJ25	XD47	AM26	VCCC
A25	VCCP	E21	ADDR16	H22	VSSC	P2	DATA22	W35	VCCP	AE33	ADDR26	AJ27	XD52	AM28	XD51
A27	SYNC	E23	ADDR22	H24	DPAR01	P4	VSSC	Y2	VSSPX	AE35	ADDR30	AJ29	XD56	AM30	VSSPX
B8	VSSC	E25	SIZE1	H26	VSSP	P6	DATA16	Y4	LDATA6	AF2	TMS	AJ31	XD60	AM32	IRL1
B10	CMDS	E27	DPAR2	H28	DATA33	P8	VSSP	Y6	VCCC	AF4	VCCC	AJ33	XD61	AN5	TDIODE1
B12	VSSP	E29	WEO	H30	VCCI	P28	VSSP	Y8	LDATA3	AF6	XD02	AK4	VSSC	AN7	XD14
B14	RD	E31	DATA32	H32	DATA36	P30	DATA50	Y28	VCCCKP	AF8	VSSC	AK6	XD06	AN9	XD21
816	VCCP	F4	VSSC	H34	VSSP	P32	VSSC	Y30	VCCP	AF28	XD58	AK8	VSSI	AN11	XD26
B18	ADDR08	F6	VCCP	J1	DATA08	P34	DATA52	Y32	PLLBYP	AF30	XD59	AK10	XD20	AN13	XPAR0
B20	VCCP	F8	VSSI	J3	DATA15	R1	VCCP	Y34	vccc	AF32	VCCC	AK12	VCCPX	AN15	XREQ00
B22	ADDR17	F10	DPAR06	J5	DATA03	R3	DATA30	AA1	VCCPX	AF34	ADDR25	AK14	XD29	AN17	XREQ20
B24	VSSP	F12	VSSP	J7	DATA01	R5	DATA20	AA3	LDATA4	AG1	TDI	AK16	VCCC	AN19	XGNT1
326	ADDR20	F14	MEXC	J29	DATA35	R7	DATA17	AA5	LDATA2	AG3	ASTIN	AK18	XREQ21	AN21	XGNT3
B28	VSSC	F16	VCCC	J31	DATA37	R29	DATA54	AA7	LCMD2	AG5	XD00	AK20	vccc	AN23	XD36
C7	DPAR4	F18	ADDR07	J33	DATA38	R31	DATA53	AA29	BPLLRC	AG7	XD05	AK22	XD37	AN25	XD41
C9	CSA	F20	vccc	J35	DATA42	R33	DATA56	AA31	ADDR34	AG29	VSSC	AK24	VCCPX	AN27	XD45
C11	WGRT	F22	ADDR21	K2	DATA12	R35	VCCP	AA33	DATA63	AG31	XD63	AK26	XD49	AN29	XD53
C13	PEND	F24	VSSP	K4	vccc	T2	VSSP	AA35	DATA61	AG33	IRL3	AK28	VSSI	AP8	PMC2
C15	ADDR01	F26	RESET	K6	DATA7	T4	DATA23	AB2	LCMDS	AG35	ADDR24	AK30	XD55	AP10	XD25
C17	ADDR06	F28	VSSI	К8	vssc	T6	vccc	AB4	VSSC	AH2	VSSPX	AK32	VSSC	AP12	VSSPX
C19	ADDR10	F30	VCCP	K28	VSSC	T8	DATA21	AB6	LCMD1	AH4	XD03	AL3	TEST	AP14	XD23
C21	ADDR14	F32	VSSC	K30	DATA39	T28	DATA55	AB8	VSSPX	AH6	VCCI	AL5	XD10	AP16	VCCPX
C23	ADDR19	G3	DATA02	K32	VCCC	T30	VCCP	AB28	VCCC	AH8	XD09	AL7	XD12	AP18	PMC3
C25	SÚ	G5	DATA05	K34	DATA43	T32	DATA57	AB30	ADDR31	AH10	VSSPX	AL9	XD17	AP20	VCCPX
C27	ERROR	G7	DATA00	Li	VSSP	T34	VSSP	AB32	VSSC	AH12	XD18	AL11	XD11	AP22	XD34
C29	DPAR3	G9	WE4	L3	DATA19	U1	LDATA7	AB34	ADDR35	AH14	vssc	AL13	XD13	AP24	VSSPX
D4	N.C.	G11	DPAR5	L5	DATA10	UЗ	DATA25	AC1	CCERR	AH16	XPAR1	AL15	XPAR2	AP26	XD44
D6	VSSP	G13	RGRT	L7	DATA04	U5	DATA27	AC3	LDATAO	AH18	VCCPX	AL17	PMC0	AP28	VSSC
D8	LDST	G15	BURST	129	DATA40	U7	DATA26	AC5	LCMD0	AH20	XD32	AL19	XGNTO	AP30	PMC1
D10	VCCC	G17	ADDR04	L31	DATA44	U29	PCLK	AC7	TRST	AH22	VSSC	AL21	XD33	AR9	XD22
D12	RADY	G19	ADDR13	L33	DATA45	U31	DATA60	AC29	BCLK	AH24	XD46	AL23	XD38	AR11	VCCPX
D14	VSSC	G21	ADDR20	L35	VSSP	U33	DATA59	AC31	ADDR32	AH26	VSSPX	AL25	XD39	AR13	XD15
D16	ADDR02	G23	SIZE0	M2	VCCP	U35	DATA58	AC33	ADDR33	AH28	XD54	AL27	XD50	AR15	XD27
D18	VSSP	G25	DPARG	M4	DATA13	V2	LDATA5	AC35	VSSPX	AH30	VOCI	AL29	XD48	AR17	XPAR3
D20	ADDR12	G27	WE1	M6	VSSP	V4	VSSI	AD2	VCCPX	AH32	XD62	AL31	XD57	AR19	XREQ11
D22	VSSC	G29	WE2	M8	DATA06	V6	DATA28	AD4	TDO	AH34	VSSPX	AL33	IBL2	AR21	XREQ31
D24	ADDR23	G31	WE3	M28	DATA41	V8	VCCI	AD6	VSSPX	AJ3	XD07	AM4	TDIODE0	AR23	XD35
D26	VCCC	G33	DATA34	M30	VSSP	V28	PPLLRC	AD8	GTLREF	AJ5	XD04	AM6	VSSPX	AR25	VCCPX
D28	WEE	H2	VSSP	M32	DATA46	V30	DATA62	AD28	VSSCKB	AJ7	XD08	AM8	XD16	AR27	XD43
				+						-	· · · · · · · · · · · · · · · · · · ·			AHZ/	AD43
D30	VSSP	H4	DATA09	M34	VCCP	V32	VSSI	AD30	VSSPX	AJ9	XD13	AM10	VCCC		1

PACKAGE DIMENSIONS

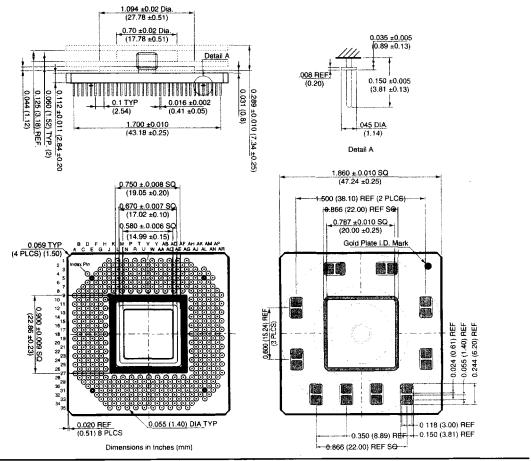
376-Pin PGA Package



Thermal Resistance vs. Air Flow [1] [2]

O.IA	6.8	4.7	3.7	2.5
		AND THE		
				George VI.
MARKET STATE AND A STATE OF THE	Make / As halfun all Maren Seede		SEC. TO SEC. OF SECRETARISTS	COLOR CONTROL CONTROL CONTROL

- T_J can be calculated by: T_J = T_A + P_d x Θ_{JA}
- Thermal resistance measured using the disk-type fin supplied by Texas instruments.





ORDERING INFORMATION [1]

			a contract section	Section 11 and 12 and 1
STP1091PGA-75	75 MHz	Production Parts (for use with SuperSPARC)	· <u> </u>	
STP1091PGA-90	90 MHz	Production Parts (for use with SuperSPARC)	_	
STP1020HS	_	Disk-Fin Type Heat Sink.		, , , , , , , , , , , , , , , , , , , ,

^{1.} Standard parts do not have heat sinks. Heat sinks should be ordered separately.

Document Part Number: STP1091