Crystal Clock Oscillators **NEL**

CMOS Operating Conditions and Output Characteristics

Surface Mount-CMOS
25.1 MHz to 85.0 MHz

HJ-370 Series and
HJ-1420 Series
(Enable/Disable)

HJ-370/HJ-1420 Series

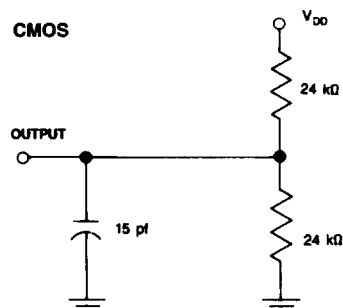| PARAMETER	CONDITIONS	MINIMUM	MAXIMUM
General Characteristics			
Supply voltage	V_{DD} [2]	4.75V	5.25V
	Breakdown	-0.5V	7.0V[1]
Supply current (I_{CC})	No output load @ 100 MHz	- - - - -	- - - - -
HJ-370 Series	- - - -	0.0 mA	50 mA
HJ-1420 Series	- - - -	0.0 mA	40 mA
Output current (I_O)	- - - -	0.0 mA	16mA
Operating temperature (T_A)	- - - -	0°C	70°C
Storage temperature (T_S)	- - - -	-55°C	+125°C
Power dissipation(P_D)	- - - -	- - - - -	450 mW
Lead temperature(T_L)	Soldering, 10s	- - - - -	300°C
Output Characteristics			
Frequency	- - - -	25.1 MHz	85.0 MHz
Tolerance	User specified	±100ppm	- - - - -
Symmetry	@0.5 V_{DD}	40/60%	60/40%
Logic 0 (V_{OL})	Driving equiv. load	- - - - -	0.2V
Logic 1 (V_{OH})	Driving equiv. load	V_{DD}-0.2V	- - - - -
Logic 0 (I_{OL} sink)	Driving equiv. load	- - - - -	600µA
Logic 1 (I_{OH} source)	Driving equiv. load	- - - - -	600µA
Rise & fall time (t_r, t_f)	@10% to 90% of V_{DD}		
	< 40 MHz	N/A	8 ns
	≥ 40 MHz	N/A	6 ns
3-state enable/disable time (t_{pz})	HJ-370	N/A	N/A
	HJ-1420	- - - - -	25 ns

Footnotes:

(1) Overvoltage causes the oscillator to draw extreme current, and damage occurs.

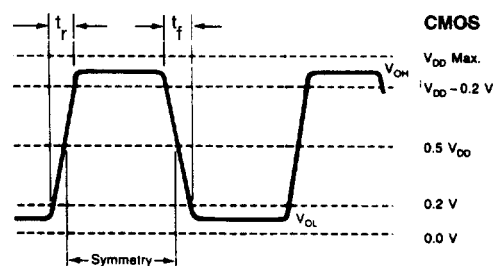(2) Lower voltage operation option to 3V available.

CAUTION:

Permanent damage occurs if reverse voltage is applied to the device from V_{CC}/V_{DD} to ground.

CMOS

V_{DD}

24 kΩ

OUTPUT

15 pf

24 kΩ

Output Waveform

t_r t_f

CMOS

V_{DD} Max.

V_{OH} V_{DD} – 0.2 V
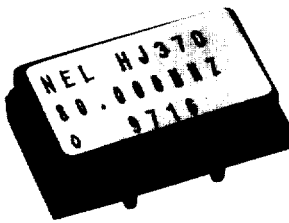
0.5 V_{DD}
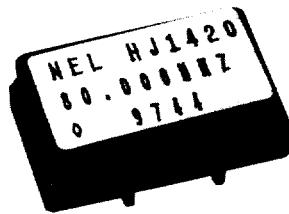
0.2 V

V_{OL} 0.0 V

Symmetry

NEL Crystal Clock Oscillators

Surface Mount-CMOS
25.1 MHz to 85.0 MHz

HJ-370 Series and HJ-1420 Series (Enable/Disable)

HJ-370 Series

HJ-1420 Series

Description

The HJ-370 Series of quartz crystal clock oscillators are general purpose CMOS oscillators (including 4000 series, CMOS, ACMOS, MOS, HCMOS, 74C, 74HC and NMOS).

The HJ-1420 Series of quartz crystal clock oscillators provide enable/disable three-state CMOS compatible signals for bus connected systems. Supplying Pin 1 of the units with a logic "1" enables Pin 3 output. In the disable mode, Pin 3 presents a high impedance to the output.
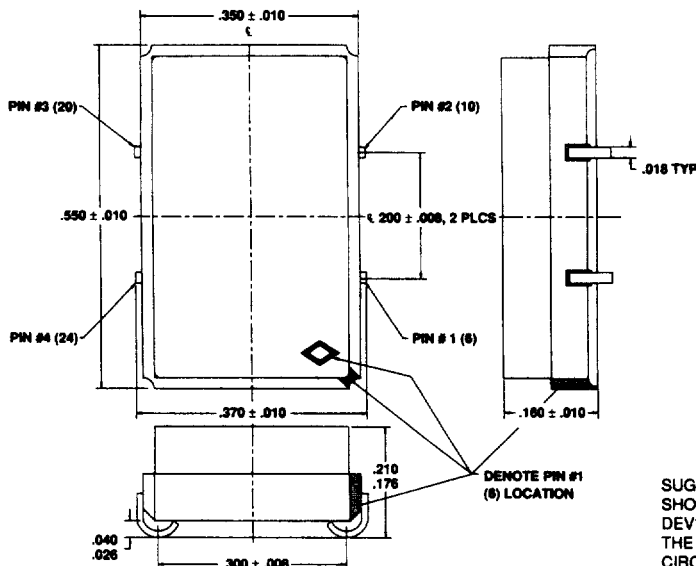
Features

- ☐ Wide frequency range – 25.1 MHz to 85.0 MHz
- ☐ User specified tolerance from ±100ppm
- ☐ Low power consumption
- ☐ Hermetically sealed ceramic SMD package
- ☐ J-lead termination
- ☐ .200" x .300" footprint
- ☐ Solderable at 300°C for 10 seconds
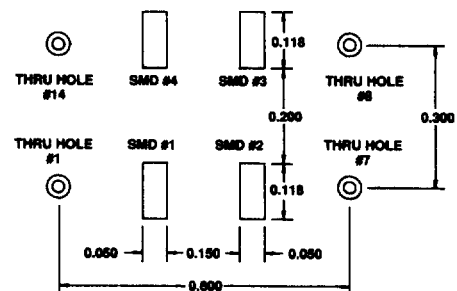- ☐ High shock resistance, to 3000g

NEL TYPE, FREQUENCY RANGE, PIN CONNECTIONS

NEL OSC. TYPE	FREQUENCY RANGE	PIN CONNECTIONS (Jedec/Crystal Industry)				ENABLE	
		6/1	10/2	20/3	24/4	LOG.1	LOG.0
HJ-370	25.1 to 85.0 MHz	N/C	GRD	OUTPUT	V_{DD}	N/A	N/A
HJ-1420	25.1 to 85.0 MHz	EN/DIS.	GRD	OUTPUT	V_{DD}	YES	NO

PACKAGE OUTLINE AND DIMENSIONS

- .350 ± .010
- PIN #3 (20)
- PIN #2 (10)
- .018 TYP
- .550 ± .010
- .200 ± .008, 2 PLCS
- PIN #4 (24)
- PIN # 1 (6)
- .370 ± .010
- .160 ± .010
- .210 / .176
- DENOTE PIN #1 (6) LOCATION
- .040 / .026
- .300 ± .008

SUGGESTED SOLDER PAD LAYOUT

THRU HOLE #14 | SMD #4 | SMD #3 | THRU HOLE #8
THRU HOLE #1 | SMD #1 | SMD #2 | THRU HOLE #7
0.118 | 0.200 | 0.300 | 0.118
0.060 | 0.150 | 0.060 | 0.600

SUGGESTED PAD LAYOUT FOR THE NEL HJ SERIES OF CLOCK OSCILLATORS. ALSO SHOWN IS PLACEMENT OF THE PLATED HOLES FOR A 14 PIN COMPATIBLE THRU HOLE DEVICE. THIS IS NOT INTENDED AS A REQUIREMENT BUT AS A GUIDE TO BE MODIFIED BY THE END USER PER THEIR STANDARD SMD PC BOARD LAYOUT TECHNIQUES FOR RF CIRCUITS. GOOD HIGH FREQUENCY POWER SUPPLY DECOUPLING IS ENCOURAGED.