DN74LS293 N74LS293

4-bit Binary Counters

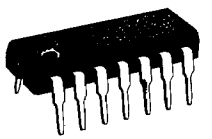
■ Description

DN74LS293 is an asynchronous 4-bit binary (hexadecimal) counter with direct-coupled reset input.

■ Features

- Direct-coupled reset input
- Capability for independent use as binary and octal counters
- High-speed counting (f_{max} = 42MHz typical)
- Wide operating temperature range (Ta = −20 to +75°C)

P-1

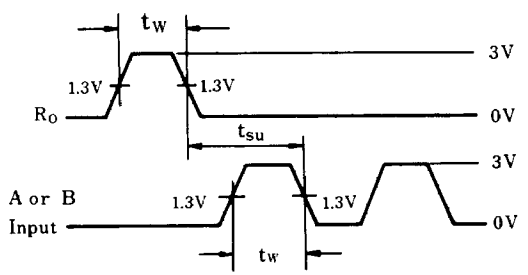


14-pin plastic DIL package

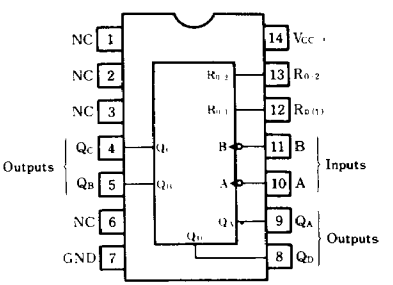
P-4

14-pin Panaflat package (SO-14D)

■ Timing definition



Pin configuration (top view)



■ Absolute maximum ratings

Parameter		Sym.	Rating		Unit
Input voltage	R	V_I	−0.5	7.0	V
	A, B		−0.5	5.5	

* Refer to the family ratings for other parameters.

■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Count frequency	A input	f_{count}	0		32	MHz
	B input		0		16	MHz
Pulse width	A input	t_W	15			ns
	B input		30			ns
	Reset input		15			ns
Set-up time		t_{su}	25			ns

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage**		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
		V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	Any Reset	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	A input						40	μA
	B input						40	μA
	Any Reset	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	A input						−2.4	mA
	B input						−1.6	mA
	Any Reset	I_I	$V_{CC}=5.25V$	$V_I=7V$			0.1	mA
	A input			$V_I=5.5V$			0.2	mA
	B input						0.2	mA
Output short circuit current***		I_{OS}	$V_O=0V$ $V_{CC}=5.25$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				1.5	V
Supply current****		I_{CC}	$V_{CC}=5.25V$			9	15	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** When testing Q_A output, a current to which the rated upper limit value for the I_{IL} of the B input has been added is applied to the specified I_{OL}.

*** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

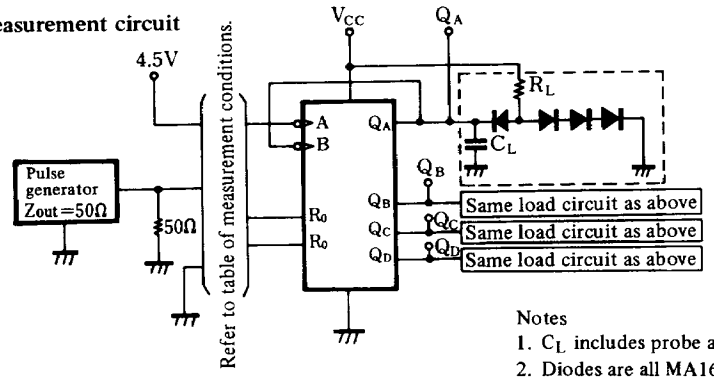
**** I_{CC} is measured with all outputs open and all inputs except both R_O inputs grounded; 4.5V applied momentarily to both R_O inputs, following which they are grounded.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum count frequency	f_{max}	A	Q_A	$C_L=15pF$ $R_L=2k\Omega$	32	42		MHz
		B	Q_B		16			MHz
Propagation delay time	t_{PLH}	A	Q_A			10	16	ns
	t_{PHL}					12	18	ns
	t_{PLH}	A	Q_D			46	70	ns
	t_{PHL}					46	70	ns
	t_{PLH}	B	Q_B			10	16	ns
	t_{PHL}					14	21	ns
	t_{PLH}	B	Q_C			21	32	ns
	t_{PHL}					23	35	ns
	t_{PLH}	B	Q_D			34	51	ns
	t_{PHL}					34	51	ns
	t_{PHL}	Set-to-0	$Q_A \sim Q_D$			26	40	ns

※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

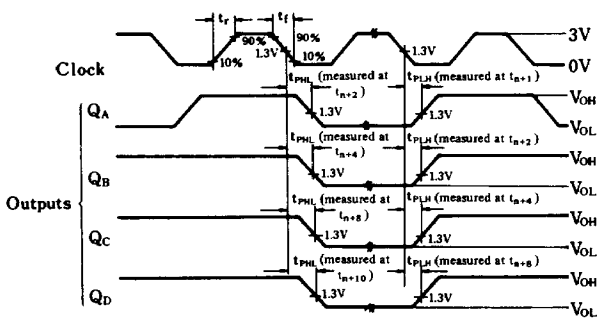
2. Table of measurement conditions

Parameter	Inputs/Outputs	Inputs			Outputs			
		A	B	R_0	Q_A	Q_B	Q_C	Q_D
f_{max}	A →Q	IN	to Q_A	GND	OUT	OUT	OUT	OUT
	B **→Q	4.5V	IN	GND		OUT	OUT	OUT
t_{PLH} t_{PHL}	A →Q_A	IN	to Q_A	GND	OUT			
	A →Q_D	IN	to Q_A	GND				OUT
	B **→Q_B	4.5V	IN	GND		OUT		
	B **→Q_C	4.5V	IN	GND			OUT	
	B **→Q_D	4.5V	IN	GND				OUT
	R_0 →Q	IN *	to Q_A	IN	OUT	OUT	OUT	OUT

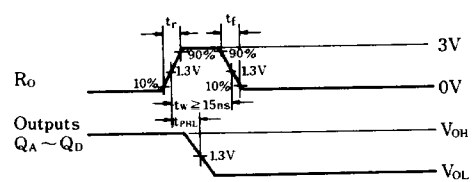
* Applied for initialization.
** For characteristic measurement from B input, Q_A and B are disconnected and pulse is applied to B input.
*** Measured for each input terminal; 4.5V applied to terminals to which input pulse is not applied.

3.Waveforms

Waveforms-1 f_{max}, t_{PLH}, t_{PHL} (Clock → Q)



Waveforms-2 t_{PHL} (R_0 → Q)



Notes 1. $t_r \leqq 15ns$, $t_f \leqq 5ns$

Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$,
PRR = 1MHz, duty cycle = 50%.
2. Pulse generator output impedance: $Z_{out} = 50$ ohms.
3. t_n is the bit time when all outputs are LOW.

■ Truth tables

Reset inputs		Outputs			
$R_{O(1)}$	$R_{O(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	×	Count			
×	L	Couot			

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. Output Q_A is connected to input B and count pulse is applied to input A.

■ Logic diagram