Features

- **Monolithic Dual-Channel 16/18-Bit A/D Converters**
  - **On-Chip Sample/Hold**
  - **Automatic Linearity Error Correction**
- **High Conversion Rates to 96K Samples Per Second at 18 Bits for Each Channel**
- **Capable of Single or Continuous Conversions**
- **Operates from a Single 5 V ± 10% Supply**
- **High Signal-to-Noise Ratio: 90 dB**
- **Single Multiplexed Serial Data Output**
- **High Reliability CMOS Technology**
- **Full Military, Commercial and Industrial Temperature Ranges**

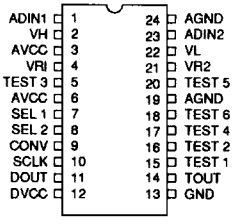
CMOS Dual-Channel 16/18-Bit A/D Converters

Description

The AT76C120 provides two complete Analog-to-Digital (A/D) Converters integrated on a monolithic substrate. It is designed for Digital Audio and Signal Processing applications as well as Industrial Control and Datacommunication. The Sample/Hold function is incorporated in both A/D channels. Each channel can independently perform 96K 18-Bit conversions per second. The AT76C120 needs a minimum of external components and provides a simple and cost effective solution for applications requiring high resolution A/D conversion.

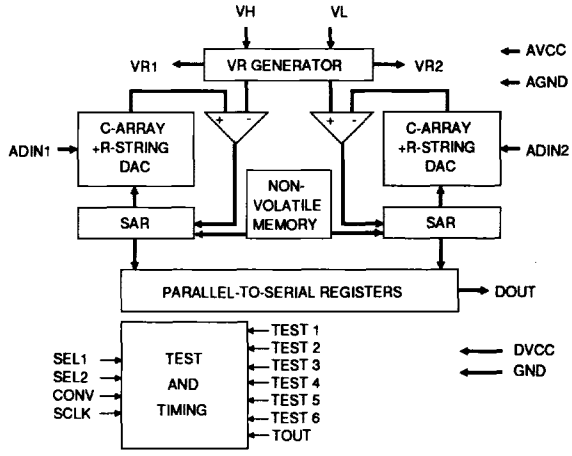
The AT76C120 is fabricated in a state-of-the-art, low power CMOS process and operates from a single 5 V supply. A modified successive approximation algorithm is used to optimize conversion speed. The AT76C120 can perform a single conversion at random or continuous conversions. Linearity errors caused by tap weight variations are automatically compensated by adding a correction factor to each A/D conversion result. The optimum correction factors are factory programmed into each individual chip. The digital output code is presented serially, in 2's complement format.

Pin Configuration



Pin Name	Function
AGND, GND	Analog Ground, Ground
ADIN1	Analog Input for Channel-1
ADIN2	Analog Input for Channel-2
AVCC	+5 V Analog Supply Input
DOUT	Digital Data Output
DVCC	+5 V Digital Supply Input
CONV	Convert Clock Input
SCLK	System Clock Input
SEL1	DOUT Mode Select Input
SEL2	16/18-Bit Mode Select Input
TEST 1,2,3,4,5,6	Test Inputs
TOUT	Test I/O
V_H,V_L	Reference Voltage Inputs
VR1,VR2	Channel-1,-2 Reference Voltage Outputs

Block Diagram



Device Operation

Each analog input to the AT76C120 is sampled and held simultaneously once every CONV clock period. As shown in the block diagram, the AT76C120 uses a combination of binary ratioed double-polysilicon Capacitor Arrays and Resistor String networks to generate the analog decision levels (or tap weights). The Capacitor Arrays also provide the internal Sample-and-Hold function. A high-gain auto-zeroed Comparator is used to compare an analog input with the decision levels. The Vr Generator supplies internal reference voltages equal to (VH + VL)/2 used by the comparators.

A/D conversion is accomplished through 18-bit Successive Approximation Registers (SARs). An improved successive approximation scheme is used to optimize conversion speed. The A/D output codes are stored in Parallel-to-Serial Shift Registers and are available at a single multiplexed serial data output port.

System Clock input, SCLK, provides the internal timing reference and the Convert Clock, input CONV, initiates an A/D conversion. The Test and Timing circuits shown in the block diagram generate all the timing control signals from SCLK and CONV for sample-and-hold, A/D conversion and tap weight error correction during normal operation as well as tap weight error calibration at the factory.

A minimum of 64 SCLK clock cycles are required for one A/D conversion. The maximum SCLK clock frequency is 6.144 MHz. The minimum 18-bit conversion time for each channel is 10.4 µs, which corresponds to a maximum conversion rate of 96 kHz, making 2X sampling in Digital Audio applications possible.

To minimize overall system cost while achieving high resolution, the AT76C120 compensates for linearity errors caused by tap weight variations by adding a correction factor to each A/D conversion result. This operation is done automatically without the intervention of the host processsor. The optimum correction factors are factory programmed into on-chip nonvolatile storage.

The AT76C120 requires only a single 5-volt supply for operation.

System Implementation Considerations

POWER SUPPLY DECOUPLING AND GROUNDING: To obtain the highest performance possible with the AT76C120, critical signal paths, power supply lines and ground planes on the circuit board should be laid out carefully to minimize noise coupling or aliasing into sensitive analog paths. As illustrated in the diagram showing a Sample Connection for Typical Application, a separate AVCC line decoupled to AGND with a tantalum capacitor in parallel with a smaller ceramic chip capacitor should be used for the analog circuits on the AT76C120. Similarly, a separate analog ground return, AGND, which is connected to the most quiet point in the system ground plane, should be used.

For best results, four layer PC boards with separate ground and power supply planes are recommended. The AGND plane should be laid out as an island or tub underneath pins 1 to 6 and pins 19 to 24.

High frequency noise on the power and ground lines can be aliased into the passband by the sampling action of the AT76C120. If a switching power supply has to be used, both AVCC and AGND need to be isolated from the system supplies with inductors of appropriate values.

ANALOG INTERFACE: Due to the high sampling rate of the AT76C120, little if any anti-alias filtering is required for most industrial applications. For high performance Digital Audio applications, external Anti-Alias Lowpass or Bandpass Filters, shown as AAFs' in the Sample Connection diagram, should be used to eliminate signals outside the desired passband. Low noise op amps with low output impedances should also be used to supply the analog inputs.

The A/D full-scale range is determined by the voltage applied across pins VH and VL, i.e. (VH - VL). VL is normally connected to the analog ground, AGND, while VH should be supplied by a stable voltage reference.

The internal reference voltage appearing at output pins VR1 and VR2 is nominally (VH + VL)/2.

If the voltage of the input signal can swing below ground, it is necessary to apply an offset to the input to make the AC ground correspond to the mid point of the full scale range, (VH + VL)/2. Outputs VR1 and VR2 provide the AC ground reference as shown in the diagram for Sample Connection.

SYSTEM TIMING: Internal and output data timing of the AT76C120 are synchronized with the system clock, SCLK. To avoid possible synchronization and aliasing problems, deriving the convert clock, CONV, by dividing SCLK by 64 is recommended.

The AT76C120 samples both analog inputs, ADIN1 and ADIN2, once every CONV period. Both inputs are sampled simultaneously, i.e. in-phase. The AT76C120 then performs an A/D conversin on both samples and returns the two resulting 18-bit codes at the serial data output pin, DOUT, during the following CONV clock period.

The convert clock, CONV, is used inside the AT76C120 to initiate sample-and-hold and can also be used by the host processor to latch in the serial 16-bit or 18-bit wide output data.

DIGITAL INTERFACE: The AT76C120 uses a single multiplexed serial data output pin, DOUT. CH-1 and CH-2 data bits are synchronized with SCLK and are available during either the "High" or the "Low" period of convert clock, CONV. A logic "1" at DOUT Mode Select, SEL1, results in the AT76C120 returning the A/D output of CH-1 during the CONV "Low" period, and CH-2 output during the CONV "High" period. A logic "0" at SEL1 results in CH-1 output during the CONV "High" period and CH-2 output during the CONV "Low" period.

The convert clock, CONV, if equal to SCLK divided by 64, makes a transition from "High" to "Low" or vice versa after the LSB is shifted out of DOUT. This allows the serial data to be easily latched into most popular D/A converters or digital signal processors by using CONV rising or falling edges. To further enhance digital interface compatibility, DOUT Mode Select Input, SEL1, allows the user to choose either CONV transitions for both channels.

The AT76C120 allows the user to choose either 16-bit wide or 18- bit wide A/D outputs in 2's complement format. A logic "1" at 16/18 Mode Select Input, SEL2, returns two 18-bit codes at DOUT, while a logic "0" results in 16-bit output codes at CONV rising or falling edges as shown in Input/Output Timing diagram.

In Digital Audio and many signal processing applications, the A/D outputs are further processed by a digital filter. The 18-bit output mode provides better dynamic range and resolution than 16- bit outputs. However, for applications with a 8-bit or 16-bit host microprocessor, 16-bit wide data are more convenient to manage.

SINGLE CONVERSION MODE: When using the AT76C120 in a single conversion mode, please note that the first 15 SCLK periods in each CONV cycle is used for internal sample-and-hold for both channels CH-1 and CH-2. Since the AT76C120 returns the digital conversion results in a subsequent CONV cycle, two CONV periods are in general required to perform a random A/D conversion.

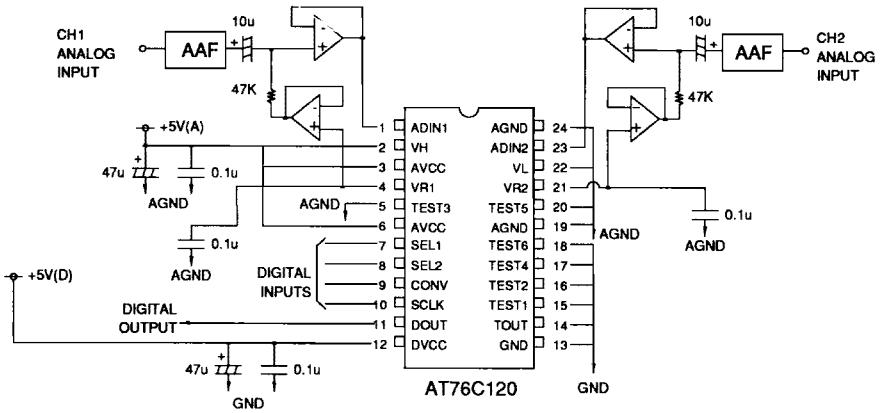
Pin Definitions

	Symbol	Functional Descriptions
Analog Interface	ADIN1 ADIN2	Analog Inputs for Channel-1 (CH-1) and Channel-2 (CH-2). The Sample/Hold function is provided on-chip for both channels. The analog inputs at ADIN1 and ADIN2 are sampled in-phase. Each A/D conversion takes at least 64 SCLK periods.
	V_L V_H	Reference Voltage Inputs. V_L and V_H are normally tied to Analog Ground and the desired full-scale voltage respectively. The full scale range is given by (V_H-V_L). The maximum full-scale voltage can be as high as AVCC.
	VR1 VR2	Reference Voltage Outputs for CH-1 and CH-2. The nominal value at these pins is (V_H+V_L)/2.
Digital Interface	CONV	Convert Clock Input. CONV is normally obtained by dividing the system clock SCLK by 64. The internal Sample/Hold pulse and A/D data output are synchronized with CONV.
	DOUT	Serial Digital Output. DOUT returns two 18-bit serial outputs for CH-1 and CH-2 in 2's complement format. The output data bits are synchronized with SCLK. Please refer to DOUT Timing Diagram for detailed timing relationship with CONV and SCLK.
	SCLK	System Clock Input. The maximum frequency for 18-bit operation is 6.144 MHz. This corresponds to a minimum conversion time of 10.4 µs.
	SEL1	DOUT Mode Select Input. i) SEL1 = "1", CH-1 data output during CONV "Low" CH-2 data output during CONV "High" ii) SEL1 = "0", CH-1 data output during CONV "High" CH-2 data output during CONV "Low"
	SEL2	16/18-Bit Mode Select. i) SEL2 = "1" selects 18-bit A/D mode, ii) SEL2 = "0" selects 16-bit A/D mode.

Pin Definitions (cont'd)

	Symbol	Functional Descriptions
Test Interface	TEST1 TEST2 TEST3 TEST4 TEST5 TEST6	Test Inputs. Normally tied to Ground for TEST 1, 2, 4, 6 and to AGND for TEST 3, 5. These inputs are used for testing and calibration at the factory and are not required for normal A/D operations.
	TOUT	Test I/O. Normally tied to Ground. Like the Test Input pins, this pin is not used for normal A/D operations.
Power Supply	AVCC	Analog Power Input. Nominal 5 Volts. AVCC should be connected to a filtered system supply and kept separate from the Digital Supply.
	DVCC	Digital Power Input. Nominal 5 Volts.
	AGND	Analog Ground. AGND should be kept separate from the digital Ground.
	GND	Digital Ground.

Sample Connection for Typical Application



Notes: 1. AVCC, AGND, +5V (A)— analog supply
2. DVCC, GND, +5V (D)— digital supply
3. Use high quality 0.1-µF ceramic chip capacitors.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to 125°C
Storage Temperature	-65°C to 150°C
Voltage on Any Pin with Respect to AGND and GND	-2.0 V to 7.0 V(1)
Power Dissipation	1 W
Reference Current	10 mA
Analog Input Current	10 mA
DC Digital Output Current	25 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6 V DC which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is AVCC/DVCC+0.75 V DC which may overshoot to 7.0 V for pulses of less than 20 ns.

D.C. and A.C. Operating Range

		AT76C120-1	AT76C120-2	AVCC/DVCC Power Supplies
Operating Temperature Range(Case)	Com.	0° C - 70° C	0° C - 70° C	5 V ± 10%
	Ind.	-40° C - 85° C	-40° C - 85° C	5 V ± 10%
	Mil.	-55° C -125° C	-55° C -125° C	5 V ± 5%

D.C. Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
I_{LI}	Digital Input Load Current	V_{IN} = -0.1 V to DVCC+0.1 V		10	µA
I_{LO}	Digital Output Leakage Current	V_{OUT} = -0.1 V to DVCC+0.1 V		10	µA
I_{CCD}	Digital Supply Current			40	mA
I_{CCA}	Analog Supply Current			10	mA
I_{REF}	Reference Input Current			5	mA
V_{IL}	Digital Input Low Voltage		-0.5	0.8	V
V_{IH}	Digital Input High Voltage		2.2	DVCC+0.5	V
V_{OL}	Digital Output Low Voltage	IO = 5 mA		0.4	V
V_{OH}	Digital Output High Voltage	IO = -5 mA	2.4		V
V_{AIN}	Analog Input Voltage		V_L	V_H	V
V_H	Analog Input Voltage at V_H Pin		AVCC-0.5	AVCC	V
V_L	Analog Input Voltage at V_L Pin		0.0	0.5	V

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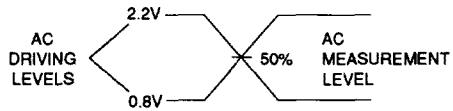
Analog Characteristics (AVCC = DVCC = 5 V, Ta = 25° C)

			AT76C120-1			AT76C120-2			
Symbol	Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Units
RES	A/D Resolution			18			18		bits
ILE	Integral Linearity Error				±0.006			±0.01	% FSR
Fs	A/D Sampling Frequency	18-Bit Mode			96			96	kHz
FSE	Full Scale Error				±0.15			±0.15	% FSR
THD	Total Harmonic Distortion	0dB, 1kHz Input			0.01			0.02	%
		-20dB, 1kHz Input			0.02			0.04	%
		-60dB, 1kHz Input			2			4	%
S/N	Signal-to-Noise Ratio				90			84	dB

Input Test Waveforms



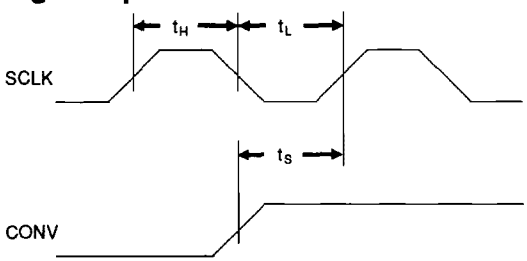
Notes: 1. tR, tF < 30 ns (10% to 90%)
2. Input timing reference is at 1.5 V

Digital Output Codes vs. Analog Inputs

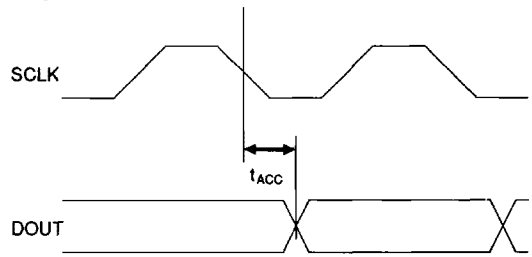
Analog Input	Digital Output Codes MSB...																	...LSB
V_H	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
V_H - 1 LSB[1]	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
:									:									
$(V_H + V_L) / 2 + 1$ LSB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
$(V_H + V_L) / 2$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$(V_H + V_L) / 2 - 1$ LSB	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
:									:									
$V_L + 1$ LSB	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
V_L	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: 1. 1 LSB = $(V_H-V_L)/262$, 144 in 18-bit mode.

Digital Input Waveforms



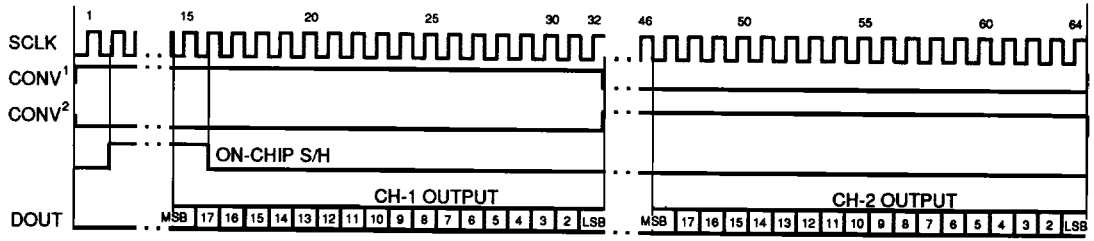
Digital Output Timing Waveforms



Digital Timing Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
t_R	Input Rise Time			30	ns
t_F	Input Fall Time			30	ns
t_H	SCLK High Width		50		ns
t_L	SCLK Low Width		50		ns
t_S	CONV Setup Time		40		ns
t_{ACC}	DOUT Access Time	C_{LOAD} = 30 pF		50	ns
T_{CONV}	CONV Period		10.4		µs
T_{SCLK}	SCLK Period		162		ns

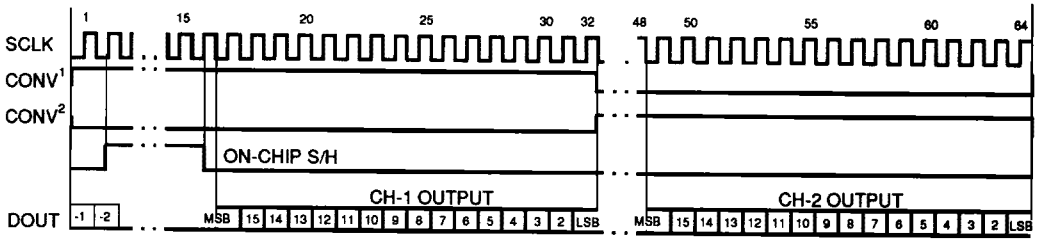
Input/Output Timing for 18-Bit Mode (SEL2 = "1")



i) SEL1 = "0", CONV [1]
ii) SEL1 = "1", CONV [2]

Notes: CONV = Fs (96 kHz Max)
SCLK = CONV x 64

Input/Output Timing for 16-Bit Mode (SEL2 = "0")



i) SEL1 = "0", CONV [1]
ii) SEL1 = "1", CONV [2]

Notes: CONV = Fs (96 kHz Max)
SCLK = CONV x 64

Ordering Information

Speed (KHz)	Signal-to-Noise (dB)	Power Supply	Ordering Code	Package	Operation Range
96	90	±10%	AT76C120-1PC	24P6	Commercial (0°C to 70°C)
			AT76C120-1PI	24P6	Industrial (-40°C to 85°C)
96	90	±5%	AT76C120-1DM	24D6	Military (-55°C to 125°C)
96	84	±10%	AT76C120-2PC AT76C120-2RC	24P6 24R	Commercial (0°C to 70°C)
			AT76C120-2PI AT76C120-2RI	24P6 24R	Industrial (-40°C to 85°C)
96	84	±5%	AT76C120-2DM	24D6	Military (-55°C to 125°C)

Package Type	
24D6	24 Lead, 0.600" Wide, Non-Windowed (OTP), Ceramic Dual Inline Package (Cerdip)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
24R	24 Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC)