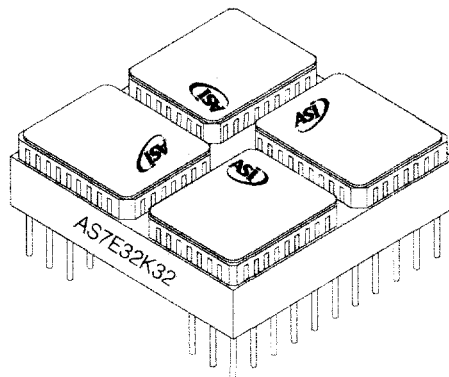ASI AUSTIN SEMICONDUCTOR INC.

EEPROM MODULE

PRELIMINARY

FEATURES

- Built in decoupling caps for low noise operation
- Organized as 32K x32
- Operation with single 5 volt supply
- Low power CMOS
- TTL Compatible Inputs and Outputs
- Fast Write Cycle Times
    Page Write Cycle Time: 3 ms or 10 ms max.
    1 to 64 Byte Page Write Option
- High Reliability CMOS Technology
    Endurance: 10K and 100K Write Cycles
   Data Retention: 10 Years

OPTIONS

- Timing
    70, 90ns Access
- Package
    66 pin PGA type 1.09 inch square

GENERAL DESCRIPTION

The Austin Semiconductor, Inc. AS7E32K32 is a 1 Megabit CMOS EEPROM Module organized as 32Kx32 and is user configurable to 64K x 16 and 128K x 8. The module achieves high speed access, low power consumption and high reliability by employing advanced CMOS memory technology. These advanced features make ASI modules ideally suited for military or space applications.

The AS7E32K32 module is constructed using a 1.09 sq inch ceramic substrate. This compact layout reduces space requirements for board assembly to a minimum.
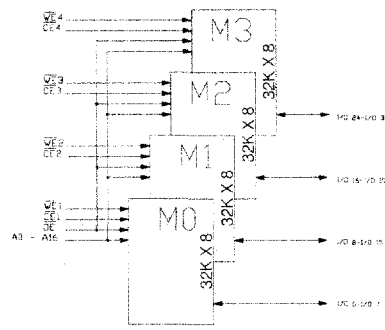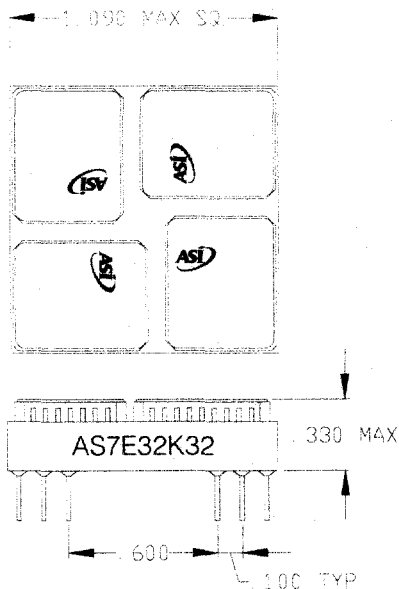
PIN CONFIGURATION (TOP VIEW)

I/O8	1	WE2	12	I/O15	23		I/O24	34	VCC	45	I/O31	56
I/O9	2	CE2	13	I/O14	24		I/O25	35	CE4	46	I/O30	57
I/O10	3	GND	14	I/O13	25		I/O26	36	WE4	47	I/O29	58
A13	4	I/O11	15	I/O12	26		A6	37	I/O27	48	I/O28	59
A14	5	A10	16	OE	27		A7	38	A3	49	AO	60
NC	6	A11	17	NC	28		NC	39	A4	50	A1	61
NC	7	A12	18	WE1	29		A8	40	A5	51	A2	62
NC	8	VCC	19	I/O7	30		A9	41	WE3	52	I/O23	63
I/OO	9	CE1	20	I/O6	31		I/O16	42	CE3	53	I/O22	64
I/O1	10	NC	21	I/O5	32		I/O17	43	GND	54	I/O21	65
I/O2	11	I/O3	22	I/O4	33		I/O18	44	I/O19	55	I/O20	66

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DEVICE OPERATION:

The AS7E32K32 is an electricaly erasable and programmable memory module that is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte-page register to allow writing of up to 64 bytes of data simultaneously. During a write cycle, the address and 1 to 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

READ:

The AS7E32K32 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is High, the data stored at the memory location determined by the address pins is asserted on the outputs. The module can be read as a 32 bit, 16 bit or 8 bit device. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE:

A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte, word or double word (BWDW) write has been started it will automatically time itself to completion.

PAGE WRITE:

The page write operation of the AS7E32K32 allows 1 to 128 BWDWs of data to be written into the device during a single internal programming period. Each new BWDW must be written within 150µs (tBLC) of the previous BWDW. If the tBLC limit is exceeded the AS7E32K32 will cease accepting data and commence the internal programming operation. For each $\overline{WE}$ high to low transition during the page write operation, A7-A16 must be the same. The A0-A6 inputs are used to specify which BWDW within the page are to be written. The BWDW may be loaded in any order and may be altered within the same load period. Only BWDW which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

DATA POLLING:

The AS7E32K32 features DATA Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7 of each byte. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. DATA Polling may begin at anytime during the write cycle.

TOGGLE BIT:

In addition to DATA Polling the AS7E32K32 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 of each byte toggling between one and zero. Once the write has completed, I/O6 of each byte will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION:

If precautions are not taken, inadvertent writes may occur during transitions of the host power supply. The E^2 module has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION:

Hardware features protect against inadvertent writes to the AS7E32K32 in the following ways: (a) VCC sense - if VCC is below 3.8 V (typical) the write function is inhibited; (b) VCC power-on delay - once VCC has reached 3.8 V the device will automatically time out 5 ms (typical) before allowing a write; (c) write inhibit - holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION:

A software controlled data protection feature has been implemented on theAS7E32K32. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user and is shipped with SDP disabled, SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the three byte command sequence and after t_{wc} the entire AS7E32K32 will be protected from inadvertent write operations. It should be noted, that once protected the host may still perform a byte of page write to the AS7E32K32. This is done by preceding the data to be written by the same three byte command sequence used to enable SDP. Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AS7E32K32 during power-up and Power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte of page write operation.

After setting SDP, any attempt to write to the device without the three byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{wc}, read operations will effectively be polling operations.

Absolute Maximum Ratings*

Temperature Under Bias.....................-55°C - 125°C
Storage Temperature.........................-65°C - 150°C
All Input Voltages
(Including NC Pins)
with Respect to Ground..................-0.6V to +6.25V
All Output Voltages
with Respect to Ground................-0.6 to Vcc +0.6V
Voltage to $\overline{OE}$ and A9
with Respect to Ground...................-0.6V to +13.5V

*NOTICE: Stress beyond those listed under "Absolute Maximum Ratings"
may cause permanent damage to the device.

Pin Capacitance (f=1MHz, T=25°C) [1]

	Max	Units	Conditions
C_{IN}	50	pF	$V_{IN}=0V$
C_{OUT}	20	pF	$V_{OUT}=0V$

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IH}	V_{IH}	D_{OUT}
Write (2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	$X^{(1)}$	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

DC operating conditions. (-55°C ≤ TA ≤125°C; Vcc = 5V ± 10%)

Parameter	Symbol	Condition	Min	Max	Units
Input Load Current	I_{LI}	V_{IN}=0v to Vcc + 1v		43	uA
Output Leakage Current	I_{LO}	VI/O=0vtoVCC		43	uA
Vcc Standby Current CMOS	I_{SB1}	$\overline{CE}$=VCC-0.3V to Vcc+1		1.3	mA
Vcc Standby Current TTL	I_{SB2}	$\overline{CE}$=2.0v to Vcc+1		13	mA
Vcc Active Current	I_{CC}	f=5MHz; I_{OUT}=0mA		340	mA
Input Low Voltage	V_{IL}			0.8	V
Input High Voltage	V_{IH}		2		V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA		0.45	V
Output High Voltage	V_{OH1}	I_{OH}=400ua	2.4		V
Output High Voltage CMOS	V_{OH2}	I_{OH}=-100uA; Vcc=4.5V	4.2		V

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AC READ Characteristics (-55°C ≤ TA ≤125°C; Vcc = 5V ± 10%)

Parameter	Symbol	Min	Max	Min	Max	Min	Max	Units
Address to Output Delay	t_{ACC}	120		150		200		ns
$\overline{CE}$ to Output Delay	$t_{CE(1)}$		120		150		200	ns
$\overline{OE}$ to Output Delay	$t_{OE(2)}$	0	50	0	55	0	55	ns
$\overline{CE}$ or $\overline{OE}$ to Output Float	$t_{DF(3,4)}$	0	50	0	55	0	55	ns
Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurs first	t_{OH}	0		0		0		ns

A.C. Read Waveforms [1,2,3,4]
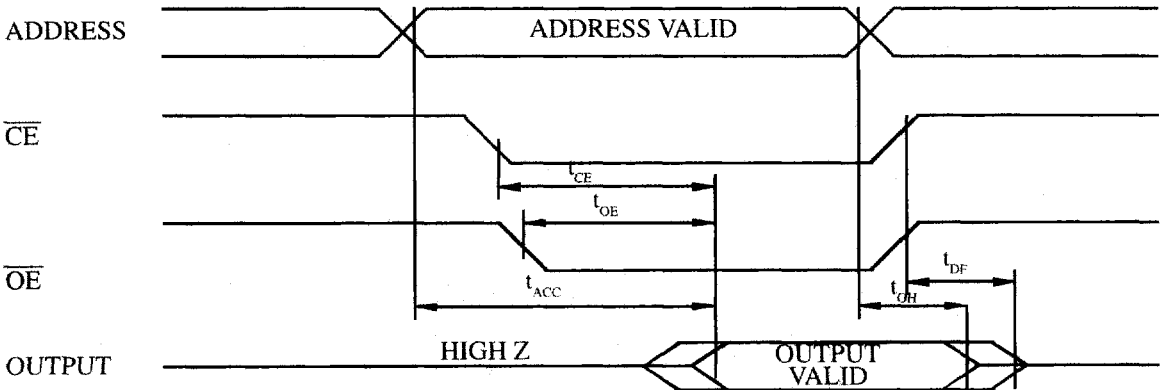
Notes:
1. CE may be delayed to $t_{ACC}-t_{CE}$ after the address transition without inpact on t_{ACC}.
2. OE may be delayed to $t_{CE}-t_{OE}$ after the falling edge of CE without inpact on t_{CE} or by $t_{ACC}-t_{OE}$ after an address change without inpact on t_{ACC}.

3. t_{DF} is specified from OE or CE whichever occurs first ($C_L = 5pF$).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement level

AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5nS
Input and Output Timing Reference Levels	1.5V

Output Test Load

5.0V

1.8K

1.3K   100pF

AC Write Characteristics

Parameter	Symbol	Min	Max	Units
Address, $\overline{OE}$ Set-up time	t_{AS}, t_{OES}	0		ns
Address Hold Time	t_{AH}	50		ns
Chip Select Set-up Time	t_{CS}	0		ns
Chip Select Hold Time	t_{CH}	0		ns
Write Pulse Width ($\overline{WE}$ or $\overline{CE}$	t_{WP}	100		ns
Data Set-up Time	t_{DS}	50		ns
Data, $\overline{OE}$ Hold Time	t_{OH}, t_{OEH}	0		ns

AC Write Wave Forms - $\overline{WE}$ Controlled
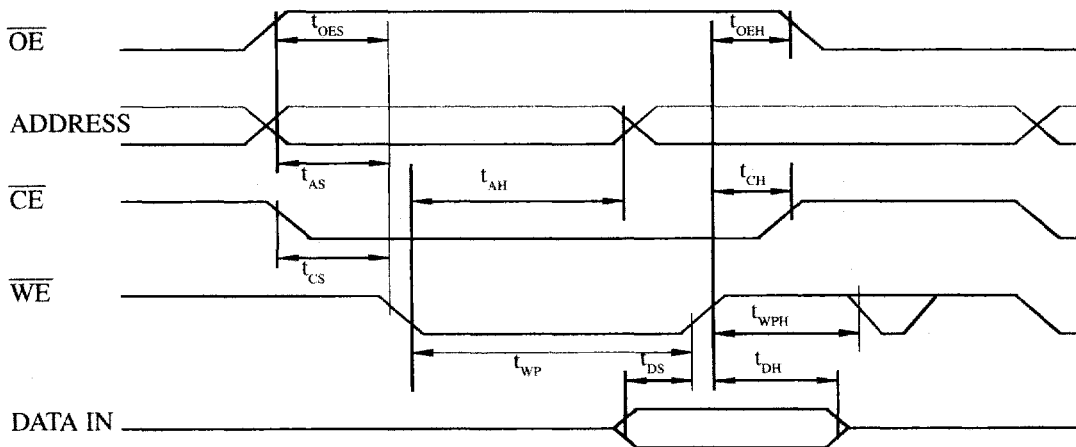
AC Write Wave Forms - $\overline{CE}$ Controlled

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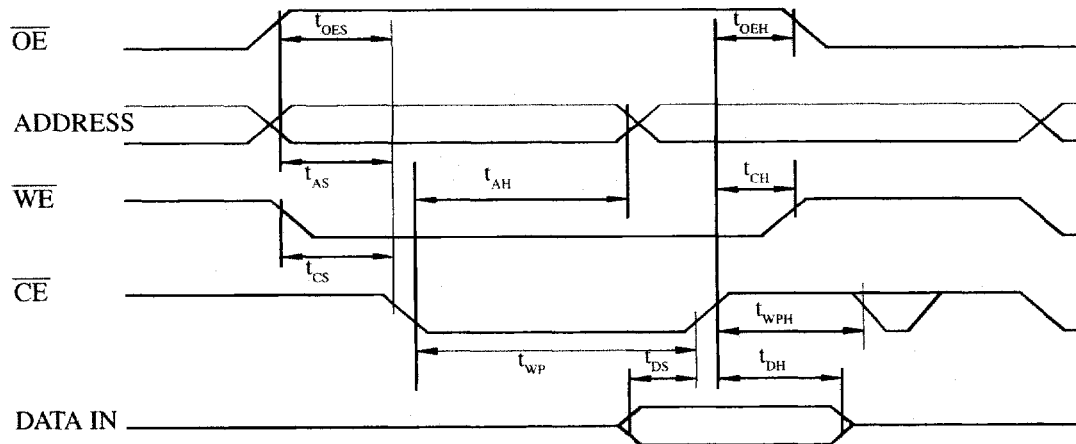
Page Mode Characteristics

Parameter	Symbol	Min	Max	Units
Write Cycle	t_{WC}		10	ms
Address Set-up Time	t_{AS}	50		ns
Address Hold Time	t_{AH}	0		ns
Data Set-up Time	t_{DS}	0		ns
Data Hold Time	t_{DH}	100		ns
Write Pulse Width	t_{WP}	50		ns
Byte Load Cycle	t_{BLC}	0		us
Write Pulse Width High	t_{WPH}	50		ns

Page Mode Write Waveforms [1,2]
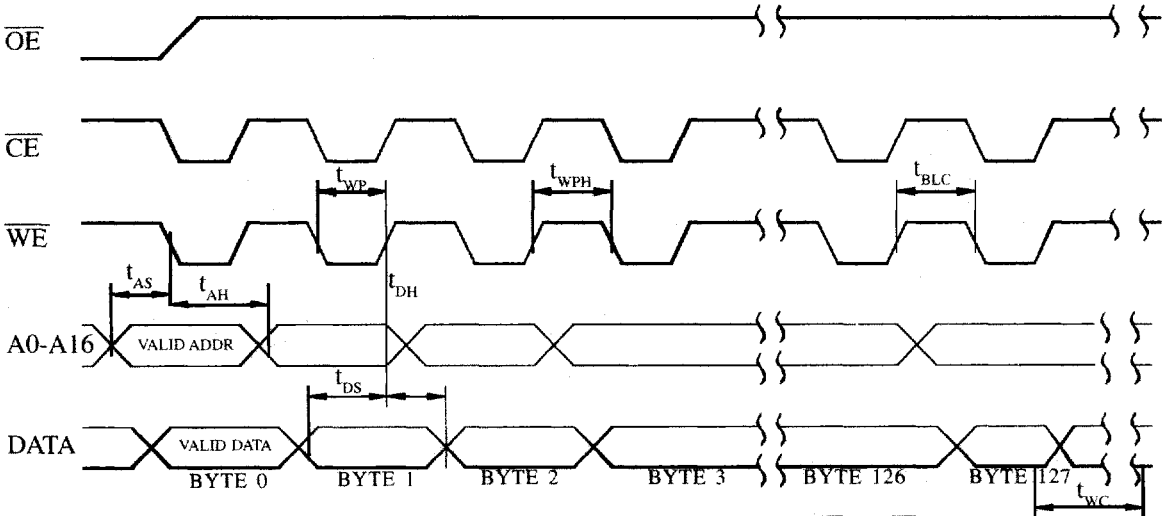
Notes: 1. A7 through A16 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
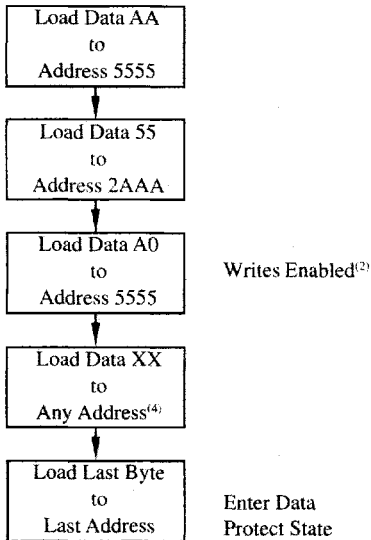2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.
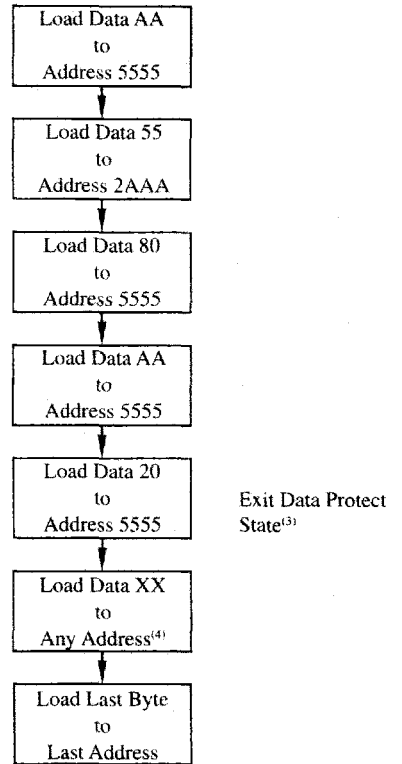
Chip Erase Waveforms

t_S = 5used (min)
$t_W = t_H$ = 10 msec (min)
V_H = 12.0 V +/- 0.5 V

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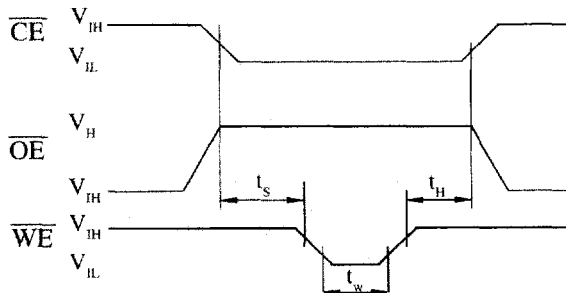
Software Data Protection Enable Algorithm[1]

Load Data AA
to
Address 5555

↓

Load Data 55
to
Address 2AAA

↓

Load Data A0
to
Address 5555   Writes Enabled[2]
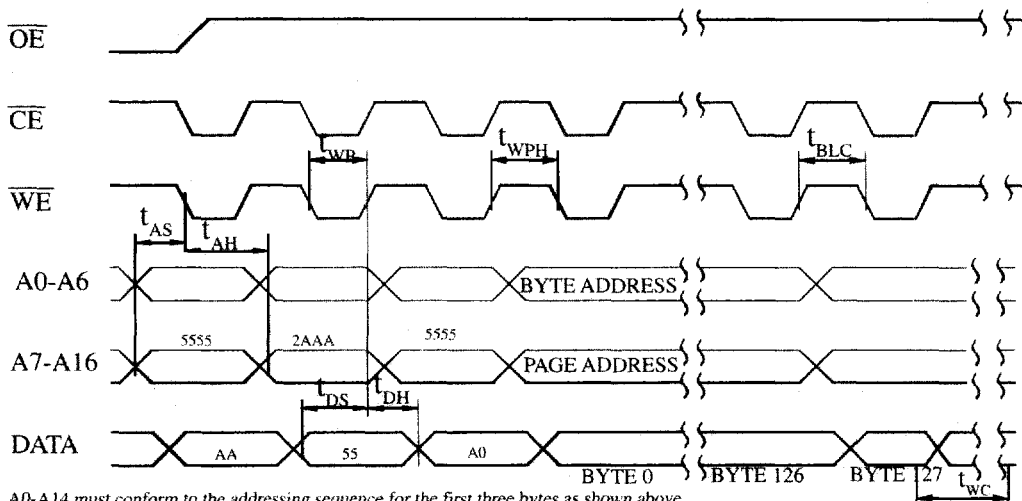
↓

Load Data XX
to
Any Address[4]

↓

Load Last Byte
to   Enter Data
Last Address   Protect State

Notes:
1. Data Format: I/O 7 - I/O0 (Hex)
2. Write Protect state will be active at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of period even if no other data is loaded.
4. 1 to 128 bytes of data are loaded.

Software Data Protection Disable Algorithm[1]

Load Data AA
to
Address 5555

↓

Load Data 55
to
Address 2AAA

↓

Load Data 80
to
Address 5555

↓

Load Data AA
to
Address 5555

↓

Load Data 20
to   Exit Data Protect
Address 5555   State[3]

↓

Load Data XX
to
Any Address[4]

↓

Load Last Byte
to
Last Address

Software Protected Program Cycle Waveform[1,2,3]

Note: 1. A0-A14 must conform to the addressing sequence for the first three bytes as shown above.
    2. After the command sequence has been issued and a page write operation follows, the page address inputs
    (A7-A16) must be the same for each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
    3. $\overline{OE}$ Must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Data Polling Characteristics[1]

Parameter	Symbol	Min	Typ	Max	Units
Data Hold Time	t_{DH}	10			ns
OE Hold Time	t_{OEH}	10			ns
OE to Output Dalay (2)	t_{OE}				ns
Write Recovery Time	t_{WR}	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See A.C. Read Characteristics.

Data Polling Waveforms
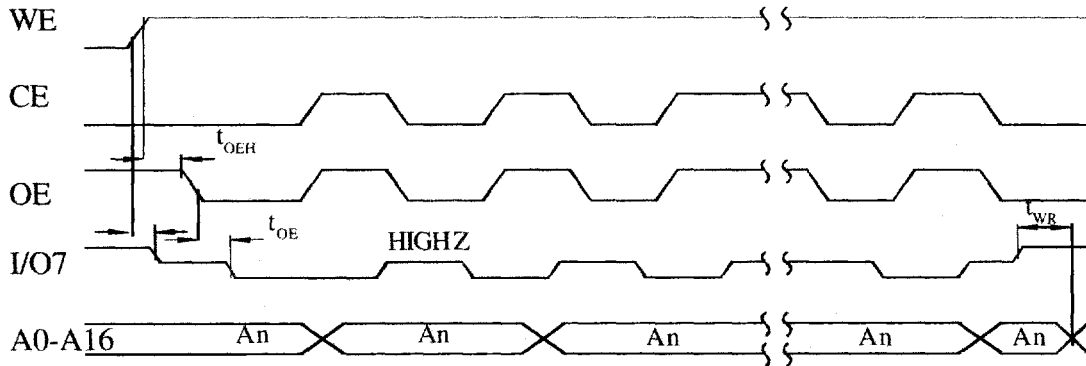
Toggle Bit Characteristics[1]

Parameter	Symbol	Min	Typ	Max	Units
Data Hold Time	t_{DH}	10			ns
OE Hold Time	t_{OEH}	10			ns
OE to Output Dalay (2)	t_{OE}				ns
OE High Pulse	t_{OEHP}	150			ns
Write Recovery Time	Icc	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See A.C. Read Characteristics.

Toggle Bit Waveforms[1,2,3]
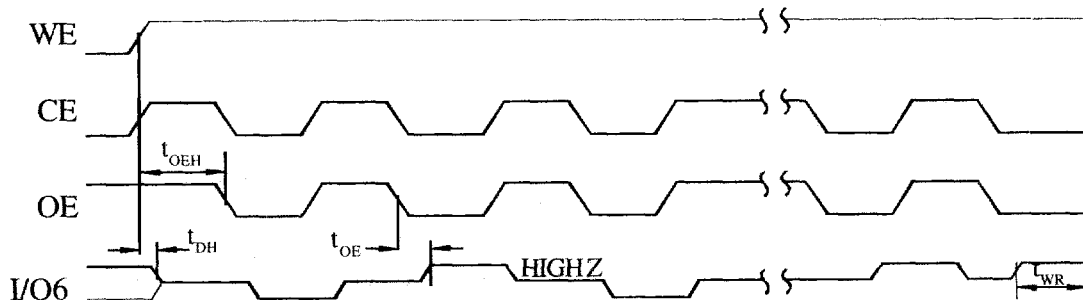
Notes: 1. Toggling either OE or CE or Both OE and CE will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

DEVICE IDENTIFICATION:

An extra 128 bytes of EEPROM memory are available to the user for identification. By raising A9 to 12 V +/- 0.5V and using address locations 1FF80H to 1FFFFH the bytes may be written to or read from in the same manner as the regular memory array.

OPTIONAL CHIP ERASE MODE:

The entire device can be erased using a six byte software code. Please see Software Chip Erase application note for details.