California Micro Devices Corp.

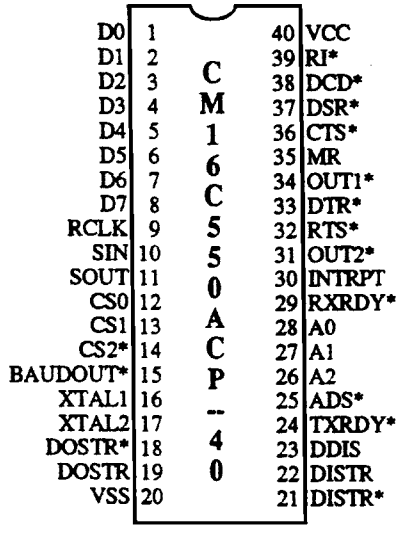
CM16C550A

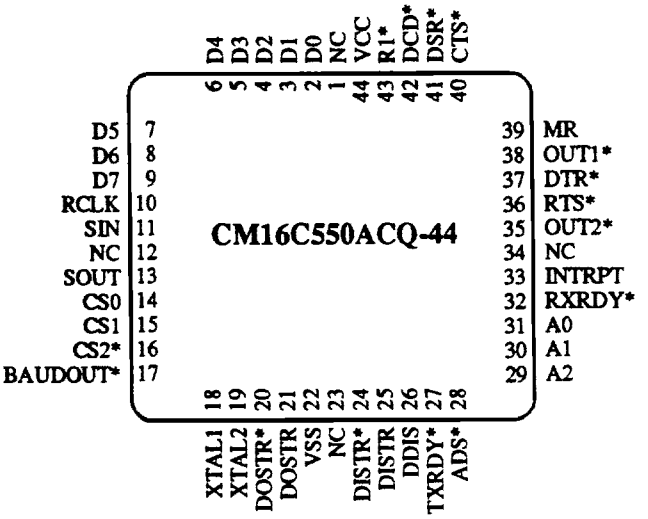
FIFO UART

FEATURES

- Programmable FIFO or character mode (CM16C450 compatible) operation
- Upward compatible with all CM16C450 software
- Pin and function compatible with the existing CM16C450 except for CSOUT and NC pins. The former CSOUT and NC pins are TXRDY* and RXRDY* pins, respectively
- After reset, all registers are identical to the CM16C450 register set
- In FIFO mode 16-byte FIFO buffers on the transmitter and receiver reduce the number of interrupts presented to the CPU
- Designed to be easily interfaced to most 8, 16 and 32-bit microprocessors
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from the serial data
- Independently controlled transmit, receive, line status and data set interrupts
- Programmable baud rate generator allows division of input clock by 1 to (2^{16}-1) and generates internal 16 x clock
- Independent receiver clock input
- MODEM control functions (CTS*, RTS*, DSR*, DTR*, RI* and DCD*)
- Fully programmable serial-interface characteristics:
  - 5, 6, 7, or 8-bit characters
  - Even, odd, forced 0/1 or no-parity bit generation and detection
  - 1, 1½, or 2 stop bit generation
  - Baud rate generation (DC to 512K baud)
- False start bit detection
- Complete status reporting capabilities
- Tri-State® TTL drive for the data bus and control bus
- Line break generation and detection
- Internal diagnostic capabilities include:
  - Loopback controls for communications link fault isolation
  - Break, parity, overrun, framing error simulation
- Fully prioritized interrupt system controls
- Advanced CMOS low power technology with single +5 volt supply

PIN CONFIGURATION





* Denotes inverted signal.

215 TOPAZ STREET, MILPITAS, CA 95035 • (408)263-3214 • FAX (408)263-7846

GENERAL DESCRIPTION

The CM16C550A is an enhanced version of the CM16C450 Universal Asynchronous Receiver/Transmitter (UART). The improved specifications ensure easy interface with existing microprocessor systems with DMA controller. Functionally identical to the CM16C450 on power up (in Character Mode) the CM16C550A can be configured into an alternate mode (FIFO mode) to relieve the CPU of excessive software overhead due to interrupts.

In FIFO mode, internal FIFO's are activated allowing 16 bytes (plus 3 bits of error data per byte in the RCVR FIFO) to be stored in both receive and transmit modes. All the logic is on chip to minimize system overhead and maximize system efficiency. Two FIFO control pins have been added to allow signalling of DMA transfers.

The UART performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the UART, as well as any error conditions (parity, overrun, framing, or break interrupt).

The UART includes a programmable baud rate generator that is capable of dividing the timing reference clock input by divisors of 1 to (2^{16}-1), and producing a 16 x clock to drive the internal transmitter logic. Provisions are also included to use this 16 x clock to drive the receiver logic. The UART has complete MODEM-control capability, and a processor interrupts system. Interrupts can be programmed to the user's requirements, minimizing the computing required to handle the communications link. UART is designed to work either in a polled or an interrupt driven environment selected by software.

The UART is fabricated using CMD's advanced double metal CMOS process.

Tri-State® is a Registered Trademark of National Semiconductor, Inc.

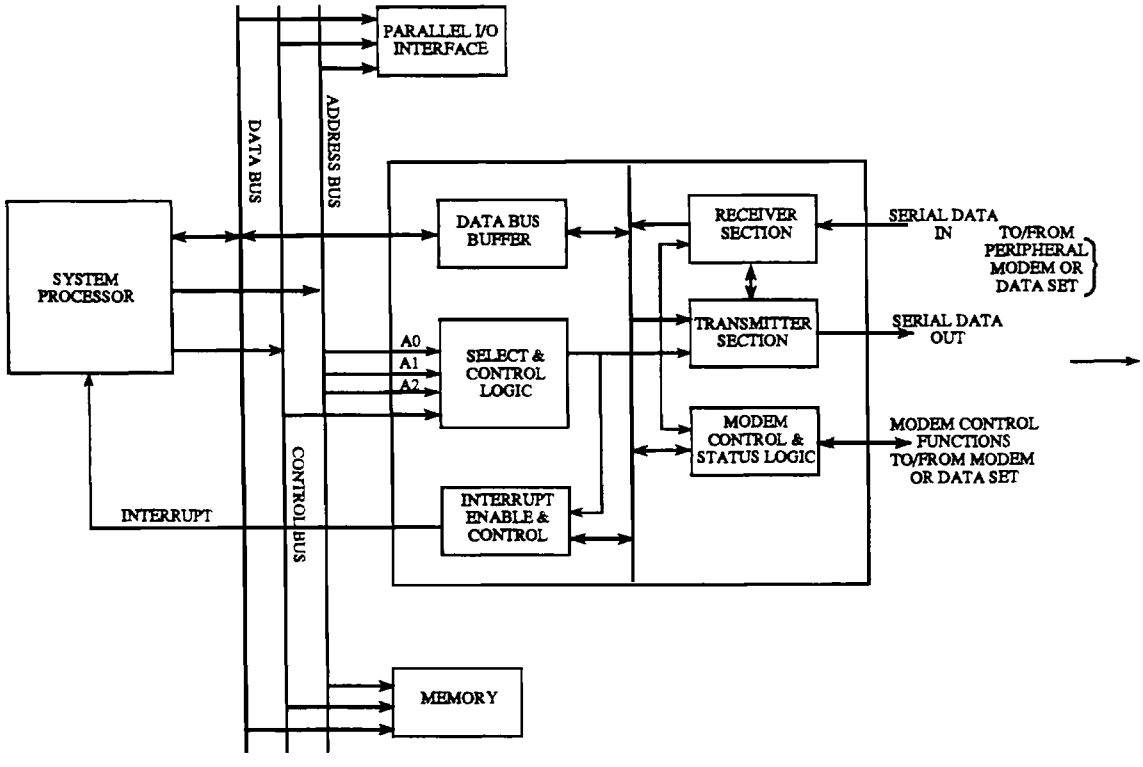
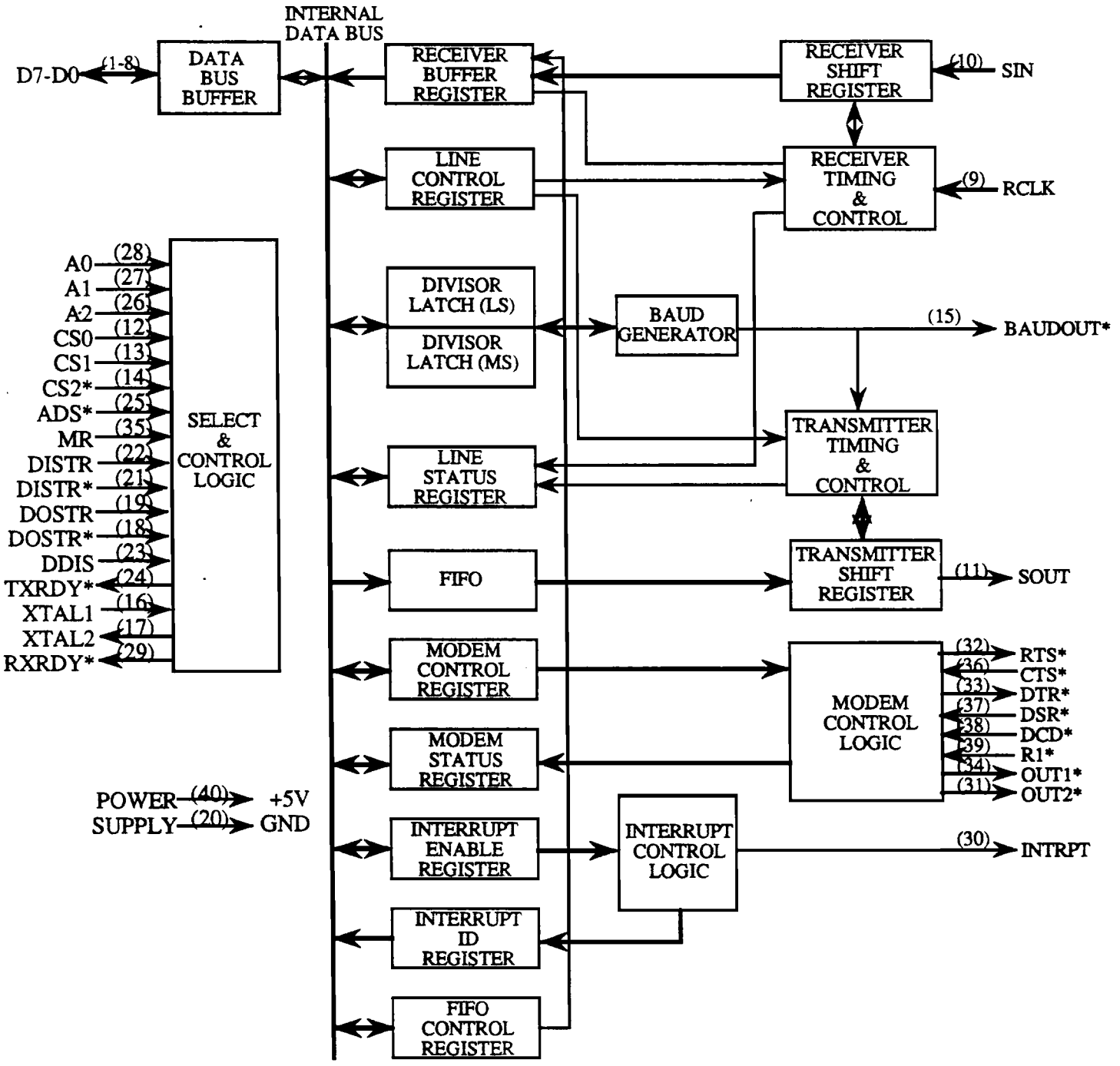


Figure 1 - CM16C550A General System Configuration

* Denotes inverted signal.



Note: Pin numbers for 40 Pin DIP are indicated in ().

Figure 2 - CM16C550A Block Diagram

* Denotes inverted signal.

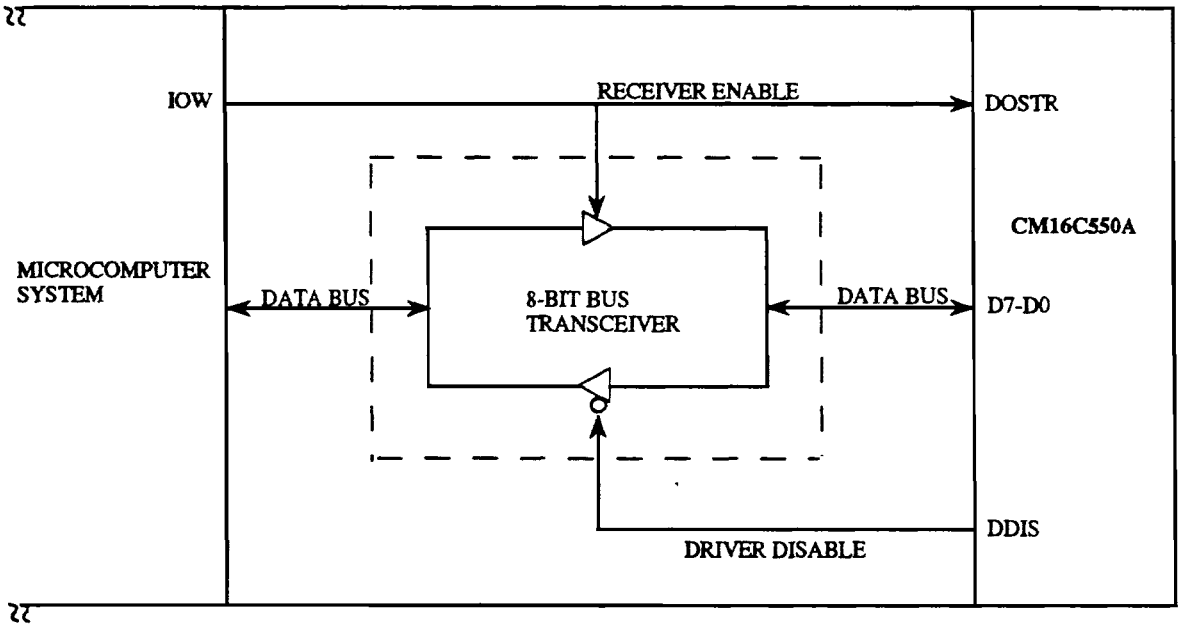


Figure 3 - Typical Interface for a high-capacity data bus

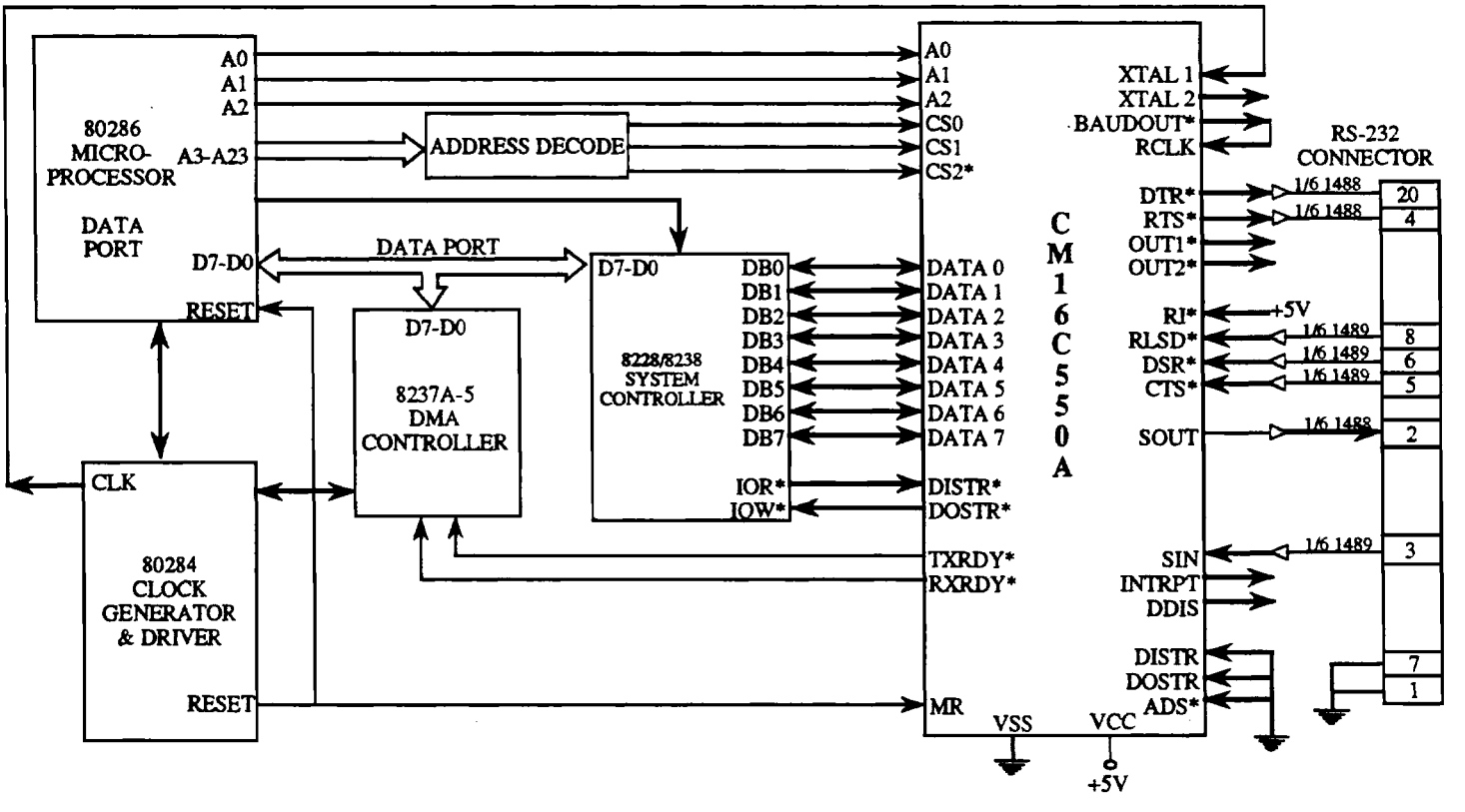


Figure 4 - Typical 16-Bit Microprocessor/RS-232 Terminal Interface using the FIFO UART

* Denotes inverted signal.

PIN DESCRIPTION

Note: In the following descriptions, a low represents a logic 0 and a high represents a logic 1.

Mnemonic	Pin Type	PIN# for 40-DIP/ 44-PLCC	Description
CS0, CS1, CS2*	IN	12:14/14:16	**Chip Select pins:** When CS0 and CS1 are high and CS2* is low, the chip is selected. This enables communication between the UART and the CPU. The positive edge of an active Address Strobe signal latches the decoded chip select signals, completing chip selection. If ADS* is always low, valid chip selects should stabilize according to the tCSW parameter.
DISTR* DISTR	IN	22,23/25,26	**Data In strobe:** When DISTR is high or DISTR* is low while the chp is selected, the CPU can read status information or data from the selected UART register. Note: Only an active DISTR or DISTR* input is required to transfer data from the UART during a read operation. Therefore, tie either the DISTR input permanently low or the DISTR* input permanently high, when it is not used.
DOSTR* DOSTR	IN	18,19/20,21	**Data Out strobe:** When DOSTR is high or DOSTR* is low while the chip is selected, the CPU can write control words or data into the selected UART register. Note: Only an active DOSTR or DOSTR* input is required to transfer data to the UART during a write operation. Therefore, tie either the DOSTR input permanently low or the DOSTR* input permanently high, when it is not used.
ADS*	IN	25/28	**Address strobe:** The positve edge of an active Address Strobe signal (ADS*) latches the Register Select pins (A0, A1, A2) and chip Selects signals (CS0, CS1, CS2*). Note: An Active ADS* input is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, tie the ADS* input permanently low.
A2, A1, A0	IN	26:28/29:31	**Register Select pins:** Address signals connected to these 3 inputs select a UART register for the CPU to read from or write to during data transfer. A table of registers and their addresses is shown below. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the line control register, affects the selection of certain UART registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches. REGISTER ADDRESSES DLAB A2 A1 A0 Register 0 0 0 0 Receiver Buffer Register (read) 0 0 0 0 Transmitter Holding Register (write) 0 0 0 1 Interrupt Enable Register X 0 1 0 Interrupt Identification Register (read) X 0 1 0 FIFO Control Register (write) X 0 1 1 Line Control Register X 1 0 0 MODEM Control Register X 1 0 1 Line Status Register X 1 1 0 MODEM Status Register X 1 1 1 Scratch Pad Register 1 0 0 0 Divisor Latch Register (least significant byte) 1 0 0 1 Divisor Latch Register (most significant byte)

* Denotes inverted signal.

Mnemonic	Pin Type	PIN# for 40-DIP/ 44-PLCC	Description
MR	IN	35/39	**Master Reset:** When this input is high, it clears all the registers (except the Receiver Buffer, Transmitter Holding and Divisor Latches), and the control logic of the UART. The states of various output signals (SOUT, INTR, OUT1* OUT2*, RTS*, DTR*) are affected by an active MR input (Refer to Table 1). This input is buffered with a TTL-compatible Schmitt Trigger with 0.5V typical hysteresis.
RCLK	IN	9/10	**Receiver Clock:** This input is the 16 x baud rate clock for the receiver section of the chip.
SIN	IN	10/11	**Serial Input:** Serial data input from communication link such as peripheral device, MODEM or data set.
CTS*	IN	36/40	**Clear To Send:** When low, this pin indicates that the MODEM or data set is ready to exchange data. The CTS* signal is a MODEM status input whose conditions can be tested by the CPU reading bit 4 (CTS) of the MODEM Status Register. Bit 4 is the complement of the CTS* signal. Bit 0 (DCTS) of the MODEM Status Register indicates whether the CTS* input has changed state since the previous reading of the modem Status Register. CTS* has no effect on the Transmitter. Note: Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.
DSR*	IN	37/41	**Data Set Ready:** When low, this pin indicates that the MODEM or data set is ready to establish the communications link with the UART. The DSR* signal is a MODEM status input whose condition can be tested by the CPU reading bit 5 (DSR) of the MODEM Status Register. Bit 5 is the complement of the DSR signal. Bit 1 (DDSR) of the MODEM Status Register indicates whether the DSR* input has changed state since the previous reading of the MODEM Status Register. DSR* has no effect on the transmitter. Note: Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.
RLSD*	IN	38/42	**Receiver Line Signal Detect:** When low, this pin indicates that the data carrier has been detected by the MODEM or data set. The DCD* signal is a MODEM status input whose condition can be tested by the CPU reading bit 7 (RLSD) of the MODEM Status Register. Bit 7 is the complement of the RLSD* signal. Bit 3 (DRLSD) of the MODEM Status Register indicates whether the RLSD* input has changed state since the previous reading of the MODEM Status Register. RLSD* has no effect on the receiver. Note: Whenever the DCD bit of the MODEM Status Register changes state, an interrupt is generated if the MODE Status Interrupt is enabled.
RI*	IN	39/43	**Ring Indicator:** When low, this pin indicates that a telephone ringing signal has been received by the MODEM or data set. The RI* signal is a MODEM status input whose condition can be tested by the CPU reading bit 6 (RI) of the MODEM Status Register. Bit 6 is the complement of the RI* signal. Bit 2 (TERI) of the MODEM Status Register indicates whether the RI* input signal has changed from a low to a high state since the previous reading of the MODEM Status Register. Note: Whenever the RI bit of the MODEM Status Register changes from a low to a high state, an interrupt is generated if the MODEM Status Interrupt is enabled.

* Denotes inverted signal.

Mnemonic	Pin Type	PIN# for 40-DIP/ 44-PLCC	Description
VCC	IN	40/44	+5V supply.
VSS	IN	20/22	Ground.
DTR*	OUT	33/37	**Data Terminal Ready:** When low, this informs the MODEM or data set that the UART is ready to establish a communication link. The DTR* output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a 1. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.
RTS*	OUT	32/36	**Request To Send:** When low, this informs the MODEM or data set that the UART is ready to exchange data. The RTS* output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Resister to a 1. A Master Reset operation sets this signal to its inactive (high) state. Loop operation holds this signal in its inactive state.
OUT1*	OUT	34/38	**Output 1:** This user-designated output can be set to an active low by programming bit 2 (OUT1) of the MODEM Control Register to a 1. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.
OUT2*	OUT	31/35	**Output 2:** This user-designated output can be set to an active low by programming bit 3 (OUT2) of the MODEM Control Register to a 1. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.
TXRDY*	OUT	24/27	**Transmitter Ready pin:** Transmitter DMA signalling is available through this pin. When operating in the FIFO mode, one of two types of DMA signalling can be selected via FCR3. When operating as in the CM16C450 Mode, only DMA mode 0 is allowed. Mode 0 supports single transfer DMA where a transfer is made between CPU bus cycles. Mode 1 supports multi-transfer DMA where multiple transfers are made continuously until the XMIT FIFO has been filled. TXRDY Mode 0: In the CM16C450 Mode (FCR3=0) or in the FIFO Mode (FCR0=1, FCR3=0) there are no characters in the XMIT FIFO or XMIT holding register, the TXRDY* pin will be low active. Once it is activated the TXRDY pin will go inactive after the first character is loaded into the XMIT FIFO or holding register. TXRDY Mode 0: In the FIFO Mode (FCR0=1, FCR3=1) there is at least one unfilled position in the XMIT FIFO, it will go low active. This pin will become inactive when the XMIT FIFO is completely full.
RXRDY*	OUT	29/32	**Receiver Ready pin:** Receiver DMA signalling is available through this pin. When operating in the FIFO mode, one of two types of DMA signalling can be selected via FCR3. When operating as in the CM16C450 Mode, only DMA mode 0 is allowed. Mode 0 supports single transfer DMA where a transfer is made between CPU bus cycles. Mode 1 supports multi-transfer DMA where multiple transfers are made continuously until the RCVR FIFO has been emptied.

* Denotes inverted signal.

Mnemonic	Pin Type	PIN# for 40-DIP/ 44-PLCC	Description
			RXRDY Mode 0: When in the CM16C450 Mode (FCR0=0) or in the FIFO Mode (FCR0=1, FCR3=0) there is at least 1 character in the RCVR FIFO or RCVR holding register, the RXRDY* pin will be low active. Once it is activated the RXRDY* pin will go inactive when there are no more characters in the FIFO or holding register. RXRDY Mode 1: In the FIFO Mode (FCR0=1, FCR3=1) the trigger level or the timeout has been reached, the RXRDY* pin will go low active. Once it is activated it will go inactive when there are no more characters in the FIFO or holding register.
DDIS	OUT	23/26	**Driver Disable:** This goes low whenever the CPU is reading data or status from the UART. It can be used to disable or control the direction of a data bus transceiver between the CPU and the UART.
BAUDOUT*	OUT	15/17	**Baud Out Clock:** This is the 16 x clock signal from the transmitter section of the UART. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Rate Generator Divisor Latches. The BAUDOUT* may also be used for the receiver section by tying this output to the RCLK input of the chip.
INTRPT	OUT	30/33	**Interrupt:** This pin goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag; Received Data Available; Timeout (FIFO Mode only); Transmitter Holding register Empty; and MODEM Status. The INTRPT signal is reset low upon the appropriate interrupt service or a Master Reset operation.
SOUT	OUT	11/13	**Serial Output:** Composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Master Reset operation.
D0-D7	I/O	1:8/2:9	**Data Bus D0-D7:** This 3-state bus provides bidirectional communications between the UART and the CPU. Data, control words, and status information are transferred via the D0-D7 Data Bus.
XTAL1 XTAL2	IN/OUT	16/18	**External Clock Input/Output:** These two pins connect the main timing reference (crystal or signal clock) to the UART. See Figure 5 for circuit connection diagram.
NC	NA	-/1,12,23,34	**Pins not connected.**

* Denotes inverted signal.

UART OPERATIONAL DESCRIPTION

Master Reset: A high level input on MR pin resets UART and forces internal register and output pins as shown in Table 1.

Table 1 - Reset Configuration of Registers and Output Signals

Register/Signal	Reset Control	Reset State
Receiver Buffer Register	First word received	Undefined data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Undefined data
Interrupt Enable Register	Master Reset	All bits low - Bits (4-7) are permanently low
Interrupt Identification Register	Master Reset	Bit 0 is forced high and Bits (1-3), 6, 7 are forced low - Bits 4 and 5 are permanently low
Line Control Register	Master Reset	All bits low
Modem Control Register	Master Reset	All bits low - Bits (5-7) are permanently low
Line Status Register	Master Reset	All bits low - except Bits 5, 6 which are high
Modem Status Register	Master Reset MODEM Signal inputs	Bits (0-3) low Bits (4-7) follow input signals
Divisor Latch (low order byte)	Writing 00(H) into the Latch	Undefined data
Divisor Latch (high order byte)	Writing 00(H) into the Latch	Undefined data
SOUT	Master Reset	High
BAUDOUT*	Writing into either Divisor Latch	Low

* Denotes inverted signal.

Table I - Reset Configuration of Registers and Output Signals (continued)

Register/Signal	Reset Control	Reset State
DDIS	According to CS0, CS1, CS2*, DISTR, DISTR*	According to CS0, CS1, CS2*, DISTR, DISTR*
INTRPT (RCVR ERRS)	Master Reset/Read LSR	Low
INTRPT (RCVR DATA READY)	Master Reset/Read RBR	Low
INTRPT (THRE)	Master Reset/Read IIR/Write THR	Low
OUT2*	Master Reset	High
OUT1*	Master Reset	High
RTS*	Master Reset	High
DTR*	Master Reset	High
RCVR FIFO	Master Reset	Undefined data
XMIT FIFO	Master Reset	Undefined data
FIFO CONTROL	Master Reset	All bits low {(0-3), 6, 7 forced and 4, 5 permanent}
Data bus (D0-D7)	According to CS0, CS1, CS2*, DISTR, DISTR*, DOSTR, DOSTR*	According to CS0, CS1, CS2*, DISTR, DISTR*, DOSTR, DOSTR*

* Denotes inverted signal.

INTERNAL REGISTER DESCRIPTION

The system programmer has access to any of the registers as summerized in Table II.

Table II - Accessible CM16C550A Registers

	Register Address					
	0 DLAB=0	0 DLAB=0	1 DLAB=0	2	2	3
Bit no.	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Identification Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register
	RBR	THR	IER	IIR	FCR	LCR
0	Data Bit 0	Data Bit 0	Enable Received Data Register Interrupt (ERBFI)	"0" if Interrupt Pending	FIFO Enable (FEWO)	Word Length Select Bit 0 (WLSO)
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit 0 (IIDB0)	Receiver FIFO Reset (RFR)	Word Length Select Bit 1 (WLS1)
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ERLSI)	Interrupt ID Bit 1 (IIDB1)	Transmitter FIFO Reset (TFR)	Number of Stop Bits (STB)
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	Interrupt ID Bit 2 (IIDB2)	DMA Mode Select (DMS)	Parity Enable (PEN)
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity (STP)
6	Data Bit 6	Data Bit 6	0	FIFO Enable (*) (FE)	RCVR FIFO Trigger level (LSB)	Set Break Control
7	Data Bit 7	Data Bit 7	0	FIFO Enable (*) (FE)	RCVR FIFO Trigger level (MSB)	Divisor Latch Access bit (DLAB)

(*) These bits are read 0 in Character Mode.

Table II - Accessible CM16C550A Registers (continued)

	Register Address					
	4	5	6	7	0 DLAB=1	1 DLAB=1
Bit no.	MODEM Control Register	Line Status Register (Read Only)	MODEM Status Register	Scratch Pad Register	Divisor Latch (LSB)	Divisor Latch (MSB)
	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Out 2	Framing Error (FE)	Delta Receive Line Signal Detect (DRLSD)	Bit 3	Bit 3	Bit 11
4	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	0	Error in RCVR FIFO(*) (EIRF)	Receive Line Signal Detect (RLSD)	Bit 7	Bit 7	Bit 15

(*) These bits are read 0 in Character Mode.

Line Control Register

The system programmer specifies the format of the asynchronous data communications exchange and sets the Divisor Latch Access bit via the Line Control Register (LCR). The programmer can also read the contents of the Line Control Register. The read capability simplifies system programming and eliminates the need for separate storage in system memory of the line charactertistics.

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Character Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits transmitted and received in each serial character. If bit 2 is a logic 0, one Stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one and a half Stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated. The Receiver checks the first Stop-bit only, regardless of the number of Stop bits selected.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1's when the data word bits and the Parity bit are summed).

Bit 4: This bit is the Even Parity Selects bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1's is transmitted or checked in the data word bits and parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1's is transmitted or checked in the data word bits and Parity bit.

Bit 5: This bit is the Stick Parity bit. When bits 3 and 5 are logic 1 the parity bit is transmitted and detected by the receiver in the opposite state indicated by bit 4. If bit 5 is zero, Stick parity is disabled.

Bit 6: This bit is the Break Control bit. It causes a break condition to be transmitted to the receiving UART. When bit 6 is set to a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state and remains there until bit 6 is set to a logic 0. This bit acts only on SOUT pin and has no effect on transmitter logic. This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous characters will be transmitted because of break.

1. Load an all 0's, pad character, in response to THRE.
2. Set Break after the next THRE.
3. Wait for the transmitter to be idle, (TEMT=1), and clear break when normal transmission has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Programmable Baud Rate Generator

The UART contains a programmable Baud Generator that is capable of taking any clock input from DC to 8.0 MHz and dividing it by any divisor from 1 to 2^{16}-1. The output frequency of the Baud Generator is 16 x the Baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization to ensure proper operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables III, IV and V illustrate the use of the Baud Rate Generator with three different driving frequencies. Table III references to a 1.8430 MHz clock, Table IV to a 3.070 MHz clock, and Table V to a 8 MHz clock. For baud rates of 38,400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen. Using a divisor of zero is not recommended. In no case should the data rate be greater than 512K baud.

* Denotes inverted signal.

Table III - Baud Rates Using 1.8432 MHz Clock

Desired Baud Rate	Divisor Used to Generate 16 x clock	Percent Error Difference Between Desired and Actual
50	2304	-
75	1536	-
110	1047	0.026
134.5	857	0.058
150	768	-
300	384	-
600	192	-
1200	96	-
1800	64	-
2000	58	0.690
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	-
56000	2(*)	2.860

Table IV - Baud Rates Using 3.072 MHz Clock

Desired Baud Rate	Divisor Used to Generate 16 x clock	Percent Error Difference Between Desired and Actual
50	3840	-
75	2560	-
110	1745	0.026
134.5	1428	0.034
150	1280	-
300	640	-
600	320	-
1200	160	-
1800	107	0.312
2000	96	-
2400	80	-
3600	53	0.628
4800	40	-
7200	27	1.230
9600	20	-
19200	10	-
38400	5	-
56000	3(*)	14.285

* Smallest allowable divisor when using corresponding crystal.

Table V - Baud Rates Using 8.0 MHz Clock

Desired Baud Rate	Divisor Used to Generate 16 x clock	Percent Error Difference Between Desired and Actual
50	10000	-
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	-
2400	208	1.160
3600	139	0.080
4800	104	1.160
7200	69	0.644
9600	52	1.160
19200	26	1.160
38400	13	1.160
56000	9	0.790
128000	4	2.344
256000	2(*)	2.344

Line Status Register

This register provides status information to the CPU concerning the data transfer. Table II shows the contents of the Line Status Register. Description of each bit follows:

Bit 0: This bit is the Receiver Data Ready (RDR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register of the FIFO. Bit 0 is reset to a logic 0 by reading all of the data in the Receiver Buffer Register (for character mode) or the RCVR FIFO (for FIFO mode).

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is set to a logic 1 upon detection of an overrun condition and reset whenever the CPU reads the contents of the Line Status Register. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. An OE is indicated as soon as it happens. The character in the shift register is overwritten, but nothing will be transferred to FIFO.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character dos not have the correct even or odd parity, as selected by the even-parity-select bit. The PE is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO and revealed to the CPU when the associated character is at the top of the FIFO.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a logic 0 bit (Spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. The UART will resynchronize after a

* Smallest allowable divisor when using corresponding crystal.

Framing Error.

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Lines Status Register. When in FIFO mode, BI is associated to the particular character in the FIFO, and this bit is set when the associated character is at the top of the FIFO. When a break occurs, only one zero character is loaded into the FIFO. The next character transferred is enable after SIN goes to the marking state (logic 1) and receives the next valid start bit.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU. In the FIFO mode, this bit will be set when XMIT FIFO is empty and cleared when at least one character is written to XMIT FIFO.

Bit 6: This bit is the Transmitter Empty (TEMT) Indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to a logic 0 whenever either the THR or the TSR contains a data character. In the FIFO mode this bit is set to 1 whenever the transmitter FIFO and shift register are both empty.

Bit 7: In the Character Mode, this bit (LSR7) is a 0. In the FIFO mode it is set when there is at least one parity error, framing error or break indication in the FIFO. LSR7 is cleared when the CPU reads the LSR, if there are no subsequent errors in the FIFO.

Note: The Line Status Register is intended for read operations only. Writing to this register is not recommended.

Interrupt Identification Register

In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1), Received Data Ready (priority 2), Transmitter Holding Register Empty (priority 3), and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and source of that interrupt is stored in the Interrupt Identification Register. Register IIR, when addressed during chip select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. Its contents are indicated in Table VI and are described below:

Bit 0: This bit can be used in a prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1, 2: These two bits of the IIR are used to identify the highest priority interrupt pending (see Table VI).

Bit 3: In the Character Mode this bit is 0. In the FIFO Mode this bit is set along with bit 2 when a timeout interrupt is pending.

Bits 4, 5: These two bits of the IIR are always logic 0.

Bits 6, 7: These two bits, when set, indicate that the device is in FIFO Mode, i.e., when FCR0=1.

Interrupt Enable Register

This 8-bit register enables the four interrupt sources of the UART to separately activate the chip interrupt (INTRPT) output signal. Each interrupt can individually activate the interrupt (INTRPT) output signal. Its contents are indicated in Table 3-2 and are described as follows. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register (IER). Similarly, setting bits of the IER register to a logic 1 enables the selected interrupt(s). Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the INTRPT output signal. All other system functions operate in their normal manner, including the setting of the Line Status and MODE Status Registers.

Bit 0: This bit enables the Received Data Available Interrupt

Table VI - Interrupt Control Functions

Interrupt Identification Registers				Interrupt Set and Reset Functions			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	0	1	-	None	None	-
0	1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Receiver Data Available	Receiver Data Available or Trigger Level Reached	Reading the Receiver Buffer Register or the FIFO Drops below the Trigger Level
1	1	0	0	Second	Character Timeout Identification	No characters have been input to or removed from the RCVR FIFO during the last 4 character times, and there is at least one character in it during this time.	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to send or Data Set ready or Ring Indicator or Received Line Signal Detect	Reading the MODEM status Register

(and timeout interrupts in the FIFO mode) when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4-7: These four bits are always logic 0.

Scratch Pad Register

This 8-bit Read/Write Register does not control the UART in any way. It is intended as a scratch pad register to be used by the programmer to hold general purpose data temporarily.

FIFO Control Register

This write only register is located at the same address as the IIR (read only). This register is used to enable FIFO Mode, clear FIFO's, set the RCVR FIFO trigger levels, and select the mode of DMA signaling.

Bit 0: Writing a 1 to this bit enables both the XMIT and RCVR FIFO's. When changing from FIFO Mode to Character Mode and vice versa, data is not automatically cleared from the FIFO's. This bit must be a 1 when writing to other FCR bits or they will not be programmed.

Bit 1: Writing a 1 to FCR1 will reset the receiver FIFO counters to 0, and then self clear this bit to 0. The shift register is not cleared.

Bit 2: Functions the same as bit 1, except for XMIT FIFO counters.

BIT 3: If FCR0=1, setting FCR3 to a 1 will cause the RXRDY and TXRDY pins to change from mode 0 to mode 1 (see description of RXRDY and TXRDY pins).

Bits 4, 5: FCR4 and FCR5 are reserved for future use.

Bits 6, 7: FCR6 and FCR7 are used to set the trigger level for the RCVR FIFO interrupt as follows:

7	6	RCVR FIFO Trigger Level (in bytes)
0	0	01
0	1	04
1	0	08
1	1	14

MODEM Control Register

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table II and are described below:

Bit 0: This bit controls the Data Terminal Ready (DTR*) output. When bit 0 is set to a logic 1, the DTR* output is forced to a logic 0. When bit 0 is reset to a logic 0, the DTR* output is forced to a logic 1.

Note: The DTR* output of the UART may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send (RTS*) output. Bit 1 affects the RTS* output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 (OUT1*) signal, which is an auxiliary user-designated output. Bit 2 affects the OUT1* output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 (OUT2*) signal, which is an auxiliary user-designated output. Bit 3 affects the OUT2* output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to a logic 1 (high) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control inputs (CTS*, DSR*, RLSD* and RI*) are disconnected, and the MODEM Control output pins (RTS*, DTR*, OUT2* and OUT1*) are forced to their inactive state (high). In the diagnostic

* Denotes inverted signal.

mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the UART.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM control Interrupts are also operational, but the sources of interrupts are now the lower four bits of the MODEM Control Register instead of the four MODEM control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5-7: These bits are permanently set to logic 0.

MODEM Status Register

This 8-bit register provides the current state of the control lines from the MODEM or data set (or a peripheral device emulating a modem) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table II and described below:

Bit 0: This bit is the Delta Clear To Send (DCTS) indicator. Bit 0, when set to logic 1, indicates that the CTS* input to the chip has changed state since the last time this bit was cleared to logic 0 by reading this bit by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1, when set to logic 1, indicates that the DSR* input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Rin Indicator (TREI) detector. Bit 2 indicates that the RI* input to the chip has changed from a low to a high state since the last time it was read by the CPU.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3, when set to logic 1, indicates that the RLSD input to the chip has changed state since the last time it was read by the CPU.

Note: Whenever bits 0, 1, 2, or 3 are set to logic 1, a MODEM Status Interrupt is generated, if bit 3 (EDSSI) of the interrupt enable register is set.

Bit 4: This bit is the complement of the Clear To Send (CTS*) input, This bit is equivalent to bit RTS of the MODEM control register, if bit 4 of the MCR is set to 1 (loop mode).

Bit 5: This bit is the complement of the Data Set Ready (DSR*) input. This bit is equivalent to bit DTR of the MODEM control register, if bit 4 of the MCR is set to 1 (loop mode).

Bit 6: This bit is the complement of the Ring Indicator (RI*) input. Thid bit is equivalent to bit OUT1 of the MODEM control register, if bit 4 of the MCR is set to 1 (loop mode).

Bit 7: This bit is the complement of the Received Line Signal Detect (RLSD*) input. This bit is equivalent to bit OUT2 of the MODEM control register, if bit 4 of the MCR is set to 1 (loop mode).

FIFO Interrupt Mode Operation

When the RCVR FIFO and receiver interrupts are enabled (FCR0=1, IER0=1) RCVR interrupts will occur as follows:

A. The receive data available interrupt will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B. The IIR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt, it is cleared when the FIFO drops below the trigger level.

C. The receiver line status interrupt (IIR=06), as before, has higher priority than the received data available (IIR=04) interrupt.

D. The data ready bit (LSR bit 0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts will occur as follows:

A. A FIFO timeout interrupt will occur, if the following conditions exist:
   - at least one character is in the RCVR FIFO,
   - the most recent serial character received was longer than 4 continuous character times ago (if 2 stop bits are programmed, the second one is included in this time delay),

* Denotes inverted signal.

- the most recent CPU read of the FIFO was longer than 4 continuous character times ago.

This will cause a maximum character received to interrupt issued delay of 160 ms at 300 BAUD with a 12-bit character.

B. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).

C. When a timeout interrupt has occurred, it is cleared and the timer is reset when the CPU reads one character from the RCVR FIFO.

D. When a timeout interrupt has not occurred, the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR0=1, IER1=1), XMIT interrupts will occur as follows:

A. The transmitter holding register interrupt (02) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 to 16 characters may be written to this XMIT FIFO while servicing this interrupt) or the IIR is read.

B. The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE=1 and there have not been at least two bytes at the same time in the transmit FIFO, since the last THRE=1. The first transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

FIFO Polled Mode Operation

With FCR0=1 resetting IERO, IER1, IER2, IER3 or all to zero puts the UART in the FIFO Polled Mode of operation. Since the RCVR and XMITTER are controlled separately, either one or both can be in the polled mode of operation.

In this mode the user's program will check RCVR and XMITTED status via the LSR. As stated previously:

LSR0 will be set as long as there is one byte in the RCVR FIFO.

LSR1 to LSR4 will specify which error(s) has occurred. Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since IER2=0.

LSR5 will indicate when the XMIT FIFO is empty.

LSR6 will indicate that both the XMIT FIFO and shift register are empty.

LSR7 will indicate whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode. However, the RCVR and XMIT FIFO's are still fully capable of holding characters.

AC, DC TIMING SPECIFICATION

Absolute Maximum Ratings

Temperature Under Bias	0°C to +70°C
Storage or Output Voltage	-65°C to +150°C
All Input or Output Voltages with respect to VSS	-0.5°C to +7.0°C
Power Dissipation	1W

If Military/Aerospace specified devices are required, contact CMD for availability and specifications. Note: Maximum rating indicates limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC electrical characteristics.

DC Electrical Characteristics

TA = 0°C to +70°C, VCC = +5V ± 5%, VSS = 0V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Units
VILX	Clock Input Low Voltage		-0.5V	0.8	V
VIHX	Clock Input High Voltage		2.0	VCC	V
VIL	Input Low Voltage		-0.5V	0.8	V
VIH	Input High Voltage		2.0	VCC	V
VOL	Output Low Voltage	IOL = 2 mA on all (Note 1)		0.4	V
VOH	Output High Voltage	IOH = -1.0 mA (Note 1)	2.4		V
ICC(AV)	Avg. Power Supply Current (VCC)	VCC = 5.25V, f = 4MHz No Loads on outputs SIN, DSR, DCD CTS, RI = 2.0V All other inputs = 0.8V		10	mA
IIL	Input Leakage	VCC = 5.25V, VSS = 0V All other pins floating		±10	μA
ICL	Clock Leakage	VOUT = 0V, 5.25V		±10	μA
IOZ	Tri-State® Leakage	VCC = 5.25V, VSS = 0V VOUT = 0V, 5.25V 1) Chip deselected 2) WRITE mode, chip selected		±10	μA
VILMR	MR Schmitt VIL			0.8	V
VIHMR	MR Schmitt VIH		2.0		V

(Note 1): Does not apply to XOUT

Capacitance

TA = 25°C, VCC = VSS = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CXIN	Clock Input Capacitance			15	20	pF
CXOUT	Clock Output Capacitance	fc = 1MHz		20	30	pF
CIN	Input Capacitance	Unmeasured pins returned		6	10	pF
COUT	Output Capacitance	to VSS		10	20	pF

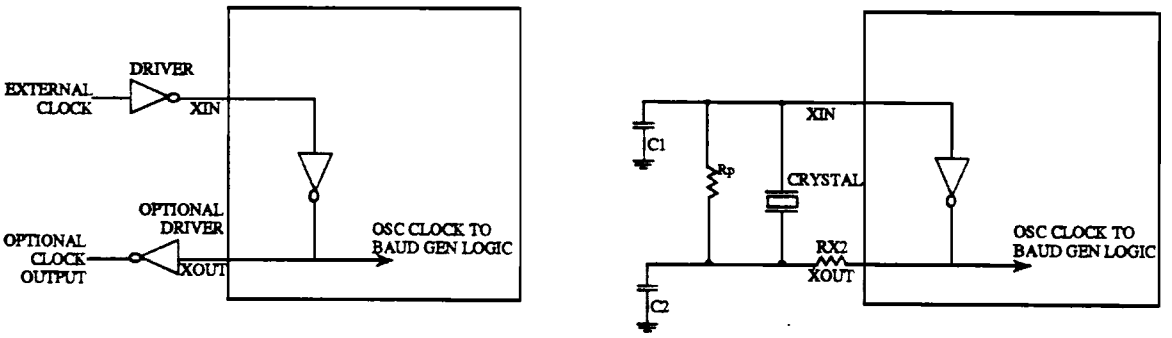
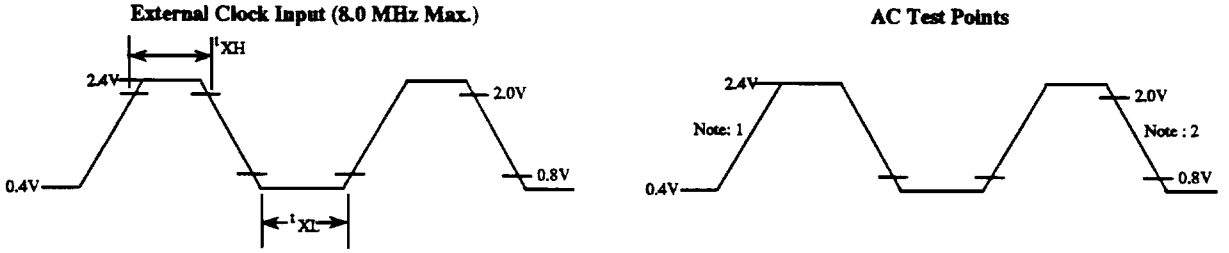


Figure 5 - Typical Crystal Oscillator Network

CRYSTAL	Rp	RX2	C1	C2
3.1 MHz	1MΩ	1.5k	10-30pF	40-60pF
1.8 MHz	1MΩ	1.5k	10-30pF	40-60pF



Note 1: Input drive levels are 0.4V (low) and 2.4V (high) for AC tests.
Note 2: Output compare levels are 0.8V (low) and 2.0V (high) for AC tests.

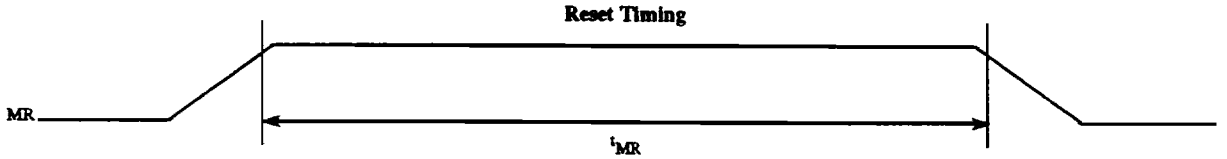


Figure 6 - Clock and Reset Timing

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{XH}	Duration of External Clock High Pulse	55		nsec	External Clock (8.0 MHz Max)
t_{XL}	Duration of External Clock Low Pulse	55		nsec	1TTL Load (8.0 MHz Max)
t_{MR}	Master Reset Pulse Width	5.0		μsec	1 TTL Load

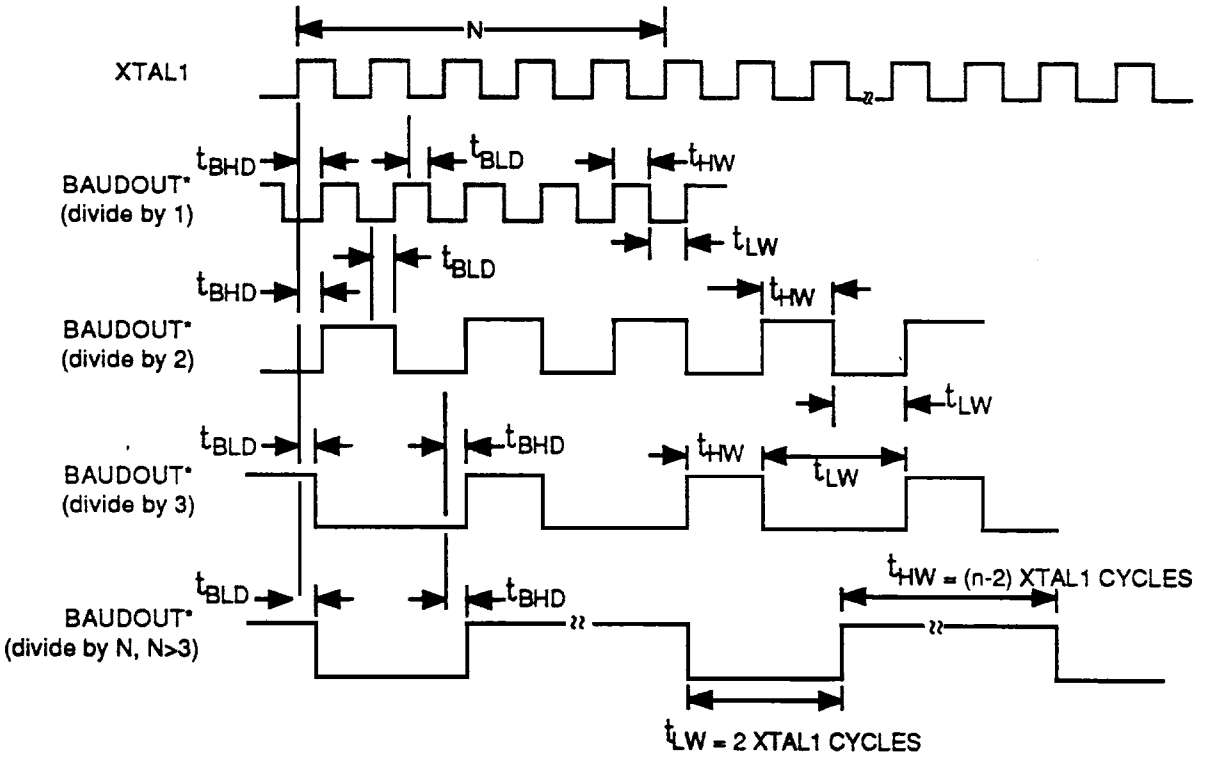


Figure 7 - Baud Rate Generator Timing

Symbol	Parameter	Min	Max	Units	Test Conditions
N	Baud Rate Divisor	1	(2^{16}-1)		
t_{BLD}	Baud Output Negative Edge Delay		125	nsec	100pF Load
t_{BHD}	Baud Output Positive Edge Delay		125	nsec	100pF Load
t_{LW}	Baud Output Low Time	75		nsec	100pF Load (fx = 8.0 MHz + 2)
t_{HW}	Baud Output High Time	100		nsec	100pF Load (fx = 8.0 MHz + 2)

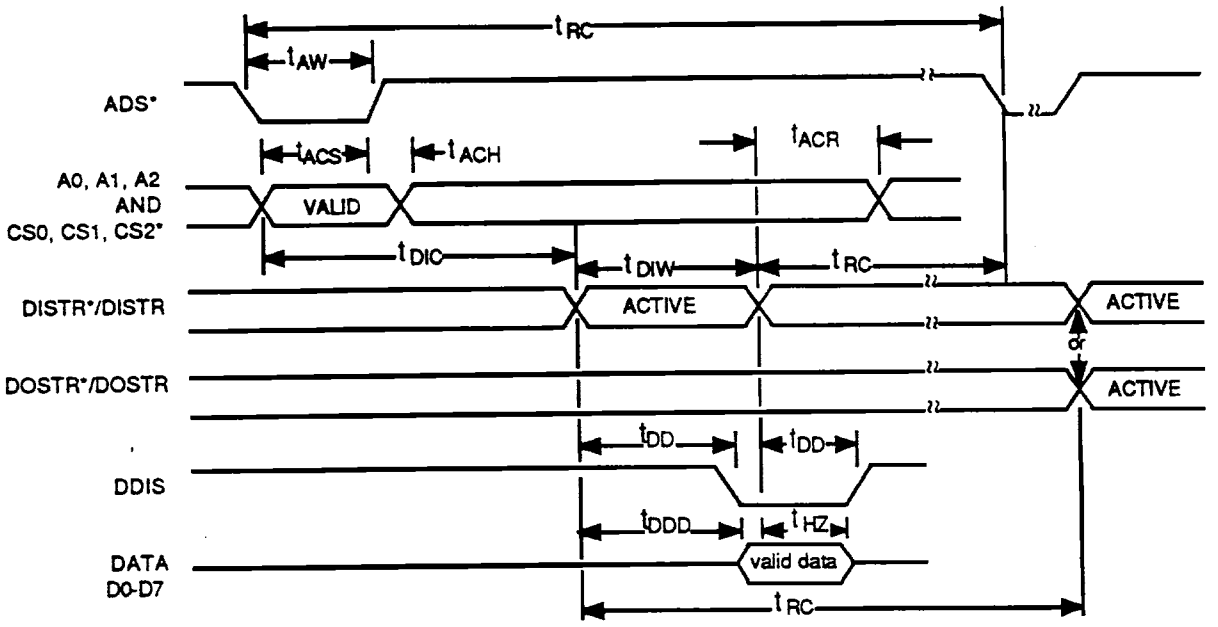


Figure 8 - Read Cycle Timing

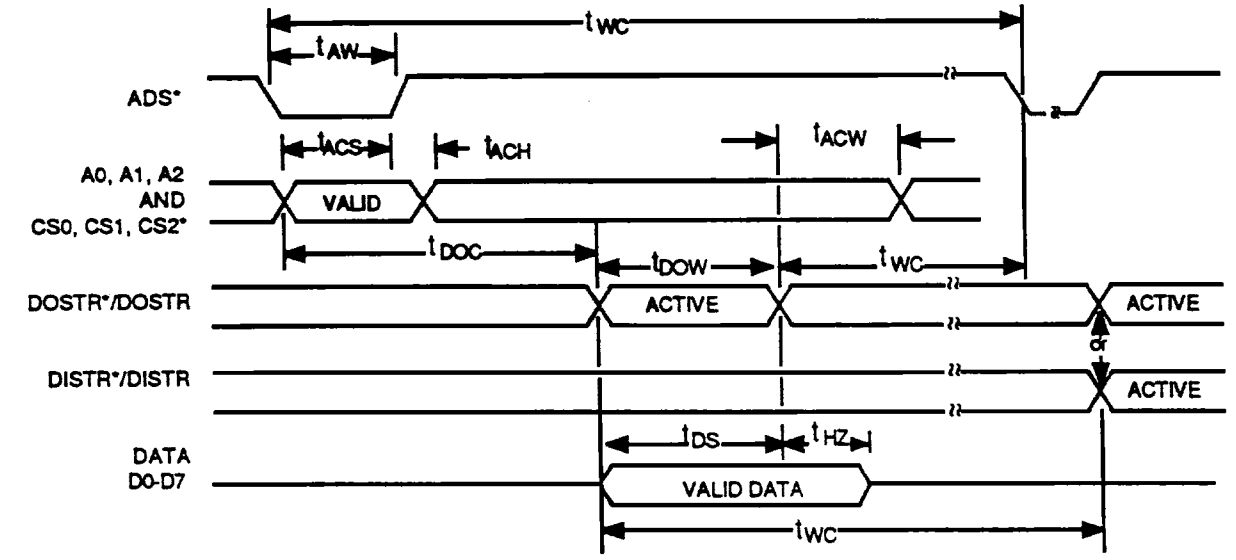
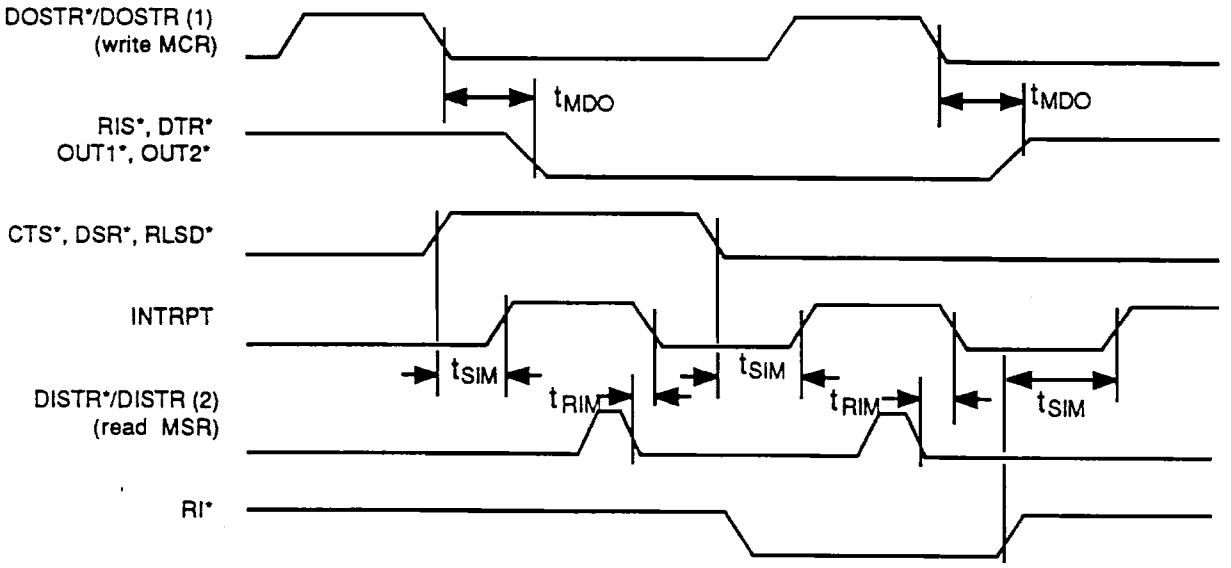


Figure 9 - Write Cycle Timing

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{AW}	Address Strobe Width	60		nsec	1 TTL Load
t_{ACS}	Address and Chip Select Setup Time	60		nsec	1 TTL Load
t_{ACH}	Address and Chip Select Hold Time	0		nsec	1 TTL Load
t_{DIW}	DISTR*/DISTR Strobe Width	125		nsec	1 TTL Load
t_{RC}	Read Cycle Delay	125		nsec	1 TTL Load
RC	Read Cycle (t_{DIC} + t_{DIW} + t_{RC})	280 (non FIFO mode) 425 (FIFO mode)		nsec	1 TTL Load
t_{DD}	DISTR*/DISTR to Driver Disable Delay	0	60	nsec	@ 100pF Load
t_{DDD}	Delay from DISTR*/DISTR to Data		125	nsec	@ 100pF Load
t_{HZ}	DISTR*/DISTR to floating Data Delay	0	100	nsec	@ 100pF Load
t_{DOW}	DOSTR*/DOSTR Strobe Width	100		nsec	1 TTL Load
t_{WC}	Write Cycle Delay	150		nsec	1 TTL Load
WC	Write Cycle (t_{DOC} + t_{DOW} + t_{WC})	280		nsec	1 TTL Load
t_{DS}	Data Setup Time	30		nsec	1 TTL Load
t_{DH}	Data Hold Time	30		nsec	1 TTL Load
t_{DIC}(*)	DISTR*/DISTR delay from chip Select or Address	30		nsec	1 TTL Load
t_{DOC}(*)	DOSTR*/DOSTR delay from chip Select or Address	30		nsec	1 TTL Load
t_{ACR}(*)	Address and Chip Select Hold time from DISTR*/DISTR	20		nsec	1 TTL Load
t_{ACW}(*)	Address and Chip Select Hold time from DISTR*/DISTR	30		nsec	1 TTL Load

(*) Only applicable when ADS* is tied low.

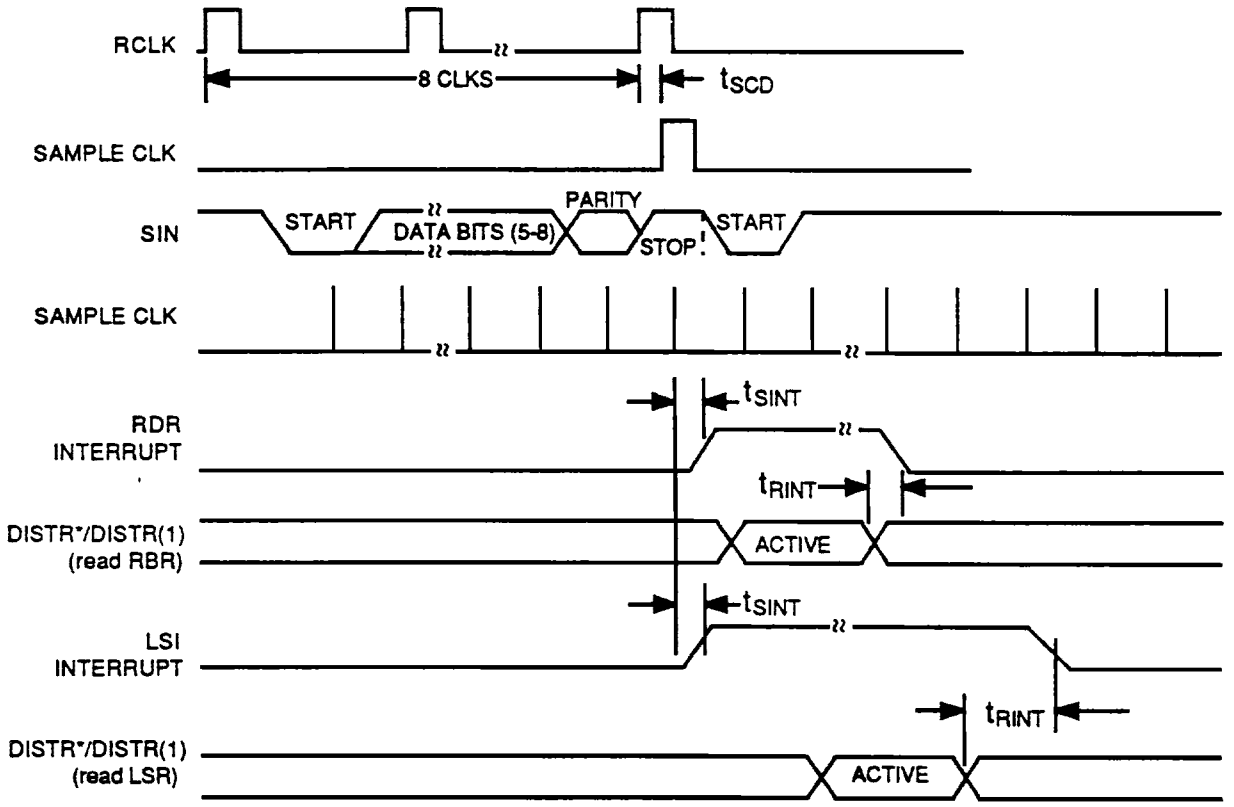


NOTES :
(1) See Write cycle Timing
(2) See Read cycle Timing

Figure 10 - Modem Control Timing

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{MDO}	Delay from DOSTR*/DOSTR (WR MCR) to Output		0.200	μsec	100pF Load
t_{SIM}	Delay to Set Interrupt from MODEM Input		0.250	μsec	100pF Load
t_{RIM}	Delay to Reset Interrupt from DISTR*/DISTR (RD MSR)		0.250	μsec	100pF Load

(*) Only applicable when ADS* is tied low.



Note:
(1) See Read Cycle timing

Figure 11 - Receiver Timing

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{SCD}	Delay from RCLK to Sample Time		2	μsec	
t_{SINT}	Delay from Stop to Set Interrupt		1(*)	RCLK Cycles	
t_{RINT}	Delay from DISTR*/DISTR (RD RBR or RD LSR) Reset Interrupt		1	μsec	100pF Load

(*) When receiving the first byte in FIFO mode t_{SINT} will be delayed 3 RCLK cycles, except for a timeout interrupt where t_{SINT} will be delayed 8 RCLK cycles.

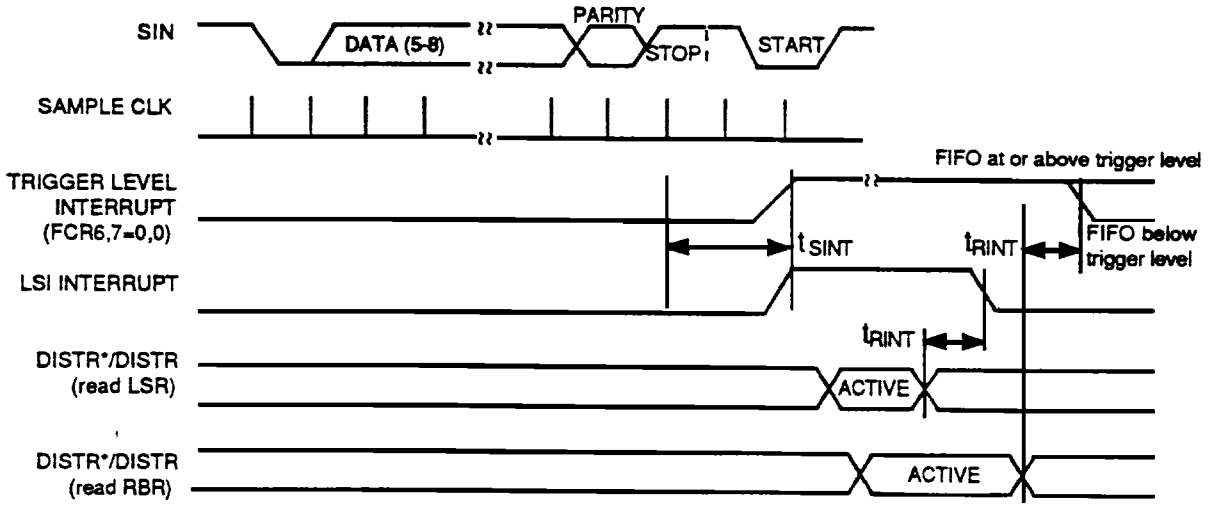


Figure 12 - RCVR FIFO Timing for First Byte

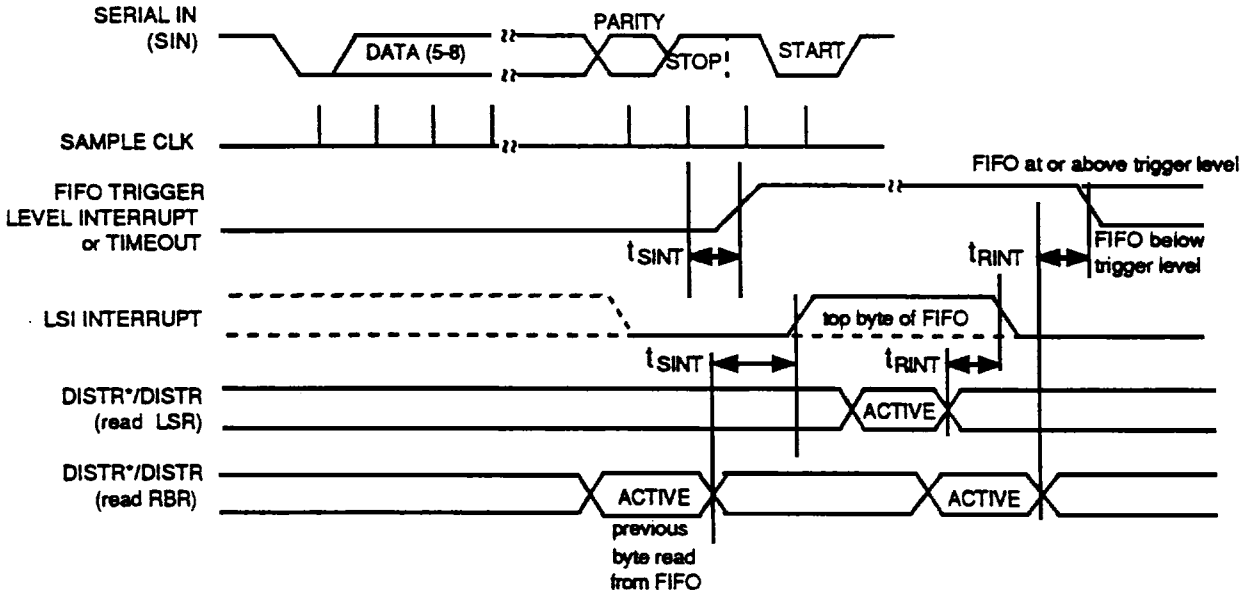
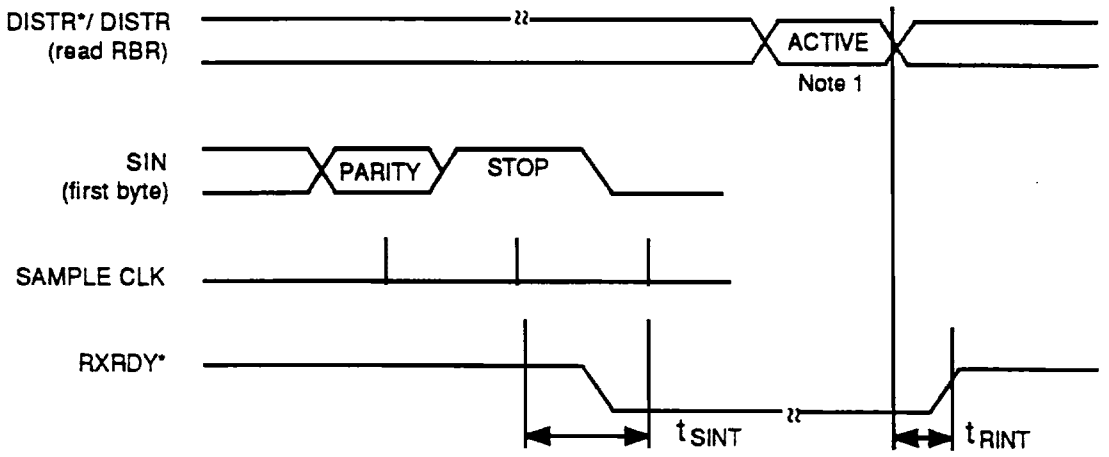
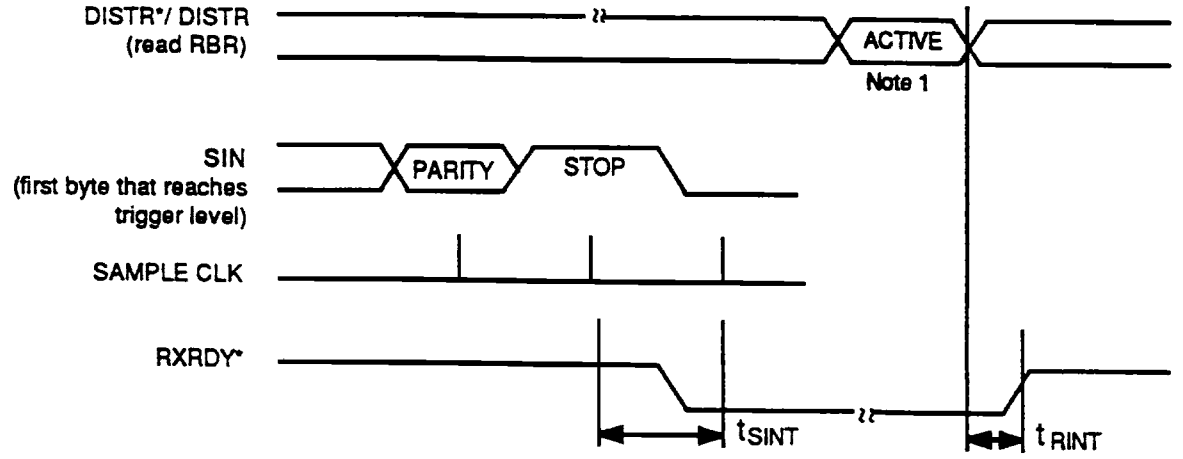


Figure 13 - RCVR FIFO Timing after First Byte (RDR already set)



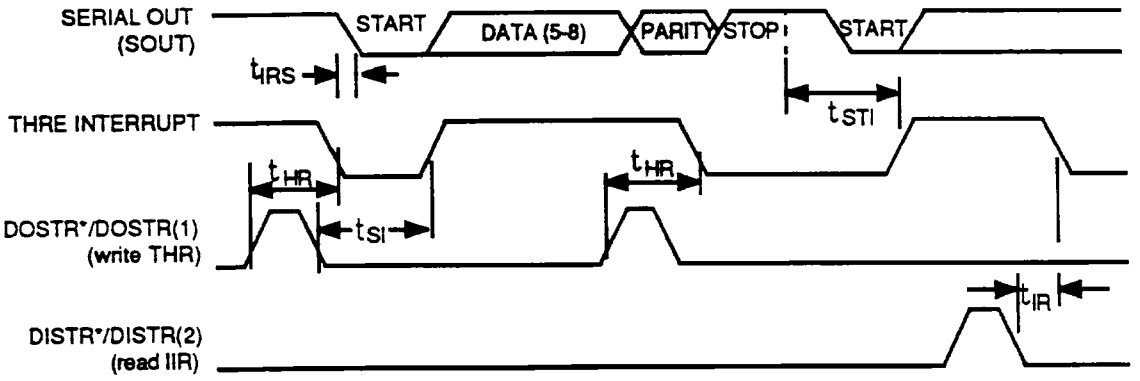
Note 1
FCR0 = 1 : Reading of last byte from FIFO
FCR0 = 0 : Reading RBR

Figure 14 - Receiver DMA Timing (FCR0 = 0 or FCR0 = 1 and FCR3 = 0) Mode 0



Note 1
Reading of last byte from FIFO

Figure 15 - Receiver DMA Timing (FCR0 = 1 and FCR3 = 1) Mode 1



NOTES:
(1) See Write Cycle Timing
(2) See Read Cycle Timing

Figure 16 - Transmitter Timing

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{HR}	Delay from DOSTR*/ DOSTR/ (WR THR) to Reset Interrupt		0.175	µsec	100pF Load
t_{IR}	Delay from DISTR*/DISTR (RD IIR) to Reset Interrupt (THRE)		0.250	µsec	100pF Load
t_{IRS}	Delay from Initial INTRPT reset to transmit Start	0	16	BAUDOUT Cyles	
t_{SI}	Delay from Initial Write to Interrupt	16	32	BAUDOUT Cycles	(Note 1)
t_{STI}	Delay from Stop to Interrupt (THRE)	8	8	BAUDOUT Cyles	(Note 1)
t_{SXA}	Delay from Start to TXRDY Active	0	8	BAUDOUT Cycles	100pF Load
t_{WXI}	Delay from Write to TXRDY Inactive	0	0.195	µsec	100pF Load

Note 1: This delay will be lengthened by 1 character time minus the last STOP bit time if the transmitter internal circuit is active (see FIFO Interrupt Mode Operation).

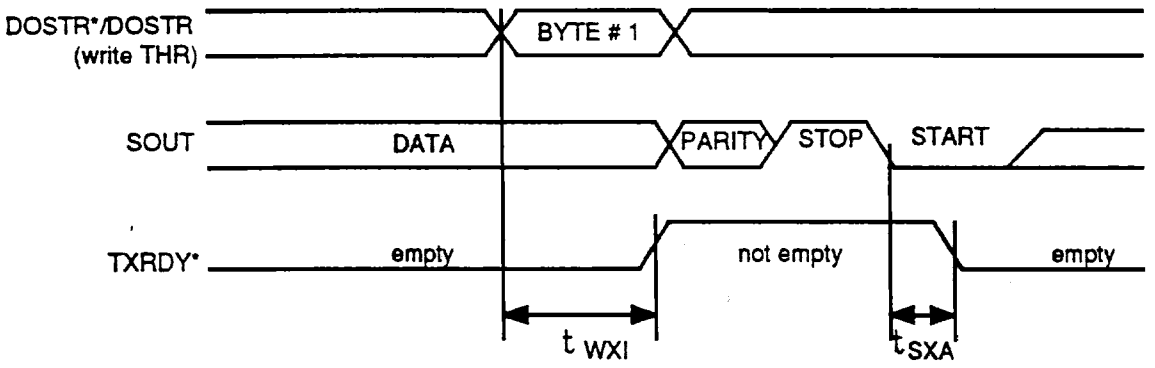


Figure 17 - Transmitter Ready Timing in DMA
(FCR0 = 0 or FCR0 = 1 and FCR3 = 0)
Mode 0

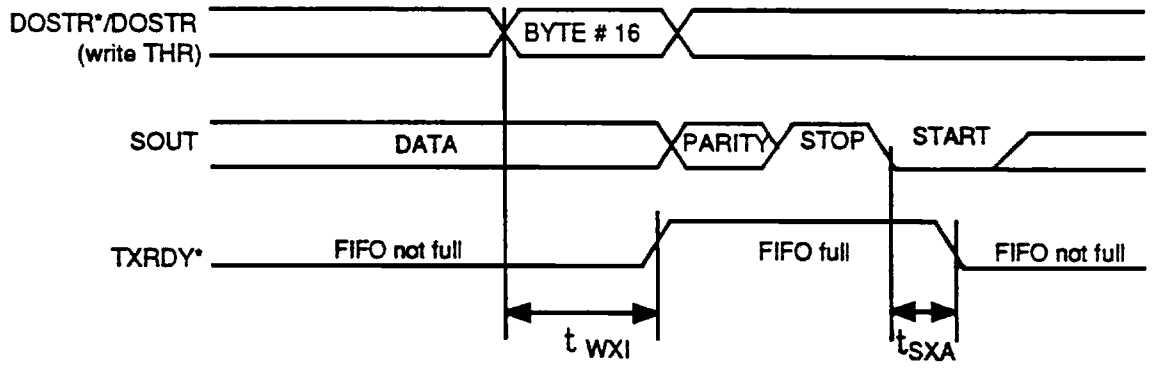


Figure 18 - Transmitter Ready Timing in DMA
(FCR0 = 0 or FCR0 = 1 and FCR3 = 0)
Mode 1

Ordering Information

Part Number	Package	Operating Temperature
CM16C550ACP-40	DIP	0°C to +70°C
CM16C550ACQ-44	PLCC	0°C to +70°C

Life Support Policy

CMD's products are not to be used in life support devices without prior written authorization.

Disclaimer

No responsibility is assumed by California Micro Devices Corp. for use of this product nor for any infringements of patents and trademarks or other rights of third parties resulting from its use. No license is granted under any patents, patent rights or trademarks of California Micro Devices Corp. California Micro Devices Corp. reserves the right to make changes in specifications at any time without notice.

NOTES: