HARRIS SEMICONDUCTOR

CD4098BMS

December 1992

CMOS Dual Monostable Multivibrator

Features

- High Voltage Type (20V Rating)
- Retriggerable/Resettable Capability
- Trigger and Reset Propagation Delays Independent of RX, CX
- Triggering from Leading or Trailing Edge
- Q and $\overline{Q}$ Buffered Outputs Available
- Separate Resets
- Wide Range of Output Pulse Widths
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Standardized Symmetrical Output Characteristics
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

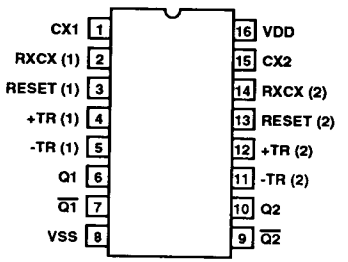
Applications

- Pulse Delay and Timing
- Pulse Shaping

Astable Multivibrator

Pinout

CD4098BMS
TOP VIEW



TERMINALS 1, 8, 15 ARE ELECTRICALLY CONNECTED INTERNALLY

Description

CD4098BMS dual monostable multivibrator provides stable retriggerable/resettable one shot operation for any fixed voltage timing application.

An external resistor (RX) and an external capacitor (CX) control the timing for the circuit. Adjustment of RX and CX provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of RX and CX.

Leading edge triggering (+TR) and trailing edge triggering (-TR) inputs are provided for triggering from either edge of an input pulse. An unused +TR input should be tied to VSS. An unused -TR input should be tied to VDD. A RESET (on low level) is provided for immediate termination of the output pulse or to prevent output pulses when power is turned on. An unused RESET input should be tied to VDD. However, if an entire section of the CD4098BMS is not used, its RESET should be tied to VSS. See Table 9.

In normal operation the circuit triggers (extends the output pulse one period) on the application of each new trigger pulse. For operation in the non-retriggerable mode, $\overline{Q}$ is connected to -TR when leading edge triggering (+TR) is used or Q is connected to +TR when trailing edge triggering (-TR) is used.

The time period (T) for this multivibrator can be approximated by: $TX = {}^{1}/_{2}RXCX$ for CX 3 0.01μF. Time periods as a function of RX for values of CX and VDD are given in Figure 8. Values of T vary from unit to unit and as a function of voltage, temperature, and RXCX.

The minimum value of external resistance, RX, is 5kΩ. The maximum value of external capacitance, CX, is 100μF. Figure 9 shows time periods as a function of CX for values of RX and VDD.

The output pulse width has variations of ±2.5% typically, over the temperature range of -55°C to +125°C for CX = 1000pF and RX = 100kΩ.

For power supply variations of ±5%, the output pulse width has variations of ±0.5% typically, for VDD = 10V and 15V and ±1% typically, for VDD = 5V at CX = 1000pF and RX = 5kΩ.

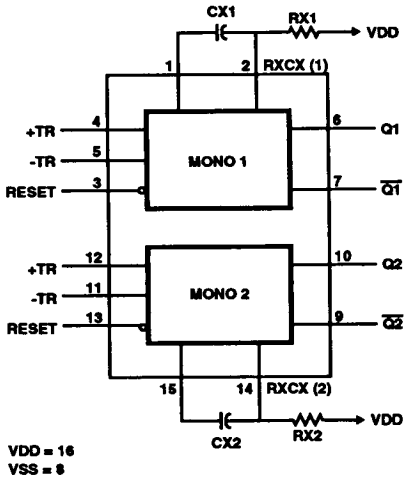
The CD4098BMS is supplied in these 16-lead outline packages:

Braze Seal DIP	H4T
Frit Seal DIP	H1F
Ceramic Flatpack	H6W

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3332

Functional Diagram



Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs ..... -0.5V to VDD +0.5V
DC Input Current, Any One Input ..... ±10mA
Operating Temperature Range ..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) ..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20V	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20V	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES:
1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay +TR, -TR to Q, $\overline{Q}$	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND RX = 5K to 10KΩ, CX ≥ 15pF	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Transition Time	TTHL1	VDD = 5V, VIN = VDD or GND RX = 5K to 10KΩ, CX = 15pF to 10,000pF	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Transition Time (Note 2)	TTLH1	VDD = 5V, VIN = VDD or GND RX = 5K to 10KΩ, CX ≥ 15pF	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay +TR, -TR to Q, $\overline{Q}$ CX ≥ 15pF	TPHL1 TPLH1	VDD = 10V	1, 2, 3, 4	+25°C	-	250	ns
		VDD = 15V	1, 2, 3, 4	+25°C	-	200	ns
Propagation Delay Reset CX ≥ 15pF	TPHL2 TPLH2	VDD = 5V	1, 2, 3	+25°C	-	450	ns
		VDD = 10V	1, 2, 3, 4	+25°C	-	250	ns
		VDD = 15V	1, 2, 3,4	+25°C	-	150	ns
Transition Time CX = 15pF to 10,000pF	TTHL1	VDD = 10V	1, 2, 3, 4	+25°C	-	100	ns
		VDD = 15V	1, 2, 3, 4	+25°C	-	80	ns
Transition Time CX = 0.01µF to 0.1µF	TTLH2 TTHL2	VDD = 5V	1, 2, 3	+25°C	-	300	ns
		VDD = 10V	1, 2, 3, 5	+25°C	-	150	ns
		VDD = 15V	1, 2, 3, 5	+25°C	-	130	ns
Transition Time CX = 0.1µF to 1µF	TTHL3	VDD = 5V	1, 2, 3	+25°C	-	500	ns
		VDD = 10V	1, 2, 3, 4	+25°C	-	300	ns
		VDD = 15V	1, 2, 3, 4	+25°C	-	160	ns
Transition Time CX ≥ 15pF	TTLH1	VDD = 10V	1, 2, 3, 4	+25°C	-	100	ns
		VDD = 15V	1, 2, 3, 4	+25°C	-	80	ns
Minimum Reset Pulse Width, CX = 15pF	TW	VDD = 5V	1, 2, 3, 5	+25°C	-	200	ns
		VDD = 10V	1, 2, 3, 5	+25°C	-	80	ns
		VDD = 15V	1, 2, 3, 5	+25°C	-	60	ns
Minimum Reset Pulse Width, CX = 1000pF	TW	VDD = 5V	1, 2, 3, 5	+25°C	-	1200	ns
		VDD = 10V	1, 2, 3, 5	+25°C	-	600	ns
		VDD = 15V	1, 2, 3,5	+25°C	-	500	ns
Minimum Reset Pulse Width, CX = 0.1µF	TW	VDD = 5V	1, 2, 3, 5	+25°C	-	50	µs
		VDD = 10V	1, 2, 3, 5	+25°C	-	30	µs
		VDD = 15V	1, 2, 3, 5	+25°C	-	20	µs
Pulse Width Match Between Circuits In Same Package	TW	VDD = 5V	1, 2, 3, 6	+25°C	-	10	%
		VDD = 10V	1, 2, 3, 6	+25°C	-	15	%
		VDD = 15V	1, 2, 3, 6	+25°C	-	15	%
Trigger Rise or Fall Time	TRTR TFTR	VDD = 5V to 15V	1, 2	+25°C	-	100	µs
Input Capacitance	CIN	Any Inputs	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, inputs tR, tF < 20ns.
4. RX = 5K to 10MΩ.
5. RX = 100kΩ
6. RX = 10kΩ

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	6, 7, 9, 10	1-5, 8, 11-15	16			
Static Burn-In 2 Note 1	6, 7, 9, 10	1, 8, 15	2-5, 11-14, 16			
Dynamic Burn-In Note 1	-	1, 4, 8, 12, 15	2, 14, 16	6, 7, 9, 10	5, 11	3, 13
Irradiation Note 2	2, 6, 7, 9, 10, 14	1, 8, 15	3-5, 11-13, 16			

NOTE:

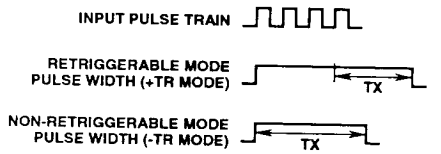
1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

TABLE 9. FUNCTIONAL TERMINAL CONNECTIONS

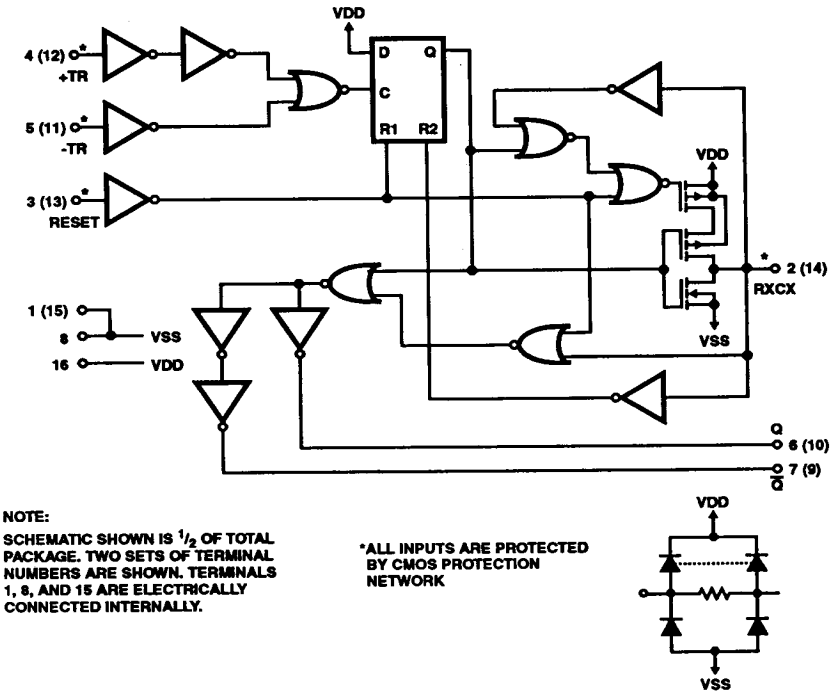
FUNCTION	VDD TO TERM. NO.		VSS TO TERM. NO.		INPUT PULSE TO TERM. NO.		OTHER CONNECTIONS	
	MONO 1	MONO 2	MONO 1	MONO 2	MONO 1	MONO 2	MONO 1	MONO 2
Leading Edge Trigger/ Retriggerable	3, 5	11, 13			4	12		
Leading Edge Trigger/ Non-Retriggerable	3	13			4	12	5-7	11-9
Trailing Edge Trigger/ Retriggerable	3	13	4	12	5	11		
Trailing Edge Trigger/ Non-Retriggerable	3	13			5	11	4-6	12-10
Unused Section	5	11	3, 4	12, 13				

NOTES:

1. A retriggerable one-shot multivibrator has an output pulse width which is extended one full time period (TX) after application of the last trigger pulse. The minimum time between retriggering edges (or trigger and retrigger edges) is 40% of (TX).
2. A non-retriggerable one-shot multivibrator has a time period TX referenced from the application of the first trigger pulse.



Logic Diagram



NOTE:
SCHEMATIC SHOWN IS $^1/_2$ OF TOTAL PACKAGE. TWO SETS OF TERMINAL NUMBERS ARE SHOWN. TERMINALS 1, 8, AND 15 ARE ELECTRICALLY CONNECTED INTERNALLY.

*ALL INPUTS ARE PROTECTED BY CMOS PROTECTION NETWORK

FIGURE 1. LOGIC DIAGRAM

Typical Performance Characteristics

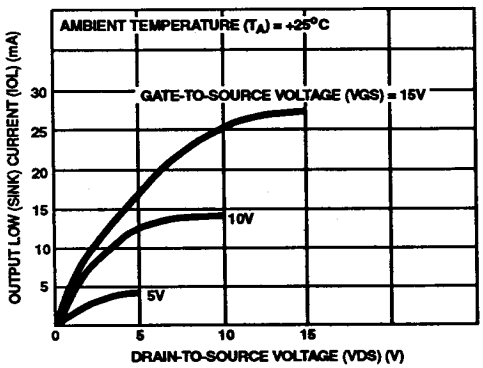


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

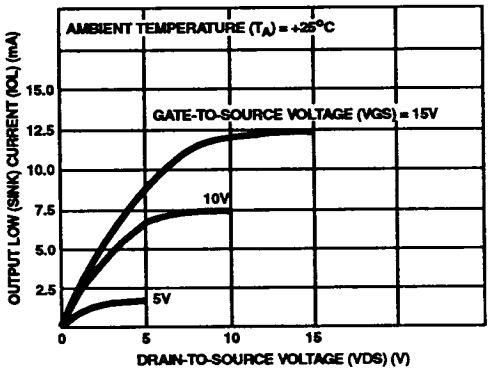


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

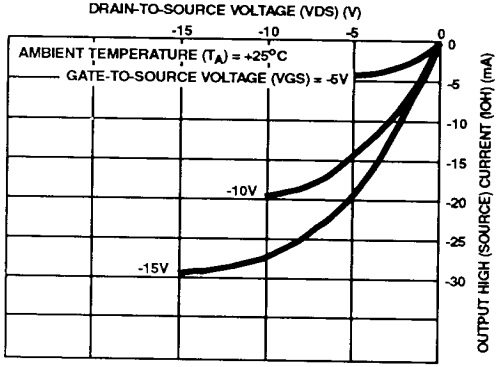


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

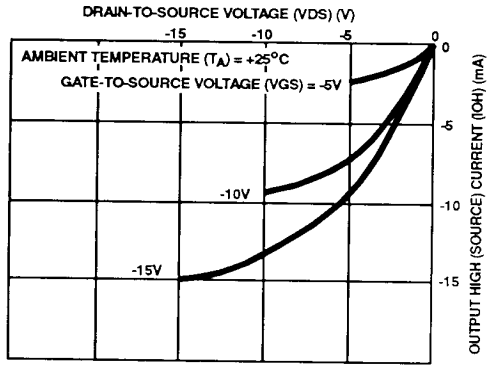


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

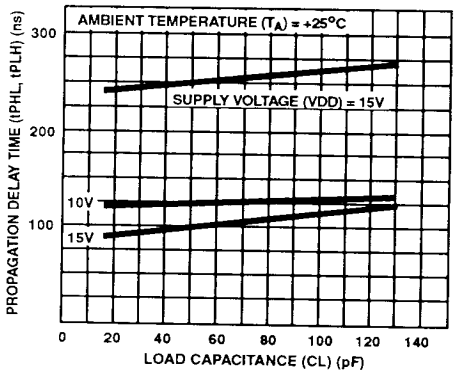


FIGURE 6. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE, TRIGGER INTO Q OUT (ALL VALUES OF CX AND RX).

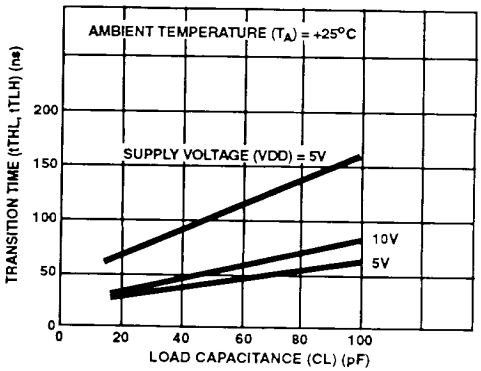


FIGURE 7. TRANSITION TIME vs LOAD CAPACITANCE FOR RX = 5kΩ-10000kΩ AND CX = 15pF-10000pF

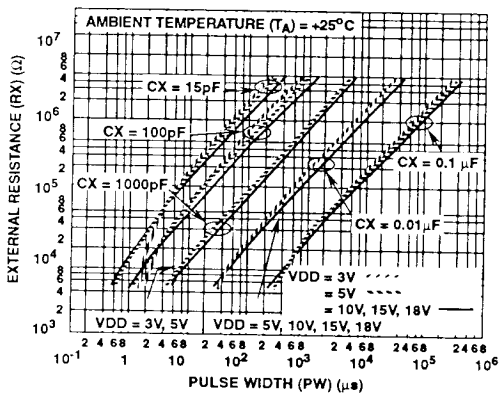


FIGURE 8. TYPICAL EXTERNAL RESISTANCE vs PULSE WIDTH

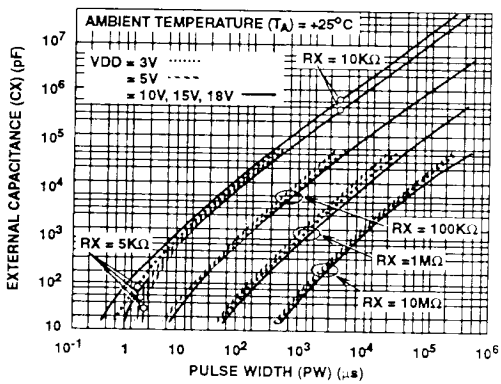


FIGURE 9. TYPICAL EXTERNAL CAPACITANCE vs PULSE WIDTH

Typical Performance Characteristics (Continued)

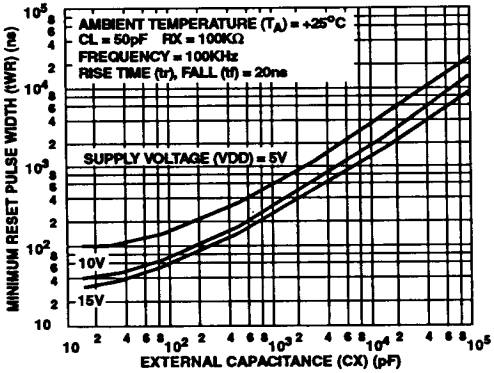
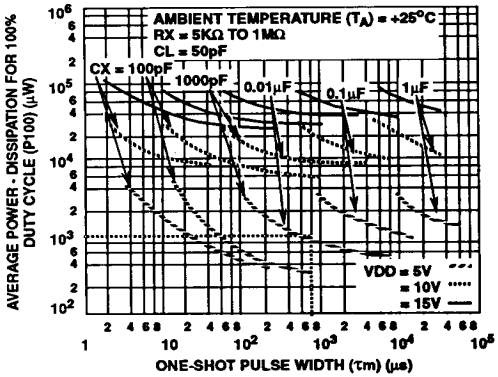


FIGURE 10. TYPICAL MINIMUM RESET PULSE WIDTH vs EXTERNAL CAPACITANCE



To calculate average power dissipation(P) for less than 100% duty cycle:

P100 = average power for 100% duty cycle:

$$P = \left(\frac{tm}{\tau T}\right) P100 \text{ where } \tau m = \text{one shot pulse width}$$

τT = trigger pulse period

e.g. For τm = 600μs, τT = 1000μs. CX = 0.01mF

VDD = 5V

$$P1 = \left(\frac{600}{1000}\right) 10^3\ \mu W = 600\mu W \text{ (see dotted line on graph)}$$

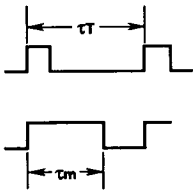


FIGURE 11. AVERAGE POWER DISSIPATION vs ONE-SHOT PULSE WIDTH

Applications

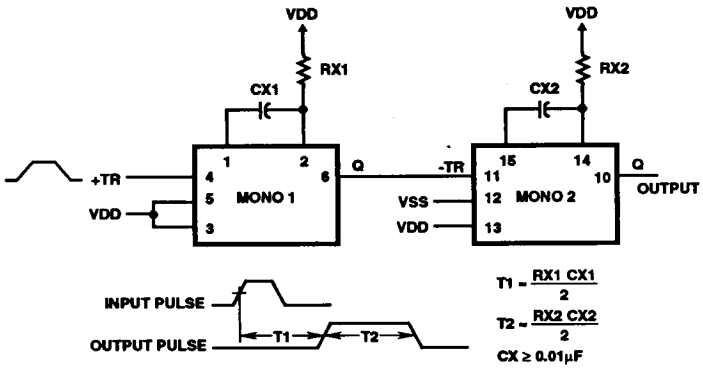
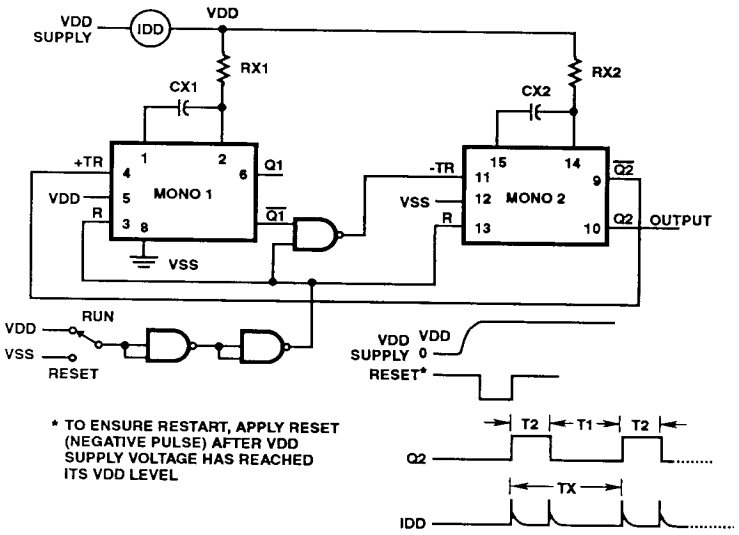


FIGURE 12. PULSE DELAY

Applications (Continued)



* TO ENSURE RESTART, APPLY RESET (NEGATIVE PULSE) AFTER VDD SUPPLY VOLTAGE HAS REACHED ITS VDD LEVEL

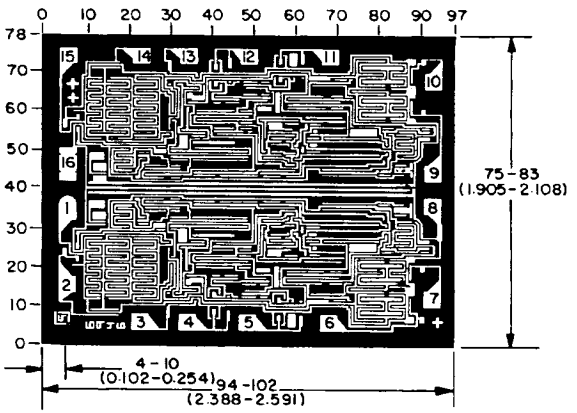
IDD, TX vs RX

RX	IDD (AVG.)	TX (T1 + T2)	VDD
10kΩ ↓ 10MΩ	1mA ↓ 0.05mA	3.8µs ↓ 0.5s	5V
	2.5mA ↓ 0.5mA	3.2µs ↓ 0.5s	10V
	5mA ↓ 1mA	3µs ↓ 0.5s	10V

NOTES:
1. All values are typical.
2. CX range: 0.0001µF to 0.1µF

FIGURE 13. ASTABLE MULTIVIBRATOR WITH RESTART AFTER RESET CAPABILITY

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches