Am29BDD160G Known Good Die

Data Sheet Supplement, Revision I

July 2003

The following document specifies Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal datasheet improvement and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

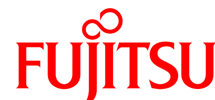
Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

Publication Number **26994** Revision **A** Amendment **4** Issue Date **September 9, 2004**



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SUPPLEMENT

AMD

Am29BDD160G Known Good Die—Die Revision 1

16 Megabit (1 M x 16-Bit/512 K x 32-Bit)
CMOS 2.5 Volt-only Burst Mode, Dual Boot, Simultaneous Read/Write Flash Memory

DISTINCTIVE CHARACTERISTICS

ARCHITECTURE ADVANTAGES

- **Simultaneous Read/Write operations**
  - Data can be continuously read from one bank while executing erase/program functions in other bank
  - Zero latency between read and write operations
  - Two bank architecture: 75%/25%
- **User-Defined x16 or x32 Data Bus**
- **Dual Boot Block**
  - Top and bottom boot in the same device
- **Flexible sector architecture**
  - Eight 8 Kbytes, thirty 64 Kbytes, and eight 8 Kbytes sectors
- **Manufactured on 0.17 µm process technology**
- **SecSi (Secured Silicon) Sector (256 Bytes)**
  - *Factory locked and identifiabl*e: 16 bytes for secure, random factory Electronic Serial Number; remainder may be customer data programmed by AMD
  - *Customer lockable:* Can be read, programmed or erased just like other sectors. Once locked, data cannot be changed
- **Programmable Burst interface**
  - Interface to any high performance processor
  - Modes of Burst Read Operation:
  - *Linear Burst*: 4 double words (x32), 8 words (x16) and double words (x32), and 32 words (x16) with wrap around
- **Single power supply operation**
  - Optimized for 2.5 to 2.75 Volt read, erase, and program operations
- **Compatibility with JEDEC standards (JC42.4)**
  - Software compatible with single-power supply Flash
  - Backward-compatible with AMD Am29LV and Am29F flash memories

PERFORMANCE CHARACTERISTICS

- **High performance read access**
  - Initial/random access times as fast as 64 ns
  - Burst access time as fast as 10 ns
- **Ultra low power consumption**
  - Burst Mode Read: 90 mA @ 56 MHz max
  - Program/Erase: 50 mA max
  - Standby mode: CMOS: 250 µA max
- **Minimum 1 million write cycles guaranteed per sector**
- **20 year data retention at 125°C**
- **VersatileI/O™ control**
  - Device generates data output voltages and tolerates data input voltages as determined by the voltage on the V_{IO} pin
  - 1.65 V to 2.75 V compatible I/O signals

SOFTWARE FEATURES

- **Persistent Sector Protection**
  - A command sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector (requires only V_{CC} levels)
- **Password Sector Protection**
  - A sophisticated sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector using a user-definable 64-bit password
- **Supports Common Flash Interface (CFI)**
- **Unlock Bypass Program Command**
  - Reduces overall programming time when issuing multiple program command sequences
- **Data# Polling and toggle bits**
  - Provides a software method of detecting program or erase operation completion

HARDWARE FEATURES

- **Program Suspend/Resume & Erase Suspend/Resume**
  - Suspends program or erase operations to allow reading, programming, or erasing in same bank
- **Hardware Reset (RESET#), Ready/Busy# (RY/BY#), and Write Protect (WP#) inputs**
- **ACC input**
  - Accelerates programming time for higher throughput during system production
- **Quality and reliability levels equivalent to standard packaged components**

Publication No. **26994** Revision **A** Amendment **4**
Issue Date: **September 9, 2004**

GENERAL DESCRIPTION

The Am29BDD160G in Known Good Die (KGD) form is an 16 Mbit, 2.5 volt-only Flash memory. AMD defines KGD as standard product in die form, tested for functionality and speed. AMD KGD products have the same reliability and quality as AMD products in packaged form.

Am29BDD160G Features

The Am29BDD160G is a 16 Megabit, 2.5 Volt-only single power supply burst mode flash memory device. The device can be configured for either 1,048,576 words in 16-bit mode or 524,288 double words in 32-bit mode. The device can also be programmed in standard EPROM programmers. The device offers a configurable burst interface to 16/32-bit microprocessors and microcontrollers.

To eliminate bus contention, each device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls. Additional control inputs are required for synchronous burst operations: Load Burst Address Valid (ADV#), and Clock (CLK).

Each device requires only a **single 2.5 or 2.6 Volt power supply** (2.5 V to 2.75 V) for both read and write functions. A 12.0-volt V_{PP} is not required for program or erase operations, although an acceleration pin is available if faster programming performance is required.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**.

The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

The **Simultaneous Read/Write architecture** provides simultaneous operation by dividing the memory space into two banks. The device can begin programming or erasing in one bank, and then simultaneously read from the other bank, with zero latency.

The device provides a 256-byte **SecSi™ (Secured Silicon) Sector** with an one-time-programmable (OTP) mechanism.

In addition, the device features several levels of sector protection, which can disable both the program and erase operations in certain sectors or sector groups: **Persistent Sector Protection** is a command sector protection method that replaces the old 12 V controlled protection method; **Password Sector Protection** is a highly sophisticated protection method that requires a password before changes to certain sectors or sector groups are permitted; **WP# Hardware Protection** prevents program or erase in the two outermost 8 Kbytes sectors of the larger bank.

The device defaults to the Persistent Sector Protection mode. The customer must then choose if the Standard or Password Protection method is most desirable. The WP# Hardware Protection feature is always available, independent of the other protection method chosen.

The **VersatileI/O™ (V_{CCQ})** feature allows the output voltage generated on the device to be determined based on the V_{IO} level. This feature allows this device to operate in the 1.8 V I/O environment, driving and receiving signals to and from other 1.8 V devices on the same bus. In addition, inputs and I/Os that are driven externally are capable of handling 3.6 V.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, by reading the DQ7 (Data# Polling), or DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **password and software sector protection** feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system at V_{CC} level.

The **Program/Erase Suspend/Erase Resume** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

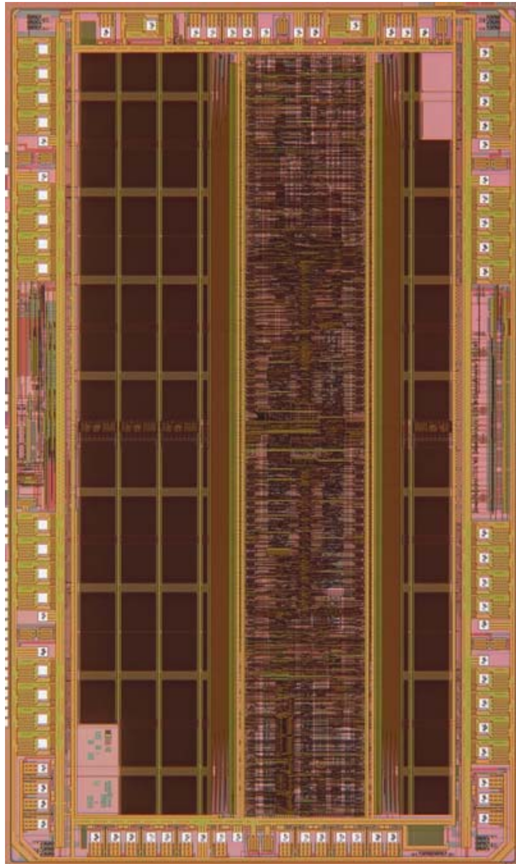
Electrical Specifications

Refer to the Am29BDD160G data sheet, publication number 24960, for full electrical specifications on the Am29BDD160G in KGD form.

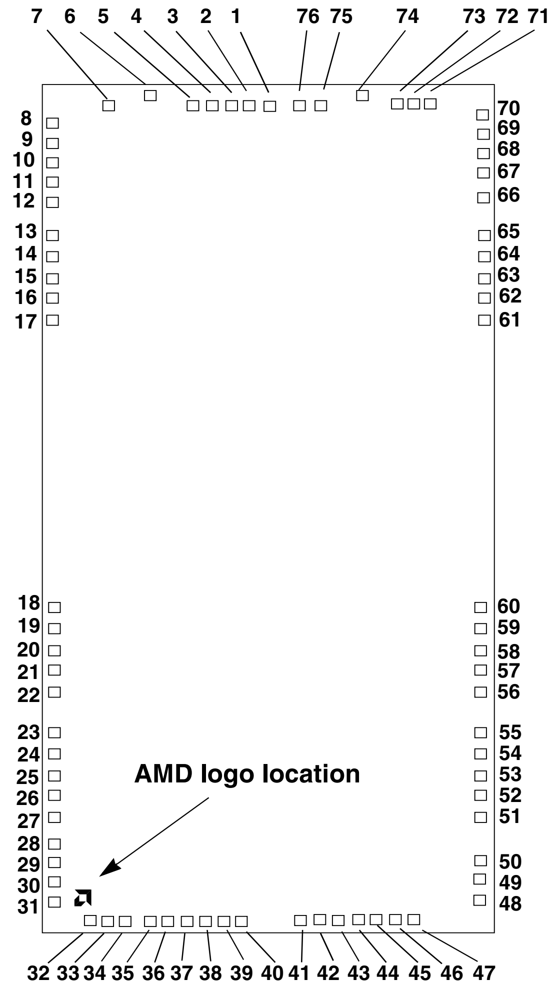
PRODUCT SELECTOR GUIDE

Part Number	Am29BDD160 KGD	
Standard Voltage Range: V_{CC} = 2.5 – 2.75 V	Synchronous/Burst or Asynchronous	
Speed Option (Clock Rate)	64C (56 MHz)	65A (40 MHz)
Max Initial/Asynchronous Access Time, ns (t_{ACC})	64	67
Max Burst Access Delay (ns)	10	17
Max Clock Rate (MHz)	56	40
Max CE# Access, ns (t_{CE})	69	71
Max OE# Access, ns (t_{OE})	20	28

DIE PHOTOGRAPH



DIE PAD LOCATIONS



PAD DESCRIPTION

Pads relative to die center.

Pad	Signal	Pad Center (mils)		Pad Center (millimeters)	
		X	Y	X	Y
1	V_{CC}	–0.56	137.36	–0.01	3.49
2	CE#	–5.56	137.36	–0.14	3.49
3	OE#	–10.92	137.36	–0.28	3.49
4	WE#	–17.34	137.36	–0.45	3.49
5	WP#	–23.37	137.36	–0.59	3.49
6	IND/WAIT#	–38.38	139.77	–0.97	3.55
7	WORD#	–53.99	137.36	–1.37	3.49
8	DQ16	–75.30	131.69	–1.91	3.34
9	DQ17	–75.30	123.36	–1.91	3.13
10	DQ18	–75.30	115.02	–1.91	2.92
11	DQ19	–75.30	106.69	–1.91	2.71
12	V_{CCQ}	–75.30	100.30	–1.91	2.55
13	V_{SS}	–75.30	88.18	–1.91	2.24
14	DQ20	–75.30	81.89	–1.91	2.08
15	DQ21	–75.30	73.56	–1.91	1.87
16	DQ22	–75.30	65.23	–1.91	1.66
17	DQ23	–75.30	56.90	–1.91	1.45
18	DQ24	–75.30	–30.34	–1.91	–0.77
19	DQ25	–75.30	–38.67	–1.91	–0.98
20	DQ26	–75.30	–46.99	–1.91	–1.19
21	DQ27	–75.30	–55.33	–1.91	–1.41
22	V_{CCQ}	–75.30	–61.69	–1.91	–1.57
23	V_{SS}	–75.30	–73.71	–1.91	–1.87
24	DQ28	–75.30	–80.04	–1.91	–2.03
25	DQ29	–75.30	–88.38	–1.91	–2.24
26	DQ30	–75.30	–96.71	–1.91	–2.46
27	DQ31	–75.30	–105.04	–1.91	–2.67
28	A-1	–75.30	–113.55	–1.91	–2.88
29	A0	–75.30	–120.37	–1.91	–3.06
30	A1	–75.30	–125.73	–1.91	–3.19
31	A2	–75.30	–132.55	–1.91	–3.37
32	A3	–57.26	–137.01	–1.45	–3.48
33	A4	–50.44	–137.01	–1.28	–3.48
34	A5	–45.08	–137.01	–1.15	–3.48
35	A6	–38.27	–137.01	–0.97	–3.48
36	A7	–32.91	–137.01	–0.84	–3.48
37	A8	–26.09	–137.01	–0.66	–3.48
38	V_{SS}	–20.69	–137.01	–0.53	–3.48
39	ACC	–14.40	–137.01	–0.37	–3.48
40	V_{CC}	–8.74	–137.01	–0.22	–3.48
41	A9	7.49	–137.01	0.19	–3.48
42	A10	14.49	–137.01	0.37	–3.48
43	A11	19.85	–137.01	0.50	–3.48
44	A12	26.67	–137.01	0.68	–3.48
45	A13	32.03	–137.01	0.81	–3.48
46	A14	38.84	–137.01	0.99	–3.48
47	A15	44.20	–137.01	1.12	–3.48
48	A16	75.36	–130.61	1.91	–3.32

Pad	Signal	Pad Center (mils)		Pad Center (millimeters)	
		X	Y	X	Y
49	A17	75.36	–123.80	1.91	–3.14
50	A18	75.36	–118.44	1.91	–3.01
51	DQ0	75.34	–107.97	1.91	–2.74
52	DQ1	75.34	–99.65	1.91	–2.53
53	DQ2	75.34	–91.31	1.91	–2.32
54	DQ3	75.34	–82.98	1.91	–2.11
55	V_{CCQ}	75.34	–76.72	1.91	–1.95
56	V_{SS}	75.34	–64.58	1.91	–1.64
57	DQ4	75.34	–58.29	1.91	–1.48
58	DQ5	75.34	–49.96	1.91	–1.27
59	DQ6	75.34	–41.63	1.91	–1.06
60	DQ7	75.34	–33.29	1.91	–0.85
61	DQ8	75.34	55.77	1.91	1.42
62	DQ9	75.34	64.09	1.91	1.63
63	DQ10	75.34	72.43	1.91	1.84
64	DQ11	75.34	80.76	1.91	2.05
65	V_{CCQ}	75.34	87.02	1.91	2.21
66	V_{SS}	75.34	99.14	1.91	2.52
67	DQ12	75.34	105.53	1.91	2.68
68	DQ13	75.34	113.86	1.91	2.89
69	DQ14	75.34	122.19	1.91	3.10
70	DQ15	75.34	130.52	1.91	3.32
71	V_{CCQ}	54.86	137.36	1.39	3.49
72	RESET#	48.74	137.36	1.24	3.49
73	CLK	43.38	137.36	1.10	3.49
74	RY/BY#	31.18	139.77	0.79	3.55
75	ADV#	17.45	137.36	0.44	3.49
76	V_{SS}	11.88	137.36	0.30	3.49

Note: *The coordinates above are relative to the die center and can be used to operate wire bonding equipment.*

PAD DESCRIPTION

Pads relative to V_{CC}.

Pad	Signal	Pad Center (mils)		Pad Center (millimeters)	
		X	Y	X	Y
1	V_{CC}	0.00	0.00	0.00	0.00
2	CE#	–5.00	0.00	–0.13	0.00
3	OE#	–10.36	0.00	–0.27	0.00
4	WE#	–16.78	0.00	–0.44	0.00
5	WP#	–22.81	0.00	–0.58	0.00
6	IND/WAIT#	–37.82	2.41	–0.96	0.06
7	WORD#	–53.43	0.00	–1.36	0.00
8	DQ16	–74.74	–5.67	–1.90	–0.15
9	DQ17	–74.74	–14.00	–1.90	–0.36
10	DQ18	–74.74	–22.34	–1.90	–0.57
11	DQ19	–74.74	–30.67	–1.90	–0.78
12	V_{CCQ}	–74.74	–37.06	–1.90	–0.94
13	V_{SS}	–74.74	–49.18	–1.90	–1.25
14	DQ20	–74.74	–55.47	–1.90	–1.41
15	DQ21	–74.74	–63.80	–1.90	–1.62
16	DQ22	–74.74	–72.13	–1.90	–1.83
17	DQ23	–74.74	–80.46	–1.90	–2.04
18	DQ24	–74.74	–167.70	–1.90	–4.26
19	DQ25	–74.74	–176.03	–1.90	–4.47
20	DQ26	–74.74	–184.35	–1.90	–4.68
21	DQ27	–74.74	–192.69	–1.90	–4.90
22	V_{CCQ}	–74.74	–199.05	–1.90	–5.06
23	V_{SS}	–74.74	–211.07	–1.90	–5.36
24	DQ28	–74.74	–217.40	–1.90	–5.52
25	DQ29	–74.74	–225.74	–1.90	–5.73
26	DQ30	–74.74	–234.07	–1.90	–5.95
27	DQ31	–74.74	–242.40	–1.90	–6.16
28	A-1	–74.74	–250.91	–1.90	–6.37
29	A0	–74.74	–257.73	–1.90	–6.55
30	A1	–74.74	–263.09	–1.90	–6.68
31	A2	–74.74	–269.91	–1.90	–6.86
32	A3	–56.7	–274.37	–1.44	–6.97
33	A4	–49.88	–274.37	–1.27	–6.97
34	A5	–44.52	–274.37	–1.14	–6.97
35	A6	–37.71	–274.37	–0.96	–6.97
36	A7	–32.35	–274.37	–0.83	–6.97
37	A8	–25.53	–274.37	–0.65	–6.97
38	V_{SS}	–20.13	–274.37	–0.52	–6.97
39	ACC	–13.84	–274.37	–0.36	–6.97
40	V_{CC}	–8.18	–274.37	–0.23	–6.97
41	A9	8.05	–274.37	0.20	–6.97
42	A10	15.05	–274.37	0.38	–6.97
43	A11	20.41	–274.37	0.51	–6.97
44	A12	27.23	–274.37	0.69	–6.97
45	A13	32.59	–274.37	0.82	–6.97
46	A14	39.40	–274.37	1.00	–6.97
47	A15	44.76	–274.37	1.13	–6.97
48	A16	75.92	–267.97	1.92	–6.81

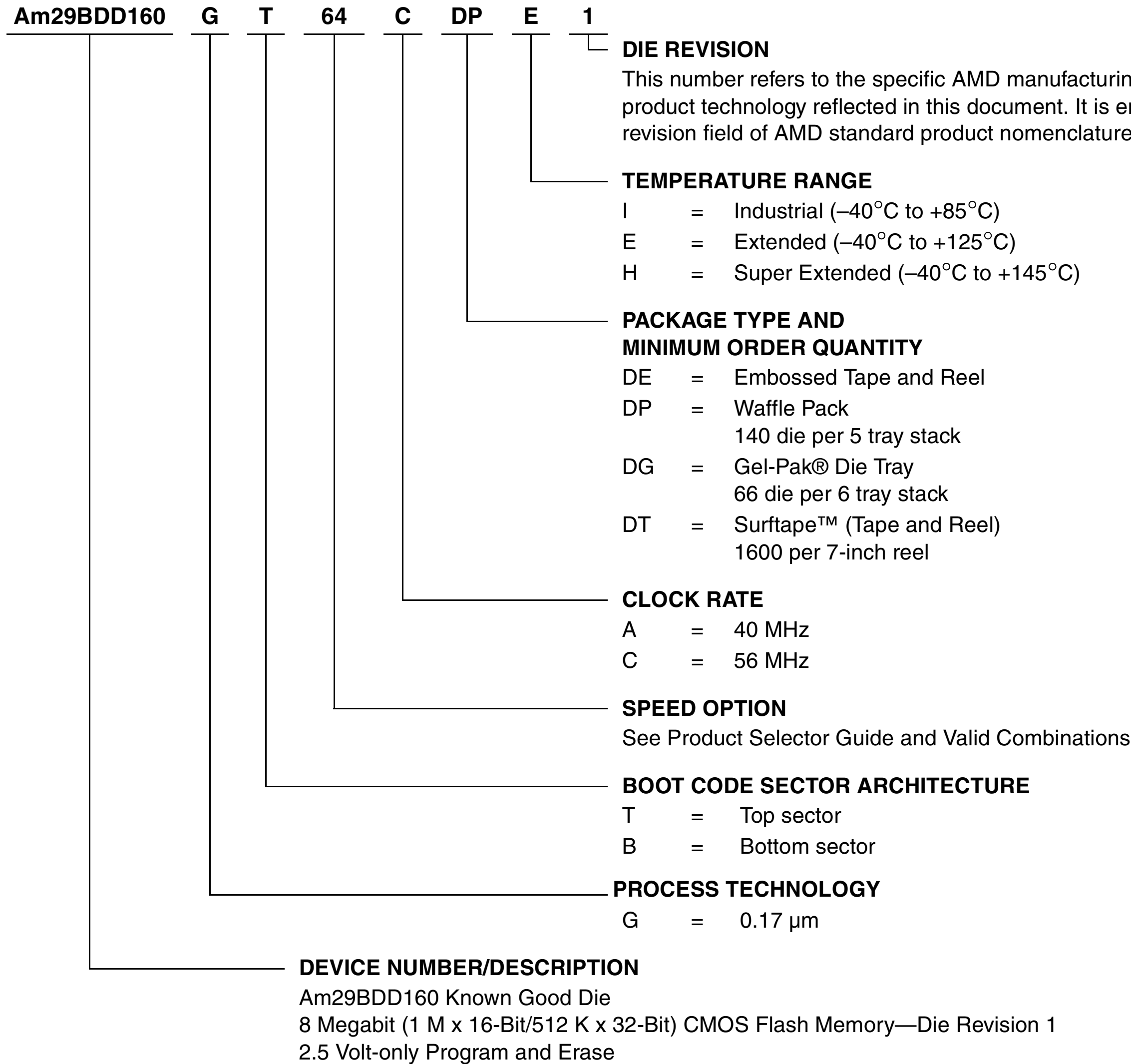
Pad	Signal	Pad Center (mils)		Pad Center (millimeters)	
		X	Y	X	Y
49	A17	75.92	–261.16	1.92	–6.63
50	A18	75.92	–255.80	1.92	–6.50
51	DQ0	75.90	–245.33	1.92	–6.23
52	DQ1	75.90	–237.01	1.92	–6.02
53	DQ2	75.90	–228.67	1.92	–5.81
54	DQ3	75.90	–220.34	1.92	–5.60
55	V_{CCQ}	75.90	–214.08	1.92	–5.44
56	V_{SS}	75.90	–201.94	1.92	–5.13
57	DQ4	75.90	–195.65	1.92	–4.97
58	DQ5	75.90	–187.32	1.92	–4.76
59	DQ6	75.90	–178.99	1.92	–4.55
60	DQ7	75.90	–170.65	1.92	–4.34
61	DQ8	75.90	–81.59	1.92	–2.07
62	DQ9	75.90	–73.27	1.92	–1.86
63	DQ10	75.90	–64.93	1.92	–1.65
64	DQ11	75.90	–56.60	1.92	–1.44
65	V_{CCQ}	75.90	–50.34	1.92	–1.28
66	V_{SS}	75.90	–38.22	1.92	–0.97
67	DQ12	75.90	–31.83	1.92	–0.81
68	DQ13	75.90	–23.50	1.92	–0.60
69	DQ14	79.27	–15.17	2.01	–0.39
70	DQ15	79.27	–6.84	2.01	–0.17
71	V_{CCQ}	55.42	0.00	1.40	0.00
72	RESET#	49.30	0.00	1.25	0.00
73	CLK	43.94	0.00	1.11	0.00
74	RY/BY#	31.74	2.41	0.80	0.06
75	ADV#	18.01	0.00	0.45	0.00
76	V_{SS}	12.44	0.00	0.31	0.00

Note: *The coordinates above are relative to the center of pad 1 and can be used to operate wire bonding equipment.*

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



Valid Combinations	
AM29BDD160GT-64C AM29BDD160GB-64C	DPI 1, DPE 1, DPH1 DGI 1, DGE 1, DGH1 DTI 1, DTE 1, DTH1 DEI 1, DEE 1, DEH 1
AM29BDD160GT-65A AM29BDD160GB-65A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PACKAGING INFORMATION

Surftape Packaging

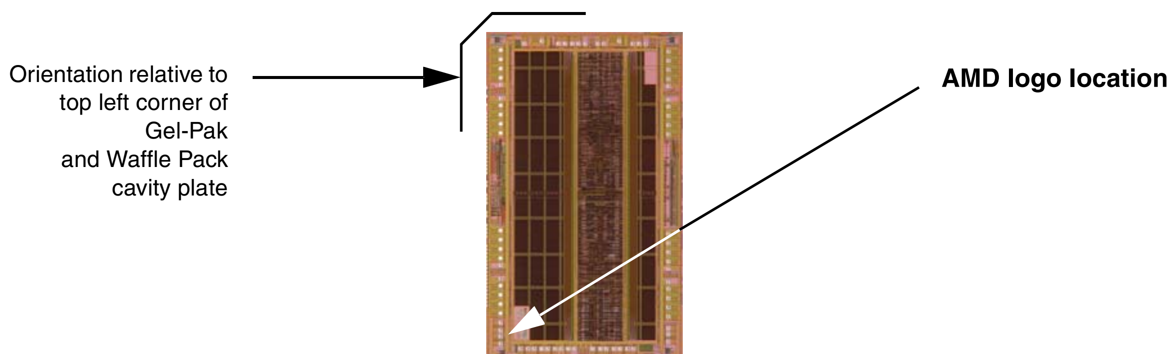
Direction of Feed

16 mm

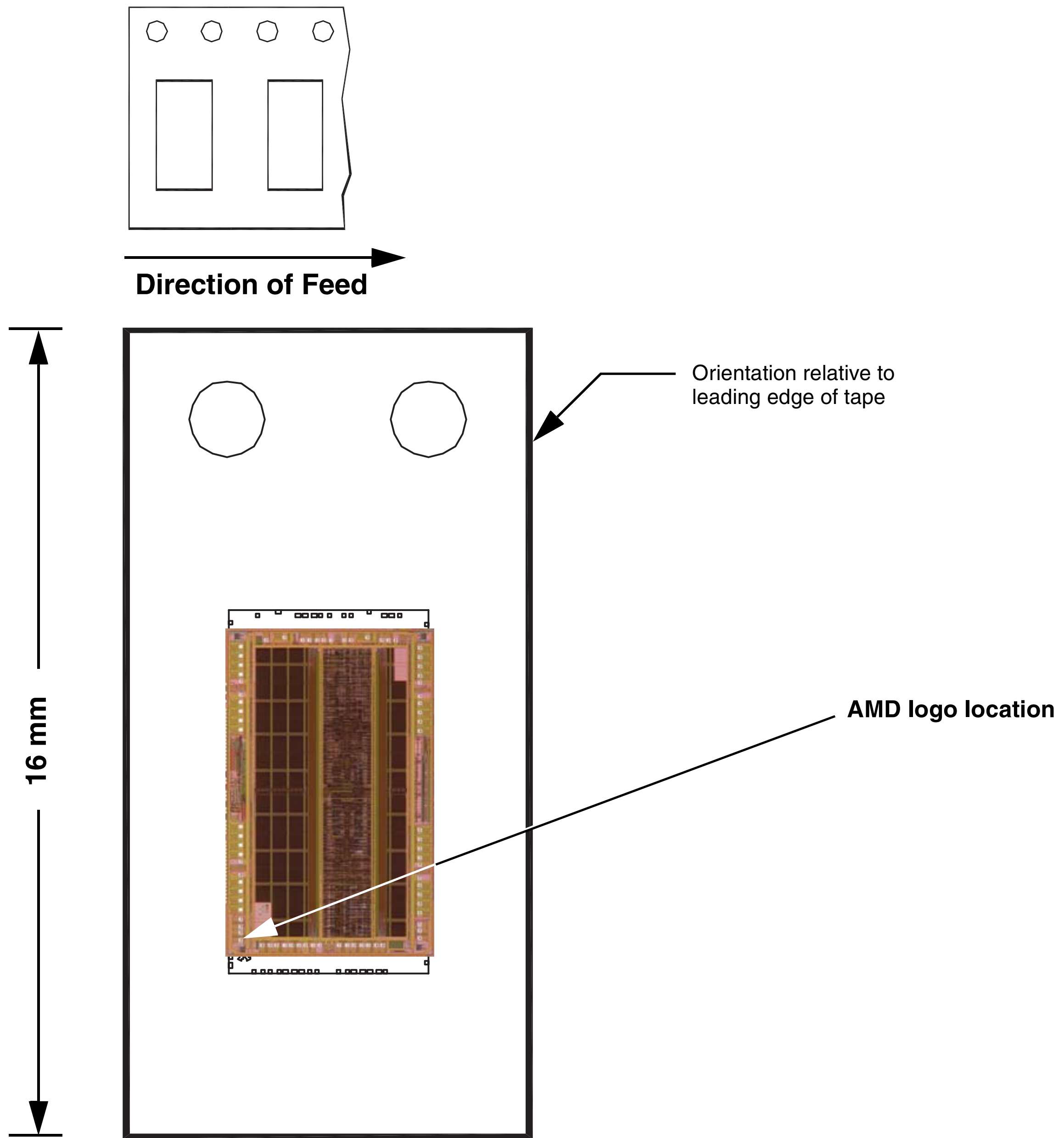
Orientation relative to leading edge of tape and reel

AMD logo location

Gel-Pak and Waffle Pack Packaging



Embossed Tape Packaging



PRODUCT TEST FLOW

Figure 1 provides an overview of AMD's Known Good Die test flow. For more detailed information, refer to the Am29BDD160G product qualification database. AMD implements quality assurance procedures throughout the product test flow. These QA procedures also allow AMD to produce KGD products without requiring or implementing burn-in. In addition, an off-line quality monitoring program (QMP) further guarantees AMD quality standards are met on Known Good Die products.

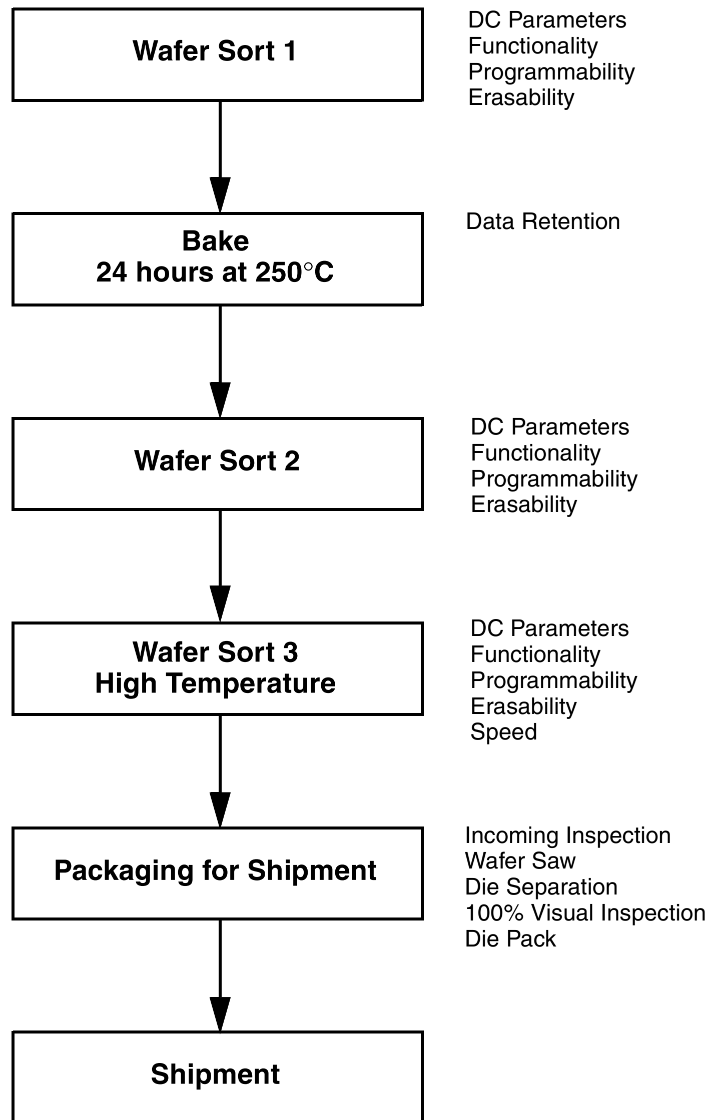


Figure 1. AMD KGD Product Test Flow

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature
with Power Applied. . . . . –40°C to +145°C

V_{CC}/V_{IO} (Note 1). . . . . –0.5 V to + 3.0 V

A9, OE#, and RESET# (Note 2) . . –0.5 V to +13.0 V

Addresses, Data, Control Signals
(with the exception of CLK) . . . . –0.5 V to 3.6 V

All other pins (Note 1). . . . . –0.5 V to +5.5 V

Output Short Circuit Current (Note 3) . . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input at I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 13. Maximum DC voltage on output and I/O pins is 3.6 V. During voltage transitions output pins may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See Figure 14.*
2. *Minimum DC input voltage on pins A9, OE#, and RESET# is -0.5 V. During voltage transitions, A9, OE#, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 13. Maximum DC input voltage on pin A9 and OE# is +13.0 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
4. *Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

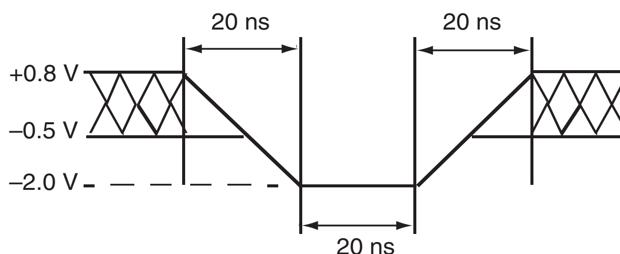


Figure 1. Maximum Negative Overshoot Waveform

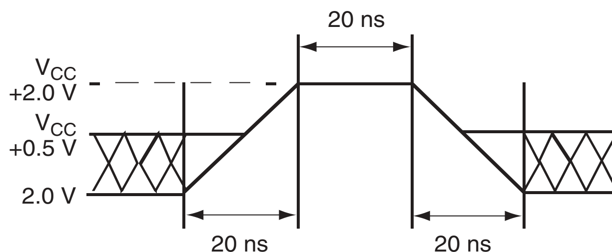


Figure 2. Maximum Positive Overshoot Waveform

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A) . . . . –40°C to +85°C

Extended (E) Devices

Ambient Temperature (T_A) . . . . –40°C to +125°C

V_{CC} Supply Voltages

V_{CC} for regulated voltage range. . . . . . 2.5 V to 2.75 V

V_{IO} Supply Voltages

V_{IO} . . . . 1.65 V to 2.75 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

PHYSICAL SPECIFICATIONS

Die dimensions . . . . 179 mils x 295mils
. . . . 4.54 mm x 7.50 mm

Die Thickness. . . . . .500 µm

Bond Pad Size . . . . 3.43 mils x 3.43 mils
. . . . 87 µm x 87 µm

Pad Area Free of Passivation . . . . .264.72 $mils^2$
. . . . 6,724 $µm^2$

Pads Per Die 76

Bond Pad Metalization . . . . Al/Cu

Die Backside . . . . No metal,
may be grounded (optional)

Passivation. . . . . SiN/SOG/SiN

DC OPERATING CONDITIONS

V_{CC} (Supply Voltage) . . . . 2.5 V to 2.75 V

Operating Temperature
- Industrial . . . . –40°C to +85°C
- Extended . . . . –40°C to +125°C
- Super Extended . . . . –40°C to +145°C

V_{IO} Supply Voltages

V_{IO} . . . . 1.65 V to 2.75 V

MANUFACTURING INFORMATION

Manufacturing . . . . FASL

Test . . . . KYEC

Manufacturing ID (Top Boot) 98P03AK
(Bottom Boot). 98P03ABK

Preparation for Shipment . . . . Penang, Malaysia

Fabrication Process CS59LS

Die Revision 1

SPECIAL HANDLING INSTRUCTIONS

Processing

Do not expose KGD products to ultraviolet light or process them at temperatures greater than 250°C. Failure to adhere to these handling instructions will result in irreparable damage to the devices. For best yield, AMD recommends assembly in a Class 10K clean room with 30% to 60% relative humidity.

Storage

Store at a maximum temperature of 30°C in a nitrogen-purged cabinet or vacuum-sealed bag. Observe all standard ESD handling procedures.

DC CHARACTERISTICS FOR KGD DEVICES AT 145°C

CMOS Compatible

Parameter	Description	Test Conditions		Min	Typ	Max	Unit
I_{CC1}	V_{CC} Active Asynchronous Read Current	CE# = V_{IL}, OE# = V_{IL}	1 MHz		25	50	mA
I_{CC5} (Note 1)	V_{CC} Standby Current (CMOS)	$V_{CC} = V_{CCmax}$, CE# = $V_{CC} \pm$ 0.3 V			15	250	µA
I_{CC7} (Note 1)	V_{CC} Reset Current	Reset = V_{IL}				250	µA
I_{CC8} (Note 1)	Automatic Sleep Mode Current	$V_{IH} = V_{CC} \pm 0.3$ V, $V_{IL} = V_{SS} \pm 0.3$ V				250	µA

Notes:

1. *Current maximum has been significantly increased (x27) from KGD Supplement Revision A, Amendment 1, dated April 21, 2003.*
2. *The I_{CC} current listed includes both the DC operating current and the frequency dependent component.*

AC CHARACTERISTICS

Erase/Program Operation – KGD Devices at 145°C

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{DH}	Data Hold from WE# Rising Edge	min	2	ns

Alternate CE# Controlled Erase/Program Operation – KGD Devices at 145°C

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{DH}	Data Hold from WE# Rising Edge	min	2	ns

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All transactions relating to unpackaged die under this agreement shall be subject to AMD's standard terms and conditions of sale, or any revisions thereof, which revisions AMD reserves the right to make at any time and from time to time. In the event of conflict between the provisions of AMD's standard terms and conditions of sale and this agreement, the terms of this agreement shall be controlling.

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This limited warranty does not extend beyond the first purchaser of said Die or Wafer(s).

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REVISION SUMMARY

Revision A (December 10, 2002)

Initial release.

Revision A + 1 (April 21, 2003)

Distinctive Characteristics

Architectural Advantages, Single power supply operation: changed 2.7 Volt to 2.75 Volt.

Performance Characteristics, Ultra low power consumption: changed Standby mode: CMOS to 60 µA max.

Product Selector Guide

Removed Min Initial Clock Delay

Absolute Maximum Ratings

Added this new section.

DC Operating Conditions

Changed V_{CC} from 2.5 V – 2.7 V to 2.5 V – 2.75 V.

Added V_{IO} Supply Voltages.

AC Characteristics

CMOS Compatible: changed I_{CC5} Max to 60 µA.

Erase/Program Operation: changed t_{DH} speed to 2 ns.

Alternate CE# Controlled Erase/Program Operation: changed t_{DH} speed to 2 ns.

Terms and Conditions of sale for AMD Non-volatile memory die

Revised text following first paragraph.

Revision A + 2 (May 9, 2003)

Performance Characteristics

Ultra low power consumption: changed Standby mode: CMOS to 250 µA

Product Selector Guide

Changed t_{ACC} for 65A (40 MHz) to 67 ns.

AC Characteristics for KGD Devices at 145C, CMOS Compatible

Changed I_{CC5} Max to 250, Added I_{CC7}, I_{CC8}, added Note 1.

Revision A + 3 (July 16, 2003)

Pad Description table

Pads Relative to V_{CC}: Corrected signal names for pads 35 to 51.

Revision A + 4 (September 9, 2003)

Packaging Information

Added Embossed Tape and Reel Packaging.

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