DUAL SYNCHRONOUS PWM CONTROLLER CIRCUITRY AND LDO CONTROLLER

PRELIMINARY DATA SHEET

FEATURES

- Dual Synchronous Controller in 16-Pin Package with 180° out-of-phase operation
- LDO Controller with 40mA drive
- Configured as 2-Independent PWM Controller
- Flexible, Same or Separate Supply Operation
- Operation from 4V to 25V Input
- Internal 200KHz Oscillator
- Soft-Start controls all outputs
- Fixed Frequency Voltage Mode
- 500mA Peak Output Drive Capability
- Programmable Outputs
- RoHS Compliant

APPLICATIONS

- DDR Memory Source Sink Vtt Application
- Graphic Card
- Hard Disk Drive
- Power supplies requiring multiple outputs

DESCRIPTION

The APU3048 IC combines a Dual synchronous Buck controller and a linear regulator controller, providing a cost-effective, high performance and flexible solution for multi-output applications. The Dual synchronous controller is configured as 2-independent PWM controller. APU3048 provides a separate adjustable output by driving a switch as a linear regulator. This device features an internal 200KHz oscillator, under-voltage lockout for all input supplies, an external programmable soft start function as well as output under-voltage detection that latches off the device when an output short is detected.

TYPICAL APPLICATION

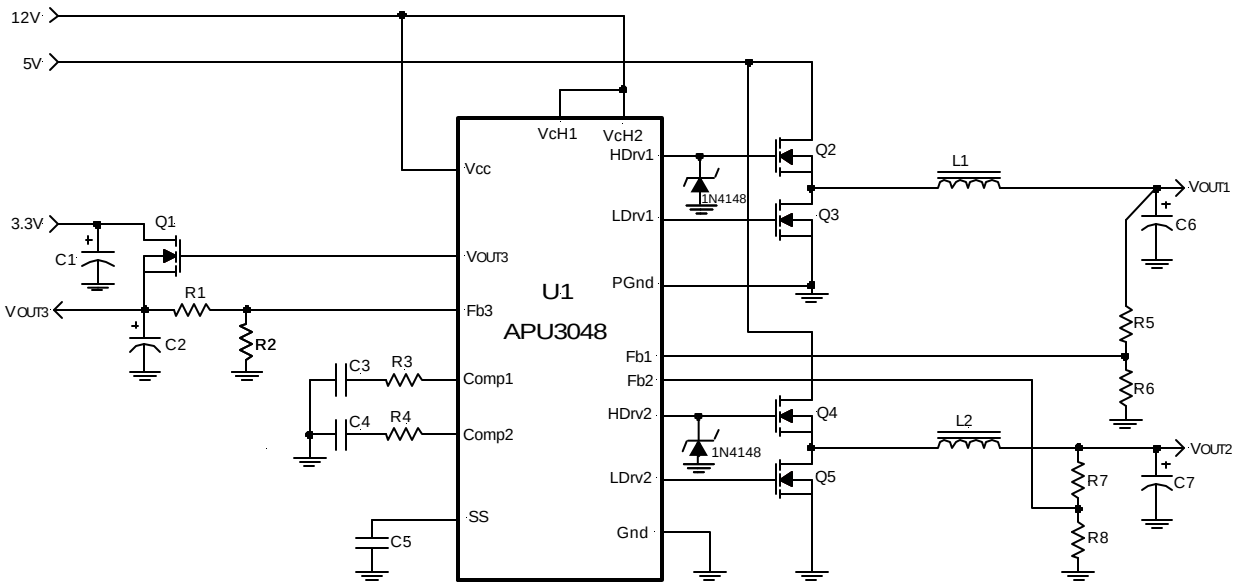


Figure 1 - Typical application of APU3048 configured as 2-independent converter.

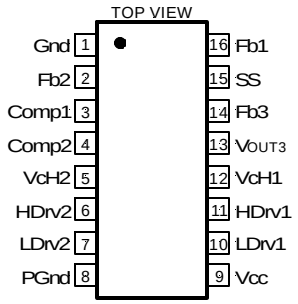
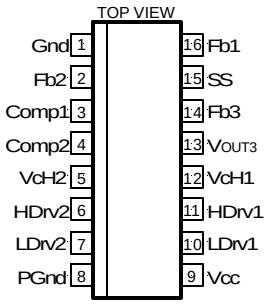
PACKAGE ORDER INFORMATION

T_A (°C)	DEVICE	PACKAGE
0 To 70	APU3048O	16-Pin TSSOP
0 To 70	APU3048M	16-Pin SOIC NB

ABSOLUTE MAXIMUM RATINGS

Vcc Supply Voltage 25V
VcH1=VcH2 Supply Voltage ..... 30V (not rated for inductive load)
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 125°C

PACKAGE INFORMATION

16-PIN PLASTIC TSSOP (O)	16-PIN PLASTIC SOIC NB (M)
	
θ_{JA}=90°C/W	θ_{JA}=85°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc=5V, VcH1=VcH2=12V, T_A=0 to 70°C. Typical values refer to T_A=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Voltage						
Fb Voltage	V_{FB}		1.225	1.250	1.275	V
Fb Voltage Line Regulation	L_{REG}	5<Vcc<12		0.2		%
UVLO						
UVLO Threshold - Vcc	$UVLO_{VCC}$	Supply Ramping Up		4.2		V
UVLO Hysteresis - Vcc				0.25		V
UVLO Threshold - VcH1	$UVLO_{VcH1}$	Supply Ramping Up		3.5		V
UVLO Hysteresis - VcH1				0.2		V
UVLO Threshold - VcH2	$UVLO_{VcH2}$	Supply Ramping Up		3.5		V
UVLO Hysteresis - VcH2				0.2		V
UVLO Threshold - Fb	$UVLO_{FB}$	Fb Ramping Down		0.6		V
UVLO Hysteresis - Fb				0.1		V
Supply Current						
Vcc Dynamic Supply Current	Dyn I_{CC}	Freq=200KHz, C_L=1500pF		5		mA
VcH1 Dynamic Supply Current	Dyn I_{cH1}	Freq=200KHz, C_L=1500pF		7		mA
VcH2 Dynamic Supply Current	Dyn I_{cH2}	Freq=200KHz, C_L=1500pF		7		mA
Vcc Static Supply Current	I_{CCQ}	SS=0V		3.5		mA
VcH1 Static Supply Current	I_{cH1Q}	SS=0V		2		mA
VcH2 Static Supply Current	I_{cH2Q}	SS=0V		2		mA
Soft-Start Section						
Charge Current	SS_{IB}	SS=0V	15	25	30	µA

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Error Amp						
Fb Voltage Input Bias Current	I_{FB1}	SS=3V		-0.1		μA
Fb Voltage Input Bias Current	I_{FB2}	SS=0V		-64		μA
Transconductance 1	g_{m1}			400		μmho
Transconductance 2	g_{m2}			600		μmho
Oscillator						
Frequency	Freq		180	200	220	KHz
Ramp Amplitude	V_{RAMP}			1.25		V_{PP}
Output Drivers						
Rise Time	Tr	C_L=1500pF		35	100	ns
Fall Time	Tf	C_L=1500pF		50	100	ns
Dead Band Time	T_{DB}		50	150	250	ns
Max Duty Cycle	T_{ON}	Fb=1V, Freq=200KHz	85	90		%
Min Duty Cycle	T_{OFF}	Fb=1.5V	0	0		%
LDO Controller						
Drive Current	I_{LDO}		30	45		mA
Fb Voltage	V_{FB}LDO		1.225	1.25	1.275	V
Input Bias Current	$I_{LDO(BIAS)}$			0.5	2	μA

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	Gnd	Ground pin.
2 16	Fb2 Fb1	Inverting inputs to the error amplifiers. These pins work as feedback inputs for each channel, and are connected directly to the output of the switching regulator via a resistor divider to set the output voltages.
3 4	Comp1 Comp2	Compensation pins for the error amplifiers.
5 12	VcH2 VcH1	Supply voltage for the high side output drivers. These are connected to voltages that must be at least 4V higher than their bus voltages (assuming 5V threshold MOSFET). A minimum of 1μF high frequency capacitor must be connected from these pins to PGnd pin to provide peak drive current capability.
6 11	HDrv2 HDrv1	Output driver for the high side power MOSFET. Connect a diode, such as BAT54 or 1N4148, from these pins to ground for the application when the inductor current goes negative (Source/Sink), soft-start at no load and for the fast load transient from full load to no load.
7 10	LDrv2 LDrv1	Output driver for the synchronous power MOSFET.
8	PGnd	This pin serves as the separate ground for MOSFET's driver and should be connected to the system's ground plane.
9	Vcc	Supply voltage for the internal blocks of the IC.
13	V_{OUT3}	Driver signal for the LDO's external transistor.
14	Fb3	LDO's feedback pin, connected to a resistor divider to set the output voltage of LDO.
15	SS	Soft-Start pin. The converter can be shutdown by pulling this pin below 0.5V.

BLOCK DIAGRAM

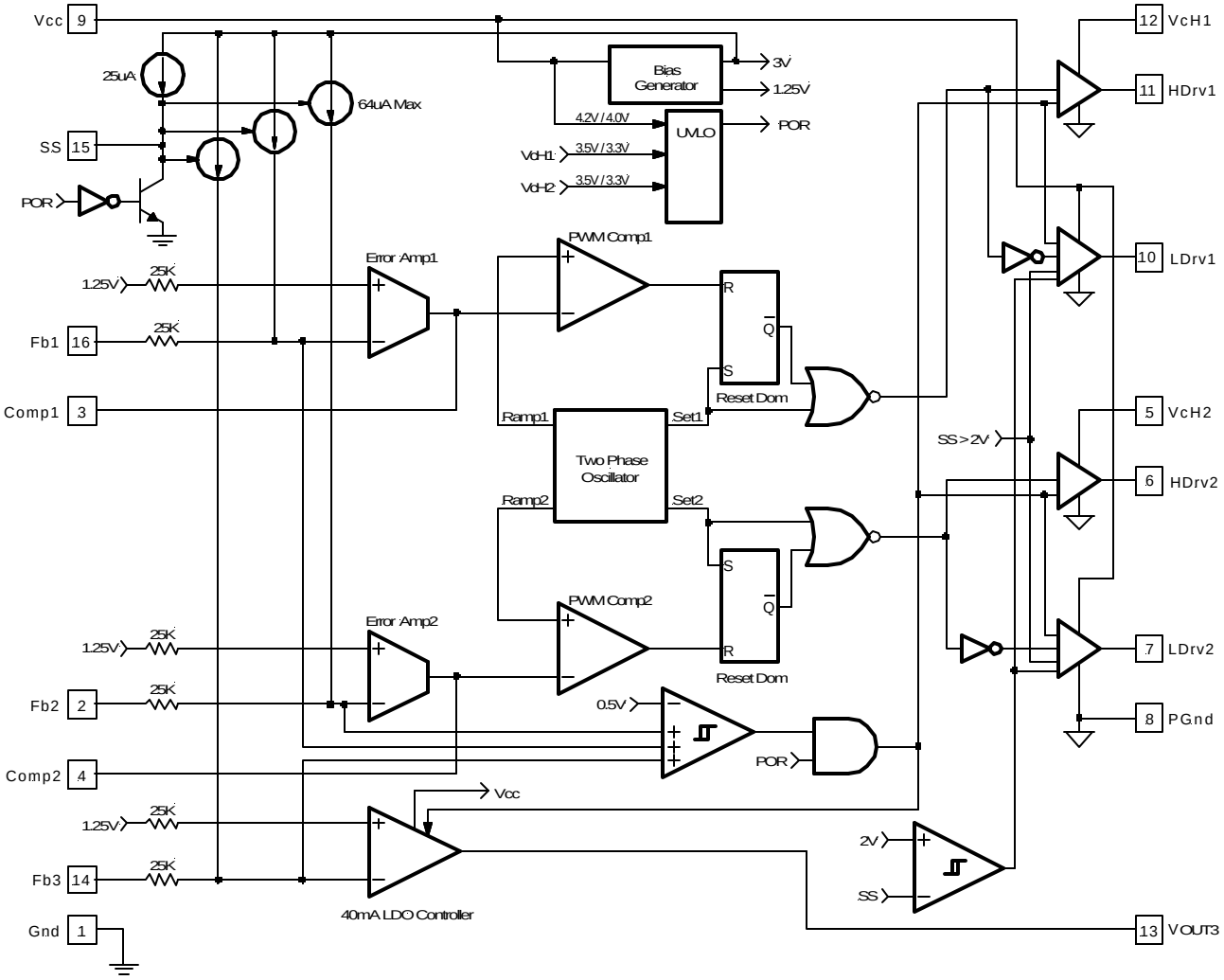


Figure 2 - Block diagram of the APU3048.

THEORY OF OPERATION

Introduction

The APU3048 is designed for multi-outputs applications. It includes two synchronous buck controllers and a linear regulator controller. The two synchronous controller operates with fixed frequency voltage mode and is configured as two independent controllers. The timing of the IC is provided through an internal oscillator circuit. These are two out of phase oscillators.

Soft-Start

The APU3048 has a programmable soft start to control the output voltage rise and limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the Vcc, VcH1 and VcH2 rise above their threshold and generates the Power On Reset (POR) signal. Soft-start function operates by sourcing an internal current to charge an external capacitor to about 3V. Initially, the soft-start function clamps the E/A's output of the PWM converter. As the charging voltage of the external capacitor ramps up, the PWM signals increase from zero to the point the feedback loop takes control.

Out of Phase Operation

The APU3048 drives its two output stages 180° out of phase. In application with single input voltage, the out of phase operation reduces the input ripple current. This results in much smaller RMS current in the input capacitor and reduction of input capacitors.

Shutdown

The converter can be shutdown by pulling the soft-start pin below 0.5V. This can be easily done by using an external small signal transistor. During shutdown the MOSFET drivers and the LDO controller turn off.

Short-Circuit Protection

The outputs are protected against the short circuit. The APU3048 protects the circuit for shorted output by sensing the output voltages. The APU3048 shuts down the PWM signals and LDO controller, when the output voltages drops below the set values.

Under-Voltage Lockout

The under-voltage lockout circuit assures that the MOSFET driver outputs and LDO controller remain in the off state whenever the supply voltages drop below set parameters. Normal operation resumes once the supply voltages rise above the set values.

APPLICATION INFORMATION

Design Example:

The following example is a typical application for APU3048 in current sharing mode. The schematic is Figure 9 on page 12.

For Switcher	For Linear Regulator
V_{IN1} = 12V	V_{IN3} = 3.3V
V_{OUT1} = 3.3V	V_{OUT3} = 2.5V
I_{OUT1} = 4A	I_{OUT3} = 2A
V_{IN2} = 5V	
V_{OUT2} = 1.8V	
I_{OUT2} = 4A	
ΔV_{OUT} = 75mV	
f_S = 200KHz	

PWM Section

Output Voltage Programming

Output voltage is programmed by reference voltage and external voltage divider. The Fb1 pin is the inverting input of the error amplifier, which is internally referenced to 1.25V. The divider is ratioed to provide 1.25V at the Fb1 pin when the output is at its desired value. The output voltage is defined by using the following equation:

$$V_{OUT1} = V_{REF} \times \left(1 + \frac{R_6}{R_8}\right) \qquad \text{---(1)}$$

When an external resistor divider is connected to the output as shown in Figure 3.

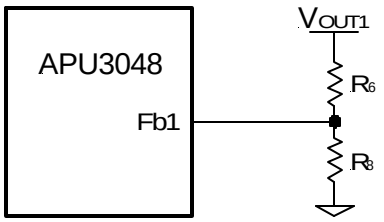


Figure 3 - Typical application of the APU3048 for programming the output voltage.

Equation (1) can be rewritten as:

$$R_6 = R_8 \times \left(\frac{V_{OUT1}}{V_{REF}} - 1\right)$$

Will result to:

V_{OUT1}=3.3V	V_{OUT2}=1.8V
V_{REF}=1.25V	V_{REF}=1.25V
R_8=1K, R_6=1.64K	R_{15}=1K, R_{14}=442Ω

If the high value feedback resistors are used, the input bias current of the Fb pin could cause a slight increase in output voltage. The output voltage set point can be more accurate by using precision resistor.

Soft-Start Programming

The soft-start timing can be programmed by selecting the soft start capacitance value. The start up time of the converter can be calculated by using:

$$t_{START} = 75 \times Css \quad (ms) \qquad ---(2)$$

Where:
C_{SS} is the soft-start capacitor (μF)

For a start-up time of 7.5ms, the soft-start capacitor will be 0.1μF. Choose a ceramic capacitor at 0.1μF.

Boost Supply Vc

To drive the high-side switch it is necessary to supply a gate voltage at least 4V greater than the bus voltage. This is achieved by using a charge pump configuration as shown in Figure 9. The capacitor is charged up to approximately twice the bus voltage. A capacitor in the range of 0.1μF to 1μF is generally adequate for most applications.

Input Capacitor selection

The input filter capacitor should be based on how much ripple the supply can tolerate on the DC input line. The ripple current generated during the on time of control MOSFET should be provided by input capacitor. The RMS value of this ripple is expressed by:

$$I_{RMS} = I_{OUT} \sqrt{D \times (1\text{-}D)} \qquad ---(3)$$

Where:
D is the Duty Cycle, simply $D=V_{OUT}/V_{IN}$.
I_{RMS} is the RMS value of the input capacitor current.
I_{OUT} is the output current for each channel.

For V_{IN1}=12V, I_{OUT1}=4A and D1=0.275
Results to: I_{RMS1}=1.78A

And for V_{IN2}=5V, I_{OUT2}=4A and D2=0.36
Results to: I_{RMS2}=1.92A

For higher efficiency, a low ESR capacitor is recommended.

For V_{IN1}=12V, choose one Poscap from Sanyo 16TPB47M (16V, 47μF, 70mΩ, 1.4A)

For V_{IN2}=5V, choose one 6TPC150M (6.3V, 150μF, 40mΩ, 1.9A).

Output Capacitor Selection

The criteria to select the output capacitor is normally based on the value of the Effective Series Resistance (ESR). In general, the output capacitor must have low enough ESR to meet output ripple and load transient requirements, yet have high enough ESR to satisfy stability requirements. The ESR of the output capacitor is calculated by the following relationship:

$$ESR \le \frac{\Delta V_O}{\Delta I_O} \qquad ---(4)$$

Where:
ΔV_O = Output Voltage Ripple
ΔI_O = Output Current
ΔV_O=75mV and ΔI_O=3A, results to: ESR=25mΩ

The Sanyo TPC series, PosCap capacitor is a good choice. The 6TPC150M 150μF, 6.3V has an ESR 40mΩ. Selecting two of these capacitors in parallel for each output, results to an ESR of $\cong$ 20mΩ which achieves our low ESR goal.

The capacitor value must be high enough to absorb the inductor's ripple current. The larger the value of capacitor, the lower will be the output ripple voltage.

The resulting output ripple current is smaller then each channel ripple current due to the 180° phase shift. These currents cancel each other. The cancellation is not the maximum because of the different duty cycle for each channel.

Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. Low inductor value causes large ripple current, resulting in the smaller size, but poor efficiency and high output noise. Generally, the selection of inductor value can be reduced to desired maximum ripple current in the inductor (Δi); the optimum point is usually found between 20% and 50% ripple of the output current.

For the buck converter, the inductor value for desired operating ripple current can be determined using the following relation:

$$V_{IN} - V_{OUT} = L \times \frac{\Delta i}{\Delta t} \; ; \; \Delta t = D \times \frac{1}{f_S} \; ; \; D = \frac{V_{OUT}}{V_{IN}}$$

$$L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times \Delta i \times f_S} \qquad ---(5)$$

Where:
V_{IN} = Max Input Voltage
V_{OUT} = Output Voltage
Δi = Inductor Ripple Current
f_S = Switching Frequency
Δt = Turn On Time
D = Duty Cycle

For Δi_1=25% of I_1, we get L_1=9.9μH
For Δi_2=25% of I_2, we get: L_2=5.7μH

Panasonic provides a range of inductors in different values and low profile for large currents.

For L_1 choose ETQP6F102HFA (10.2μH, 4A)
For L_2 choose ELLATV6R8M (6.8μH, 4A)

Power MOSFET Selection

The selections criteria to meet power transfer requirements is based on maximum drain-source voltage (V_{DSS}), gate-source drive voltage (V_{GS}), maximum output current, On-resistance $R_{DS(ON)}$ and thermal management.

The MOSFET must have a maximum operating voltage (V_{DSS}) exceeding the maximum input voltage (V_{IN}).

The gate drive requirement is almost the same for both MOSFETs. Caution should be taken with devices at very low V_{GS} to prevent undesired turn-on of the complementary MOSFET, which results a shoot-through current.

The total power dissipation for MOSFETs includes conduction and switching losses. For the Buck converter the average inductor current is equal to the DC load current. The conduction loss is defined as:

$$P_{COND}(\text{Upper Switch}) = I_{LOAD}^2 \times R_{DS(ON)} \times D \times \vartheta$$

$$P_{COND}(\text{Lower Switch}) = I_{LOAD}^2 \times R_{DS(ON)} \times (1 - D) \times \vartheta$$

ϑ = $R_{DS(ON)}$ Temperature Dependency

The total conduction loss is defined as:

$$P_{CON(TOTAL)} = P_{CON}(\text{Upper Switch})\vartheta + P_{CON}(\text{Lower Switch})\vartheta$$

The $R_{DS(ON)}$ temperature dependency should be considered for the worst case operation. This is typically given in the MOSFET data sheet. Ensure that the conduction losses and switching losses do not exceed the package ratings or violate the overall thermal budget.

For this design, AP9408AGH is a good choice. These devices provide low on-resistance in a compact TO-252 3Pin package.

The MOSFETs have the following data:

AP9408AGH
V_{DSS} = 30V
I_D = 33A @ 100°C
$R_{DS(ON)}$ = 10mΩ @ V_{GS}=10V
ϑ = 1.5 for 150°C (Junction Temperature)

The total conduction losses for channel 1 is:

P_{CON1} = 0.24W

The total conduction losses for channel 2 is:

P_{CON2} = 0.24W

The control MOSFET contributes to the majority of the switching losses in synchronous Buck converter. The synchronous MOSFET turns on under zero-voltage condition, therefore the turn on losses for synchronous MOSFET can be neglected. With a linear approximation, the total switching loss can be expressed as:

$$P_{SW} = \frac{V_{DS(OFF)}}{2} \times \frac{t_r + t_f}{T} \times I_{LOAD} \qquad \text{---(6)}$$

Where:
$V_{DS(OFF)}$ = Drain to Source Voltage at off time
t_r = Rise Time
t_f = Fall Time
T = Switching Period
I_{LOAD} = Load Current

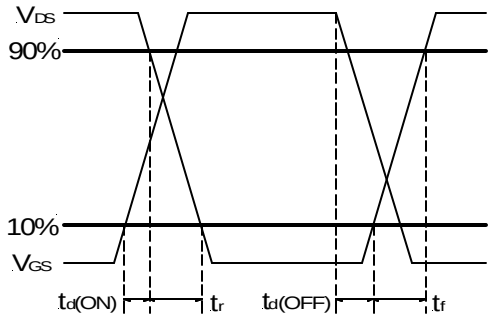


Figure 4 - Switching time waveforms.

From AP9408AGH data sheet we obtain:

AP9408AGH
t_r = 5ns
t_f = 6ns

These values are taken under a certain condition test. For more detail please refer to the AP9408AGH data sheet.

By using equation (6), we can calculate the switching losses.

P_{SW1} = 52.8mW
P_{SW2} = 22mW

Feedback Compensation

The APU3048 is a voltage mode controller; the control loop is a single voltage feedback path including error amplifier and error comparator. To achieve fast transient response and accurate output regulation, a compensation circuit is necessary. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency and adequate phase margin (greater than 45°).

The output LC filter introduces a double pole, –40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180° (see Figure 5). The Resonant frequency of the LC filter is expressed as follows:

$$F_{LC} = \frac{1}{2\pi\sqrt{Lo \times Co}} \qquad ---(7)$$

Figure 5 shows gain and phase of the LC filter. Since we already have 180° phase shift just from the output filter, the system risks being unstable.

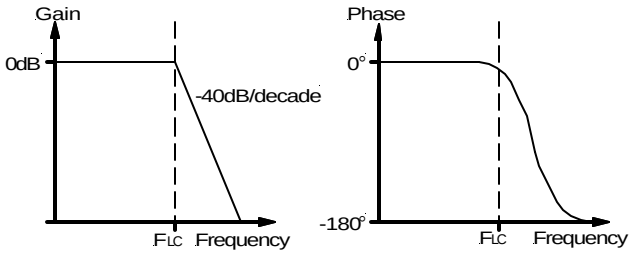


Figure 5 - Gain and phase of LC filter.

The APU3048's error amplifier is a differential-input transconductance amplifier. The output is available for DC gain control or AC phase compensation.

The E/A can be compensated with or without the use of local feedback. When operated without local feedback the transconductance properties of the E/A become evident and can be used to cancel one of the output filter poles. This will be accomplished with a series RC circuit from Comp1 pin to ground as shown in Figure 6.

The ESR zero of the LC filter expressed as follows:

$$F_{ESR} = \frac{1}{2\pi \times ESR \times Co} \qquad ---(8)$$

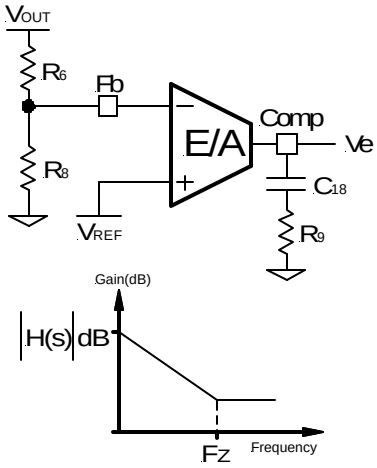


Figure 6 - Compensation network without local feedback and its asymptotic gain plot.

The transfer function (Ve / V_{OUT}) is given by:

$$H(s) = \left(g_m \times \frac{R_8}{R_6 + R_8}\right) \times \frac{1 + sR_9C_{18}}{sC_{18}} \qquad ---(9)$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$|H(s)| = g_m \times \frac{R_8}{R_6 \times R_8} \times R_9 \qquad ---(10)$$

$$F_Z = \frac{1}{2\pi \times R_9 \times C_{18}} \qquad ---(11)$$

The gain is determined by the voltage divider and E/A's transconductance gain.

First select the desired zero-crossover frequency (Fo):

$F_{O1} > F_{ESR}$ and $F_{O1} \le (1/5 \sim 1/10) \times f_S$

Use the following equation to calculate R4:

$$R_9 = \frac{V_{OSC}}{V_{IN1}} \times \frac{F_{O1} \times F_{ESR1}}{F_{LC1}^2} \times \frac{R_8 + R_6}{R_8} \times \frac{1}{g_m} \qquad ---(12)$$

Where:

V_{IN1} = Maximum Input Voltage

V_{OSC} = Oscillator Ramp Voltage

F_{O1} = Crossover Frequency for the master E/A

F_{ESR1} = Zero Frequency of the Output Capacitor

F_{LC1} = Resonant Frequency of Output Filter

g_m = Error Amplifier Transconductance

R_8 and R_6 = Resistor Dividers for Output Voltage Programming

For:

V_{IN1} = 12V
V_{OSC} = 1.25V
F_{O1} = 30KHz
F_{ESR1} = 26.5KHz
F_{LC1} = 2.8KHz
R_8 = 1K
R_6 = 1.64K
gm = 600μmho

This results to R_9=46.4KΩ; Choose R_9=46.4KΩ

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$$F_Z \cong 75\% F_{LC1}$$

$$F_Z \cong 0.75 \times \frac{1}{2\pi\sqrt{L_3 \times C_O}} \qquad ---(13)$$

For:

L_3 = 10.2μH
Co = 300μF
Fz = 2.1KHz
R_9 = 46.4KΩ

Using equations (11) and (13) to calculate C_9, we get:

C_9= 1630pF; Choose C_9 = 1800pF

Using equations (11),(12) and (13) for Ch2, where:

V_{IN2} = 5V
V_{OSC} = 1.25V
F_{O2} = 30KHz
F_{ESR2} = 26.5KHz
F_{LC2} = 3.5KHz
R_{15} = 1K
R_{14} = 442Ω
gm = 600μhmo

We get:

R_{11} = 38.9KΩ; Choose R_{11} = 39.2KΩ
C_{19} = 1554pF; Choose C_{19} = 1800pF

One more capacitor is sometimes added in parallel with C_9 and R_4. This introduces one more pole which is mainly used to supress the switching noise. The additional pole is given by:

$$F_P = \frac{1}{2\pi \times R_9 \times \frac{C_{18} \times C_{POLE}}{C_{18} + C_{POLE}}}$$

The pole sets to one half of switching frequency which results in the capacitor C_{POLE}:

$$C_{POLE} = \frac{1}{\pi \times R_9 \times f_S - \frac{1}{C_{18}}} \cong \frac{1}{\pi \times R_9 \times f_S}$$

For $F_P << \frac{f_S}{2}$

For a general solution for unconditionally stability for any type of output capacitors, in a wide range of ESR values we should implement local feedback with a compensation network. The typically used compensation network for voltage-mode controller is shown in Figure 7.

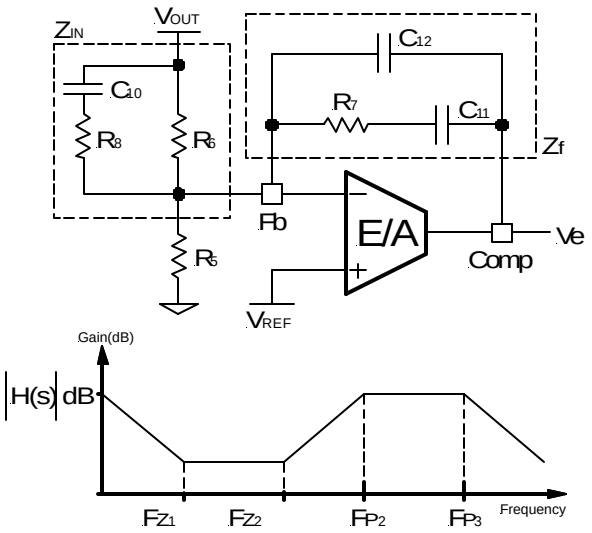


Figure 7 - Compensation network with local feedback and its asymptotic gain plot.

In such configuration, the transfer function is given by:

$$\frac{Ve}{V_{OUT}} = \frac{1 - g_m Z_f}{1 + g_m Z_{IN}}$$

The error amplifier gain is independent of the transconductance under the following condition:

$$g_m Z_f >> 1 \quad \text{and} \quad g_m Z_{IN} >> 1 \qquad ---(14)$$

By replacing Z_{IN} and Z_f according to figure 7, the transformer function can be expressed as:

$$H(s) = \frac{1}{sR_6(C_{12}+C_{11})} \times \frac{(1+sR_7C_{11}) \times [1+sC_{10}(R_6+R_8)]}{\left[1+sR_7\left(\frac{C_{12}C_{11}}{C_{12}+C_{11}}\right)\right] \times (1+sR_8C_{10})}$$

As known, transconductance amplifier has high impedance (current source) output, therefore, consider should be taken when loading the E/A output. It may exceed its source/sink output current capability, so that the amplifier will not be able to swing its output voltage over the necessary range.

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0 \qquad F_{P2} = \frac{1}{2\pi \times R_8 \times C_{10}}$$

$$F_{P3} = \frac{1}{2\pi \times R_7 \times \left(\frac{C_{12} \times C_{11}}{C_{12}+C_{11}}\right)} \cong \frac{1}{2\pi \times R_7 \times C_{12}}$$

$$F_{Z1} = \frac{1}{2\pi \times R_7 \times C_{11}}$$

$$F_{Z2} = \frac{1}{2\pi \times C_{10} \times (R_6 + R_8)} \cong \frac{1}{2\pi \times C_{10} \times R_6}$$

Cross Over Frequency:

$$F_{O1} = R_7 \times C_{10} \times \frac{V_{IN}}{V_{OSC}} \times \frac{1}{2\pi \times Lo \times Co} \quad \text{---(15)}$$

Where:
V_{IN} = Maximum Input Voltage
V_{OSC} = Oscillator Ramp Voltage
Lo = Output Inductor
Co = Total Output Capacitors

The stability requirement will be satisfied by placing the poles and zeros of the compensation network according to following design rules. The consideration has been taken to satisfy condition 14 regarding transconductance error amplifier.

1) Select the crossover frequency:

$Fo < F_{ESR}$ and $Fo \leq (1/10 \sim 1/6) \times f_S$

2) Select R_7, so that $R_7 >> \frac{2}{gm}$

3) Place first zero before LC's resonant frequency pole.

$F_{Z1} \cong 75\% F_{LC}$

$$C_{11} = \frac{1}{2\pi \times F_{Z1} \times R_7}$$

4) Place third pole at the half of the switching frequency.

$$F_{P3} = \frac{f_S}{2}$$

$$C_{12} = \frac{1}{2\pi \times R_7 \times F_{P3}}$$

$C_{12} > 50pF$
If not, change R_7 selection.

5) Place R_7 in (15) and calculate C_{10}:

$$C_{10} \leq \frac{2\pi \times Lo \times Fo \times Co}{R_7} \times \frac{V_{OSC}}{V_{IN}}$$

6) Place second pole at ESR zero.
$F_{P2} = F_{ESR}$

$$R_8 = \frac{1}{2\pi \times C10 \times F_{P2}}$$

Check if $R_8 > \frac{1}{gm}$

If R_8 is too small, increase R_7 and start from step 2.

7) Place second zero around the resonant frequency.
$F_{Z2} = F_{LC}$

$$R_6 = \frac{1}{2\pi \times C10 \times F_{Z2}} - R_8$$

8) Use equation (1) to calculate R_5:

$$R_5 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_6$$

These design rules will give a crossover frequency approximately one-tenth of the switching frequency. The higher the band width, the potentially faster the load transient speed. The gain margin will be large enough to provide high DC-regulation accuracy (typically -5dB to -12dB). The phase margin should be greater than 45° for overall stability.

LDO Section

Output Voltage Programming

Output voltage for LDO is programmed by reference voltage and external voltage divider. The Fb3 pin is the inverting input of the error amplifier, which is internally referenced to 1.25V. The divider is ratioed to provide 1.25V at the Fb3 pin when the output is at its desired value. The output voltage is defined by using the following equation:

$$V_{OUT2} = V_{REF} \times \left(1 + \frac{R_{HIGH}}{R_{LOW}}\right)$$

For:
V_{OUT2} = 2.5V
V_{REF} = 1.25V
R_{LOW} = 1K

Results to: R_{HIGH}=1K

LDO Power MOSFET Selection

The first step in selecting the power MOSFET for the linear regulator is to select the maximum $R_{DS(ON)}$ based on the input to the dropout voltage and the maximum load current.

$$R_{DS(ON)} = \frac{V_{IN3} - V_{OUT2}}{I_{OUT2}}$$

For:
V_{IN3} = 3.3V
V_{OUT2} = 2.5V
I_{OUT2} = 2A

Results to: $R_{DS(ON)(MAX)} = 0.4\Omega$

Note that since the MOSFET $R_{DS(ON)}$ increases with temperature, this number must be divided by ~1.5 in order to find the $R_{DS(ON)(MAX)}$ at room temperature. The AP20T03GH has a maximum of 0.05Ω $R_{DS(ON)}$ at room temperature, which meets our requirements.

Layout Consideration

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Start to place the power components, make all the connection in the top layer with wide, copper filled areas. The inductor, output capacitor and the MOSFET should be close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place input capacitor directly to the drain of the high-side MOSFET, to reduce the ESR replace the single input capacitor with two parallel units. The feedback part of the system should be kept away from the inductor and other noise sources, and be placed close to the IC. In multilayer PCB use one layer as power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.

TYPICAL APPLICATION

12V to 3.3V @ 4A
12V to 1.8V @ 4A
3.3V to 2.5V @ 2A

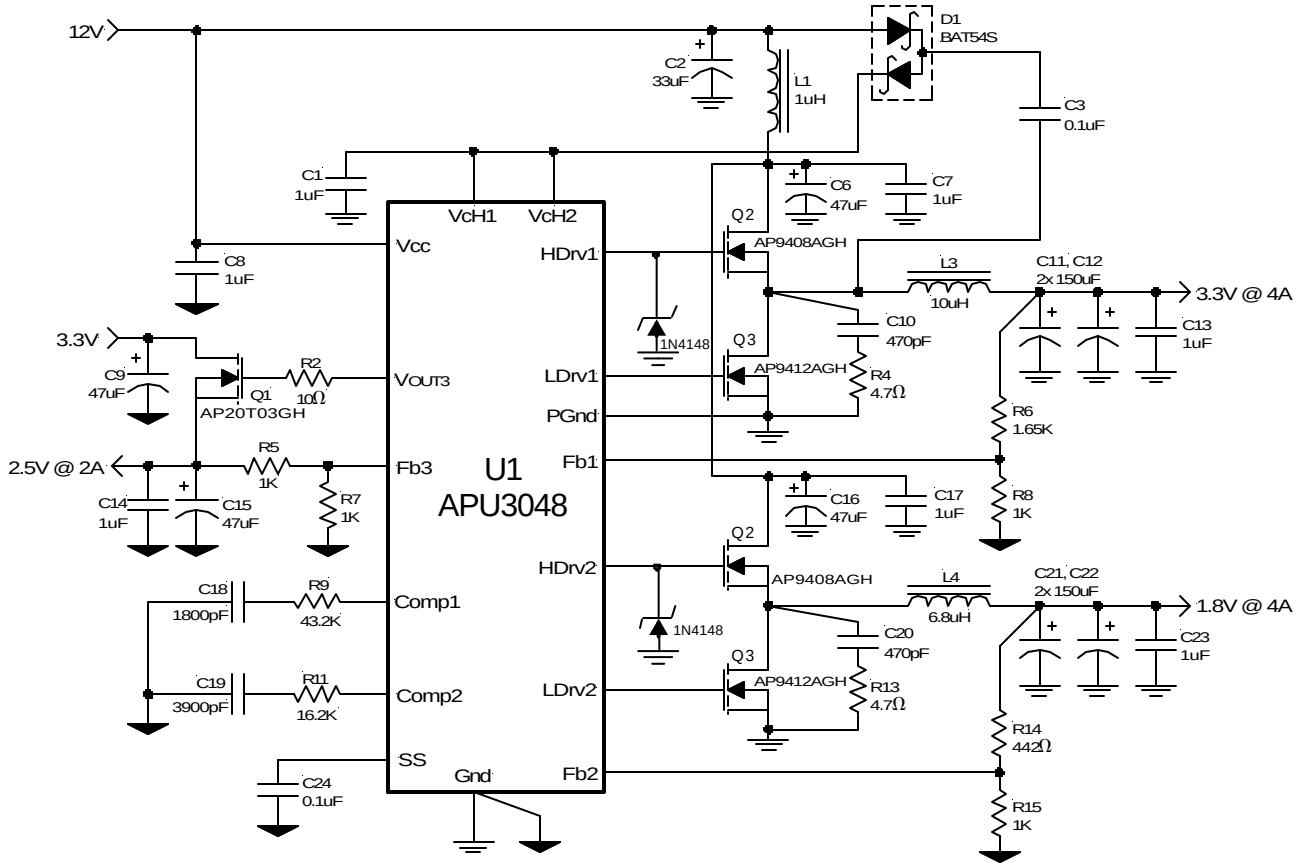


Figure 8 - Typical application of APU3048 in an on-board DC-DC converter using a single 12V supply for switcher.

DEMO-BOARD APPLICATION

12V to 3.3V @ 4A
5V to 1.8V @ 4A
3.3V to 2.5V @ 2A

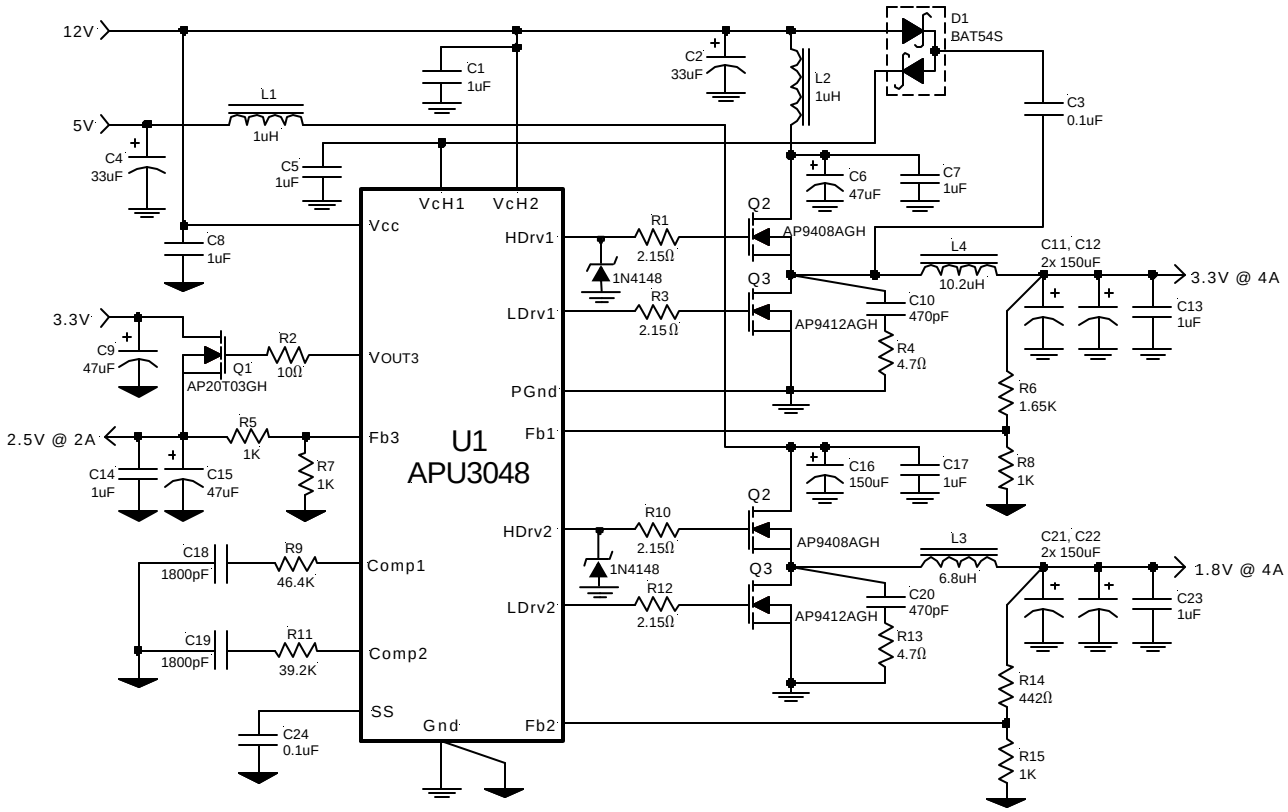


Figure 9 - Demo-board application of APU3048.

DEMO-BOARD APPLICATION

12V to 3.3V @ 4A
5V to 1.8V @ 4A
3.3V to 2.5V @ 2A

Ref Desig	Description	Value	Qty	Part#	Manuf	Web site (www.)
Q1	MOSFET	30V, 50mohm, 1.5A	1	AP20T03GH	APEC	a-power.com.tw
Q2	MOSFET	30V, 10mohm, 53A	2	AP9408AGH	APEC	
Q3	MOSFET	30V, 6mohm, 68A	2	AP9412AGH	APEC	
U1	Controller	Synchronous PWM	1	APU3048	APEC	
D1	Diode	Fast Switching	1	BAT54S	IR	
L1, L2	Inductor	1μH, 2.9A	2	ELL6SH1R0M	Panasonic	maco.panasonic.co.jp
L3	Inductor	6.8μH, 4A	1	ELLATV6R8M	Panasonic	
L4	Inductor	10.2μH, 4A	1	ETQP6F102HFA	Panasonic	
C1,7,8,13, 14,17,23	Cap, Ceramic	1μF, Y5V, 16V	7	ECJ-2VF1C105Z	Panasonic	
C2, C4	Cap, Tantalum	33μF, 16V	2	ECS-T1CD336R	Panasonic	
C3, C24	Cap, Ceramic	0.1μF, Y5V, 25V	2	ECJ-2VF1E104Z	Panasonic	
C5	Cap, Ceramic	1μF, X7R, 25V	1	ECJ-3YB1E105K	Panasonic	
C9, C15	Cap, Tantalum	47μF, 10V	2	ECS-T1AD476R	Panasonic	
C10, C20	Cap, Ceramic	470pF, X7R, 50V	2	ECJ-2VC1H471J	Panasonic	
C18, C19	Cap, Ceramic	1800pF, X7R, 50V	2	ECJ-2VB1H182K	Panasonic	
C6	Cap, Poscap	47μF, 16V, 70mΩ	1	16TPB47M	Sanyo	sanyo.com/industrial
C11,12,16 21,22	Cap, Poscap	150μF, 6.3V, 40mΩ	5	6TPC150M	Sanyo	
R1,3,10,12	Resistor	2.15Ω	4			
R2	Resistor	10Ω	1			
R4, R13	Resistor	4.7Ω	2			
R5,7,8,15	Resistor	1K, 1%	4			
R6	Resistor	1.65K, 1%	1			
R9	Resistor	46.4K	1			
R11	Resistor	39.2K	1			
R14	Resistor	442Ω, 1%	1			

WAVEFORMS

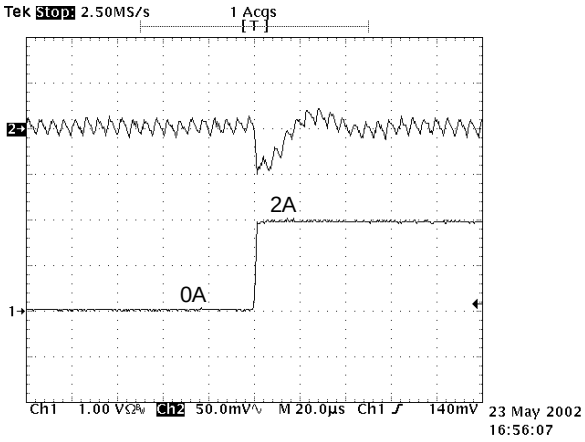


Figure 4 - Transient response @ I_{OUT} = 0 to 2A for 3.3V output.

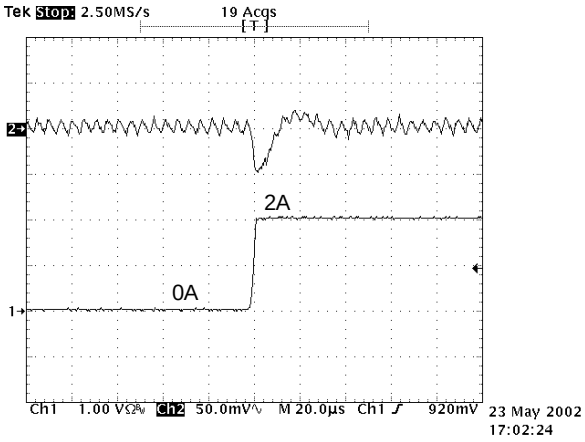


Figure 5 - Transient response @ I_{OUT} = 0 to 2A for 1.8V output.

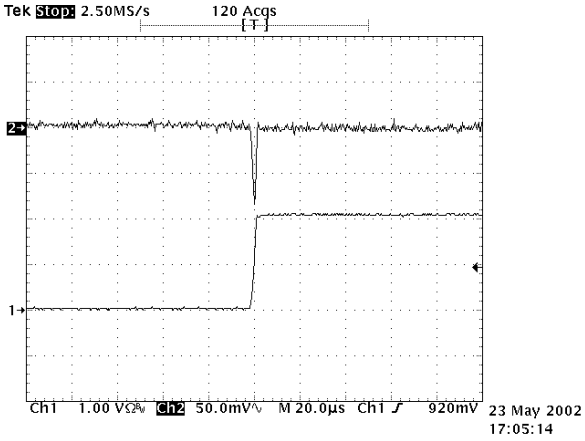


Figure 6 - Transient response @ I_{OUT} = 0 to 2A for 2.5V output.

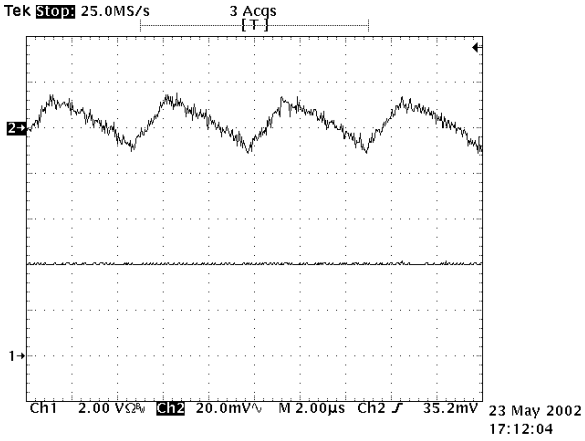


Figure 7 - Output voltage ripple for 3.3V @ 4A.

WAVEFORMS

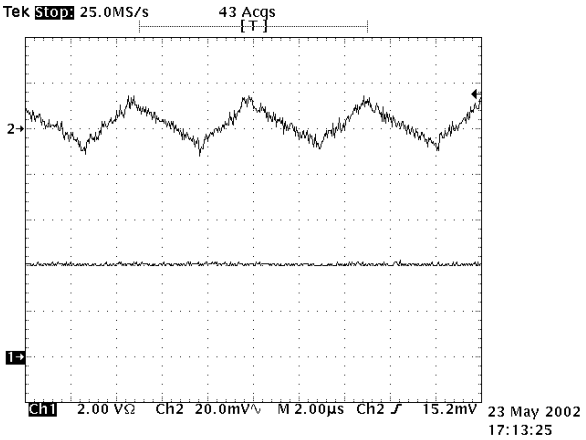


Figure 8 - Output voltage ripple for 1.8V @ 4A.

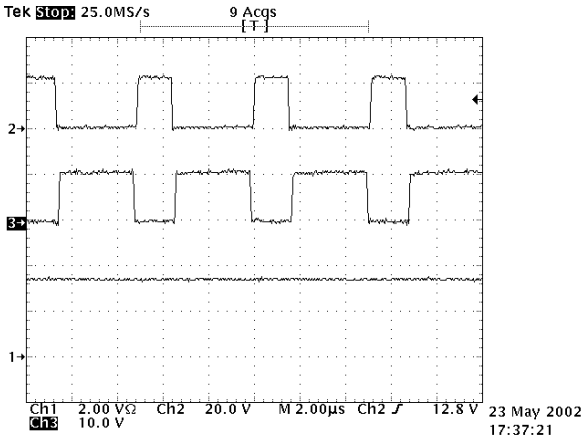


Figure 9 - Gate signals for 3.3V output.
Ch1: Output current 2A/div.
Ch2: Gate signal for control FET 20V/div.
Ch3: Gate signal for sync FET 10V/div.

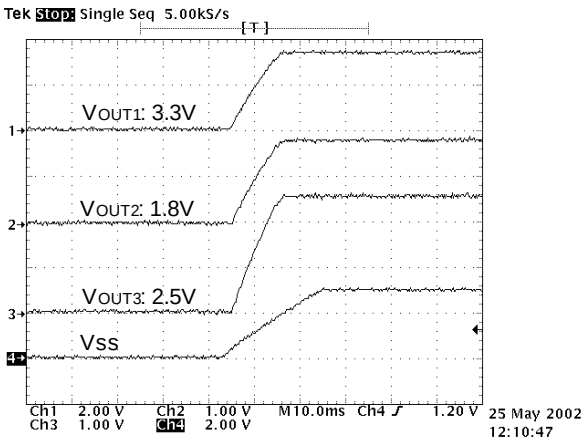


Figure 10 - Soft-start voltage Vs. output voltages.

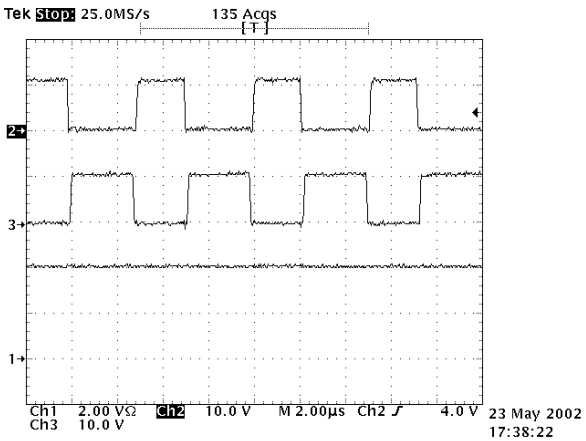
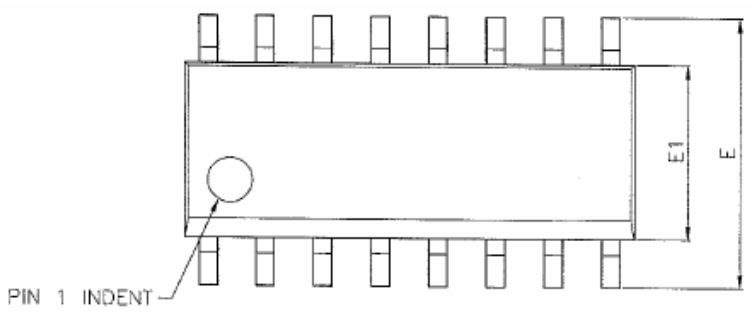
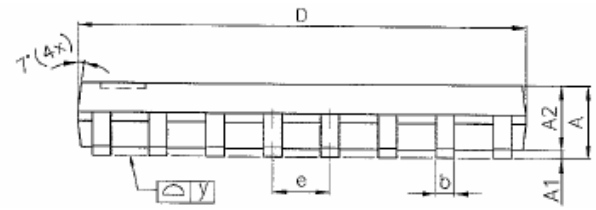
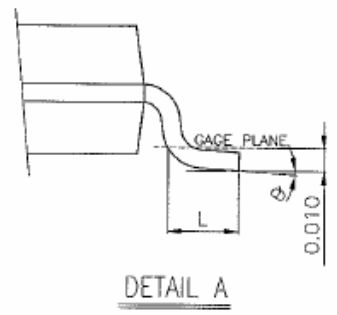


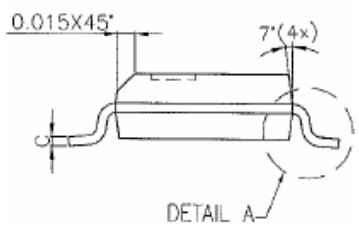
Figure 11 - Gate signals for 1.8V output.
Ch1: Output current 2A/div.
Ch2: Gate signal for control FET 10V/div.
Ch3: Gate signal for sync FET 10V/div.

Package Outline : SOP-16







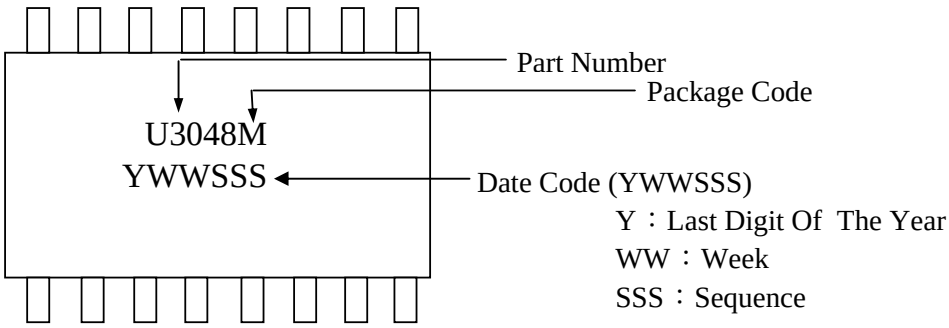


SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	1.47	1.60	1.73
A1	0.10	—	0.25
A2	—	1.45	—
b	0.33	0.41	0.51
C	0.19	0.20	0.25
D	9.80	9.91	10.01
E	5.79	5.99	6.20
E1	3.81	3.91	3.99
e	—	1.27	—
L	0.38	0.71	1.27
y	—	—	0.08
θ	0°	—	8°

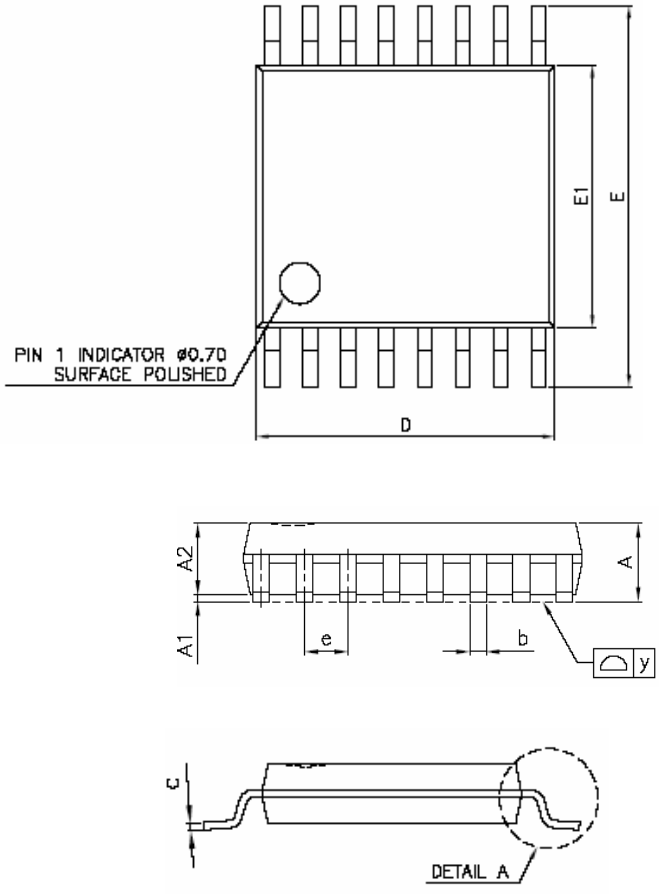
1.All Dimensions Are in Millimeters.

2.Dimension Does Not Include Mold Protrusions.

Part Marking Information & Packing : SOP-16



Package Outline : TSSOP-16



	Millimeters		
SYMBOLS	MIN	NOM	MAX
A	1.05	1.10	1.20
A1	0.05	0.10	0.15
A2	—	1.00	1.05
b	0.20	0.25	0.28
C	—	0.13	—
D	4.90	5.08	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	—	0.65	—
L	0.50	0.60	0.70
y	—	—	0.08
θ	0°	4°	8°

Part Marking Information & Packing : TSSOP-16