

LH0084/LH0085 LH0086/LH0087

Z80 SIO Serial Input/Output Controller

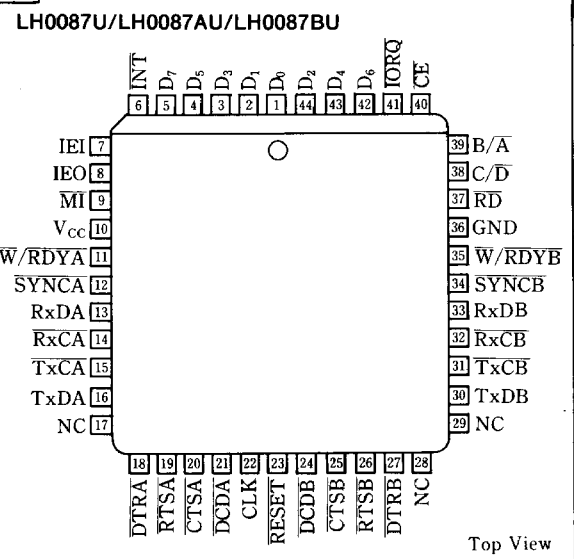
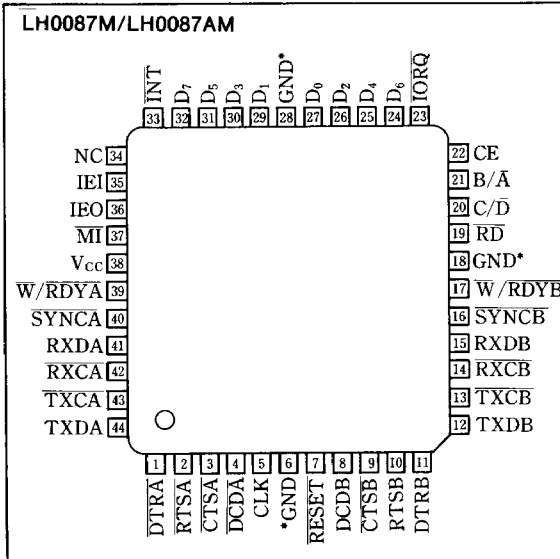
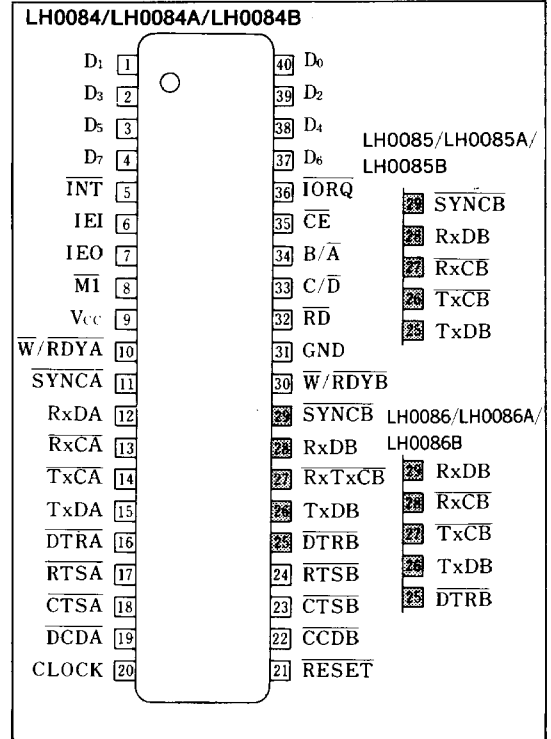
■ Description

The LH0084/85/86/87, Z80 SIO (Z80 SIO for short below) is a dual-channel multi-function peripheral component designed to satisfy a wide variety of serial data communications requirements in microcomputer systems. Its basic function is a serial-to-parallel, parallel-to-serial converter/controller, but—within that role—it is configurable by systems software so its “personality” can be optimized for a given serial data communications application.

The Z80 SIO is capable of handling asynchronous and synchronous byte-oriented protocols such as IBM Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device can also be used to support virtually any other serial protocol for applications other than data communications (cassette or floppy disk interfaces, for example).

The Z80 SIO can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The device also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for

■ Pin Connections



Top View

* The GND pins must be connected to the GND level.

general-purpose I/O.

The Z80 SIO has six types as below according to its system clock and bonding option. The Z80A SIO and the Z80B SIO are a high speed version which can operate at the 4MHz and 6MHz system clock, respectively.

- LH0084 Z80 SIO/0
- LH0085 Z80 SIO/1
- LH0086 Z80 SIO/2
- LH0087 Z80 SIO
- LH0084A Z80A SIO/0
- LH0085A Z80A SIO/1
- LH0086A Z80A SIO/2
- LH0087A Z80A SIO
- LH0084B Z80B SIO/0
- LH0085B Z80B SIO/1
- LH0086B Z80B SIO/2
- LH0087B Z80B SIO

■ Features

1. N-channel silicon-gate process
2. Single +5V power supply and single phase clock
3. Two independent full duplex channels
4. Data rates : 0. to 500K bits/second (at 2.5 MHz system clock)
: 0 to 800K bits/second (at 4MHz system clock)
: 0 to 1200K bits/second (at 6MHz system clock)
5. Asynchronous operation
 - 5, 6, 7 or 8 bits/character
 - 1, 1½ or 2 stop bits/character
 - Even, odd or no parity

- ×1, ×16, ×32 and ×64 clock modes
 - Break generation and detection
 - Parity, Overrun and Framing error detection
6. Binary synchronous operation
 - Internal or external character synchronization
 - One or two Sync characters in separate registers
 - Automatic Sync character insertion
 - CRC generation and checking
 7. HDLC or IBM SDLC operation
 - Abort sequence generation and detection
 - Automatic zero insertion and detection
 - Automatic flag insertion
 - Address field recognition
 - I-field residue handling
 - Valid receive messages protected from overrun
 - CRC generation and checking
 8. Vectored daisy chain priority interrupt logic
 9. CRC-16 or CRC-CCITT block check
 10. Separate modem control inputs and outputs for both channels
 11. Modem status can be monitored
 12. 40-pin DIP (DIP40-P-600)
44-pin QFP (QFP44-P-1010A)
44-pin QFJ (QFJ44-P-S650)

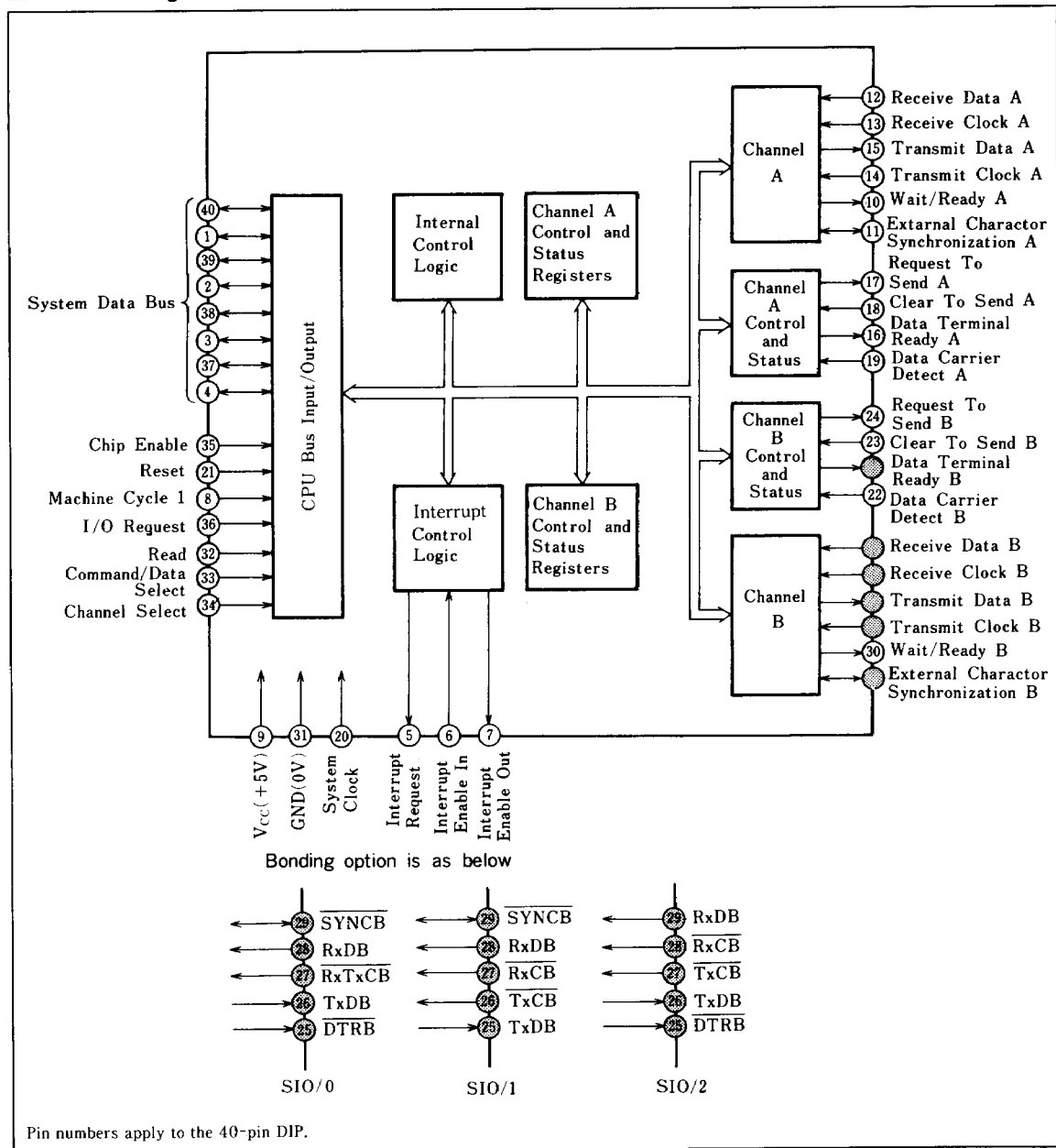
■ Ordering Information

Product	Z80 SIO	Z80A SIO	Z80B SIO	Package	Operating temperature
Clock frequency	2.5MHz	4MHz	6MHz		
Model No.	LH008X	LH008XA	LH008XB	40-pin DIP	0°C to +70°C
	LH008XH	LH008XAH			-20°C to +85°C
	LH0087M	LH0087AM		44-pin QFP	0°C to +60°C
	LH0087U	LH0087AU	LH0087BU	44-pin QFJ	0°C to +70°C

- X: It is the bonding option to select one of SIO/0, SIO/1 and SIO/2 on 40-pin DIP.
 X=4: SIO/0
 X=5: SIO/1
 X=6: SIO/2
 H: H affix indicates a wide temperature spec, packaged in 40-pin DIP.



■ Block Diagram



■ Pin Description

Pin	Meaning	I/O	Function
D ₀ -D ₇	Data bus	Bidirectional 3-state	System data bus
B/ \bar{A}	Channel A or B select	I	Defines which channel is accessed. Channel B at "High", channel A at "Low".
C/ \bar{D}	Control or data select	I	Defines the type of information transfer on the data bus. Control word at "High", data at "Low".
\bar{CE}	Chip enable	I	Active "Low". A Low enables the CPU to transmit and receive control words and data.
CLOCK	System clock	I	Standard Z80 system clock used for internal synchronization signals.
$\bar{M1}$	Machine cycle one	I	Active "Low". Indicates that the CPU is acknowledging an interrupt, when both $\bar{M1}$ and \bar{IORQ} are active.
\bar{IORQ}	Input/output request	I	Active "Low". Read operation when \bar{RD} is active, and write operation when it is not active. Indicates that the CPU is acknowledging an interrupt, when both \bar{IORQ} and $\bar{M1}$ are active.
\bar{RD}	Read cycle status	I	Active "Low". Read operation when active.
RESET	Reset	I	Active "Low". Resets the interrupt bits.
IEI	Interrupt enable in	I	Active "High". Used to form a priority-interrupt daisy chain.
IEO	Interrupt enable out	O	Active "High". Used to form a priority-interrupt daisy chain.
INT	Interrupt request	Open drain, O	Active "Low". Active when requesting an interrupt.
$\bar{W/RDYA}$ $\bar{W/RDYB}$	Wait/ready	Open drain, O	Active "Low". READY when the DMA is a bus master, WAIT when the CPU is a bus master.
\bar{CTSA} , \bar{CTSB}	Clear to send	I	Active "Low". Enables the respective transmitters. Also applicable as general-purpose input pins.
\bar{DCDA} , \bar{DCDB}	Data carrier detect	I	Active "Low". Enables the respective receivers. Also applicable as general-purpose input pins.
RxDA, RxDB	Receive data	I	Active "Low". Data line for receiving
TxDA, TxDB	Transmit data	O	Active "Low". Data line for transmitting.
RxCA, RxCB	Receiver clock	I	Active "Low". Receiving synchronization clock.
TxCA, TxCB	Transmitter clock	I	Active "Low". Transmitting synchronization clock.
\bar{RTSA} , \bar{RTSB}	Request to send	O	Active "Low". Indicates that the transmitter is empty during transfer. Also applicable as general-purpose output pins.
\bar{DTRA} , \bar{DTRB}	Data terminal ready	O	Active "Low". Also applicable as general-purpose output pins.
\bar{SYNCA} , \bar{SYNCB}	External character synchronization	I	Active "Low". Acts the same way as CTS and DCD in the asynchronous mode. Driven "Low" in the synchronous mode when a synchronizing pattern is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Input voltage	V _{IN}	-0.3 to +7.0	V	
Output voltage	V _{OUT}	-0.3 to +7.0	V	
Operating temperature	T _{opr}	0 to +70	°C	1
		0 to +60		2
		-20 to +85		3
Storage temperature	T _{stg}	-65 to +150	°C	

Note 1: Specified for 40-pin DIP and 44-pin QFJ

Note 2: Specified for 44-pin QFP

Note 3: Specified for wide temperature type

DC Characteristics

(V_{CC} = 5V ± 5%, T_a = 0 to +70°C^{Note 1})

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock input low voltage	V _{ILC}		-0.3		0.45	V
Clock input high voltage	V _{IHC}		V _{CC} - 0.6		5.5	V
Input low voltage	V _{IL}		-0.3		0.8	V
Input high voltage	V _{IH}		2.0		5.5	V
Output low voltage	V _{OL}	I _{OL} = 2.0mA			0.4	V
Output high voltage	V _{OH}	I _{OH} = -250 μA	2.4			V
Input leakage current	I _{LI}	0 < V _{IN} < V _{CC}			10	μA
3-state output/data bus input leakage current	I _Z	0 < V _{IN} < V _{CC}			10	μA
SYNC pin leakage current	I _{L(SY)}	0 < V _{IN} < V _{CC}	-40		10	μA
Current consumption	I _{CC}				100	mA

Note 1: T_a = 0 to +60°C for 44-pin QFP, T_a = -20 to +85°C for wide temperature types.

Capacitance

(f = 1MHz, T_a = 25°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock capacitance	C _{CLOCK}	Unmeasured pins returned to ground			40	pF
Input capacitance	C _{IN}				5	pF
Output capacitance	C _{OUT}				10	pF

AC Characteristics

(1) AC characteristics (I)

(V_{CC} = 5V ± 5%, T_a = 0 to +70°C^{Note 1})

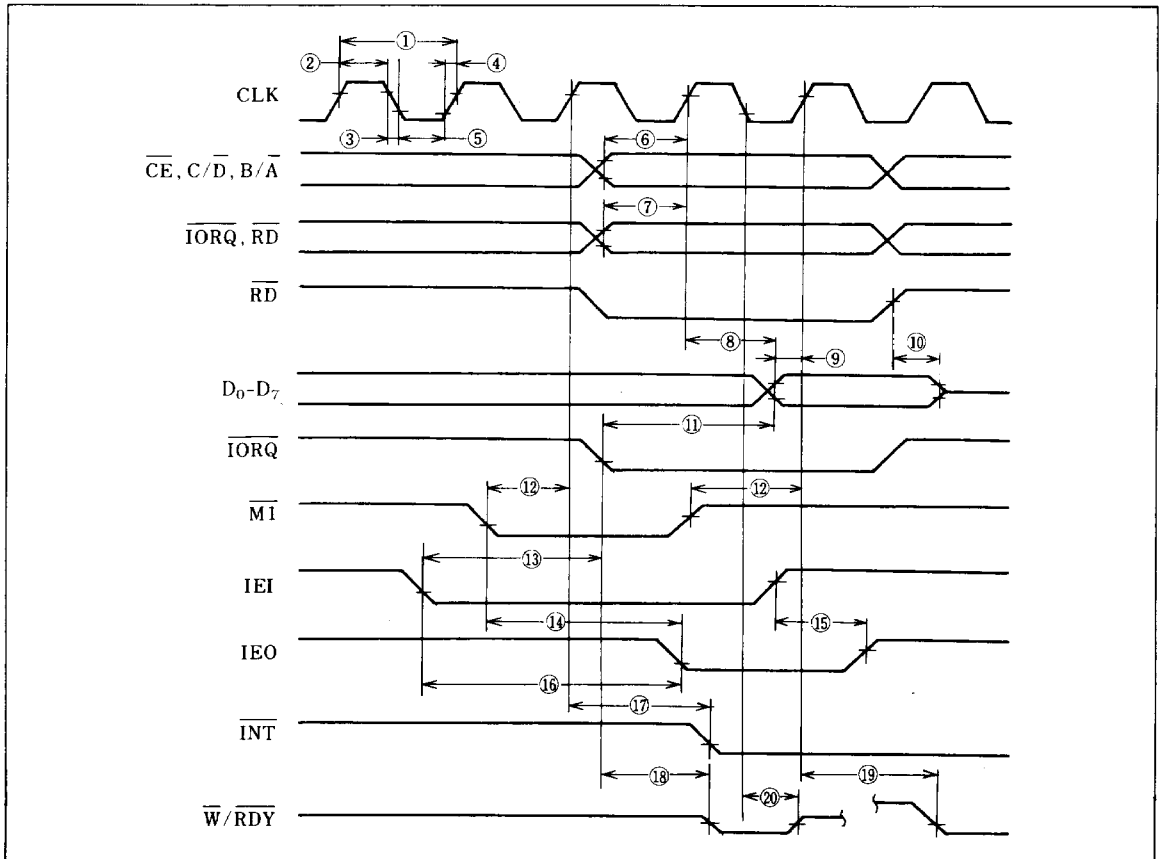
No.	Parameter	Symbol	LH0084/5/6/7		LH0084A/5A/6A/7A		LH0084B/5B/6B/7B		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
1	Clock cycle time	T _{cC}	400	4000	250	4000	165	4000	ns
2	Clock high width	T _{wCh}	170	2000	105	2000	70	2000	ns
3	Clock fall time	T _{fC}		30		30		15	ns
4	Clock rise time	T _{rC}		30		30		15	ns
5	Clock low width	T _{wCl}	170	2000	105	2000	70	2000	ns
6	CE, C/D, B/A to clock ↑ setup time	T _{sAD(C)}	160		145		60		ns
7	IORQ, RD to clock ↑ setup time	T _{sCS(C)}	240		115		60		ns
8	Clock ↑ to data out delay	T _{dC(DO)}		240		220		150	ns
9	Data in to clock ↑ setup (Write or $\overline{M1}$ cycle)	T _{sDI(C)}	50		50		30		ns
10	RD ↑ to data out float delay	T _{dRD(DOz)}		230		110		90	ns
11	IORQ ↓ to data out delay (INTACK cycle)	T _{dIO(DOI)}		340		160		100	ns

No.	Parameter	Symbol	LH0084/5/6/7		LH0084A/5A/6A/7A		LH0084B/5B/6B/7B		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
12	M1 to clock ↑ setup time	TsM1(C)	210		90		75		ns
13	IEI to IORQ ↓ setup time (INTACK cycle)	TsIEI(IO)	200		140		120		ns
14	M1 ↓ to IEO ↓ delay (interrupt before M1)	TdM1(IEO)		300		190		160	ns
15	IEI ↑ to IEO ↑ delay (after ED decode)	TdIEI(IEOr)		150		100		70	ns
16	IEI ↓ to INT ↓ delay	TdIEI(IEOf)		150		100		70	ns
17	Clock ↑ to INT ↓ delay	TdC(INT)		200		200		150	ns
18	IORQ ↓ or CE ↓ to W/RDY ↓ delay (wait mode)	TdIO(W/RWf)		300		210		175	ns
19	Clock ↑ to W/RDY ↓ delay (ready mode)	TdC(W/PR)		120		120		100	ns
20	Clock ↓ to W/RDY float delay (wait mode)	TdC(W/RWz)		150		130		110	ns
21	Any unspecified hold when setup is specified	Th	0		0		0		ns

↑ Rising edge, ↓ Falling edge.

Note 1: Ta=0 to +60°C for 44-pin QFP
 Ta=-20 to +85°C for wide temperature types

(2) AC timing chart (I)



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(3) AC characteristics (II)

($V_{CC}=5V \pm 5\%$, $T_a=0$ to $+70^\circ C$ ^{Note 1})

No.	Parameter	Symbol	LH0084/5/6/7		LH0084A/5A/6A/7A		LH0084B/5B/6B/7B		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
1	Pulse high width	T_{wPh}	200		200		200		ns
2	Pulse low width	T_{wPl}	200		200		200		ns
3	\overline{TxC} clock time	T_{cTxC}	400	∞	400	∞	330	∞	ns
4	\overline{TxC} low width	T_{wTxCl}	180	∞	180	∞	100	∞	ns
5	\overline{TxC} high width	T_{wTxCh}	180	∞	180	∞	100	∞	ns
6	$\overline{TxC} \downarrow$ to \overline{TxD} delay (xl mode)	$T_{dTxC(TxD)}$		400		300		220	ns
7	$\overline{TxC} \downarrow$ to $\overline{W/RDY} \downarrow$ delay (ready mode)	$T_{dTxC(W/RRf)}$	5	9	5	9	5	9	Clock period
8	$\overline{TxC} \downarrow$ to $\overline{INT} \downarrow$ delay	$T_{dTxC(INT)}$	5	9	5	9	5	9	Clock period
9	\overline{RxC} cycle time	T_{dRxC}	400	∞	400	∞	330	∞	ns
10	\overline{RxC} low width	T_{wRxC}	180	∞	180	∞	100	∞	ns
11	\overline{RxC} high width	T_{wRxC}	180	∞	180	∞	100	∞	ns
12	\overline{RxD} to $\overline{RxC} \uparrow$ setup time (xl mode)	$T_{sRxD(RxC)}$	0		0		0		ns
13	$\overline{RxC} \uparrow$ to \overline{RxD} hold time (xl mode)	$T_{hRxD(RxC)}$	140		140		100		ns
14	$\overline{RxC} \uparrow$ to $\overline{W/RDY} \downarrow$ delay (ready mode)	$T_{dRxC(W/RRf)}$	10	13	10	13	10	13	Clock period
15	$\overline{RxC} \uparrow$ to $\overline{INT} \downarrow$ delay	$T_{dRxC(INT)}$	10	13	10	13	10	13	Clock period
16	$\overline{RxC} \uparrow$ to $\overline{SYNC} \downarrow$ delay (output modes)	$T_{dRxC(SYNC)}$	4	7	4	7	4	7	Clock period
17	$\overline{SYNC} \downarrow$ to $\overline{RxC} \downarrow$ setup (external sync modes)	$T_{sSYNC(RxC)}$	-100		-100		100		ns

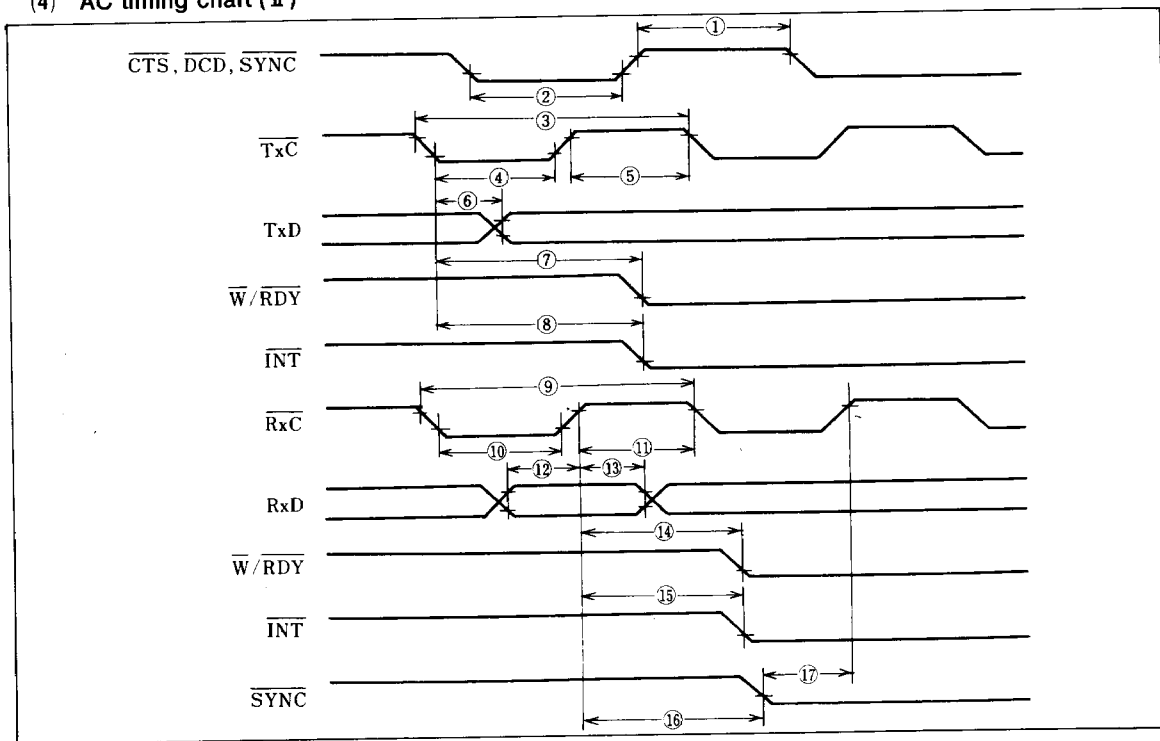
↑ Rising edge, ↓ Falling edge

Note 1: $T_a=0$ to $+60^\circ C$ for 44-pin QFP

$T_a=-20$ to $+85^\circ C$ for wide temperature types

Note 2: In all mode, the System Clock rate must be at least five times the maximum data rate.

(4) AC timing chart (II)



■ Transmit and Receive Data Path

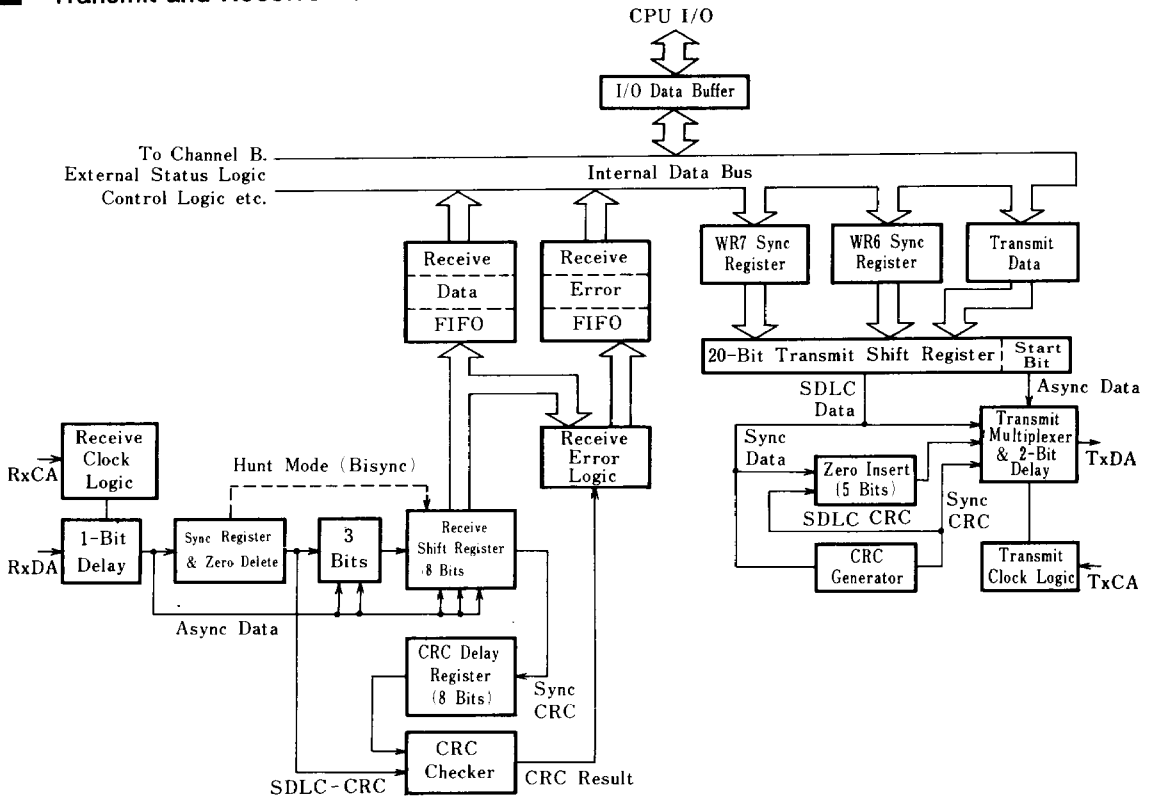


Fig. 1 Transmit and receive data path

■ Programming

The system program first issues a series of commands that initialize the basic mode of operation and then other commands that qualify conditions within the selected mode.

Both channels contain registers that must be programmed via the system program prior to operation.

(1) Read Registers

The SIO contains three read registers for Channel B and three read registers for Channel A (RR0-RR2) that can be read to obtain the status information. The status information includes error conditions, interrupt vector and standard communications-interface signals

● Read Register 0 (RR 0)

D7	D6	D5	D4	D3	D2	D1	D0
Break /abort	Tx under-run /EOM	CTS	Sync /hunt	DCD	Tx buffer empty	INT pending (ch.A only)	Rx character available

● Read Register 1 (RR 1)

The RR1 contains the status bits for specific receiving conditions as well as the one-field fraction codes for the SDLC receive mode.

D7	D6	D5	D4	D3	D2	D1	D0
End of frame	CRC/framing error	Rx overrun error	Parity error	Fraction code 2	Fraction code 1	Fraction code 0	All sent

● Read Register 2 (RR 2)

D7	D6	D5	D4	D3	D2	D1	D0
V7	V6	V5	V4	V3	V2	V1	V0

Valuable if "status affects vector" is programmed

(2) Write Registers

The SIO contains eight write registers for Channel B and eight write registers for Channel A (WR0-WR7) that are programmed separately to configure the functional personality of the channels.

● Write Register 0 (WR 0)

D7	D6	D5	D4	D3	D2	D1	D0
CRC reset code 1	CRC reset code 0	Command bit 2	Command bit 1	Command bit 0	Pointer bit 2	Pointer bit 1	Pointer bit 0
Control words				Register pointers			

● Write Register 1 (WR 1)

D7	D6	D5	D4	D3	D2	D1	D0
Wait ready enable	Wait/ready function	Wait/ready onR/T	Receive interrupt mode 1	Receive interrupt mode 0	Status affects vector	Tx INT enable	Ext INT enable

● Write Register 2 (WR 2)

The WR2 contains the interrupt vector for both channels and is only in the Channel B. When the status affected vector (WR1, D₂) is 1, the vector from the SIO during the interrupt acknowledge cycle varies (V₃ - V₁) depending on the interrupt conditions. The WR2 contents do not vary then.

D7	D6	D5	D4	D3	D2	D1	D0
V ₇	V ₆	V ₅	V ₄	V ₃	V ₂	V ₁	V ₀

● Write Register 3 (WR 3)

The WR 3 contains the bits and parameters to control the receivers.

D7	D6	D5	D4	D3	D2	D1	D0
Rx bits character 1	Rx bits character 0	Auto enable	Enter hunt phase	Rx CRC enable	Address search mode	Sync character load inhibit	Rx enable

● Write Register 4 (WR 4)

The WR4 has the bits control both receivers and transmitters.

In initializing for transmitting and receiving, these bits must be set up before the WR1, WR3, WR5, WR6, and WR7.

D7	D6	D5	D4	D3	D2	D1	D0
Clock rate 1	Clock rate 0	Sync mode 1	Sync mode 0	Stop bit 1	Stop bit 0	Parity Even/ODD	Parity enable

● Write Register 5 (WR 5)

The WR5 contains the bits (except for D₂) to control the transmitters.

D7	D6	D5	D4	D3	D2	D1	D0
DTR	Tx bits /character 1	Tx bits /character 0	Send break	Tx enable	CRC16/SDLC	RTS	Tx CRC enable

● Write Register 6 (WR 6)

D7	D6	D5	D4	D3	D2	D1	D0
SYNC 7	SYNC 6	SYNC 5	SYNC 4	SYNC 3	SYNC 2	SYNC 1	SYNC 0

● Write Register 7 (WR 7)

D7	D6	D5	D4	D3	D2	D1	D0
SYNC 15	SYNC 14	SYNC 13	SYNC 12	SYNC 11	SYNC 10	SYNC 9	SYNC 8

■ **Timing**

(1) **Read cycle**

The timing signals generated by a Z-80 CPU input instruction to read a data or status byte from the SIO are illustrated in Fig. 2.

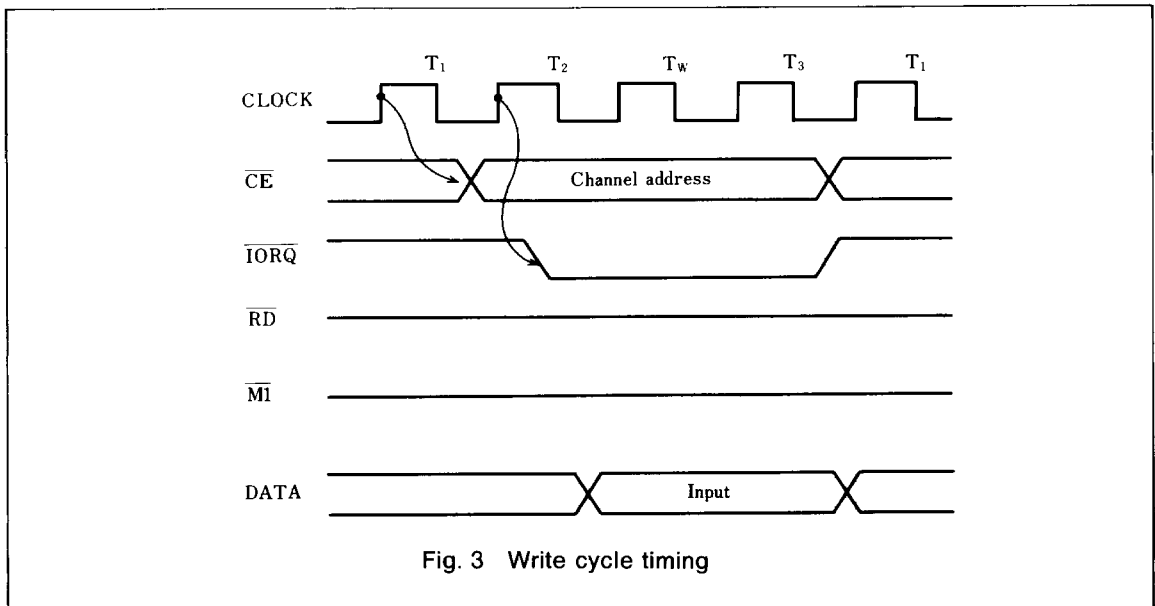
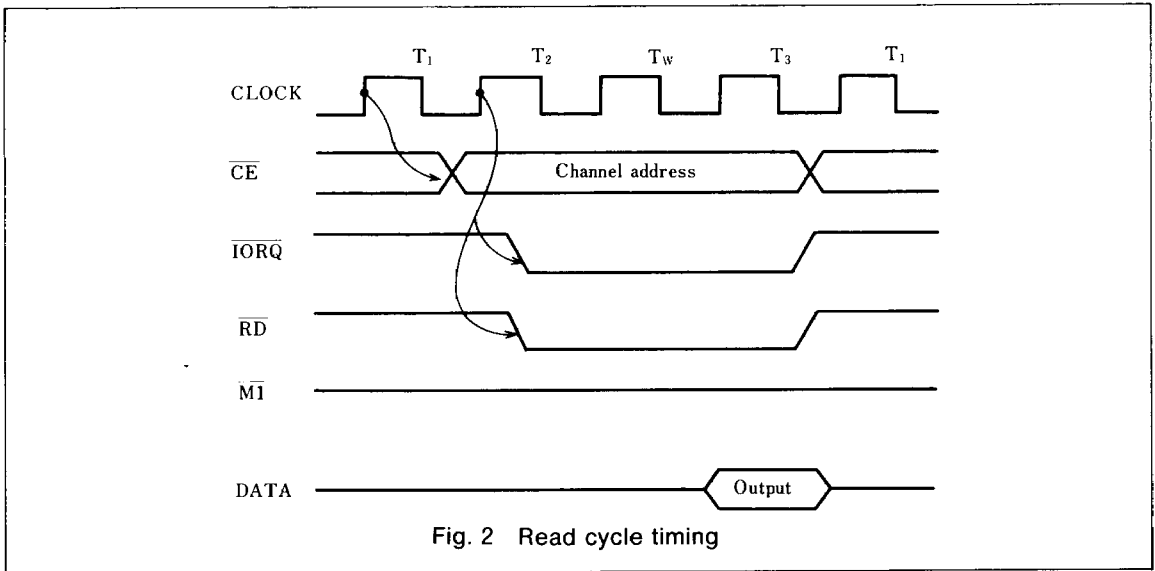
(2) **Write cycle**

Fig. 3 illustrates the timing and data signals gener-

ated by a Z-80 CPU output instruction to write a data or control byte into the SIO.

(3) **Interrupt cycle**

The interrupt-acknowledging and return-from-interrupt cycles are of the same timing as for other Z80 peripherals. (Refer to the Z80 PIO.)



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