THA9000

THA9000 Array Series

Description

The THA9000 series is an HCMOS semicustom technology offering speed equivalent to 10K ECL and high gate density ASICs. The THA9000 series is processed using 1.5-micron drawn gate length (1.1-micron effective channel length), 2-layer metal HCMOS technology, in which potentially active transistors fill the array core. Arrays ranging from 1,968 to 34,944 available gates are offered. The largest micro array has up to 174 available signal I/Os. The THA9000 series uses small device structures which exhibit low power consumption. The series is well suited to be used as a high reliability universal logic design vehicle, able to integrate entire printed circuit boards into a single array.

The larger arrays can be used for VLSI implementation of high performance subsystem architectures such as intelligent special purpose processors or multi-function controllers. The smaller members can be used for replacement of high speed Schottky TTL or 10K ECL logic. Midrange arrays are ideal for high performance dedicated peripheral controllers, intelligent support functions, etc. A large library of macrocells, macrofunctions, megafunctions, metal-megacells, RAMs and ROMs is available to simplify the conversion of existing logic designs or to easily produce new circuit designs.

Features

- ❑ 1.5-micron silicon gate length, 2-layer metal HCMOS technology
- ❑ Gate speed equivalent to 10K ECL; faster than 74S TTL; 0.57 ns through 2-input NAND gate, standard load = 2, VDD = 5 V, T_A = 25°C
- ❑ Up to 174 signal I/O capability
- ❑ Extensive macrocell, macrofunction, megafunction, metal-megacell and memory library
- ❑ Ten array sizes from 1,968 to 34,944 gates
- ❑ Fully supported by MDE® (Modular Design Environment) software for verification, simulation and layout
- ❑ Channel-Free architecture for maximum layout flexibility
- ❑ Random routing with hierarchical function placement
- ❑ Configurable output drive up to 12 mA with slew rate control
- ❑ Over voltage and latch-up protection for I/Os
- ❑ TTL/CMOS I/O compatibility
- ❑ Efficient implementation of large logic blocks
- ❑ Extensive selection of ceramic and plastic packages
- ❑ ESD protection according to MIL-STD
- ❑ Full military capability

Product Outline

Device Number	Estimated Gate Capacity [1]	Gate Complexity	Total Pads	Min Power Pads [2]		Max I/O Pads [3]
				VDD	VSS	
THA9020	1,000	1,968	44	1	2	41
THA9033	1,600	3,286	58	1	2	55
THA9050	2,500	4,992	70	1	2	67
THA9072	3,500	7,238	86	2	4	80
THA9095	4,600	9,504	98	2	4	92
THA9141	6,600	14,124	118	2	6	110
THA9190	8,700	19,000	138	2	6	130
THA9239	10,800	23,908	154	4	6	144
THA9284	12,500	28,388	168	4	6	158
THA9350	15,000	34,944	186	4	8	174

Notes:
1. Gates used will vary by design.
2. Minimum power pads required to be bonded to package pins.
3. I/O pads may be configured as VDD/VSS, subject to number and drive of output buffers.