CMOS LOW VOLTAGE GATE ARRAY

■ DESCRIPTION

The SLA100L Series is a low voltage CMOS gate array with maximum gate counts to 6,400 useable gates and I/O to 178 pads. The series is offered in 6 array sizes. It is produced on the low threshold process, which enables this series to operate from a single 1.5V or 3V battery. The MSI library of the SLA100L Series is upwardly compatible from that of the SLA6000, SLA7000 and SLA8000 Series.

■ FEATURES

- High performance with low power dissipation
- 2.0 micron drawn (1.7 micron effective) channel length CMOS, 2 layer metalization
- Low 0.9V (min) operating voltage
- Output drive:
  - –4 mA for a single output at 5.0 volts
  - –8 mA for parallel output at 5.0 volts
- CMOS level I/O
- Ideal for portable equipment
- Low power consumption
- High speed: tpd (2–input NAND)

Voltage(V)	1.5 Standard	3.0 Standard
Internal gate (ns)	8.5	3.0
Input buffer (ns)	12.0	4.0
Output buffer (ns) C_L = 15PF	40.0	14.0

■ PRODUCT CONFIGURATION

Array Member	Raw	Useable Gates		Total
SLA100X	Gates	Min	Max	# of Pads
SLA116L	1632	1061	1305	78
SLA122L	2232	1451	1785	90
SLA134L	3432	2231	2745	112
SLA149L	4900	3185	3920	136
SLA162L	6210	4036	4968	158
SLA180L	8000	5200	6400	178

NOTE: All arrays have 8 power / GND pads included within total pad count.

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
DC Supply voltage	V_{DD}	Vss -0.5 to 7.0	V
Input voltage	V_{IN}	Vss -0.5 to V_{DD} + 0.5	V
Output voltage	V_{OUT}	Vss -0.5 to V_{DD} + 0.5	V
Storage temperature	T_{stg}	-65 to +150	°C

■ RECOMMENDED OPERATING CONDITIONS

(Vss=0V, Ta = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage	V_{IN}	Vss		V_{DD}	V
DC Supply Voltage	V_{DD}	0.9		6.00	V
Operating Temperature	Topr	-20		85	°C

■ DC CHARACTERISTICS (Under Recommended Operating Conditions)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Low level input voltage						
1.5V	V_{IL}				0.4	V
3.0V					1.0	V
High level input voltage						
1.5V	V_{IH}		1.1			V
3.0V			2.0			V
Low level input current	I_{IL}	V_{IN} = Vss No pull-up			2.00	nA
High level input current	I_{IH}	V_{IN} = V_{DD} No pull-up			2.00	nA
Low level output voltage						
1.5V	V_{OL}	I_{OL} = 0.7 mA			0.2V	V
3.0V		I_{OL} = 1.7 mA			0.3V	V
High level output voltage						
1.5V	V_{OH}	I_{OH} = 0.23 mA	V_{DD} -0.2V			V
3.0V		I_{OH} = 0.6 mA	V_{DD} -0.3V			V
Pull-up and pull-down		1.5V		950		KΩ
resistor		3.0V		320		
Tri-state leakage current	I_{OZ}				10	µA
Input capacitance	C_{IN}			4		pF
Output capacitance	C_{OUT}			6		pF
Bi-directional pad capacitance	C_{BID}			10		pF
Static Current						
@ 1.5V Supply	I_{DDS}	V_{IN} = V_{DD} or Vss No output loads			2	µA
@ 3.0V Supply					2	

■ PACKAGE MATRIX

Package Type	No. of Pins	Device code	116L	122L	134L	149L	162L	180L
		No. of Pads	78	90	112	136	158	178
		No. of Gates	1632	2232	3432	4900	6210	8000
Plastic DIP	18	C18						
	24	C24	A*					
	28	C28	A*	A*				
	40	C40	A*	A*	A*			
	42	C42	A*	A*				
Plastic Shrink DIP	64	S64	A*	A*	A*			
Plastic QFP	44	F44-4	L	A	LQ	LQ		
	44	F44-6	A*	A*	A*	LQ	LQ	
	48	F48-12	A					
	52	F52-6	A*	A	L	LQ	LQ	
	60	F60-5	A*	Q	Q*	Q*	Q	
	60	F60-6	A	A*	A	A		
	64	F60-5	A					
	64	F60-6	A		A*	LQ	LQ	
	64	F64-13	A	A	A			
	80	F80-5	A*	A*	A*	A*	A*	
	80	F80-14	A	A	A	A	A	
	100	F100-5	A*	A*	A*	A*	A*	
	100	F100-15		A	A	A	A	
	120	F120-8			A*	A*	A*	L
	128	F128-5			A	A	A	
	128	F128-8			A*	A*	A*	A*
	144	F144-8				A*	A*	A*
	160	F160-8				A*	A*	A*
	196	F196-9						A
	208	F208-8						A
Plastic SOP	24	SOP1	A					
	24	SOP2	A	LQ				
	28	SOP2	A*	L				
Plastic PGA	89	G89				A		
	132	G132						
	176	G176						A*
PLCC	44	J44	A					
	68	J68	A*	A*	A*	A*	A*	
	84	J84	A	A*	A*	A*	A*	
Ceramic PGA	64	P64	A					
	72	P72			A*	A*		
	132	P132		A*	A*	A*		
	255	F256						

A: Available
*: Pin-Pad table exist
L: Need Lead frame development (2.5 months for new lead frame development)
Q: Need Qualification (reliability test) (2.5 months for reliability test)
LQ: Need Lead frame and Qualification (reliability test)(2.5 months for new lead frame development and/or 2.5 months for reliability test)

■ MACRO LIBRARY

Function	Cell Name	Gates
SIMPLE GATES		
2–INPUT NAND GATE	NA2	1
3–INPUT NAND GATE	NA3	2
4–INPUT NAND GATE	NA4	2
2–INPUT NOR GATE	NO2	1
3–INPUT NOR GATE	NO3	2
4–INPUT NOR GATE	NO4	2
3–INPUT AND GATE	A3	2
6-INPUT AND GATE	A6	4
8-INPUT AND GATE	A8	5
3–INPUT OR GATE	O3	2
6–INPUT OR GATE	O6	4
8–INPUT OR GATE	O8	5
EXCLUSIVE OR GATE	EXO	3
EXCLUSIVE NOR GATE	EXN	3
COMPLEX GATES		
2–AND 2–WIDE 3–INPUT NOR GATE	AN23	2
3–AND 2–WIDE 4–INPUT NOR GATE	AN14	2
2–AND 2–WIDE 4–INPUT NOR GATE	AN24	2
2–AND 3–WIDE 4–INPUT NOR GATE	AN34	2
2–AND 3–WIDE 6–INPUT NOR GATE	AN36	5
2–AND 2–WIDE 3–INPUT OR GATE	AO23	2
3–AND 2–WIDE 6–INPUT OR GATE	AO26	4
4–AND 2–WIDE 8–INPUT OR GATE	AO28	5
2–OR 2–WIDE 3–INPUT NAND GATE	ON23	2
3–OR 2–WIDE 4–INPUT NAND GATE	ON14	2
2–OR 2–WIDE 4–INPUT NAND GATE	ON24	2
2–OR 3–WIDE 4–INPUT NAND GATE	ON34	2
2–AND 2–OR 2–WIDE 4–INPUT NAND GATE	ON44	2
2–OR 3–WIDE 6-INPUT NAND GATE	ON36	5
2–OR 2–WIDE 3-INPUT AND GATE	OA23	2
INVERTERS/BUFFERS		
NORMAL INVERTER	IN1	1
POWER INVERTER	IN2	1
POWER INVERTER	IN4	2
NORMAL BUFFER	BUF1	1
FLIP-FLOPS		
LATCH	LF	4
LATCH WITH RESET	LFR	5
LATCH WITH SET	LFP	5
D–FF	DF	6
D–FF WITH RESET	DFR	7
D–FF WITH SET	DFS	7
D–FF WITH SET AND RESET	DFSR	8
JK–FF WITH RESET	JKR	10
JK–FF WITH SET AND RESET	JKSR	11
ADDERS		
1–BIT FULL ADDER	T183	9
COMPARATORS		
4–BIT MAGNITUDE COMPARATOR	T085	39
8–BIT MAGNITUDE COMPARATOR	T688	26
COUNTERS		
SYNCHRONOUS 4–BIT BINARY UP COUNTER WITH RESET, LOAD AND ENABLE	A161	57
SYNCHRONOUS 4–BIT BINARY UP COUNTER WITH RESET AND LOAD	T161E	51
SYNCHRONOUS 2–BIT BINARY UP COUNTER WITH RESET, LOAD AND ENABLE	A161H	29

■ **MACRO LIBRARY (cont.)**

Function	Cell Name	Gates
COUNTERS (cont.)		
SYNCHRONOUS 4–BIT BINARY UP COUNTER WITH RESET AND ENABLE	A161L	46
SYNCHRONOUS 4–BIT BINARY UP COUNTER WITH RESET	A161LE	37
SYNCHRONOUS 4–BIT BINARY UP COUNTER WITH LOAD AND ENABLE	A161E	52
SYNCHRONOUS 4–BIT BINARY UP COUNTER WITH LOAD	T161RE	46
FULLY SYNCHRONOUS 4–BIT BINARY UP COUNTER WITH RESET, LOAD AND ENABLE	A163	54
FULLY SYNCHRONOUS 4–BIT BINARY UP COUNTER WITH RESET AND LOAD	A163E	48
PRESETABLE 4–BIT BINARY UP COUNTER/LATCH WITH RESET AND LOAD	T177	39
PRESETABLE 2–BIT BINARY UP COUNTER/LATCH WITH RESET AND LOAD	T177H	21
PRESETABLE 4–BIT BINARY UP COUNTER/LATCH WITH LOAD	T177R	38
PRESETABLE 4–BIT BINARY UP COUNTER/LATCH WITH SET AND LOAD	T177V	39
PRESETABLE 2–BIT BINARY UP COUNTER/LATCH WITH SET AND LOAD	T177HV	20
SYNCHRONOUS 4–BIT UP/DOWN COUNTER WITH LOAD AND ENABLE	A191	70
SYNCHRONOUS 4–BIT UP/DOWN COUNTER WITH RESET	A191CE	47
SYNCHRONOUS 4–BIT UP/DOWN COUNTER WITH LOAD	A191E	63
SYNCHRONOUS 2–BIT UP/DOWN COUNTER WITH LOAD AND ENABLE	A191H	35
SYNCHRONOUS 4–BIT UP/DOWN COUNTER WITH RESET	A191LE	51
SYNCHRONOUS 4–BIT DUAL CLOCK BINARY UP/DOWN COUNTER WITH RESET AND LOAD	A193	69
SYNCHRONOUS 4–BIT DUAL CLOCK BINARY UP/DOWN COUNTER WITH RESET	A193L	53
SYNCHRONOUS 2–BIT DUAL CLOCK BINARY UP/DOWN COUNTER WITH RESET AND LOAD	A193H	36
SYNCHRONOUS 2–BIT DUAL CLOCK BINARY UP/DOWN COUNTER WITH RESET	A193HR	27
DECADE COUNTER WITH RESET	A390	32
4–BIT BINARY UP COUNTER WITH RESET	T393	25
4–BIT BINARY DOWN COUNTER WITH RESET	T393V	25
DECODER/DEMULTIPLEXERS		
BCD–TO–DECEMAL DECODER	T042	29
3–LINE TO 8–LINE DECODER/MULTIPLEXER WITH ENABLE G	A138G2	18
2–LINE TO 4–LINE DECODER/MULTIPLEXER WITH ENABLE G	A139	9
2–LINE TO 4–LINE DECODER/MULTIPLEXER	A139G	6
DFFS/LATCHES		
4–BIT LATCH WITH RESET	T116	17
QUADRUPLE DFF WITH RESET	T175	27
QUADRUPLE DFF WITH Q, XQ, WITHOUT RESET	T175R	22
QUADRUPLE DFF WITH Q ONLY	T175RX	22
OCTAL DFF WITH RESET	T175W	54
OCTAL DFF	T175WR	44
OCTAL D–TYPE TRANSPARENT LATCH WITH ENABLE	T373T	26
SELECTORS/MULTIPLEXERS		
4–LINE TO 1–LINE DATA SELECTOR/MULTIPLEXER WITH STROBE G	T153	12
4–LINE TO 1–LINE DATA SELECTOR/MULTIPLEXER	T153G	10
QUADRUPLE 2–LINE TO 1–LINE DATA SELECTOR/MULTIPLEXER WITH STROBE G	T157	13
QUADRUPLE 2–LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER	T157G	11
OCTAL 2–LINE TO 1–LINE DATA SELECTOR/MULTIPLEXER WITH STROBE G	T157W	26
OCTAL 2–LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER	T157WG	21
SHIFT REGISTERS		
8–BIT PARALLEL–OUT SERIAL SHIFT REGISTER WITH RESET	T164	55
8–BIT SHIFT REGISTER WITH RESET, LOAD AND ENABLE	T166	65
4–BIT SHIFT REGISTER WITH RESET, LOAD AND ENABLE	T166H	34

■ PROPAGATION DELAYS OF SELECTED MACROS

BEST CASE	WORST CASE
Temperature = 0°C Ambient	Temperature = 70°C Ambient
Supply Voltage = 1.65V	Supply Voltage = 1.35V
Process = Best case	Process = Worst Case

Name	Function	From	To	Best Case		Worst Case		Loads
				tplh	tphl	tplh	tphl	
NA2	2-Input NAND	In	Out	1.0	0.9	4.8	4.6	0
				1.5	1.42	7.18	7.09	1
				2.0	1.94	9.56	9.58	2
NO2	2-Input NOR	In	Out	1.8	0.7	8.8	3.5	0
				2.79	1.03	13.54	5.07	1
				3.78	1.36	18.28	6.64	2
IN1	1 X Inverter	In	Out	0.8	0.5	4.2	2.7	0
				1.3	0.83	6.58	4.27	1
				1.8	1.16	8.96	5.84	2
IN4	4 X Inverter	In	Out	0.5	0.3	2.4	1.8	0
				0.69	0.46	3.32	2.59	1
				0.88	0.62	4.24	3.38	2
DF	D Flip-Flop	CLK	Q	6.4	7.7	30.9	36.9	0
				6.9	8.03	33.28	38.47	1
				7.4	8.36	35.66	40.04	2
1KB	Input Clock Buffer	In	Out	6.2	5.7	29.5	27.1	0
				7.5	6.6	35.9	31.7	10
				8.8	7.5	42.3	36.3	20
OB1	2mA Output Driver	In	PAD	23.25	20.11	110.42	95.56	10pF
				53.05	29.01	251.7	200.2	50pF
				90.3	69.7	428.3	331.0	100pF
OB3	6mA Output Driver	In	PAD	14.56	15.63	69.22	74.63	10pF
				22.8	22.95	108.5	109.55	50pF
				33.1	32.1	157.6	153.2	100pF

- **Workstation Support**

  Schematic capture and functional simulation are supported on Daisy, Mentor, Valid and Intergraph workstations. In addition, our proprietary LADS software, used with OrCAD, CAD/CAM or FutureNet, is available for IBM PCs and compatibles, VAXs, Suns and other platforms.

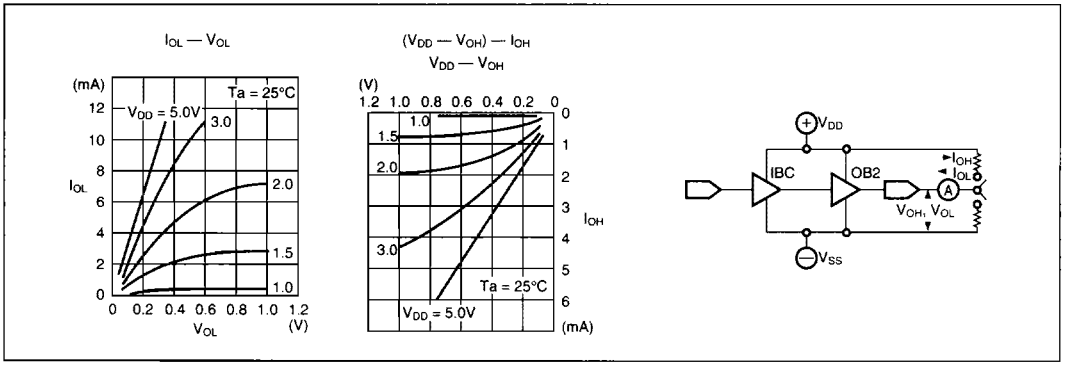
  LADS includes logic simulation and timing verification up to 6,000 gates using PCs with 640K of memory or up to 20,000 gates using 386 PCs equipped with 4 megabytes of memory.

- **Megacells**

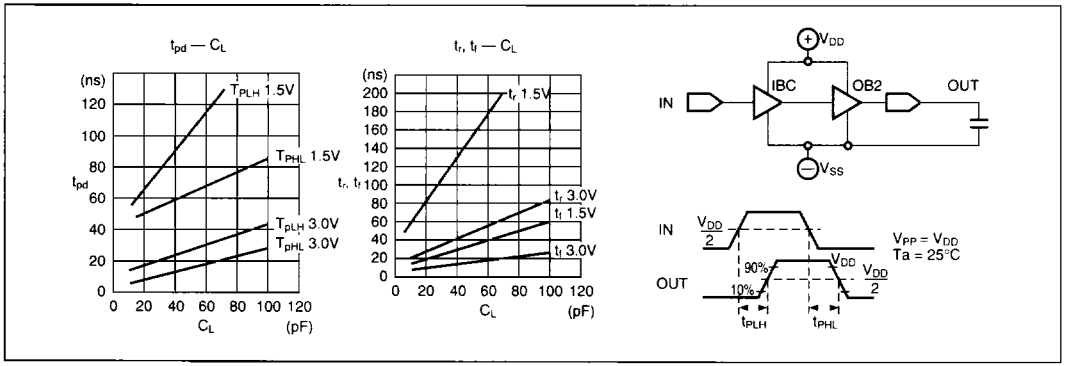
  Due to the design of the SLA100L Series, fully routed and characterized megacells can be implemented effectively along side of random logic. Megacells currently under development include microprocessors, peripheral interface devices and controllers.

■ PERFORMANCE CURVES

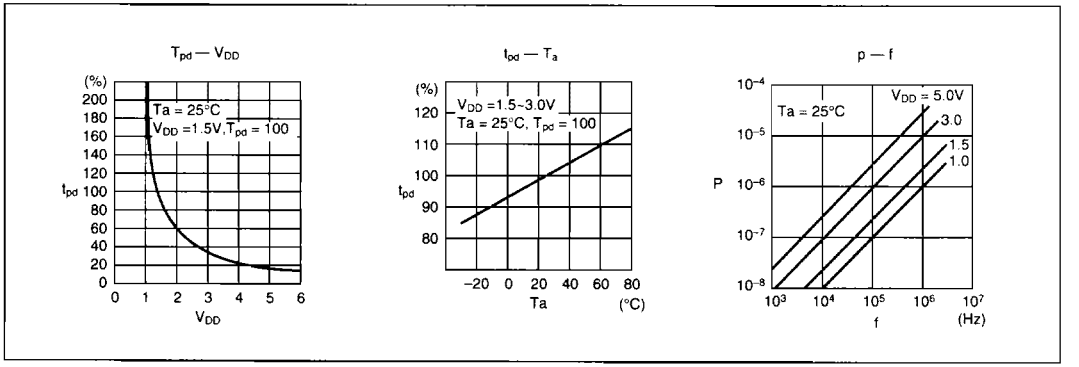
● Output Current (Bipolar Output)



● t_{pd}, t_r, t_s–C_L (Bipolar Output)



● Delay Time, Power Consumption



● Process Technology

The SLA100L Series is fabricated on our highly automated 5" fabrication line located in Fujimi, Japan. The process is similar to that used for our high–volume SLQ Watch which has been in production since 1984.

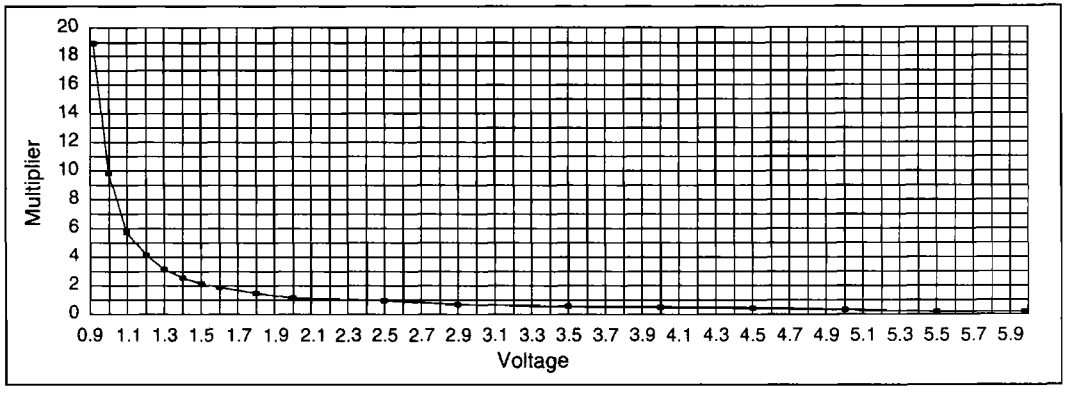
N–Channel length is 2.0 micron drawn (1.7 micron effective) and P–channel length is 2.0 micron drawn (1.7 micron effective).

- **Propagation Delay Times**

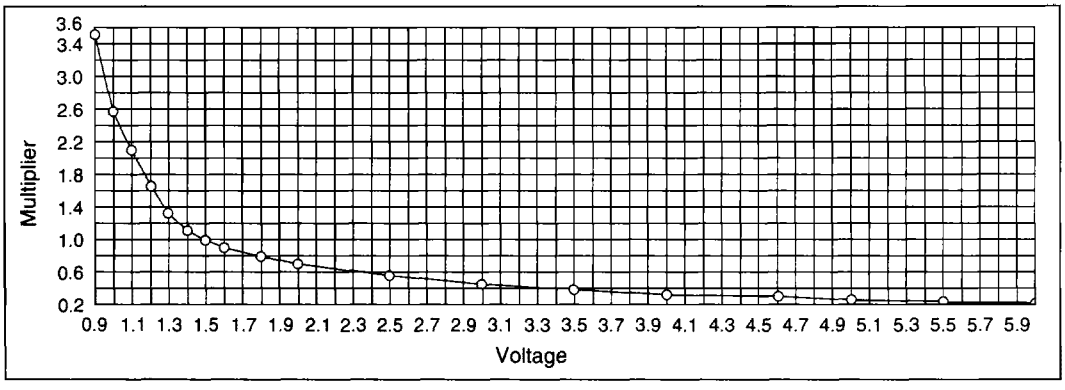
The propagation delay values printed in our cell libraries and used in simulation are derived from actual measurements of silicon, not spice simulations. The measured coefficient parameters for the CMOS macrocells are: For the SLA100L Series, the typical TO and K values (t_{pd} = T0 + nk) with V_{DD} = 1.5V which is found in the SLA100L Series data book, must be multiplied by the delay multiplier from the following curves:

■ DELAY MULTIPLIER

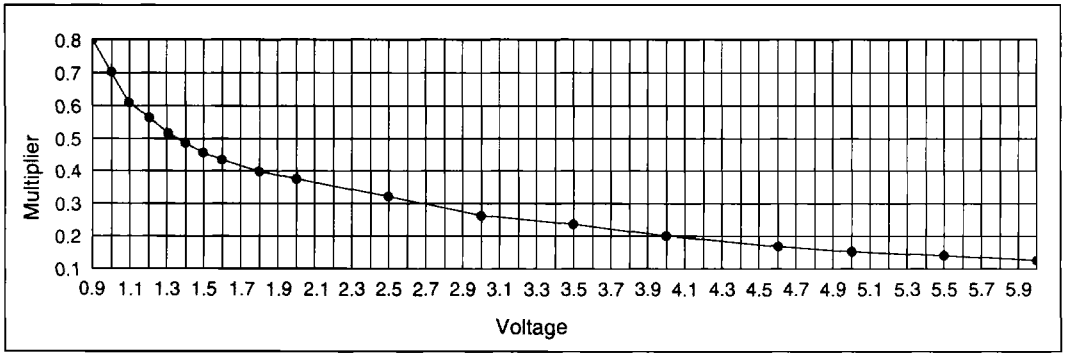
- **Maximum Voltage Factors**



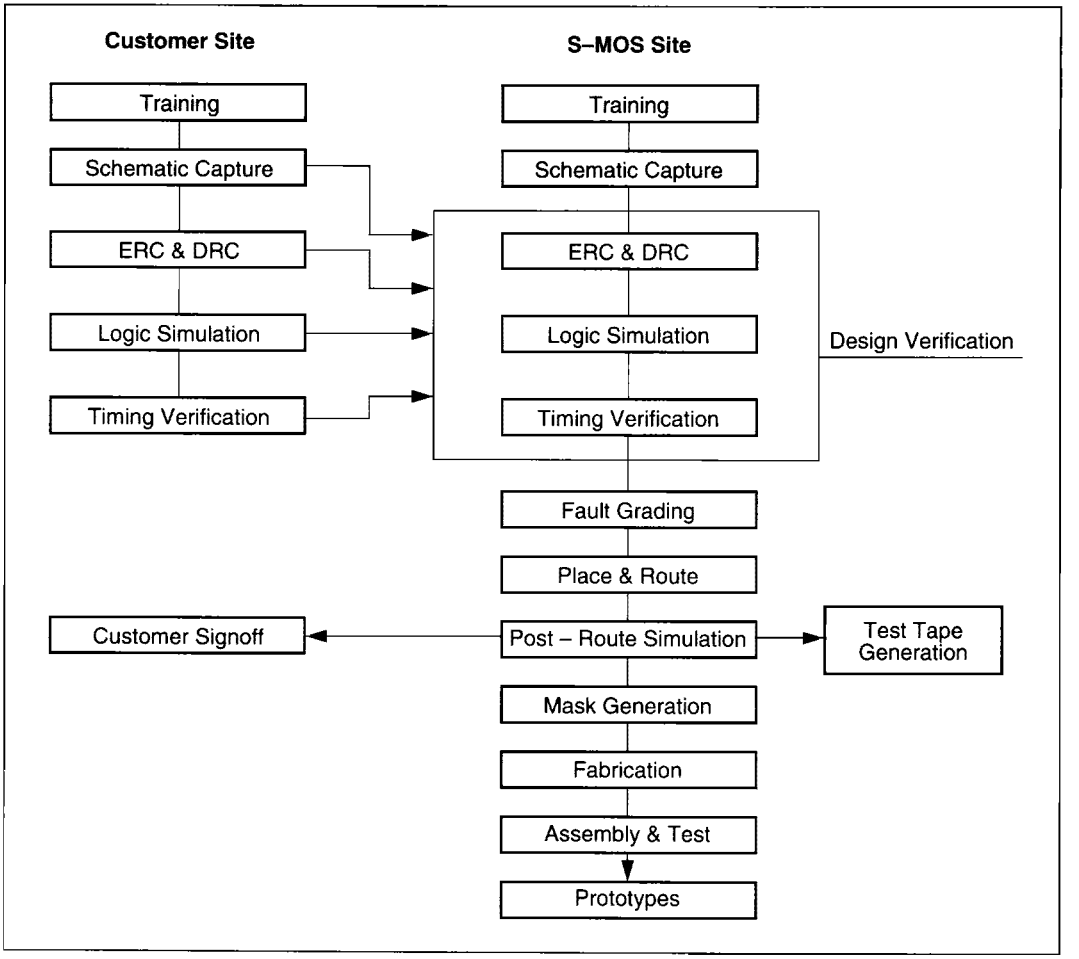
- **Typical Voltage Factors**



- **Minimum Voltage Factors**



S–MOS SYSTEMS ASIC DESIGN FLOW



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