Signetics

SG3526
Switched-Mode Power Supply Control Circuit

Product Specification

Linear Products

DESCRIPTION

Specifically designed for use in fixed-frequency switching regulators and other power control applications, this Switched-Mode Power Supply Control Circuit can be used to implement single-ended or push-pull switching regulators of either polarity, both transformerless and transformer-coupled.

Included in this monolithic integrated circuit is a temperature-compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and steering logic, and two 200mA source/sink power drivers. Also included are housekeeping functions such as soft-start and low supply voltage lockout, digital current limiting, double-pulse inhibit, a data latch for single-pulse metering, adjustable dead time, and provision for symmetry correction inputs.

The output cirtcuit has been redesigned to eliminate the current spiking problem associated with source/sink drivers. The output stage has been designed so that in the transition from source-to-sink, or sink-to-source, the conducting device is shut off one transistor delay before the other device is turned on. This output correction allows the designer to utilize the speed of the other features of this controller at system frequencies up to 400kHz.

For ease of interface, all digital inputs are TTL and CMOS compatible. Active LOW logic allows wired-OR connections for maximum flexibility.

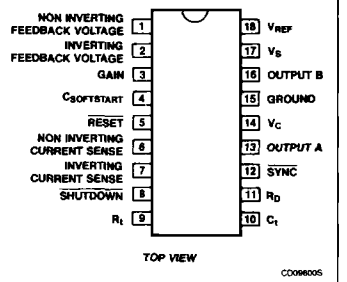
The low-cost SG3526 is rated for continuous operation over the junction temperature range of 0°C to +125°C. It is furnished in either the Cerdip package or a dual in-line plastic package with copper alloy lead frame for improved heat dissipation.

FEATURES

- **7.4 to 35V operation**
- **Dual 200mA source/sink outputs**
- **Cycle-by-cycle operation of all features up to 400kHz**
- **No current spikes on V_C line at source-to-sink or sink-to-source transitions**
- **Stabilized power supply**
- **Current limiting**
- **Temperature-compensated reference source**
- **Sawtooth generator**
- **Low supply voltage protection**
- **External synchronization**
- **Double-pulse suppression**
- **Programmable dead time**
- **Programmable soft start**
- **18-pin dual in-line plastic package, 18-pin Cerdip hermetic package, or 20-pin plastic SO**

PIN CONFIGURATIONS

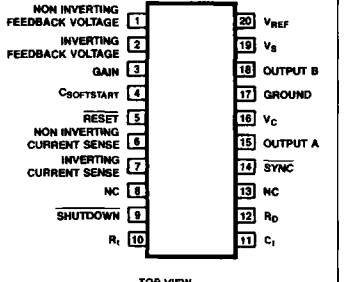
F, N Packages



TOP VIEW

CD09600S

D Package[1]



TOP VIEW

CD09590S

NOTE:
1. SOL and non-standard pinout.

ORDERING CODE

DESCRIPTION	AMBIENT TEMPERATURE	ORDER CODE
20-pin Plastic SOL DIP	0 to +70°C	SG3526D
18-pin Cerdip	0 to +70°C	SG3526F
18-pin Plastic DIP	0 to +70°C	SG3526N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage	40	V
V_C	Collector supply voltage	40	V
V_{IN}	Logic input voltage range, Pins 5, 8, 12	−0.3 to +5.5	V
V_{IN}	Analog input voltage range, Pins 1, 2, 6, 7	−0.3V to V_S	V
I_O	Output current	±250	mA
I_{REF}	Reference load current	50	mA
I_{IN}	Logic sink current	15	mA
P_D	Package power dissipation (Plastic DIP)[2] (SO), (Cerdip)[2]	1.9 1.4	W[1] W[1]
T_S	Storage temperature range	−65 to +150	°C

NOTES:
1. Maximum junction temperature, T_{JMAX} = 150°C. Rating is for T_A = 25°C.
2. Plastic θ_{JA} = 66°C/W; Cerdip θ_{JA} = 88°C/W; SO θ_{JA} = 85°C/W.

BLOCK DIAGRAM

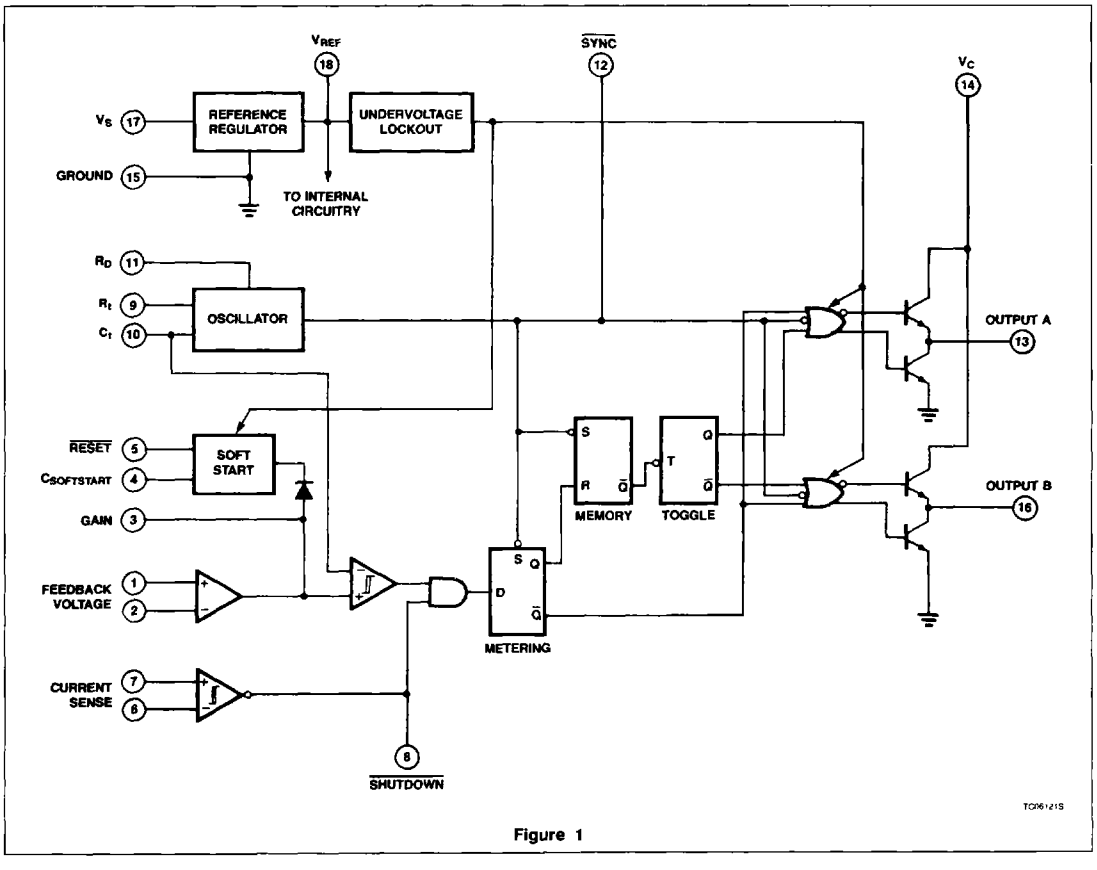


Figure 1

DC ELECTRICAL CHARACTERISTICS All specs over operating junction temperature range, V_S = 15V, unless otherwise noted.

SYMBOL	CHARACTERISTICS	TEST PINS	TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
Reference, Pin 18							
V_{REF}	Reference voltage	18	T_J = +25°C		5.00		V
	Temperature stability	18			0.2	0.4	mV/°C
	Total output variation	18	7.4V < V_S < 35V, 0 < I_L < 10mA	4.85	5.00	5.15	V
	Line regulation	18	7.4V < V_S < 35V, I_L = 0mA		0.6	2	mV/V
	Load regulation	18	0mA < I_L < 10mA		0.4	2.5	mV/mA
	Short circuit current	18	V_{REF} = 0V	−25	−75	−125	mA
	Output noise voltage	18	10Hz ≤ f ≤ 80kHz		100		μV_{RMS}
Low supply shutdown, Internal and Pin 5							
	Comparator threshold voltage			3.8	4.2	4.8	V
	Hysteresis				0.2		V
	Reset voltage out	5	When shutdown for LOW V_S		0.2	0.4	V
	Reset voltage out	5	When not shutdown	2.4	4.8		V
	Reset sink current	5	When shutdown, V_{IL} = 0.4V		−190	−360	μA
	Reset source current	5	When not shutdown, V_{IH} = 2.4V		−110	−200	μA
Oscillator, Pins 9, 10, 11 and SYNC, Pin 12[1]							
	Minimum frequency range	9, 10, 11 & 12	R_T = 150k, C_T = 20μF, R_D = 0Ω			1.0	Hz
	Maximum frequency range		R_T = 2k, C_T = 300pF, R_D = 0Ω, T_J = 125°C	400			kHz
	Initial accuracy	9, 10	R_T = 4.12k, C_T = 0.01μF, R_D = 0Ω, T_J = 25°C	36.8	40	43.2	kHz
V_{COSC}	Voltage stability[2]	9, 10	7.4V < V_S < 35V		0.02	0.04	%/V
T_{COSC}	*Temperature stability*[2]	9, 10			0.04	0.06	%/°C
	Sawtooth peak voltage	10	V_S = 35V	2.0	3.0	3.5	V
	Sawtooth valley voltage	10	V_S = 7.4V	0.5	1.0	1.5	V
	Sync. in HIGH level	12	I_{SOURCE} = 40μA	2.4	4.0		V
	Sync. in LOW level	12	I_{SINK} = 3.6mA		0.2	0.4	V
	Sync. in bias current, HIGH	12	V_{IH} = 2.4V		−105	−200	μA
	Sync. in bias current, LOW	12	V_{IL} = 0.4V		−180	−360	μA
	Min sync. in pulse width to *trigger*	12		200	150		ns

DC ELECTRICAL CHARACTERISTICS (Continued) All specs over operating junction temperature range, V_S = 15V, unless otherwise noted.

SYMBOL	CHARACTERISTICS	TEST PINS	TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
Error amp, Pins 1, 2 and 3[3]							
V_{OS}	Input offset voltage	1, 2			2.0	10	mV
I_B	Input bias current	1, 2			210	1000	nA
I_{OS}	Input offset current	1, 2			5	200	nA
A_{VOL}	DC open-loop gain	1, 2, 3		60	68		dB
V_{OH}	High output voltage	3	I_{SOURCE} = 100μA	3.6	4.2		V
V_{OL}	Low output voltage	3	I_{SINK} = 100μA		0.11	0.4	V
CMRR	Common-mode rejection ratio	1, 2, 3	R_S = 2k	70	110		dB
PSRR	Power supply rejection ratio	1, 2, 3	V_S = 10V to 20 V	90	110		dB
	Small-signal bandwidth	1, 2, 3			1.0		MHz
	Feedback resistor range	2, 3		50		1000	kΩ
	Output sink current	3		70	100		μA
	Output source current	3		70	100		μA
PWM comparator, internal and Pin 3[1]							
	Minimum duty cycle		V_{COMP} = 0.4V			0	%
	Maximum duty cycle		V_{COMP} = 3.6V	45	49		%
	Dead time accuracy		R_T = 4.12k, C_T = 0.01μF, R_D = 0Ω		1.5		μs
	Prop. delay, PWM comp to output				250		ns
	Bias current, duty cycle control	3			1		μA
Soft-start, Pins 4 and 5							
	Soft-start trip voltage	4	V_{RESET} = 0.4V		22	50	mV
	Soft-start charge current	4	V_{RESET} = 2.4V	-180	-120	-85	μA
V_{LOW}	Reset voltage, OFF	5	I_{SINK} = 3.6mA		0.2	0.4	V
V_{HIGH}	Reset voltage, ON	5	I_{SOURCE} = 40μA	2.4	4.0		V
	Reset bias current, HIGH	5	V_{IN} = 2.4V		-110	-200	μA
	Reset bias current, LOW	5	V_{IN} = 0.4V		-200	-360	μA
Remote ON/OFF (shutdown), Pin 8							
	Off (LOW)	8	I_{SINK} = 3.6mA		0.2	0.4	V
	On (HIGH)	8	I_{SOURCE} = 40μA	2.4	4.0		V
	Input current, shutdown HIGH	8	V_{IN} = 2.4V		-100	-200	μA
	Input current, shutdown LOW	8	V_{IN} = 0.4V		-190	-360	μA
	Delay to output(s)	8			400		ns
Current limit comparator, Pins 6 and 7							
	Common-mode range	6, 7	V_S = 18V	0		15	V
	Sense voltage for Min duty cycle	6, 7		70	100	140	mV
	Input bias current	6, 7	V_{CM} = 0V to 15V		-3	-20	μA
	Voltage gain	6, 7			68		dB
	Delay to outputs	6, 7	100mV overdrive		700		ns

8

DC ELECTRICAL CHARACTERISTICS (Continued) All specs over operating junction temperature range, V_S = 15V, unless otherwise noted.

SYMBOL	CHARACTERISTICS	TEST PINS	TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
Output stage, Pins 13, 14 and 16							
V_{OH}	High output voltage	13, 14, 16	I_{SOURCE} = 20mA, V_C = 15V	12.8	13.5		V
			I_{SOURCE} = 100mA, V_C = 15V	12.5	13.3		V
			I_{SOURCE} = 200mA, V_C = 15V	12.0	13.2		V
V_{OL}	Low output voltage	13, 14, 16	I_{SINK} = 20mA, V_C = 15V		0.15	0.3	V
			I_{SINK} = 100mA, V_C = 15V		1.25	1.8	V
			I_{SINK} = 200mA, V_C = 15V		2.20	3.00	V
	Output leakage	13, 14, 16	V_C = 40V		45	100	μA
	I_{SINK} Max	13, 14, 16	V_C = 15V	200	250		mA
	I_{SOURCE} Max	13, 14, 16	V_C = 15V	200	250		mA
t_R	Rise time	13, 14, 16	C_L = 1000pF, V_C = 15V		300		ns
			C_L = 0pF, V_C = 15V		50		ns
t_F	Fall time	13, 14, 16	C_L = 1000pF, V_C = 15V		200		ns
			C_L = 0pF, V_C = 15V		50		ns
Supply current[4]							
I_{CC}	Shutdown LOW	17	7.4V < V_S < 35V		24	30	mA
Operating frequency for cycle-by-cycle operation of all protect features							
	Maximum frequency			400	500		kHz

NOTES:
1. f_{OSC} = 40kHz (R_T = 4.12k, C_T = 0.01μF, R_D = 0Ω) unless otherwise noted.
2. Guaranteed by design.
3. V_{CM} = 0V to 5.2V.
4. R_T = 4.12kΩ.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_S	Logic supply voltage	7.4	35	V
V_C	Collector voltage	4.5	35	V
I_O	Output load current	0	±200	mA
I_L	Reference load current	0	10	mA
f_{OSC}	Oscillator frequency	1Hz	400	kHz
R_t	Oscillator timing resistance	2	150	kΩ
C_t	Oscillator timing capacitance	150pF	20	μF
DT	Programmed dead time	3	50	%
T_A	Ambient temperature range	0	+70	°C
T_J	Junction temperature range	0	+125	°C

THEORY OF OPERATION

Internal Reference

The internal reference is capable of maintaining 1% accuracy over the specified operating temperature range. The reference voltage is 5.00V at Pin 18. Short-circuit current is typically 50mA. The reference output remains stable within 30mV over an input range of 8 to 35V. Complete regulation characteristics versus line and load (see Figure 1) are listed in the Electrical Characteristics section of the data sheet. The maximum recommended load on the reference supply is 20mA.

THE RAMP OSCILLATOR

The ramp oscillitor is a self-sustained, fixed-frequency circuit with programmability provided by selecting the value of an external resistor and capacitor as shown in Figure 2. An internal current source is set by the resistor R_t to a certain value of charging current sufficient to generate a stable ramp over a range of 1Hz to 400kHz.

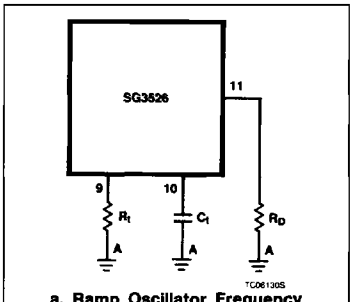
THE ERROR AMPLIFIER

The error amplifier is a transconductance-type with open-loop unity gain bandwidth of 1MHz. Typical source/sink current is 100μA. Open-loop DC gain is 68dB with a single dominant pole at 500Hz. (See Figure 3 for detailed response.) Compensation is achieved by simple 'C' (100pF) or RC network for lag-lead compensation. This network is placed in shunt to ground from Pin 3 (refer to Figure 4). Common-mode voltage is 5V for a standard positive supply and ground for negative supply.

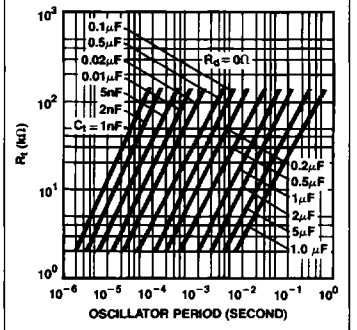
The Pulse Width Modulator

The pulse width modulator consists of a high-speed comparator with non-inverting input tied to the ramp generator and inverting input driven by the error amplifier output. (See Figure 5.) The resultant output forms a gated input to the metering flip-flop of which the '$\overline{Q}$' output feeds the 'R' input on the memory latch, and 'Q' output enables the main output gates (G2, G3). Alternate half-cycles are then enabled at the output (Pins 13 and 16) by the action of the toggle flip-flop. Initiation of the beginning of each half of the duty cycle is triggered by the start of the ramp, and termination occurs at the point in time where error output meets ramp voltage. It is with this sequence of control events that glitch-free output is guaranteed.

Pulse delay times in the PWM loop are specified in the data sheet. Maximum operating frequency must take such delay times into account in order to guarantee reliable functioning of the controller under a closed-loop condition. The Signetics SG3526 is rated at a typical maximum frequency of 500kHz.



a. Ramp Oscillator Frequency Determining Components and Dead Time Programming



b. Oscillator Period vs R_t and C_t

Figure 2

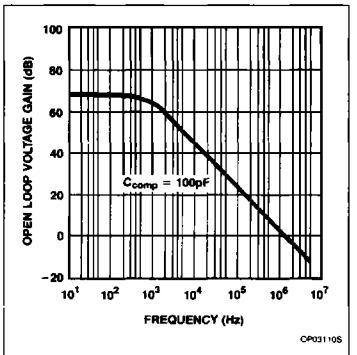


Figure 3. Error Amplifier Open-Loop Gain vs Frequency

PWM GAIN

The DC gain of the pulse width modulator is determined by the ratio of input voltage to the primary power switching circuit to the active ramp voltage differential. This is given as 3.6V and 0.4V with a differential of 3.2V.

Example:
The DC supply voltage to the power converter is 48V.

$$\text{Therefore, PWM Gain} = \frac{48}{3.2} = 15$$

(For further information on loop response calculations, please refer to references 1, 2.)

THE OUTPUT DRIVER STAGE

The output driver circuit has been carefully designed to prevent cross-conduction current spikes by eliminating any overlap conduction within the totem-pole structure. The source and sink capacity is rated at 200mA. In addition, supply voltage on the driver transistors is rated at 35V with no risk of destroying the IC due to excessive power dissipation. Note the output waveform in Figure 6 shows a full 10V drive level at the rated 200mA load current. This capability means that a Power MOS gate capacity of 4000pF can be driven with a voltage rise time of 0.2μs for a 10V output.

PROTECTIVE FUNCTIONS

Dead Time Control

The dead time control circuit, incorporated as an integral part of the ramp oscillator, is provided to allow the designer the ability to control the minimum off time between alternate half-cycles. (See Figures 7 and 8.) The value of R_D, as shown in the graph, allows the programming of this delay time from a minimum (Pin 11 grounded) of 1.5μs to a maximum of 9.7μs for a resistance of 22Ω tied from Pin 11 to ground (Figure 8b). Obviously, dead time in the oscillator must conform to the limitations imposed by the operating frequency.

Overcurrent Limit

The overcurrent limit function is an integral part of the PWM circuit and, as such, inputs on Pins 6 and 7 will control the cycle-by-cycle operation of the output stage on both halves of the duty cycle. The overcurrent comparator is specifically designed to propagate a high-speed shutdown signal to turn off the output metering flip-flop in the event of an overcurrent of predetermined magnitude. The overcurrent sense inputs must be treated with care in respect to lead length and shunt capacity in order to obtain the maximum speed of response. Some typical circuit configurations are shown in Figure 9a. Note that either Pin 6 or 7 may be used as threshold reference voltage anywhere within the common-mode voltage range of the comparator. As shown, a simple technique is to ground Pin 6 and to program Pin 7 high (≥ 100mV) for shutdown. Very little noise immunity is allow-

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Switched-Mode Power Supply Control Circuit SG3526

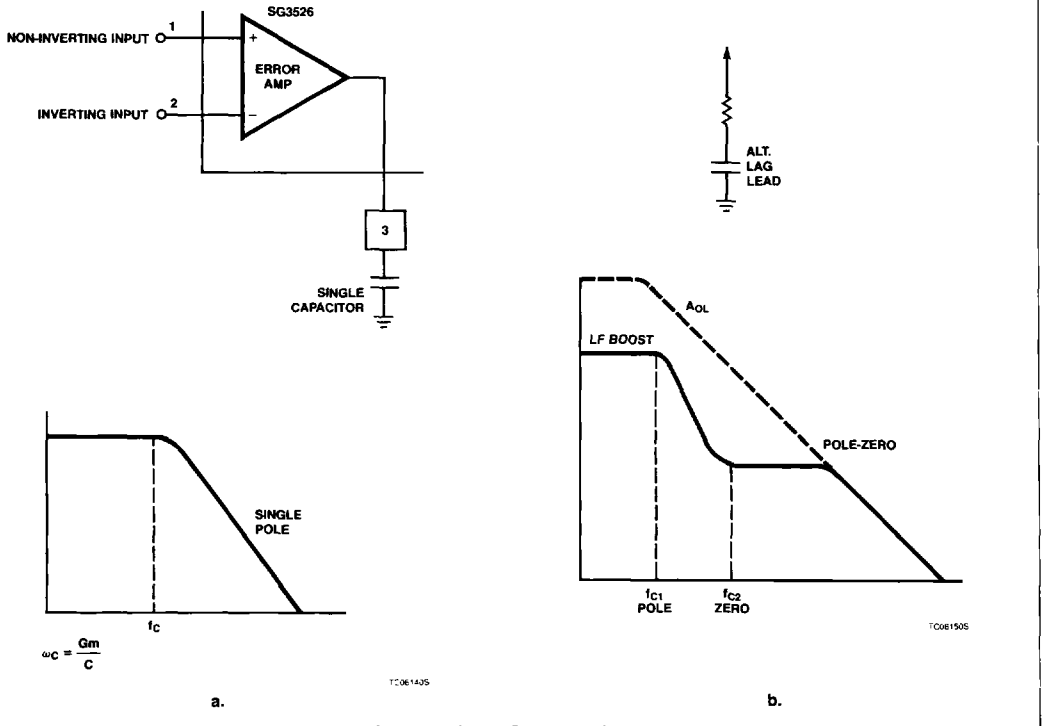

Figure 4. Loop Compensation

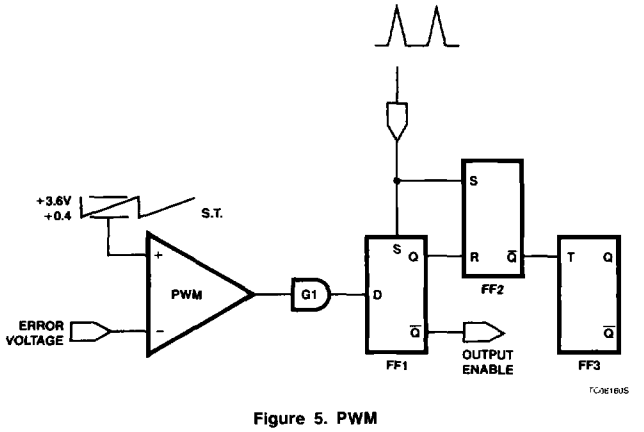

Figure 5. PWM

ed in this case. An improved method is to set Pin 6 at some positive voltage level (such as +2.5V) and thus provide an average noise threshold of 2.5V +100mV as shown in Figure 9b. This particular circuit provides a considerable improvement in noise immunity. Note that care must be taken in providing a low impedance reference at Pin 6. The overcurrent sense comparator provides a typical hysteresis of 20mV with a threshold of 100mV (Figure 9c). The typical delay time to deactivate the output drive is 700ns at T_J = 25°C rising to 1200ns at T_J = 125°C.

Soft-Start

This circuit provides a programmed ramp-up of the duty cycle at power-on, after remote shutdown (reset Pin 5) or low supply sense. A capacitor from Pin 4 to ground is charged towards the turn-on threshold by a 100μA source. Time constants for various values of capacitance are plotted for the designer's convenience as shown in Figure 10. The soft-start function is initiated by holding the reset below 0.2V which causes C to discharge. The Reset function, when low, also holds the error amplifier output low, initiating a minimum duty cycle at the output drivers. Low voltage shutdown occurs when V_S (Pin 17) drops below 4.0V.

External Synchronization

An external sync pulse may be injected into Pin 12 in order to provide synchronous operation of a switched-mode controller as shown in Figure 11. The required voltage level is active LOW with a threshold of 0.4V typical and a minimum pulse width of 150ns. A periodic signal at a rate approximately 10% higher than the free-running frequency of the ramp oscillator is required.

THERMAL CONSIDERATIONS

The power dissipation of the SG3526 must be considered in the design procedure in order to insure operation within the allowable device limits, particularly when maximum operating frequency is desired. The graph provided in Figure 12 will serve as a guide to staying within the device thermal limits in any design. Device dissipation is determined by summing all of the various current-voltage products, both pulsed and DC, noting the package type and the ambient operating temperature, then plotting this total device power on the respective derating graph.

UNDERVOLTAGE LOCKOUT

Should supply voltage in Pin 17 drop low enough to affect the internal reference regulator, an output inhibit circuit is activated. In addition, the voltage on Pin 5 (Reset) will be brought to a low state in order to signal remote sensing indicators. This characteristic is shown graphically in Figures 13a and b.

SYMMETRY CORRECTION

Should an external symmetry monitoring and correction circuit be required where drive unbalance may be critical, Pin 8, the shutdown function, is available to program either half of the output cycle off. This is accomplished by applying a TTL low signal with a pulse synchronized to the clock frequency. Keep in mind that the typical delay from Pin 8 is either output before shutdown is 400ns.

DOUBLE PULSE PROTECTION

The memory flip-flop must be reset by the PWM signal. This set-reset sequence provides insurance that alternate sync pulses initiate alternate A-B output cycle, preventing double pulses at the output.

CAUTION: Supply Decoupling —
Pin 17, the supply input to the internal regulator, should be decoupled from Pin 14 in order to prevent pulsed switching currents from interacting with outputs.

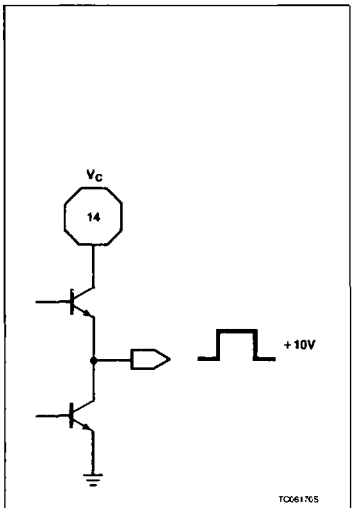

Figure 6. Output Stage

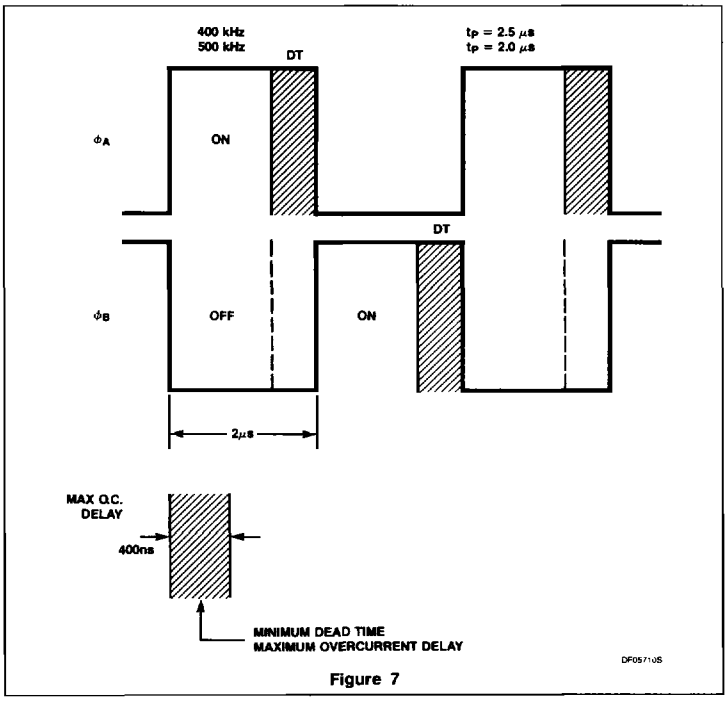

Figure 7

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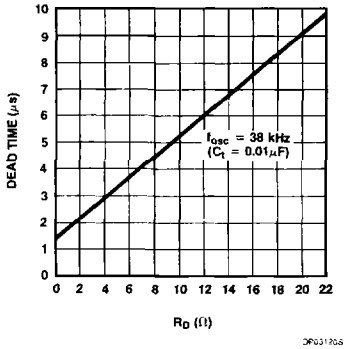
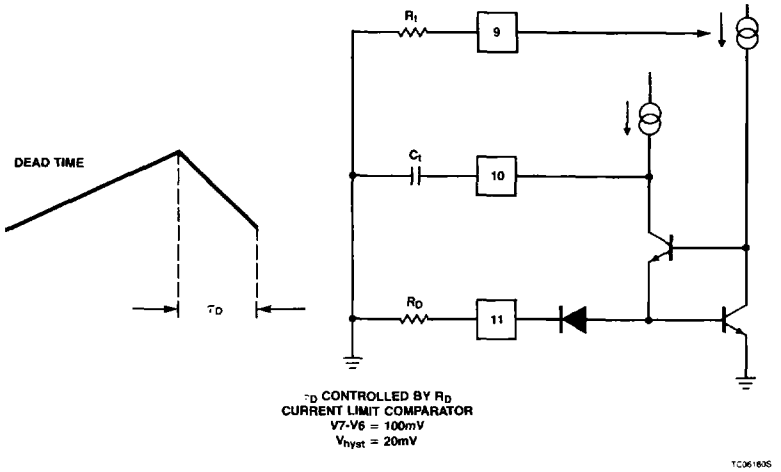
Switched-Mode Power Supply Control Circuit | SG3526

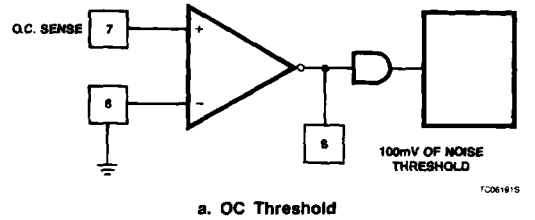


a. Output Driver Dead Time vs R_D Value

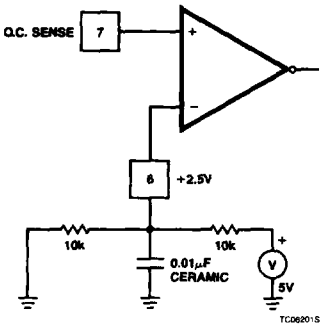


b. Dead Time

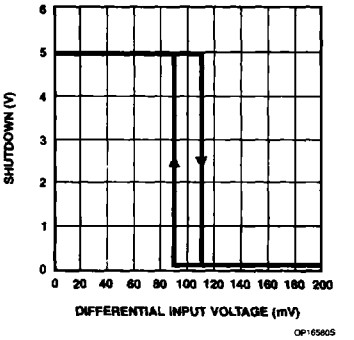
Figure 8



a. OC Threshold



b. OC Threshold



c. Current Limit Transfer Function

Figure 9

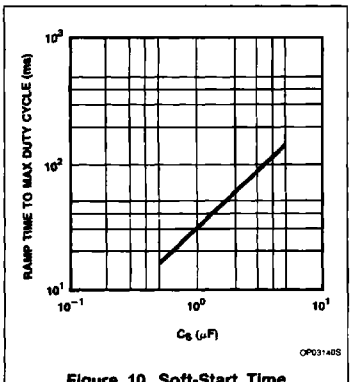


Figure 10. Soft-Start Time Constant vs C_S

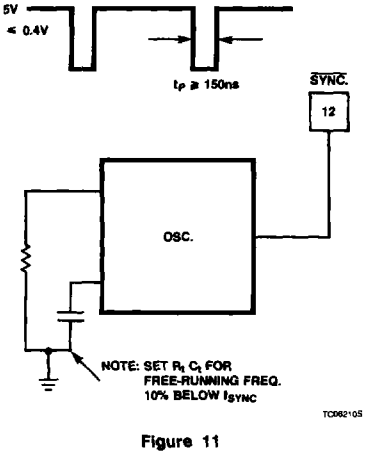


Figure 11

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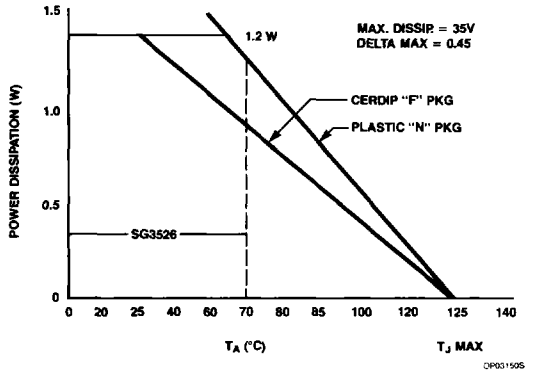
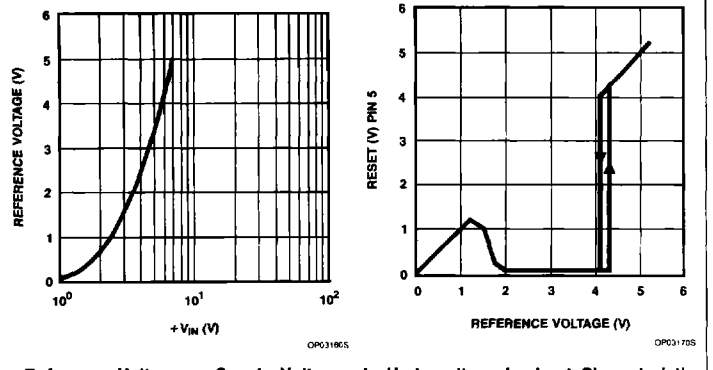


Figure 12. Power Dissipation vs Ambient Temperature



a. Reference Voltage vs Supply Voltage b. Undervoltage Lockout Characteristic

Figure 13

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