Dual asynchronous receiver/transmitter (DUART) SCN2681

DESCRIPTION

The Philips Semiconductors SCN2681 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip MOS-LSI communications device that provides two independent full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is quadruply buffered to minimize the potential of receiver over-run or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the buffer of the receiving device is full.

Also provided on the SCN2681 are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

The SCN2681 is available in three package versions: 40-pin and 28–pin, both 0.6" wide DIPs; a compact 24-pin 0.4" wide DIP; and a 44-pin PLCC.

FEATURES

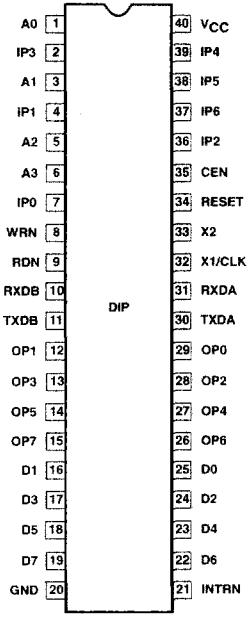
- Dual full-duplex asynchronous receiver/transmitter
- Quadruple buffered receiver data registers
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Programmable baud rate for each receiver and transmitter selectable from:
  - 22 fixed rates: 50 to 115.2k baud
- 16-bit programmable Counter/Timer
  - Non-standard rates to 115.2Kb
  - One user-defined rate derived from programmable timer/counter
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
- Multi-function programmable 16-bit counter/timer
- Multi-function 7-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
  - 100kΩ typical pull-up resistor
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
- Maximum data transfer: 1X – 1MB/sec, 16X – 125kB/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Single +5V power supply
- Commercial and industrial temperature ranges available
- DIP and PLCC packages

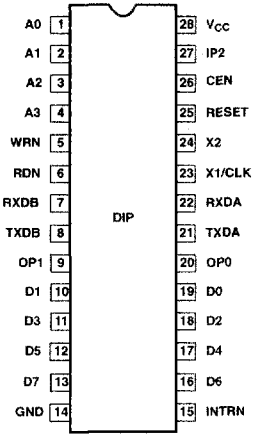
ORDERING INFORMATION

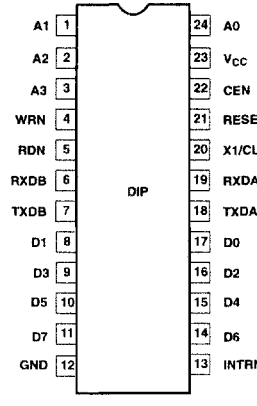
DESCRIPTION	ORDER CODE			
	Commercial		Industrial	
	V_{CC} = +5V ±5%, T_A = 0°C to +70°C		V_{CC} = +5V ±10%, T_A = -40°C to +85°C	
	Plastic DIP	Plastic LCC	Plastic DIP	Plastic LCC
24-Pin[1]	SCN2681AC1N24	Not available	SCN2681AE1N24	Not available
28-Pin[2]	SCN2681AC1N28	Not available	SCN2681AE1N28	Not available
40-Pin[2]	SCN2681AC1N40	Not available	SCN2681AE1N40	Not available
44-Pin	Not available	SCN2681AC1A44	Not available	SCN2681AE1A44

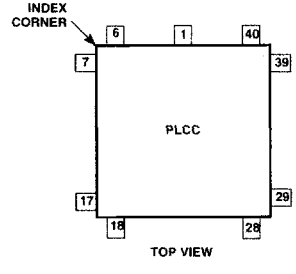
NOTES:
1. 400mil-wide Dual In-Line Package
2. 600mil-wide Dual In-Line Package

PIN CONFIGURATIONS









PIN/FUNCTION		PIN/FUNCTION	
1	NC	23	NC
2	A0	24	INTRN
3	IP3	25	D6
4	A1	26	D4
5	IP1	27	D2
6	A2	28	D0
7	A3	29	OP6
8	IP0	30	OP4
9	WRN	31	OP2
10	RDN	32	OP0
11	RXDB	33	TXDA
12	NC	34	NC
13	TXDB	35	RXDA
14	OP1	36	X1/CLK
15	OP3	37	X2
16	OP5	38	RESET
17	OP7	39	CEN
18	D1	40	IP2
19	D3	41	IP6
20	D5	42	IP5
21	D7	43	IP4
22	GND	44	VCC

SD00084

Figure 1. Pin Configurations

PIN DESCRIPTION

SYMBOL	APPLICABLE			TYPE	NAME AND FUNCTION
	40/44	28	24		
D0–D7	X	X	X	I/O	**Data Bus:** Bidirectional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	X	X	X	I	**Chip Enable:** Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0-D7 as controlled by the WRN, RDN and A0-A3 inputs. When High, places the D0-D7 lines in the 3-State condition.
WRN	X	X	X	I	**Write Strobe:** When Low and CEN is also Low, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	X	X	X	I	**Read Strobe:** When Low and CEN is also Low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0–A3	X	X	X	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESET	X	X	X	I	**Reset:** A High level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0–OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. Clears Test modes, sets MR pointer to MR1.
INTRN	X	X	X	O	**Interrupt Request:** Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	X	X	X	I	**Crystal 1:** Crystal connection or an external clock input. A crystal of a clock the appropriate frequency (nominally 3.6864 MHz) must be supplied at all times. For crystal connections see Figure 7 (included in CD-ROM version), Clock Timing.
X2	X	X		I	**Crystal 2:** Crystal connection. See Figure 7 (included in CD-ROM version). If a crystal is not used it is best to keep this pin not connected although it is permissible to ground it.
RxDA	X	X	X	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
RxDB	X	X	X	I	**Channel B Receive Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
TxDA	X	X	X	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low.
TxDB	X	X	X	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low.
OP0	X	X		O	**Output 0:** General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	X	X		O	**Output 1:** General purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	X			O	**Output 2:** General purpose output or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	X			O	**Output 3:** General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	X			O	**Output 4:** General purpose output or Channel A open-drain, active-Low, RxRDYA/FFULLA output.
OP5	X			O	**Output 5:** General purpose output or Channel B open-drain, active-Low, RxRDYB/FFULLB output.
OP6	X			O	**Output 6:** General purpose output or Channel A open-drain, active-Low, TxRDYA output.
OP7	X			O	**Output 7:** General purpose output or Channel B open-drain, active-Low, TxRDYB output.
IP0	X			I	**Input 0:** General purpose input or Channel A clear to send active-Low input (CTSAN). Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP1	X			I	**Input 1:** General purpose input or Channel B clear to send active-Low input (CTSBN). Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP2	X	X		I	**Input 2:** General purpose input or counter/timer external clock input. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP3	X			I	**Input 3:** General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP4	X			I	**Input 4:** General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.

PIN DESCRIPTION (Continued)

SYMBOL	APPLICABLE			TYPE	NAME AND FUNCTION
	40/44	28	24		
IP5	X			I	**Input 5:** General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP6	X			I	**Input 6:** General purpose input or Channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
V_{CC}	X	X		I	**Power Supply:** +5V supply input.
GND	X	X		I	**Ground**

BLOCK DIAGRAM

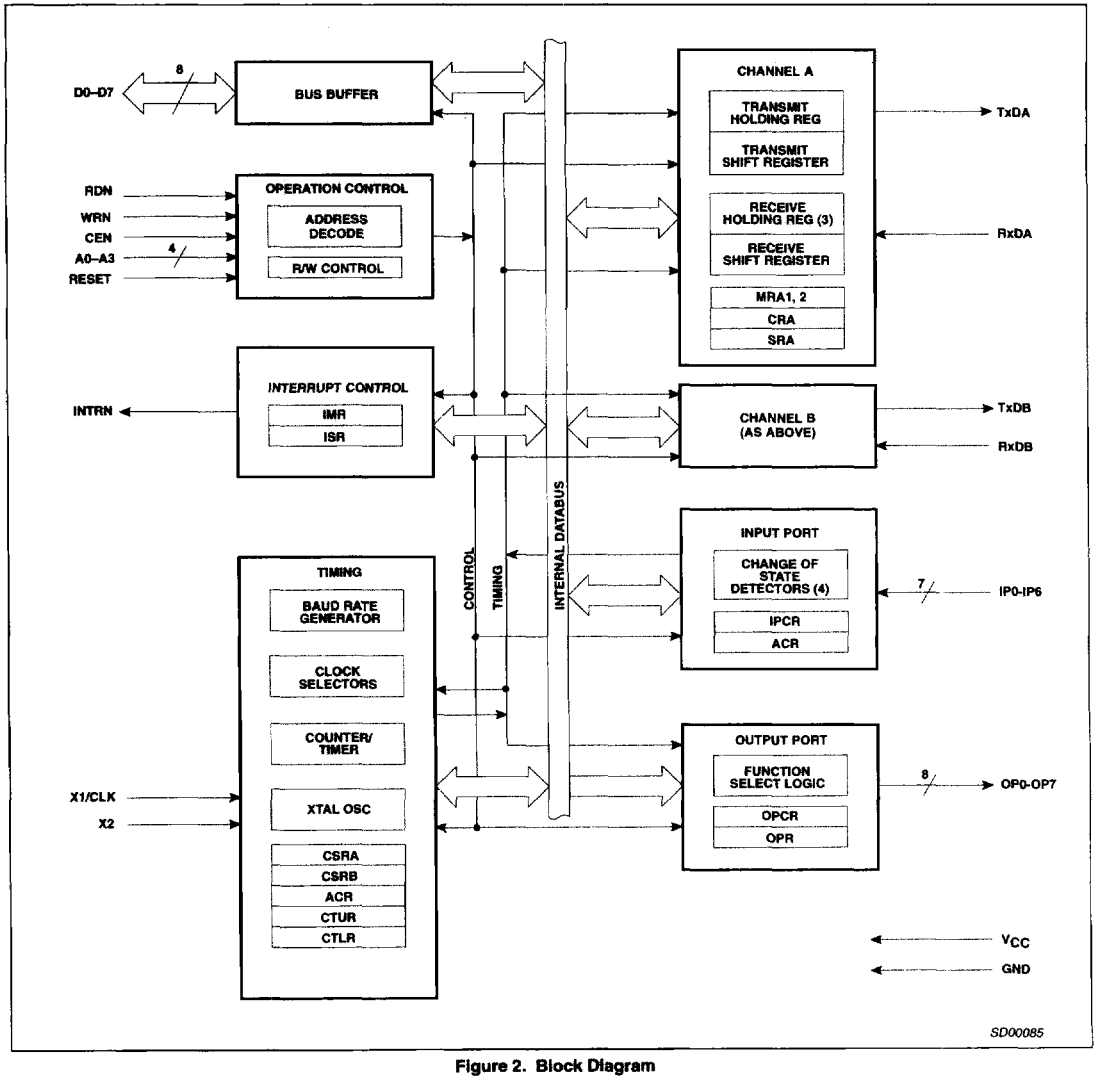


Figure 2. Block Diagram