AN8270K

VHD Video Disc Player Turntable Motor Control Circuit

■Outline

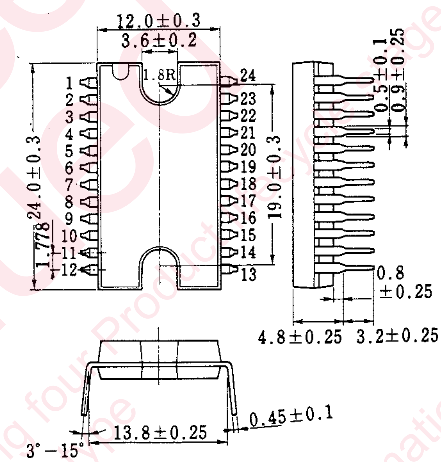
The AN8270K is an integrated circuit developed as one-chip IC for VHD video disk player turntable motor control and drive.

It is optimum for speed control and driving of a brushless motor employing a full-wave current drive system.

■ Features

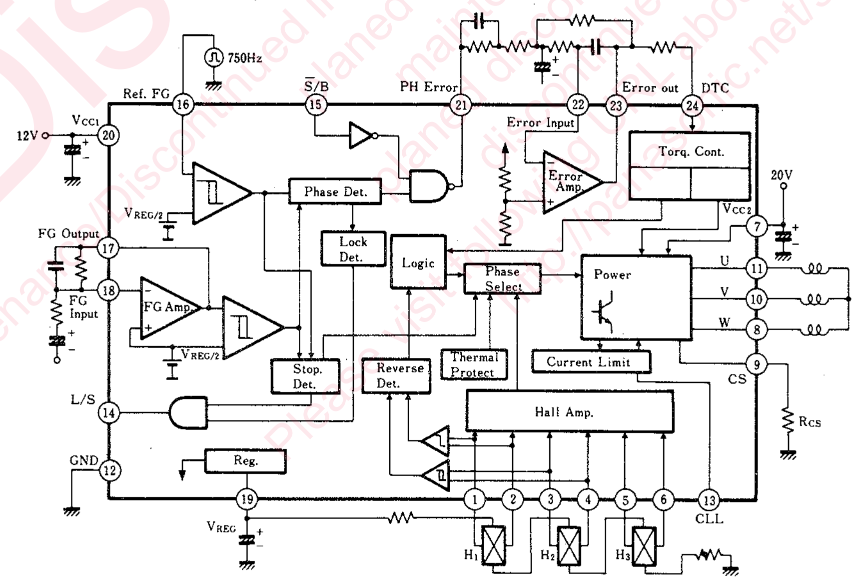
- Speed control by digital phase detector
- 2-Way torque control
- 3-Phase full-wave current drive
- Motor current limit
- Reverse detector/stop dectector
- Phase lock/stop signal output
- Built-in thermal protection

Unit : mm



24-Lead Shrunk DIL Plastic Package (Power Type)

■Block Diagram



Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	Hall Amp. 1+	13	Limit Voltage Cont.
2	Hall Amp. 1−	14	Lock/Stop Sig. Output
3	Hall Amp. 2+	15	Start/Stop Sig. Input
4	Hall Amp. 2−	16	FG Ref. Sig. Input
5	Hall Amp. 3+	17	FG Amp. Output
6	Hall Amp. 3−	18	FG Amp. Rev. Input
7	V_{CC2}	19	Reg. Voltage Output
8	Motor Drive Output W	20	V_{CC1}
9	Current Det.	21	Phase Select Output
10	Motor Drive Output V	22	Error Amp. Rev. Input
11	Motor Drive Output U	23	Error Amp. Output
12	GND	24	Torq Cont. Input

Absolute Maximum Ratings (Ta=25℃)

Item	Symbol	Rating	Unit
1st supply voltage	V_{CC1}	15	V
2nd supply voltage	V_{CC2}	24	V
1st supply current	I_{CC1}	40	mA
Motor drive terminal voltage	V_8, V_{10}, V_{11}	24	V
Hall amp input terminal impressed voltage	$V_1 \sim V_6$	$0 \sim V_{CC1}$	V
Terminal impressed voltage	$V_{14} \sim V_{21}$	$0 \sim V_{CC1}$	V
Limiter voltage control terminal impressed voltage	V_{13}	−5	V
Motor drive terminal rush current	I_8, I_{10}, I_{11}	−1.5~+1.5	A
Current detection terminal rush current	I_9	−1.5~0	A
Regulator voltage output terminal current	I_{19}	−20~+0.5	mA
Power dissipation	P_D	2.5	mW
Storage temperature	T_{stg}	−55~+150	°C
Operating ambient temperature	T_{opr}	−20~+75	°C

Electrical Characteristics (Vcc=12V, Ta=25℃)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
1st supply current	I_{CC1}*	1	V_{IH}=0V	9	14	18	mA
2nd supply current(Standby)	I_{QS}	2	V_{IH}=5V		0	0.1	mA
Regulator voltage output unit							
Output voltage	V_{OR}*	3	I_{OR}=0mA	7.5	8	8.5	V
Output current	I_{OR}*	3				−10	mA
Output impedance	Z_{OR}*	3			2	8.5	Ω
FG reference signal unit							
Threshold voltage H	V_{OHR}			1.8		2.5	V
Threshold voltage L	V_{OLR}	4		1.2	1.5	1.8	V
Hysteresis width	V_{SR}	4		0.5	0.65	0.8	V
FG amp. /Schmitt unit							
Amp. offset voltage	V_{OSF}	4				55	mV
Hysteresis width	V_{SF}	4		80	110	140	mV
Stop detection voltage	V_{RF}	4				170	mV
Amp. output voltage H	V_{OHF}	5		10			V
Amp. output voltage L	V_{OLF}	5				1	V

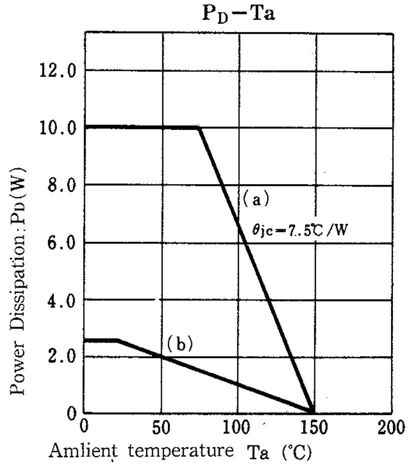
Set to the phase lock mode.

■Electrical Characteristics (Cont'd)(V_{CC}=12V, Ta=25°C)

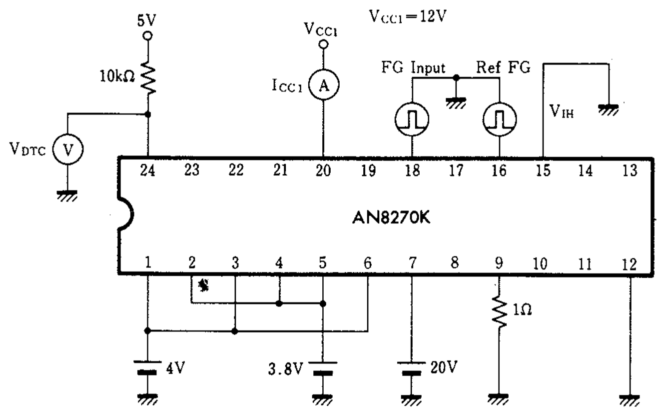
Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Output impedance	Z_{OF}	5			60	100	Ω
Phase comparator output unit							
V_{OR}− (phase comparison output H)	V_{PHH}	4				0.4	V
Phase comparison output L	V_{PHL}	4				0.4	V
Output sink current	I_{PH}^{+}	6		2.5			mA
Output source current	I_{PH}^{-}	6		300	350		μA
Output offset voltage	V_{OSE}	7				50	mV
Amp. output voltage H	V_{OHE}	7		10			V
Amp. output voltage L	V_{OLE}	7				1	V
Output impedance	Z_{OE}	7			60	100	Ω
Start/brake							
Input voltage L	V_{IHS}	8				0.8	V
Input voltage H	V_{ILS}	8		2.4			V
Input low current	I_{IS}		$V_{S/B}$=0V	−5	−1		μA
Lock/stop							
Output voltage H	V_{OHL}	6		4.5	5		V
Output voltage L	V_{OLL}	6				0.5	V
Drive unit							
Dead zone	V_{DZ}*	9		30		250	mV
Output idle voltage	V_{ID}*	9			0.8	10	mV
Forward gain	G_{DF}^{+}*	9		0.4	0.5	0.6	
Reverse gain	G_{DF}^{-}*	9		−0.6	0.5	−0.4	
Start command voltage	V_{STA}*	8		6	6.6		V
Stop command voltage	V_{STO}*	8			0.8	1.5	V
Forward limiter voltage	V_L^{+}*	9	Stop command voltage $V_{DTC}=V_{STA}$	0.73	0.82	0.9	V
Reverse limiter voltage	V_L^{-}*	9	Start command voltage $V_{DTC}=V_{STO}$	0.73	0.82	0.9	V
Hall amp.							
In-phase input range	V_{ICH}			2		$V_{CC1}/-2$	V
Differential input range	V_{IDH}					400	mV
Hall input Sensitivity	V_{ISH}	10				50	mV
Hall set voltage	V_{OSH}	10				20	mV
Power unit							
Upper saturation voltage	V_{SU}	11				1.5	V
Lower saturation voltage	V_{SL}	11				1	V
Leak current(Off)	I_{LO}	2			0		mA
Thermal protective circuit							
Thermal protection operating point	T_P		Joint		170		°C
Hysteresis width	T_{HP}				20		°C
Stop detection freq.	f_S				Fref/16		Hz

＊Set to the phase lock mode.

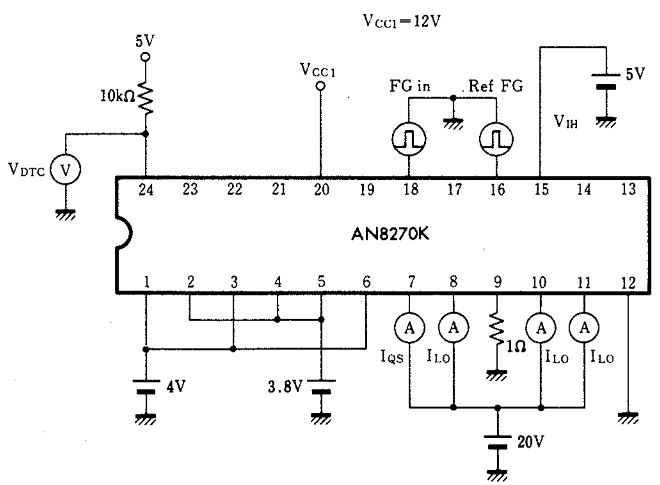
Note)Operating supply voltage range : $V_{CC(opr)}1=10\sim14V$, $V_{CC(opr)}2=16\sim22V$



Test Circuit 1 (I_{CC1})

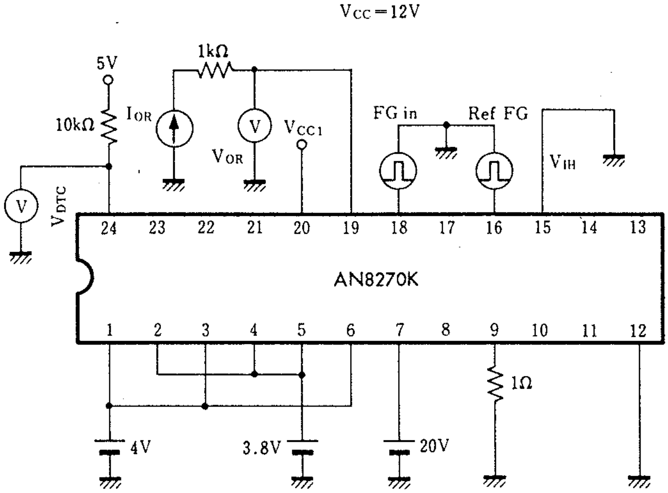


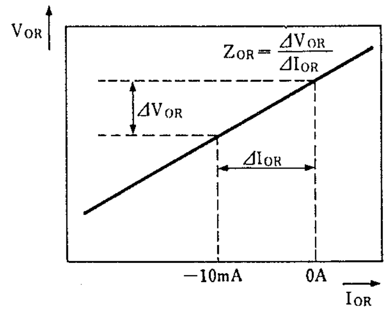
Test Circuit 2 (I_{QS}, I_{LO})



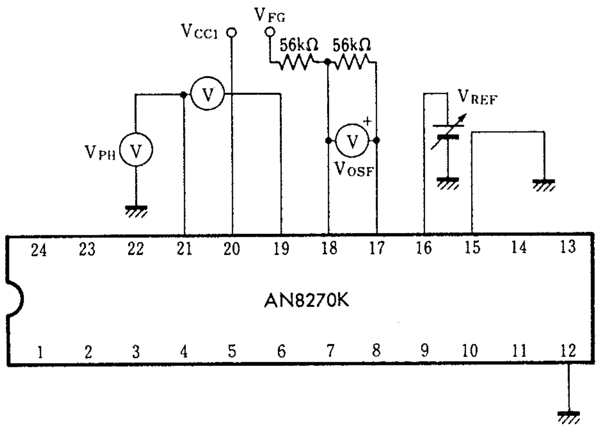
Note)See Page 895 for a forward mode setting method.
See Page 895 for a phase lock and stop setting method

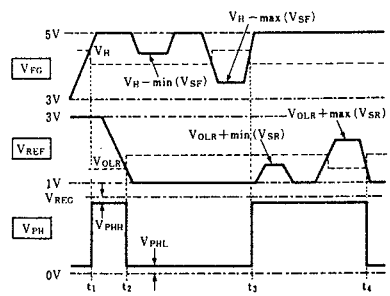
Test Circuit 3 (V_{OR}, I_{OR}, Z_{OR})





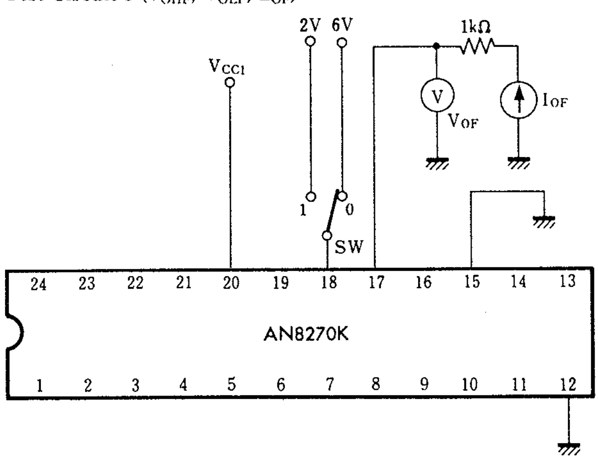
Test Circuit 4 (V_{OLR}, V_{SR}, V_{OSF}, V_{SF}, V_{RF}, V_{PHH}, V_{PHL})





Assuming a V_{OSF} value as V_{OSF1} in case of V_{FG} open and as V_{OSF2} in case of t=t1. define an amp. offset voltage by $V_{OSF}=V_{OSF2}-V_{OSF1}$. Define a stop detection voltage by $V_{RF}=V_{SF}+V_{OSF}$.

Test Circuit 5 (V_{OHF}, V_{OLF}, Z_{OF})



Amp. output voltage

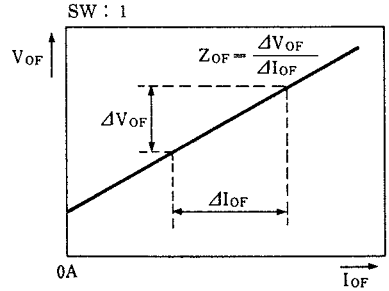
I_{OF}= zero

for SW:0 $V_{OF}=V_{OLF}$

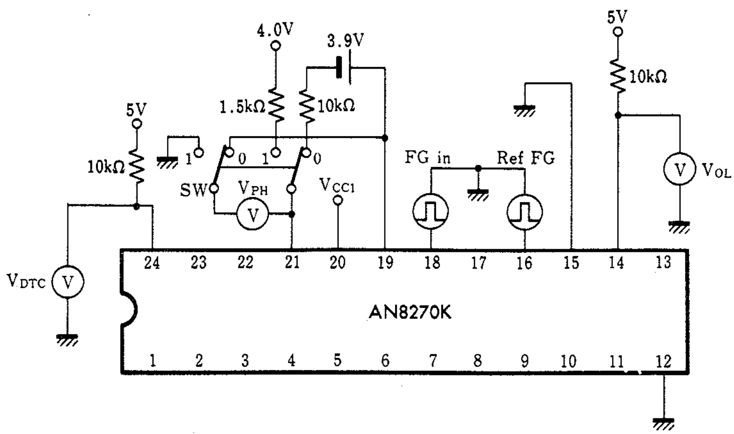
for SW1 $V_{OF}=V_{OHF}$

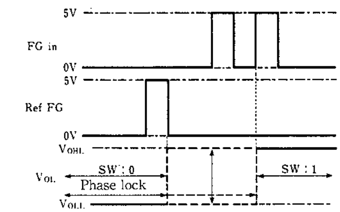
Output impedance Z_{OF}

SW : 1



Test Circuit 6 (I_{PH}^+, I_{PH}^-, V_{OHL}, V_{OLL})





Two types depending on a lock

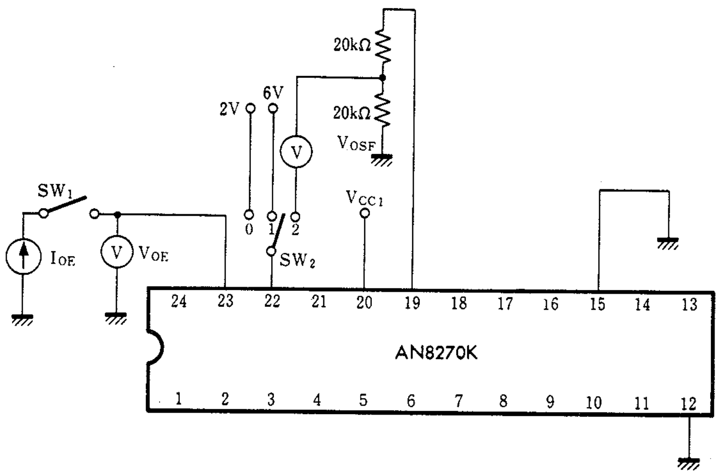
Output sink current

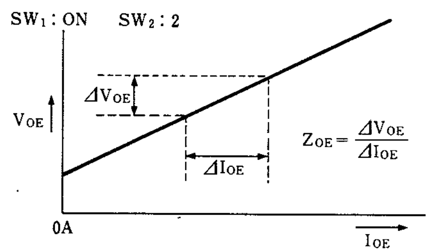
For SW:0 $I_{PH}+=\frac{V_{PH}}{10k\Omega}$

Power source current

For SW:1 $I_{PH}-=\frac{V_{PH}}{1.5k\Omega}$

Test Circuit 7 (V_{OSE}, V_{OHE}, V_{OLE}, Z_{OE})





$Z_{OE}=\frac{\Delta V_{OE}}{\Delta I_{OE}}$

Output offset voltage V_{OSE}

Set the SW2 to 2 and measure the voltage V_{OSE}.

Amp. output voltage

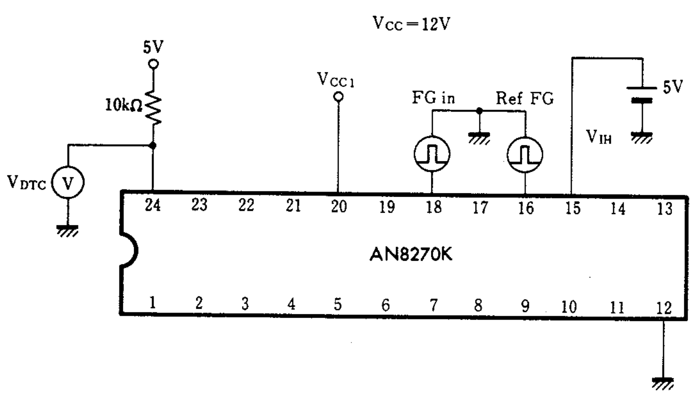
For SW1:OFF, SW2:0 $V_{OE}=V_{OHE}$

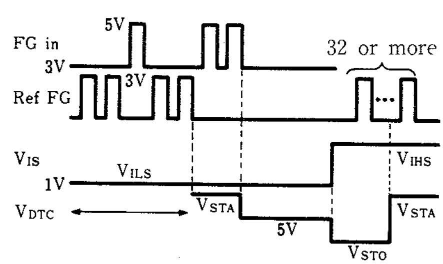
For SW2:1 $V_{OE}=V_{OLE}$

Output impedance Z_{OE}

SW1:ON SW2:2

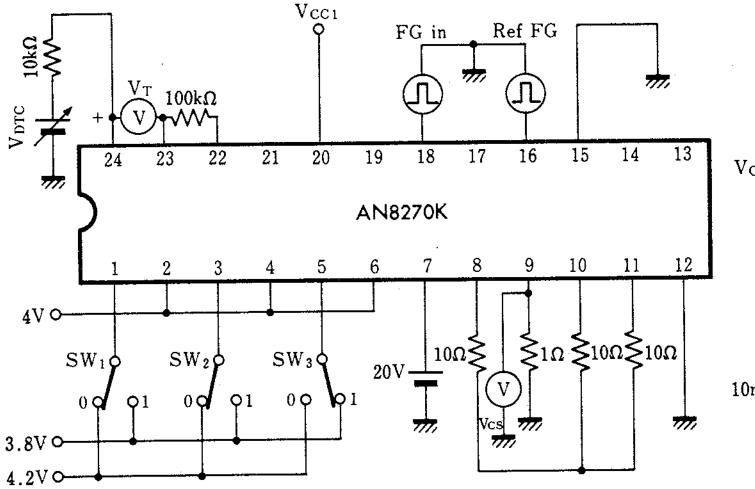
Test Circuit 8 (V_{IHS}, V_{ILS}, V_{STA}, V_{STO})





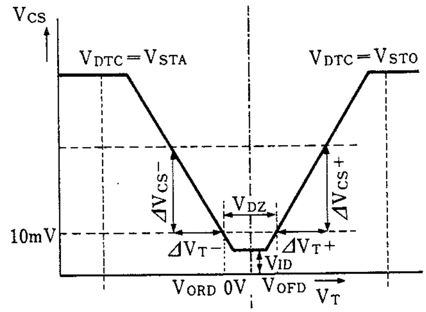
A value depends on an initial state.

Test Circuit 9 (V_{OZ}, V_{ID}, G_{OF}^{+}, G_{DF}^{-}, V_L^{+}, V_L^{-})



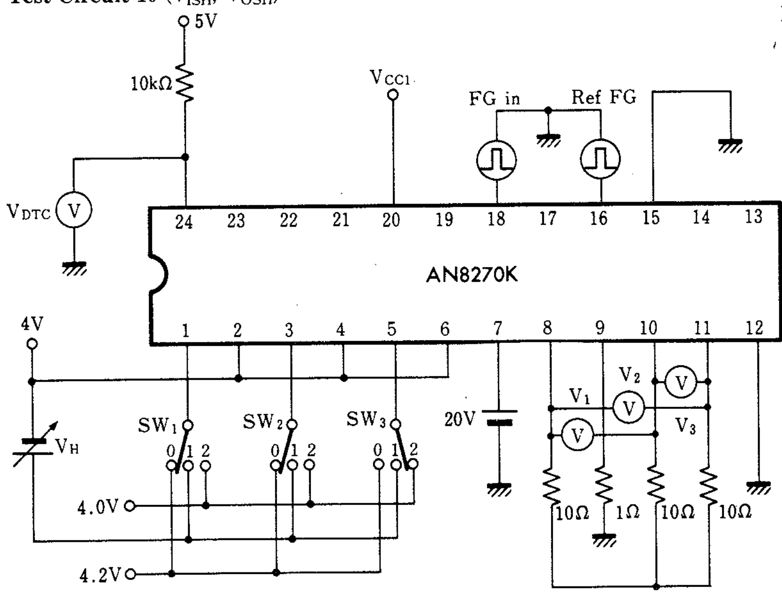
$$G_{DF}+ = \frac{\Delta V_{CS}+}{\Delta V_T+} \qquad V_{DZ} = V_{OF} - V_{OR}$$

$$G_{DF}- = \frac{\Delta V_{CS}-}{\Delta V_T-} \qquad \Delta V_T+ = 100mA \quad \Delta V_T- = 100mA$$

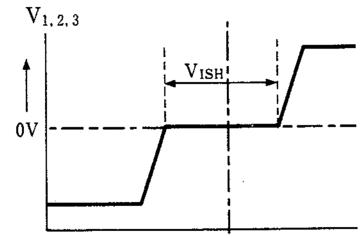


In accordance with the Logic Table on Page 895, set a state by changing the SW1-SW3 and examine.

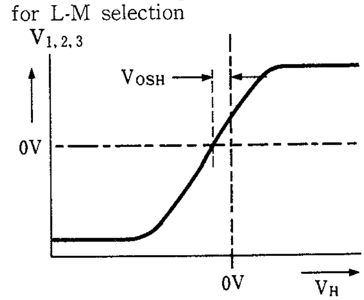
Test Circuit 10 (V_{ISH}, V_{OSH})



Differential voltage for H-M selection



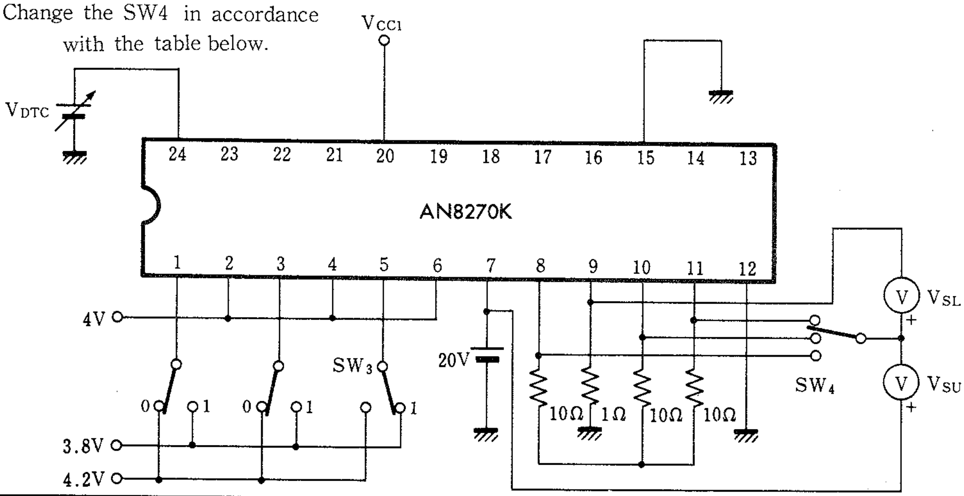
Differential voltage for L-M selection



Item	SW1	SW2	SW3	Differential voltage
V_{ISH}	1	0	2	V1
	2	1	0	V2
	0	2	1	V3
V_{OSH}	1	2	0	V1
	0	1	2	V2
	2	0	1	V3

Test Circuit 11 (V_{SO}, V_{SL})

Change the SW4 in accordance with the table below.



No.	V_{DTC}	SW1	SW2	SW3	U(Pin⑪)	V(Pin⑩)	W(Pin⑧)
1	≧ $V_{REG}/2$	1	1	1	M	M	M
2		1	1	0	M	H	L
3		1	0	0	H	M	L
4		1	0	1	H	L	M
5		0	0	1	M	L	H
6		0	1	1	L	M	H
7		0	1	0	L	H	M
8		0	0	0	M	M	M

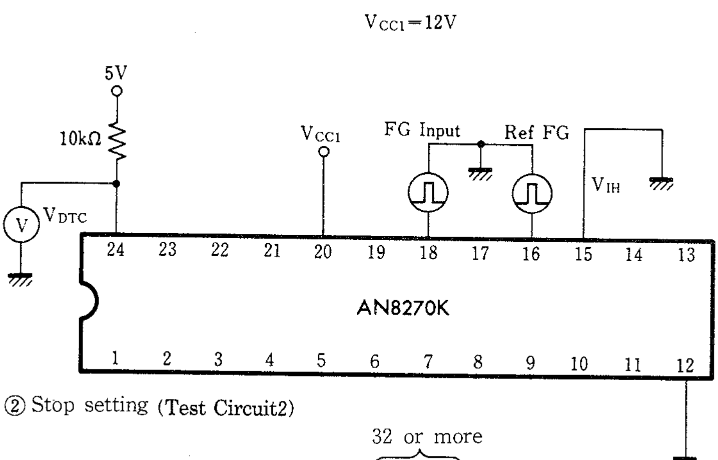
When $V_{DTC} \geqq V_{REG}/2$, H and L for U, V and W in the upper logic table.
H : high voltage L : low voltage M : medium voltage

Setting the forward mode

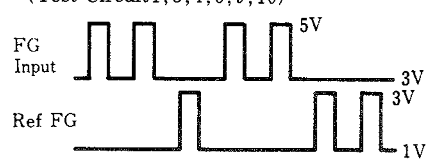
When the SW1 is turned on, it is set by changing over the SW2 from ON to OFF

If written in accordance with the numbers in the upper tabel; 6→5, 7→5, 6→8, 7→8

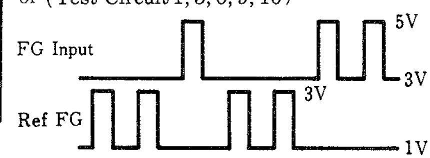
[Testing Method]



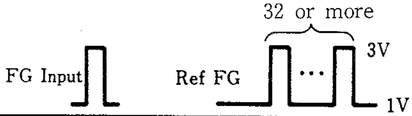
① Phase lock setting
(Test Circuit 1, 3, 4, 6, 9, 10)



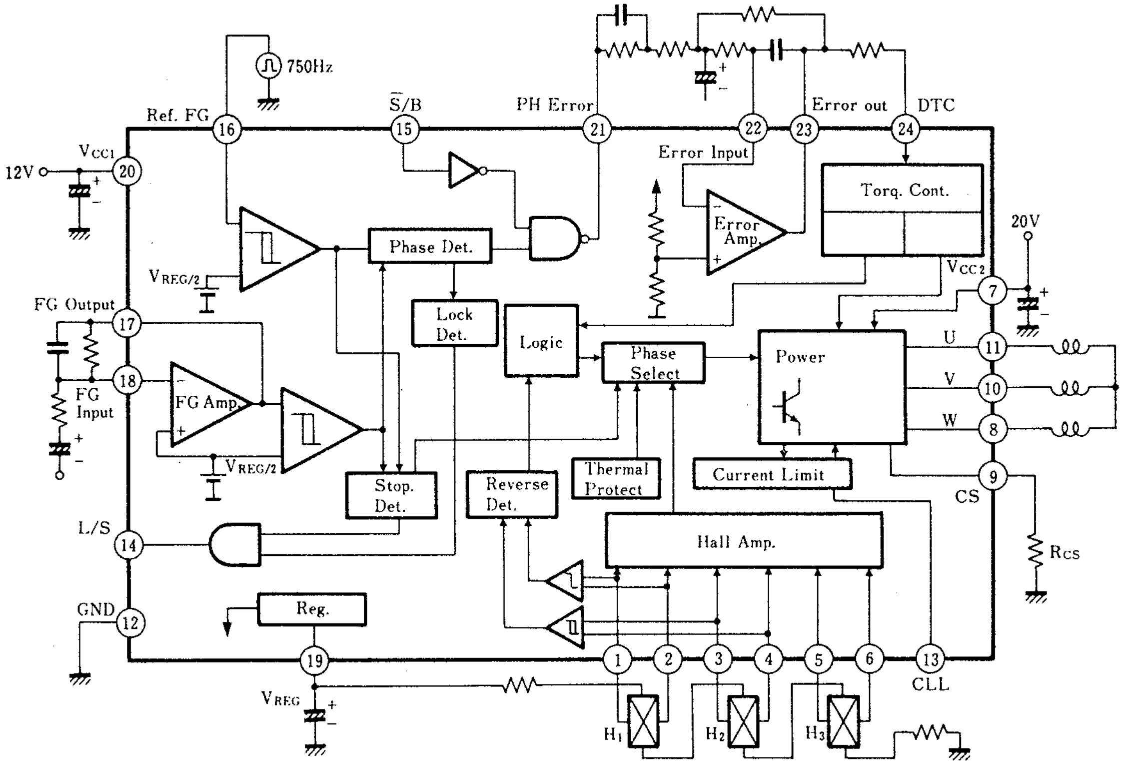
or (Test Circuit 1, 3, 6, 9, 10)



② Stop setting (Test Circuit2)



■ Application Circuit



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