MOTOROLA

TL594

Precision Switchmode Pulse Width Modulation Control Circuit

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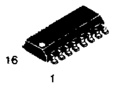
The TL594 is a fixed frequency, pulse width modulation control circuit designed primarily for Switchmode power supply control.

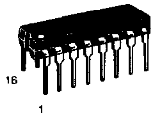
- Complete Pulse Width Modulation Control Circuitry
- On–Chip Oscillator with Master or Slave Operation
- On–Chip Error Amplifiers
- On–Chip 5.0 V Reference, 1.5% Accuracy
- Adjustable Deadtime Control
- Uncommitted Output Transistors Rated to 500 mA Source or Sink
- *Output Control for Push–Pull or Single–Ended Operation*
- Undervoltage Lockout

PRECISION SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUIT

SEMICONDUCTOR TECHNICAL DATA

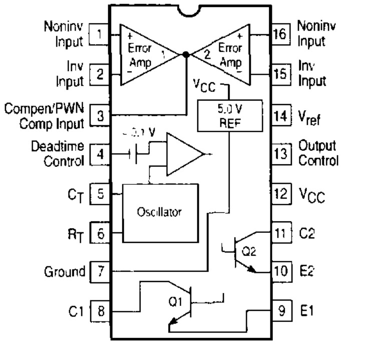


D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)



N SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	42	V
Collector Output Voltage	V_{C1}, V_{C2}	42	V
Collector Output Current (each transistor) (Note 1)	I_{C1}, I_{C2}	500	mA
Amplifier Input Voltage Range	V_{IR}	−0.3 to +42	V
Power Dissipation @ $T_A \le 45°C$	P_D	1000	mW
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	80	°C/W
Operating Junction Temperature	T_J	125	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Operating Ambient Temperature Range TL594ID, CN TL594CD, IN	T_A	 0 to +70 −25 to +85	°C
Derating Ambient Temperature	T_A	45	°C

NOTES: 1. Maximum thermal limits must be observed.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
TL594CD	$T_A = 0°$ to $+70°C$	SO–16
TL594CN		Plastic
TL594IN	$T_A = -25°$ to $+85°C$	Plastic

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_{C1}, V_{C2}	–	30	40	V
Collector Output Current (Each transistor)	I_{C1}, I_{C2}	–	–	200	mA
Amplified Input Voltage	V_{in}	0.3	–	V_{CC} – 2.0	V
Current Into Feedback Terminal	I_{fb}	–	–	0.3	mA
Reference Output Current	I_{ref}	–	–	10	mA
Timing Resistor	R_T	1.8	30	500	kΩ
Timing Capacitor	C_T	0.0047	0.001	10	μF
Oscillator Frequency	f_{osc}	1.0	40	200	kHz
PWM Input Voltage (Pins 3, 4, 13)	–	0.3	–	5.3	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ, unless otherwise noted.)
For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Voltage	V_{ref}				V
(I_O = 1.0 mA, T_A = 25°C)		4.925	5.0	5.075	
(I_O = 1.0 mA)		4.9	–	5.1	
Line Regulation (V_{CC} = 7.0 V to 40 V)	Reg_{line}	–	2.0	25	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	–	2.0	15	mV
Short Circuit Output Current (V_{ref} = 0 V)	I_{SC}	15	40	75	mA
OUTPUT SECTION					
Collector Off–State Current (V_{CC} = 40 V, V_{CE} = 40 V)	$I_{C(off)}$	–	2.0	100	μA
Emitter Off–State Current (V_{CC} = 40 V, V_C = 40 V, V_E = 0 V)	$I_{E(off)}$	–	–	–100	μA
Collector–Emitter Saturation Voltage (Note 2)					V
Common–Emitter (V_E = 0 V, I_C = 200 mA)	$V_{SAT(C)}$	–	1.1	1.3	
Emitter–Follower (V_C = 15 V, I_E = –200 mA)	$V_{SAT(E)}$	–	1.5	2.5	
Output Control Pin Current					μA
Low State (V_{OC} ≤ 0.4 V)	I_{OCL}	–	0.1	–	
High State (V_{OC} = V_{ref})	I_{OCH}	–	2.0	20	
Output Voltage Rise Time	t_r				ns
Common–Emitter (See Figure 13)		–	100	200	
Emitter–Follower (See Figure 14)		–	100	200	
Output Voltage Fall Time	t_f				ns
Common–Emitter (See Figure 13)		–	40	100	
Emitter–Follower (See Figure 14)		–	40	100	
ERROR AMPLIFIER SECTION					
Input Offset Voltage ($V_{O\,(Pin\,3)}$ = 2.5 V)	V_{IO}	–	2.0	10	mV
Input Offset Current ($V_{O\,(Pin\,3)}$ = 2.5 V)	I_{IO}	–	5.0	250	nA
Input Bias Current ($V_{O\,(Pin\,3)}$ = 2.5 V)	I_{IB}	–	–0.1	–1.0	μA
Input Common Mode Voltage Range (V_{CC} = 40 V, T_A = 25°C)	V_{ICR}	0 to V_{CC}–2.0			V
Inverting Input Voltage Range	$V_{IR(INV)}$	–0.3 to V_{CC}–2.0			V
Open Loop Voltage Gain (ΔV_O = 3.0 V, V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	A_{VOL}	70	95	–	dB
Unity–Gain Crossover Frequency (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	f_C	–	700	–	kHz
Phase Margin at Unity–Gain (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	ϕm	–	65	–	deg.
Common Mode Rejection Ratio (V_{CC} = 40 V)	CMRR	65	90	–	dB
Power Supply Rejection Ratio (ΔV_{CC} = 33 V, V_O = 2.5 V, R_L = 2.0 kΩ)	PSRR	–	100	–	dB
Output Sink Current ($V_{O\,(Pin\,3)}$ = 0.7 V)	I_{O-}	0.3	0.7	–	mA
Output Source Current ($V_{O\,(Pin\,3)}$ = 3.5 V)	I_{O+}	–2.0	–4.0	–	mA

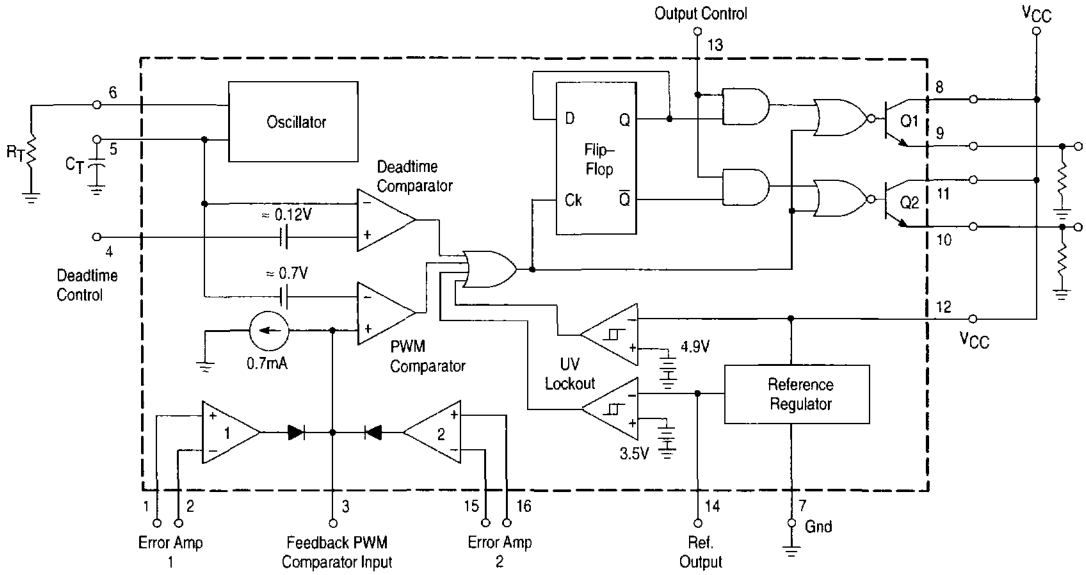
NOTE: 2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 µF, R_T = 12 kΩ, unless otherwise noted.)
For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.

Characteristics	Symbol	Min	Typ	Max	Unit
PWM COMPARATOR SECTION (Test Circuit Figure 11)					
Input Threshold Voltage (Zero Duty Cycle)	V_{TH}	–	3.6	4.5	V
Input Sink Current ($V_{Pin\ 3}$ = 0.7 V)	I_{I-}	0.3	0.7	–	mA
DEADTIME CONTROL SECTION (Test Circuit Figure 11)					
Input Bias Current (Pin 4) ($V_{Pin\ 4}$ = 0 V to 5.25 V)	$I_{IB\ (DT)}$	–	–2.0	–10	µA
Maximum Duty Cycle, Each Output, Push–Pull Mode ($V_{Pin\ 4}$ = 0 V, C_T = 0.01 µF, R_T = 12 kΩ) ($V_{Pin\ 4}$ = 0 V, C_T = 0.001 µF, R_T = 30 kΩ)	DC_{max}	 45 –	 48 45	 50 –	%
Input Threshold Voltage (Pin 4) (Zero Duty Cycle) (Maximum Duty Cycle)	V_{TH}	 – 0	 2.8 –	 3.3 –	V
OSCILLATOR SECTION					
Frequency (C_T = 0.001 µF, R_T = 30 kΩ) (C_T = 0.01 µF, R_T = 12 kΩ, T_A = 25°C) (C_T = 0.01 µF, R_T = 12 kΩ, T_A = T_{low} to T_{high})	f_{osc}	 – 9.2 9.0	 40 10 –	 – 10.8 12	kHz
Standard Deviation of Frequency* (C_T = 0.001 µF, R_T = 30 kΩ)	σf_{osc}	–	1.5	–	%
Frequency Change with Voltage (V_{CC} = 7.0 V to 40 V, T_A = 25°C)	Δf_{osc} (ΔV)	–	0.2	1.0	%
Frequency Change with Temperature (ΔT_A = T_{low} to T_{high}, C_T = 0.01 µF, R_T = 12 kΩ)	Δf_{osc} (ΔT)	–	4.0	–	%
UNDERVOLTAGE LOCKOUT SECTION					
Turn–On Threshold (V_{CC} Increasing, I_{ref} = 1.0 mA) T_A = 25°C T_A = T_{low} to T_{high}	V_{th}	 4.0 3.5	 5.2 –	 6.0 6.5	V
Hysteresis TL594C,I TL594M	V_H	 100 50	 150 150	 300 300	mV
TOTAL DEVICE					
Standby Supply Current (Pin 6 at V_{ref}, All other inputs and outputs open) (V_{CC} = 15 V) (V_{CC} = 40 V)	I_{CC}	 – –	 8.0 8.0	 15 18	mA
Average Supply Current ($V_{Pin\ 4}$ = 2.0 V, C_T = 0.01 µF, R_T = 12 kΩ, V_{CC} = 15 V, See Figure 11)		–	11	–	mA

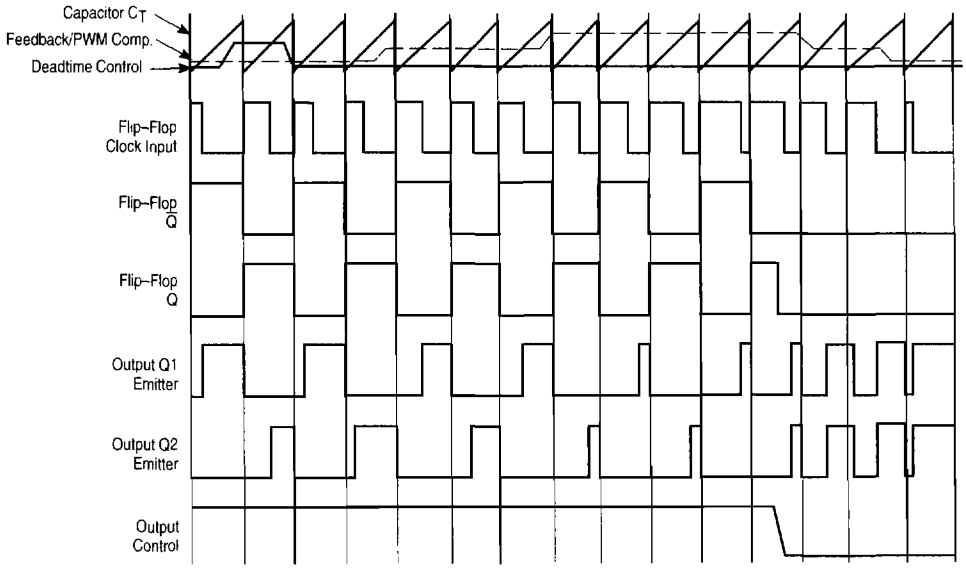
* Standard deviation is a measure of the statistical distribution about the mean as derived from the formula, $\sigma = \sqrt{\dfrac{\sum_{n=1}^{N}(X_n - \bar{X})^2}{N-1}}$

Figure 1. Representative Block Diagram



This device contains 46 active transistors.

Figure 2. Timing Diagram



APPLICATIONS INFORMATION

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Description

The TL594 is a fixed–frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal–linear sawtooth oscillator is frequency–programmable by two external components, R_T and C_T. The approximate oscillator frequency is determined by:

$$f_{osc} \approx \frac{1.1}{R_T \bullet C_T}$$

For more information refer to Figure 3.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The NOR gates, which drive output transistors Q1 and Q2, are enabled only when the flip–flop clock–input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control–signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the Timing Diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the deadtime control, the error amplifier inputs, or the feedback input. The deadtime control comparator has an effective 120 mV input offset which limits the minimum output deadtime to approximately the first 4% of the sawtooth–cycle time. This would result in a maximum duty cycle on a given output of 96% with the output control grounded, and 48% with it connected to the reference line. Additional deadtime may be imposed on the output by setting the deadtime–control input to a fixed voltage, ranging between 0 V to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on–time, established by the deadtime control input, down to zero, as the voltage at the feedback pin varies from 0.5 V to 3.5 V. Both error amplifiers have a common–mode input range from –0.3 V to (V_{CC} – 2 V), and may be used to sense power–supply output voltage and current. The error–amplifier outputs are active high and are ORed together at the noninverting input of the pulse–width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

When capacitor C_T is discharged, a positive pulse is generated on the output of the deadtime comparator, which clocks the pulse–steering flip–flop and inhibits the output transistors, Q1 and Q2. With the output–control connected to the reference line, the pulse–steering flip–flop directs the modulated pulses to each of the two output transistors alternately for push–pull operation. The output frequency is equal to half that of the oscillator. Output drive can also be taken from Q1 or Q2, when single–ended operation with a maximum on–time of less than 50% is required. This is desirable when the output transformer has a ringback winding with a catch diode used for snubbing. When higher output–drive currents are required for single–ended operation, Q1 and Q2 may be connected in parallel, and the output–mode pin must be tied to ground to disable the flip–flop. The output frequency will now be equal to that of the oscillator.

The TL594 has an internal 5.0 V reference capable of sourcing up to 10 mA of load current for external bias circuits. The reference has an internal accuracy of ±1.5% with a typical thermal drift of less than 50 mV over an operating temperature range of 0° to 70°C.

Functional Table

Input/Output Controls	Output Function	$\frac{f_{out}}{f_{osc}}$ =
Grounded	Single–ended PWM @ Q1 and Q2	1.0
@ V_{ref}	Push–pull Operation	0.5

Figure 3. Oscillator Frequency versus Timing Resistance

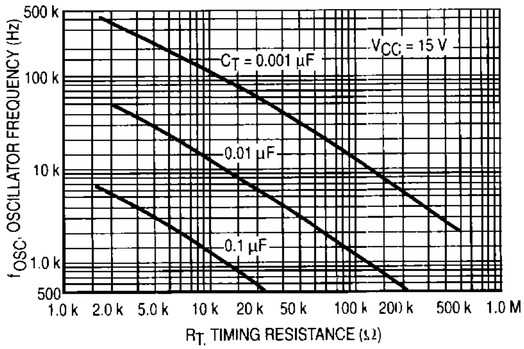

Figure 4. Open Loop Voltage Gain and Phase versus Frequency

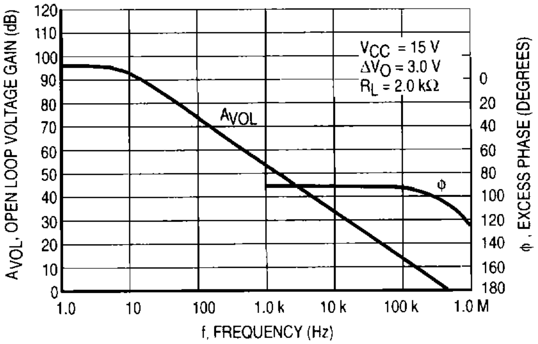

Figure 5. Percent Deadtime versus Oscillator Frequency

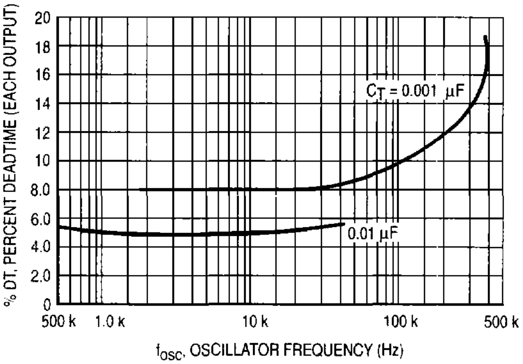

Figure 6. Percent Duty Cycle versus Deadtime Control Voltage

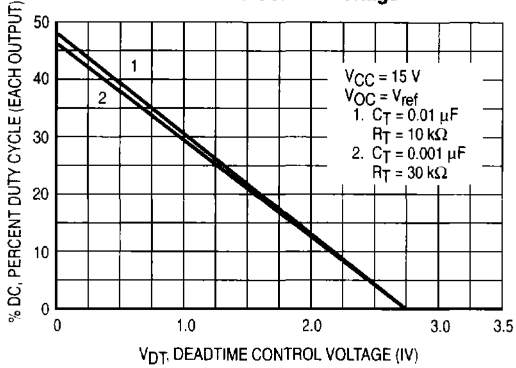

Figure 7. Emitter–Follower Configuration Output Saturation Voltage versus Emitter Current

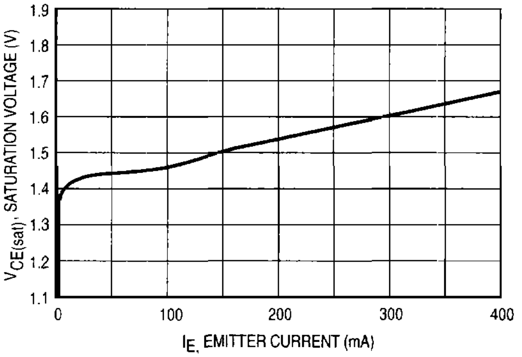

Figure 8. Common–Emitter Configuration Output Saturation Voltage versus Collector Current

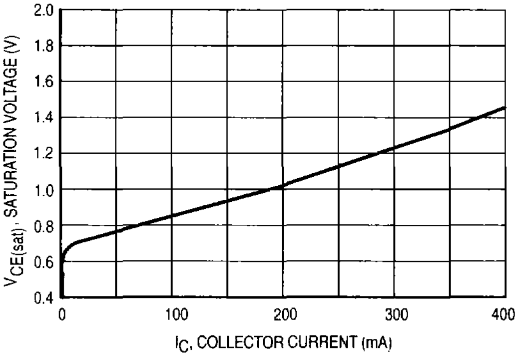

Figure 9. Standby Supply Current versus Supply Voltage

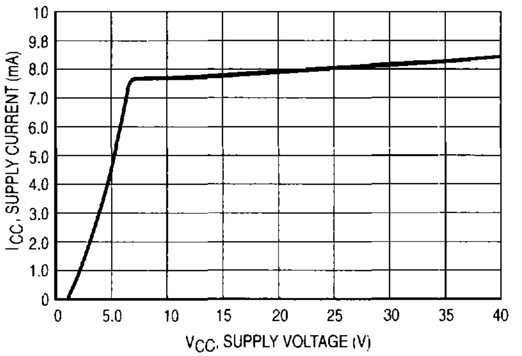

Figure 10. Undervoltage Lockout Thresholds versus Reference Load Current

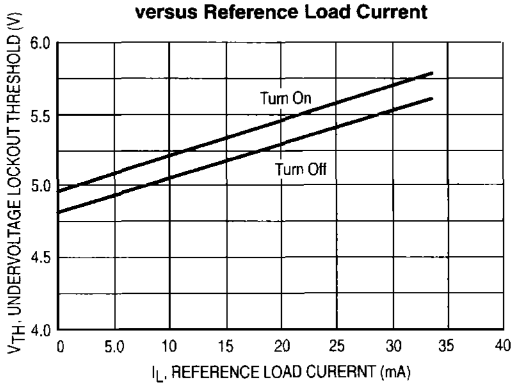

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Figure 11. Error–Amplifier Characteristics

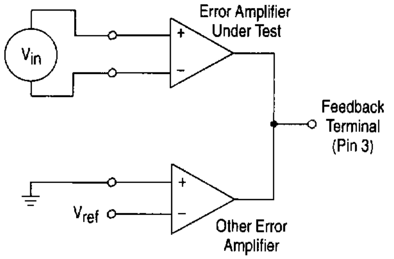

Figure 12. Deadtime and Feedback Control Circuit

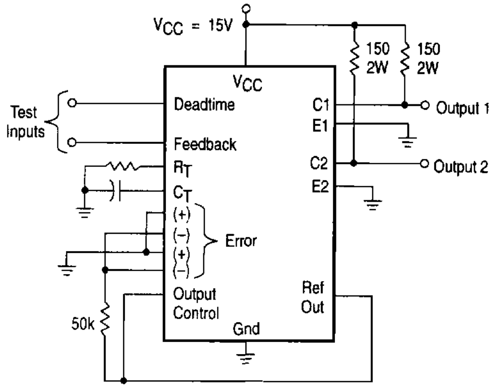

Figure 13. Common–Emitter Configuration Test Circuit and Waveform

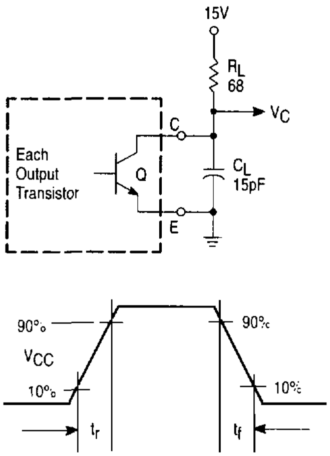

Figure 14. Emitter–Follower Configuration Test Circuit and Waveform

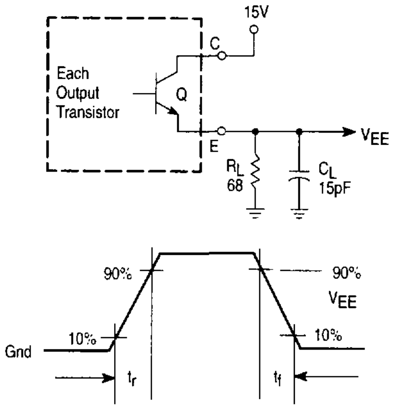

Figure 15. Error–Amplifier Sensing Techniques

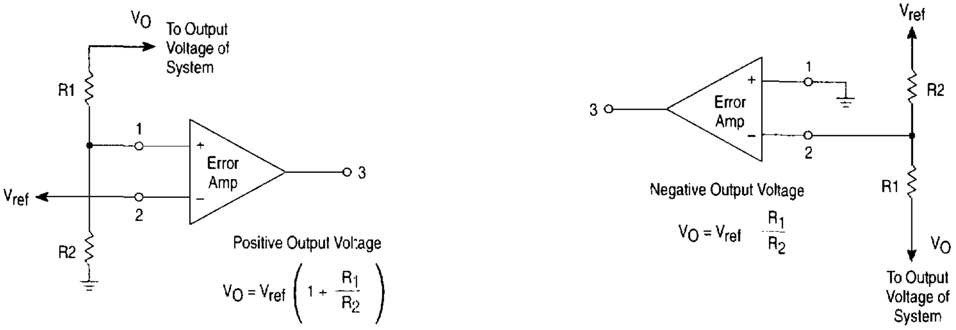

Figure 16. Deadtime Control Circuit

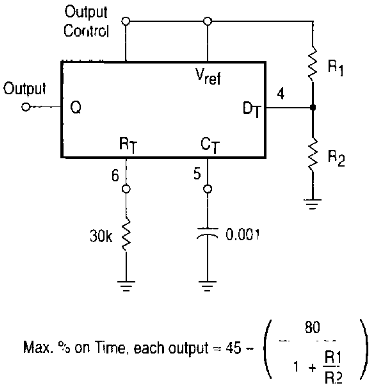

Figure 17. Soft–Start Circuit

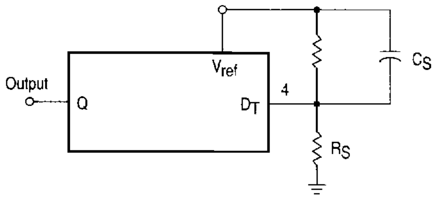

Figure 18. Output Connections for Single–Ended and Push–Pull Configurations

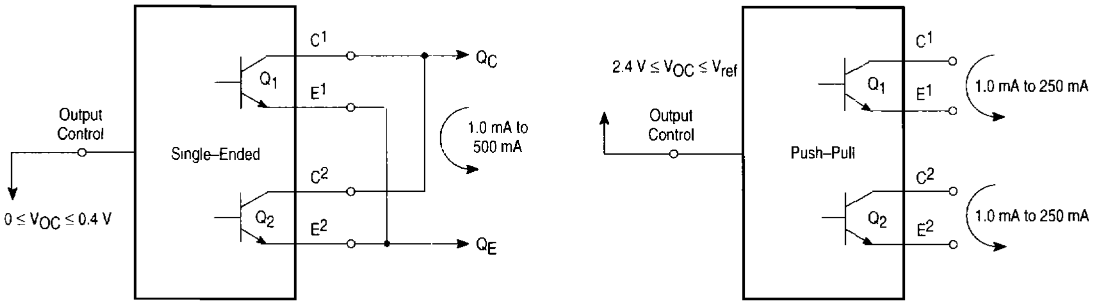

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Figure 19. Slaving Two or More Control Circuits

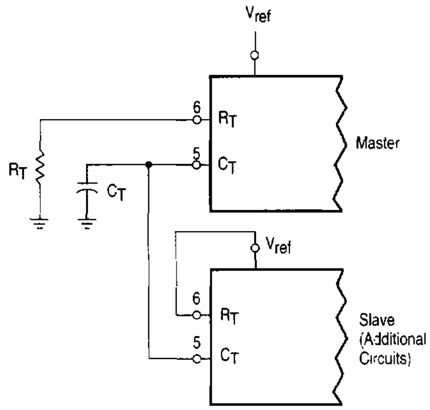


Figure 20. Operation with V_{in} > 40 V Using External Zener

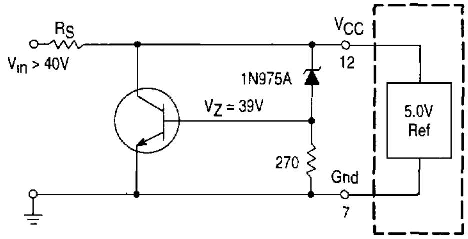
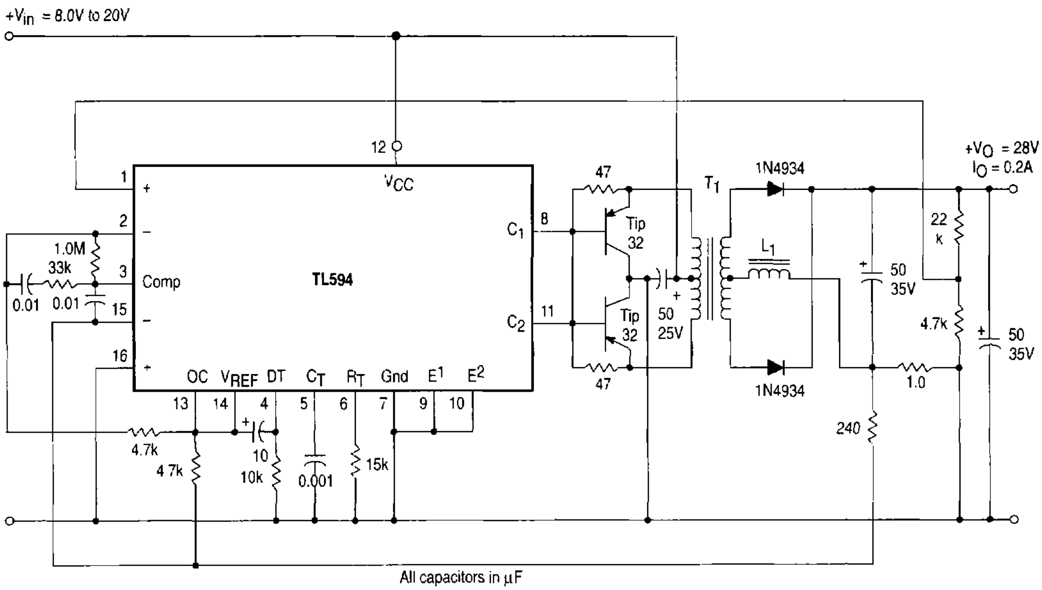


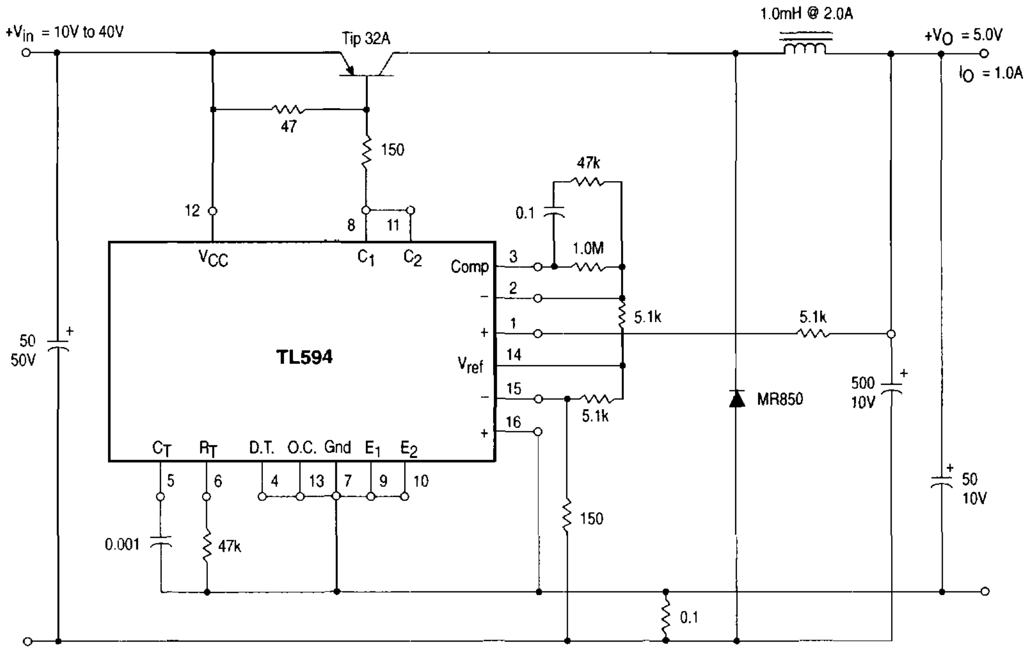
Figure 21. Pulse Width Modulated Push–Pull Converter



Test	Conditions	Results
Line Regulation	V_{in} = 10 V to 40 V	14 mV 0.28%
Load Regulation	V_{in} = 28 V, I_O = 1.0 mA to 1.0 A	3.0 mV 0.06%
Output Ripple	V_{in} = 28 V, I_O = 1.0 A	65 mVpp P.A.R.D.
Short Circuit Current	V_{in} = 28 V, R_L = 0.1 Ω	1.6 A
Efficiency	V_{in} = 28 V, I_O = 1.0 A	71%

L1 – 3.5 mH @ 0.3 A
T1 – Primary: 20T C.T. #28 AWG
Secondary: 120T C.T. #36 AWG
Core Ferroxcube 1408P–L00–3CB

Figure 22. Pulse Width Modulated Step–Down Converter



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 40 V	3.0 mV 0.01%
Load Regulation	V_{in} = 12.6 V, I_O = 0.2 mA to 200 mA	5.0 mV 0.02%
Output Ripple	V_{in} = 12.6 V, I_O = 200 mA	40 mVpp P.A.R.D.
Short Circuit Current	V_{in} = 12.6 V, R_L = 0.1 Ω	250 mA
Efficiency	V_{in} = 12.6 V, I_O = 200 mA	72%