TDC1012
Monolithic Digital-to-Analog Converter
12-Bit, 20 Msps

Description

The TDC1012 is a TTL compatible, 12-bit monolithic D/A converter capable of converting digital data into an analog current or voltage at data rates in excess of 20 Megasamples per second (Msps).

The analog performance has been optimized for dynamic performance, with very low glitch energy. The dual outputs are able to drive 50Ω load with 1 Volt output levels while keeping a spurious-free-dynamic range greater than 70 dB.

Data registers are incorporated on the TDC1012. This eliminates the temporal data skew encountered with external registers and latches and minimizes the glitches that can adversely affect performance in many applications.

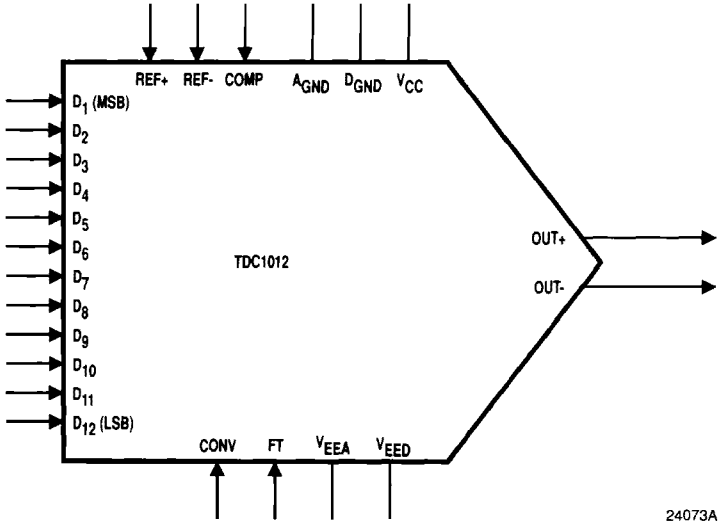
Features

- 12-bit resolution
- 20 Msps data rate
- TTL inputs
- Very low glitch with no Track-and-Hold circuit needed
- Dual +4 dBm (1V into 50Ω) outputs make output amplifiers unnecessary in many applications
- 70 dB typical spurious-free dynamic range
- Available compliant to MIL-STD-883

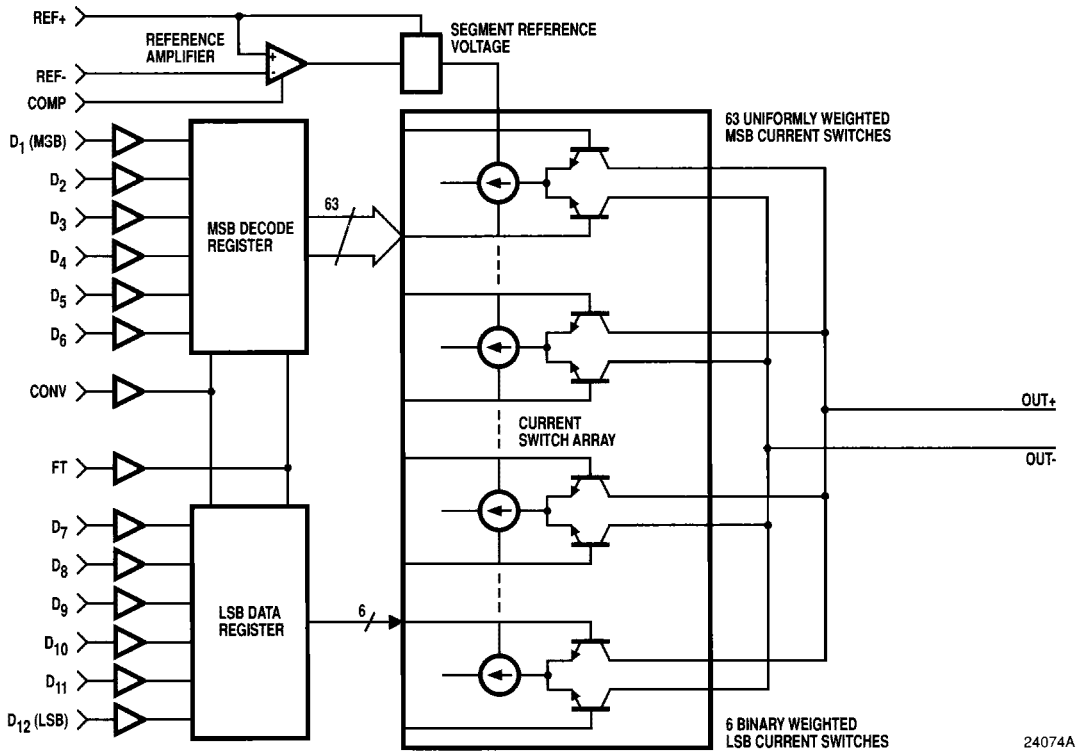
Applications

- Direct digital RF signal generation
- Test signal generation
- Arbitrary waveform synthesis
- Broadcast and studio video
- High-resolution A/D converters

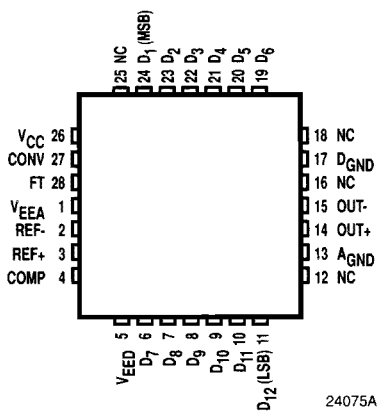
Interface Circuit



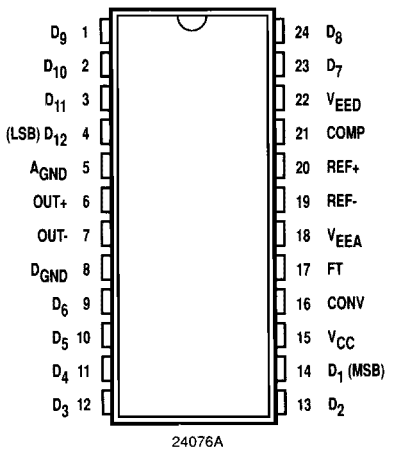
Functional Block Diagram



Pin Assignments



28 Contact Chip Carrier-C3 Package
28 Leaded Plastic Chip Carrier-R3 Package



24 Pin Hermetic Ceramic DIP-J7 Package
24 Pin Plastic DIP-N7 Package

Functional Description

General Information

The TDC1012 consists of five major circuit sections: the LSB data register, the MSB decode block, the decoded MSB register, the current switch array, and the reference amplifier. All data bits are registered just before the current switches to minimize the temporal skew that would generate glitches.

There are three major D/A architectures: segmentated, weighted current sources, and R-2R. In segmentated converters there is one current source for each possible output level. The current sources are equally weighted and for an input code of N, N current sources are turned on. An N bit segmented D/A has 2^N-1 current sources. A weighted current source D/A has one current source for each input bit, and a binary weighting for the current sources. In an R-2R D/A, there is one current source per bit and a resistor network which scales the current sources to have a binary weighting. When transitioning from a code of 011111111111 to 100000000000, both the R-2R D/A and Binary weighted D/A are turning some current sources on while turning others off. If the timing is not perfect, there is a moment where too many current sources are either on or off, resulting in a glitch. In a segmented architecture, 2047 of the current sources remain on, and one more is turned on to increment the output - no possibility of a glitch.

The TDC1012 uses an architecture with the 6 MSBs segmented and the 6 LSBs form a R-2R network. The result is a D/A converter which has very low-glitch energy, and a moderate die size.

Power, Grounds

The TDC1012 requires a –5.2V power supply and a +5.0V power supply. The analog (V_{EEA}) and digital (V_{EED}) supply voltages should be decoupled from each other, as shown in the ***Typical Interface Circuits***. The V_{CC} pin should be considered a digital power supply. The 0.1µF decoupling capacitors should be placed as close as possible to the power pins. The inductors are simple ferrite beads and are neither critical in value nor always required.

Reference

The TDC1012 has two reference inputs: REF+ and REF–. These are the inverting and noninverting inputs of the internal reference amplifier. An externally generated reference voltage is applied to the REF– pin. Current flows into the REF+ pin through an external current setting resistor (R_{REF}). This current is the reference current (I_{REF}) which serves as an internal reference for the current source array. The output current for an input code N from OUT+ is related to I_{REF} through the following relationship:

$$I_{OUT} = N \times \frac{I_{REF}}{64}$$

Where N is the value of the input code

This means that with an I_{REF} that is nominally 625µA, the full scale output is 40mA, which will drive a 50Ω load in parallel with a 50Ω transmission line (25Ω total load) with a 1V peak to peak signal. The impedance seen by the REF– and REF+ pins should be approximately equal so the effect of amplifier input bias current is minimized. The TDC1012 has been optimized to operate with a reference current of **625µA**. Significantly increasing or decreasing this current may degrade the performance of the device.

The minimum and maximum values for V_{REF} and I_{REF} are listed in the table of ***Operating conditions***. The internal reference amplifier is externally compensated to assure stability. To compensate this amplifier, a 0.1µF capacitor should be connected between the COMP pin and V_{EEA}. The amplifier has been optimized to minimize the settling time, and as a result should be considered a DC amplifier. Performance of the TDC1012 operating in a multiplying D/A mode is not guaranteed.

Stable, adjustable reference circuits are shown in the *Typical Interface Circuits, 5, 6* and *7*.

Digital Inputs

The data inputs are TTL compatible. The TDC1012 is specified with two sets of setup and hold times. One of these pairs of specifications guarantees the performance of the TDC1012 to specifications listed in the ***Minimum*** and ***Maximum*** columns of the ***System performance characteristics*** table.

The second more rigid specification is recommended for applications where lowest possible glitch and highest SFDR are desired. The more stringent t_S and t_H ensure that the data will not be slewing during times critical to the TDC1012, and will minimize the effects of capacitively coupled data feedthrough and optimize SFDR performance.

Another method for reducing the effect of capacitive coupling is to slow down the slew rates of the digital inputs. This has been done in the circuit shown in the *Typical Interface Circuits* by the addition of 50Ω series resistors to the data lines.

Clock and Feedthrough Control

The TDC1012 requires a TTL clock signal (CONV) Data is synchronously entered on the rising edge of CONV. The CONV input is ignored in the Feedthrough (FT = HIGH) mode. The Feedthrough (FT) pin is normally held LOW, where the TDC1012 operates in a clocked mode (the output changes only after a clock rising edge). An internal pull-down resistor is provided,and this pin may be left open for clocked operation.

For certain applications, such as high-precision successive approximation A/D converters, throughput delay may be more important then glitch performance. In these cases, the FT pin may be brought HIGH, which makes the input registers transparent. This allows the analog output to change immediately and asynchronously in response to the digital inputs.

Since skew in the bits of the input word will result in glitches, and will affect settling time, it is recommended that the TDC1012 be operated in clocked mode for most applications.

Analog Outputs

Two simultaneous and complementary analog outputs are provided. Both of these outputs are full-power current sources. By driving the current source outputs into a resistive load, they may be used as voltage outputs. OUT+ provides a 0 to –40mA output current (0 to –1V when terminated in 25Ω) as the input code varies from 0000 0000 0000 to 1111 1111 1111. OUT– varies in a complementary manner from –40 to 0mA (–1 to 0V when terminated with 25Ω) over the same code range. (See the *Input Coding Table*.)

The output current is proportional to the reference current and the input code. The recommended output termination is 25Ω. This can be provided by placing a 50Ω source resistor between the output pin and ground, then driving a terminated 50Ω transmission line. With this load, the output voltage range of the converter is 0 to –1.0V.

If a load is capacitively coupled to the TDC1012, it is recommended that a 25Ω load at DC, as seen by the TDC1012, continue to be maintained. The output voltage should be kept within the output compliance voltage range, V_{OC}, as specified in the *Electrical characteristics table*, or the accuracy may be impaired.

Package Interconnections

Signal Type	Signal Name	Function	Value	J7 & N7 Package Pins	C3 & R3 Package Pins
Power	V_{CC}	Digital Supply Voltage	+5.0V	15	26
	A_{GND}	Analog Ground	0.0V	5	13
	D_{GND}	Digital Ground	0.0V	8	17
	V_{EEA}	Analog Supply Voltage	−5.2V	18	1
	V_{EED}	Digital Supply Voltage	−5.2V	22	5
Reference	REF−	Reference Voltage Input	−1.0V	19	2
	REF+	Reference Current Input	625µA	20	3
	COMP	Compensation Capacitor	0.1µF, see text	21	4
Data Inputs	D_1 (MSB)	Most Significant Bit	TTL	14	24
	D_2		TTL	13	23
	D_3		TTL	12	22
	D_4		TTL	11	21
	D_5		TTL	10	20
	D_6		TTL	9	19
	D_7		TTL	23	6
	D_8		TTL	24	7
	D_9		TTL	1	8
	D_{10}		TTL	2	9
	D_{11}		TTL	3	10
	D_{12} (LSB)	Least Significant Bit	TTL	4	11
Feedthrough	FT	Feedthrough Mode Control	TTL	17	28
Convert	CONV	Convert (Clock) Input	TTL	16	27
Analog Output	OUT+	Analog Output	0 to 40mA	6	14
	OUT−	Analog Output	40 to 0mA	7	15

Input Coding Table[1]

Input Data MSB LSB	OUT+ (mA)	V_{OUT+}(mV)	OUT− (mA)	V_{OUT-}(mV)
0000 0000 0000	0.000	0.00	40.000	−1000.00
0000 0000 0001	0.009	−0.24	39.990	−999.75
0000 0000 0010	0.019	−0.49	39.980	−999.52
	•	•	•	•
	•	•	•	•
	•	•	•	•
	•	•	•	•
0111 1111 1111	19.995	−499.88	20.005	−500.12
1000 0000 0000	20.005	−500.12	19.995	−499.88
	•	•	•	•
	•	•	•	•
	•	•	•	•
1111 1111 1101	39.980	−999.52	0.019	−0.49
1111 1111 1110	39.990	−999.75	0.009	−0.24
1111 1111 1111	40.000	−1000.00	0.000	0.0

Note: 1. I_{REF} = 625µA, R_{LOAD} = 25Ω

Figure 1. Timing Diagram

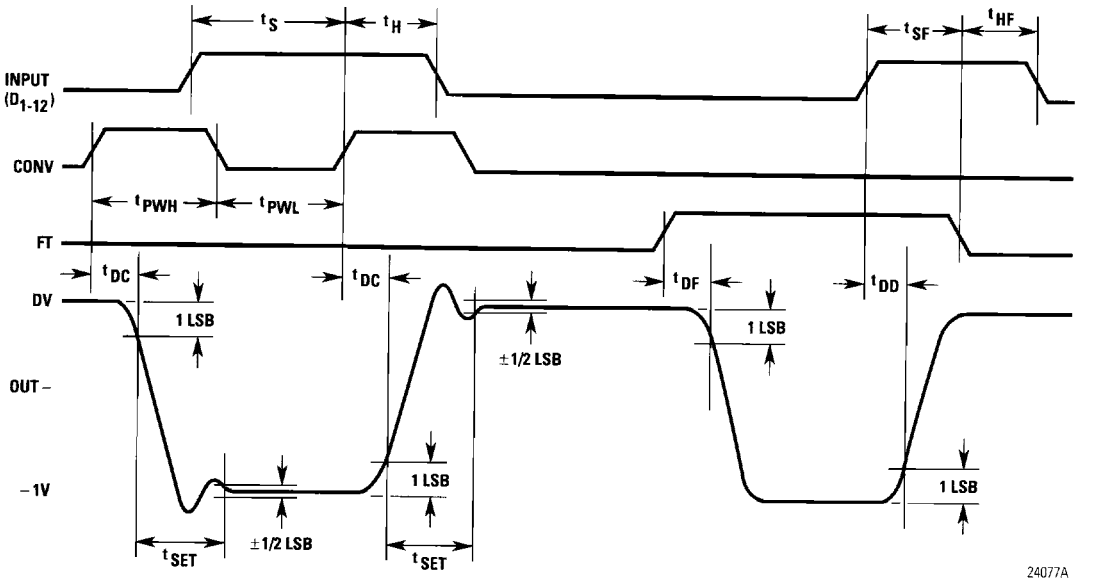


Figure 2. Equivalent Input Circuits

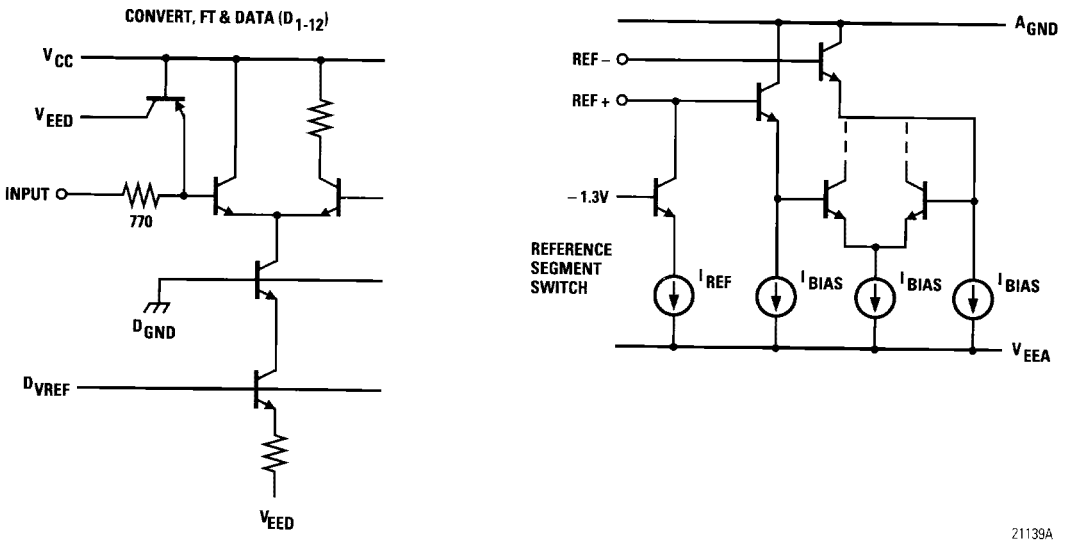


Figure 3. Equivalent Reference and Output Circuits

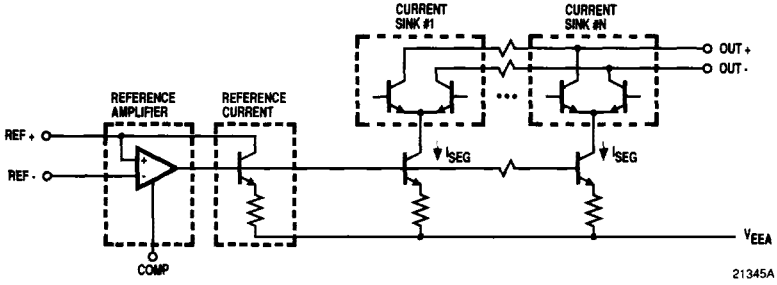
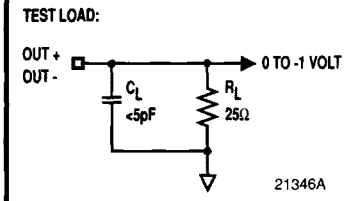


Figure 4. Output Test Load



D/A

Absolute maximum ratings (beyond which the device may be damaged)[1]

Supply Voltages

V_{CC} (Measured to D_{GND})	–0.5 to +7.0V
V_{EEA} (Measured to A_{GND})	–7.0 to +0.5V
V_{EEA} (Measured to V_{EED})	–50 to +50mV
V_{EED} (Measured to D_{GND})	–7.0 to +0.5V
A_{GND} (Measured to D_{GND})	–0.5 to +0.5V

Inputs

CONV, FT, D_{1-12} (Measured to D_{GND})[2]	V_{CC} +0.5 to –0.5V
CONV, FT, D_{1-12} Current, Externally Forced[3]	±3mA
REF+, REF–, Applied Voltage (Measured to A_{GND})[3]	V_{EEA} to +0V
REF+, REF–, Current, Externally Forced[3]	±3mA

Outputs

OUT+, OUT–, Applied Voltage (Measured to A_{GND})[2]	–2.0 to +2.0V
OUT+, OUT–, Current, Externally Forced[3]	+50mA
Short-Circuit Duration (Single Output to GND)	unlimited

Temperature

Operating, Ambient	
(Plastic Package)	–20 to +90°C
(Ceramic Package)	–60 to +150°C
Junction	
(Plastic Package)	+140°C
(Ceramic Package)	+200°C
Lead, soldering (10 seconds)	+300°C
Storage	–65 to +150°C

Note: 1. Absolute maximum ratings are limited values applied individually while other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance and reliability are guaranteed only if the Operating Conditions are not exceeded.

2. Applied voltage must be current limited to specified range.

3. Forcing voltage must be limited to specified range. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Positive Supply Voltage (Measured to D_{GND})	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{EED}	Negative Supply Voltage (Measured to D_{GND})	–4.9	–5.2	–5.5	–4.9	–5.2	–5.5	V
V_{EEA}	Negative Supply Voltage (Measured to A_{GND})	–4.9	–5.2	–5.5	–4.9	–5.2	–5.5	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	–0.1	0.0	0.1	–0.1	0.0	0.1	V
V_{EEA}	Negative Supply Voltage (Measured to V_{EED})	–20	0	20	–20	0	20	mV
t_{PWL}	CONV Pulse Width LOW (to Meet Specification)	20			20			ns
t_{PWL}	CONV Pulse Width LOW (to Optimize SFDR)	20			20			ns
t_{PWH}	CONV Pulse Width HIGH (to Meet Specifications)	20			20			ns
t_{PWH}	CONV Pulse Width HIGH (to Optimize SFDR)	20			20			ns
t_S	Setup Time, Data to CONV (to Meet Specification)	25			25			ns
t_S	Setup Time, Data to CONV (to Optimize SFDR)	32			36			ns
t_H	Hold Time (to Meet Specifications)	1			1			ns
t_H	Hold Time (to Optimize SFDR)	4			6			ns
t_{SF}	Setup Time, Data to FT	5			7			ns
t_{HF}	Hold Time, Data to FT	28			32			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
V_{REF}	Reference Voltage (REF–)	–0.7	–1.0	–1.3	–0.7	–1.0	–1.3	V
I_{REF}	Reference Current (REF+)	550	625	700	575	625	675	µA
C_C	Compensation Capacitor	0.01	0.1		0.01	0.1		µF
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				–55		125	°C

Notes: 1. A common power supply isolated with ferrite bead inductors is recommended for V_{EEA} and V_{EED}. This is shown in the *Typical Interface Circuits*.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
$I_{EEA}+I_{EED}$		$V_{EEA}=V_{EED}$=Max,static					
		T_A=0 to 70°C		−180			mA
		T_A=70°C		−150			mA
		T_C=−55 to 125°C				−200	mA
		T_C=125°C				−150	mA
I_{CC}		V_{CC}=Max, Static					
		T_A=0 to 70°C		25			mA
		T_A=70°C		20			mA
		T_C=−55 to 125°C				35	mA
		T_C=125°C				24	mA
C_{REF}	Reference Input Capacitance			15		15	pF
C_I	Digital Input Capacitance			15		15	pF
V_{OC}	Compliance Voltage		−1.2	1.2	−1.2	1.2	V
R_O	Output Resistance		12		12		kΩ
C_O	Output Capacitance			45		45	pF
I_O	Full Scale Output Current	I_{REF}=Nominal	40		40		mA
I_{IL}	Input Current, Logic LOW	V_{CC}, V_{EE}=Max , V_I=0.4V	−10	50	−10	50	µA
I_{IH}	Input Current, Logic HIGH	V_{CC}, V_{EE}=Max, V_I=2.4V	−10	100	−10	100	µA
I_{IM}	Input Current, Max Input Voltage	V_{CC}, V_{EE}=Max, V_I=V_{CC} Max	−10	100	−10	100	µA
V_{TH}	Logic Input Threshold Voltage,Typical	V_{CC}, V_{EE}=Nom, T_A=25°C	1.25	1.55	1.25	1.55	V

Switching characteristics

Parameter		Test Conditions	Temperature Range						Units
			Standard			Extended			
			Min	Typ	Max	Min	Typ	Max	
F_D	Maximum Data Rate	V_{EEA}, V_{EED}, V_{CC} = Min	20	25		20	23		MHz
t_{DC}	Clock to Output Delay	V_{EEA}, V_{EED}, V_{CC} = Min, FT =LOW			17			20	ns
t_{DD}	Data to Output Delay	V_{EEA}, V_{EED}, V_{CC} = Min, FT = HIGH			35			40	ns
t_{DF}	FT to Output Delay	V_{EEA}, V_{EED}, V_{CC} = Min			35			40	ns
t_R	Risetime	90% to 10% of FSR, FT = LOW			4			4	ns
t_F	Falltime	10% to 90% of FSR, FT = LOW			4			4	ns
t_{SET}	Settling Time, Voltage	FT = LOW, Full-Scale Voltage Transition on I_{OUT} to ±0.0188% FSR		20	30		20	35	ns

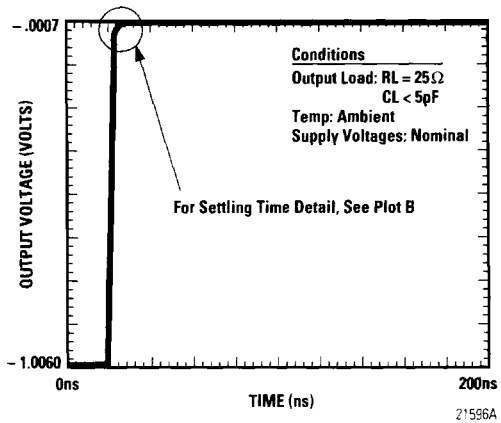
System performance characteristics

Parameter		Test Conditions	Temperature Range						Units
			Standard			Extended			
			Min	Typ	Max	Min	Typ	Max	
E_{LD}	Differential Linearity Error	V_{EEA}, V_{EED}, V_{CC}, I_{REF}= Nom[1]			±0.012			±0.012	%
		TDC1012XXY3							
		TDC1012XXY2			±0.024			±0.024	%
		TDC1012XXY1			±0.048			±0.048	%
E_{LI}	Integral Linearity Error	V_{EEA}, V_{EED}, V_{CC}, I_{REF}= Nom[1]			±0.024			±0.024	%
		TDC1012XXY3							
		TDC1012XXY2			±0.048			±0.048	%
		TDC1012XXY1			±0.048			±0.048	%
V_{OS}	REF+ to REF– Offset Voltage		–10		+10	–10		+10	mV
I_B	REF– Input Bias Current				5			10	µA
E_G	Absolute Gain Error	V_{EEA}, V_{EED}, V_{CC}, I_{REF}= Nom	–5		5	–5		5	%
I_{OF}	Output Offset Current	V_{EEA}, V_{EED}, V_{CC}= Min, D_{1-12}=LOW	–5		+5	–5		+5	µA
PSRR	Power Supply Rejection Ratio	V_{EEA}, V_{EED}, V_{CC}, I_{REF}= Nom[2]			–50			–48	dB
PSS	Power Supply Sensitivity	V_{CC}, V_{EEA}, V_{EED}=4%, I_{REF}=Nom			–140			–140	µA/V
G_A	Peak Glitch Area			25	45		25	45	pV–sec
SFDR	Spurious Free Dynamic Range	I_{REF}=Nom, 20Msps, 10MHz bandwidth F_{out}=6MHz	60			60			dBc
		F_{out}=5MHz		70					dBc
		F_{out}=2MHz		75					dBc
		F_{out}=1MHz		78					dBc

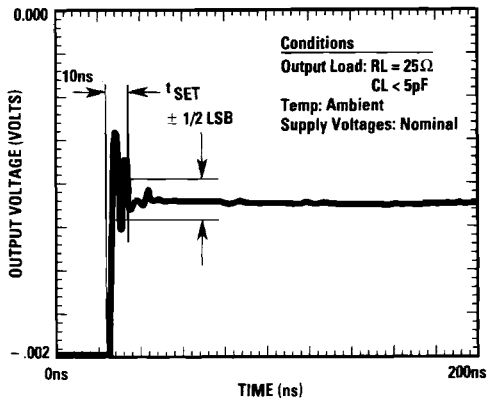
Notes: 1. OUT– connected to A_{GND}, OUT+ driving virtual ground.
2. 120 Hz, 600 mV p-p ripple on V_{EE} and V_{CC}.

Typical Performance Curves (Typical Settling Time Characteristics)

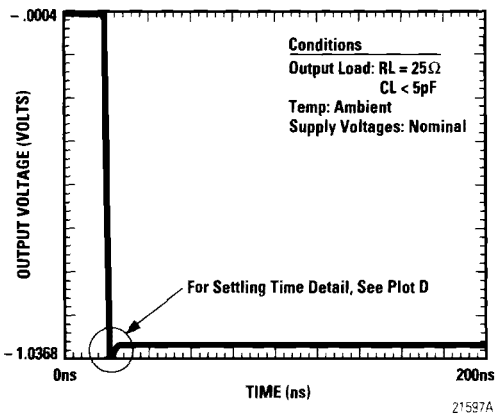
A. Full-Scale Output Transition, Rising Edge



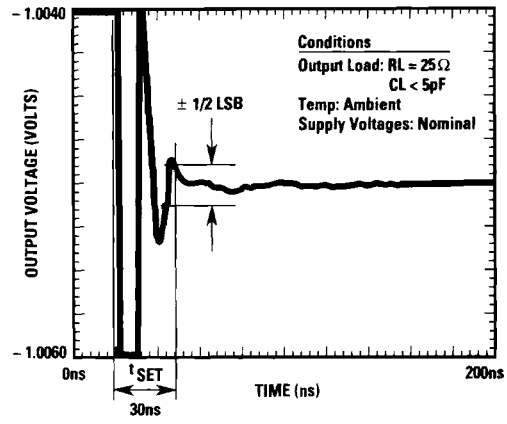
B. Settling Time, Full-Scale Output, Rising Edge



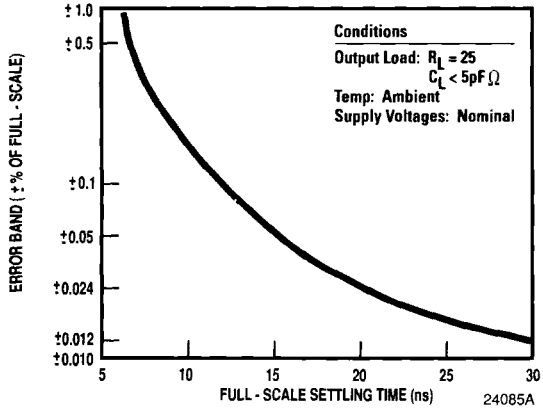
C. Full-Scale Output Transition, Falling Edge



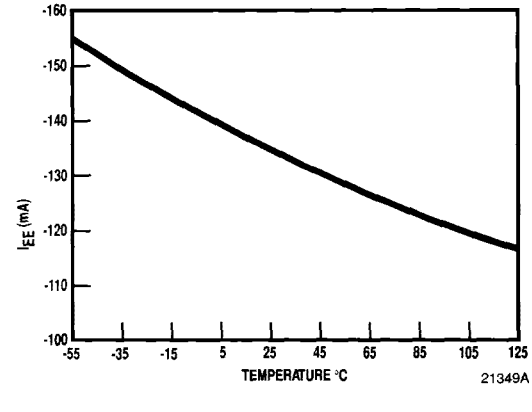
D. Settling Time, Full-Scale Output, Falling Edge



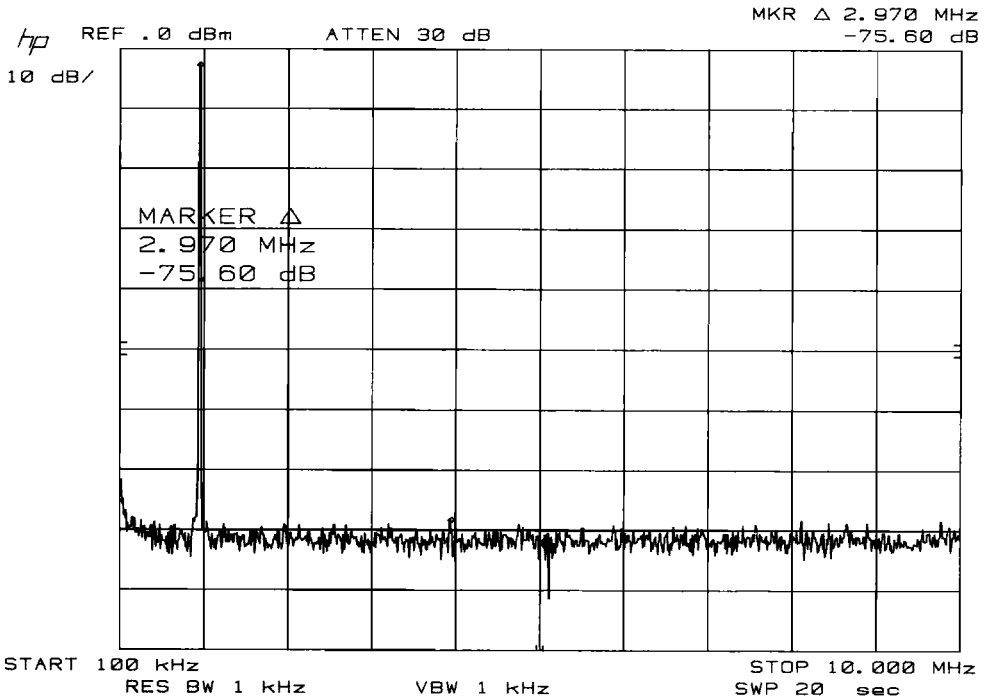
E. Typical Settling Time vs. Settling Accuracy



F. Typical Supply Current vs. Temperature



G. Typical Output Spectrum 20Msps 1MHz F_{OUT}



Applications Discussion

The TDC1012 is a high performance D/A converter. To get the best possible performance requires careful attention to the details of circuit design and layout.

Layout

The layout of grounds in any system is an important design consideration. Separate analog and digital grounds are provided at the TDC1012. All ground pins should be connected to a common low-noise, low-impedance groundplane. This groundplane should be common for the TDC1012 and all of its immediate interface circuitry, which includes all of the reference circuitry, the output load circuitry, and all of the power supply decoupling components.

The digital driving logic should use a separate system ground, and this ground should be connected to the analog groundplane in only one place. The analog and digital grounds may be connected in other ways if required by the user's system grounding plan, however, the voltage differential between the A_{GND} and D_{GND} pins must be held to within ±0.1 Volts.

The high slew-rates of digital data make capacitive coupling with the D/A output a potential problem. Since the digital signals contain high-frequency harmonics of the clock, as well as the signal that is being provided to the TDC1012, the result of data feedthrough often looks like harmonic distortion which degrades the Spurious-Free-Dynamic-Range (SFDR) performance of the D/A. Capacitive coupling can be minimized by keeping digital lines physically away from the analog output and reference. Another technique that can reduce capacitive data coupling is to use low slew rate digital drive circuits or slowing the driving edges with series resistors.

Direct Digital Synthesis Applications

For most synthesis applications, optimum signal purity is obtained with the use of a balun (a simple RF transformer made by wrapping a few turns of wire around a ferrite core) as shown in ***Figure 5***. This configuration has the benefit of canceling common mode distortion. An output

amplifier is not recommended because any amplifier will add distortion, which is likely to be much greater than that present from the outputs of the TDC1012.

The strict adherence to at least the minimum input data setup and hold times is important for the realization of the optimal performance. Spur levels may decrease as setup and hold times are increased. It is possible to achieve even higher performance in some instances by carefully "tuning" the input data setup and hold times (slightly delaying or advancing the CONV signal in relation to the data) provided to the TDC1012. The ***Operating conditions*** table has two sets of data for t_S and t_H, one which guarantees performance of the device in most applications, and one, more conservative specification, which has been found to be optimal for DDS applications.

The actual digital-data waveform which represents a sinewave contains strong harmonics of that fundamental frequency. This can be seen by connecting a digital data line to the input of a spectrum analyzer. Data feedthrough to the analog output of a system due to improper board layout or system shielding and grounding will appear as additional harmonic distortion, adversely affecting SFDR.

Harmonic distortion may improve even further with reduced AC termination impedance values, at the expense of lowered output voltage. This is achieved by a balun used as an impedance transformer as shown in ***Figure 5***.

The purity of the output of the TDC1012 is greater than that which can be measured by many spectrum analyzers. The spectral plots shown in this data sheet were generated with an HP8568B, which has a noise floor just below that of the TDC1012. When making spectral measurements it is important to remember that the TDC1012 output power is +4dBm, which is greater power than many analyzers are equipped to handle without adding distortion of their own. Accordingly, it may be necessary to introduce an attenuator to the input of the spectrum analyzer.

The CONV signal provided to the TDC1012 must be as free from clock jitter as possible. Clock jitter is the random cycle-to-cycle variation in clock period. CONV clock jitter will effectively appear at the output as phase noise. A value of 10ps or less for clock jitter is recommended for the highest performance applications. Ordinary crystal oscillators are satisfactory. High-performance synthesizers, such as the HP8662, used to trigger a precision pulse generator, are also satisfactory.

The TMC2340 direct digital synthesizer is ideal for generating a digital sinusoid for the D/A converter. The TMC2340 automatically generates a carrier frequency which may then be digitally phase, frequency or amplitude modulated. Two outputs are provided which are 90° out of phase (quadrature outputs). For more information on direct digital synthesis, and other applications of the TDC1012, please see application note ***TP46*** and ***AB-8*** from TRW LSI Products.

Bipolar Output

See ***Figure 6*** for a suggested circuit for achieving a bipolar output voltage range. Optimum DC linearity is obtained by using a differential output, either with a balun or an operational amplifier in the differential mode. If it is desired that the TDC1012 be operated in a single-ended fashion, the unused output should be connected directly to ground as is shown in ***Figure 7***.

Figure 5. Typical Interface Circuit with Balun Output

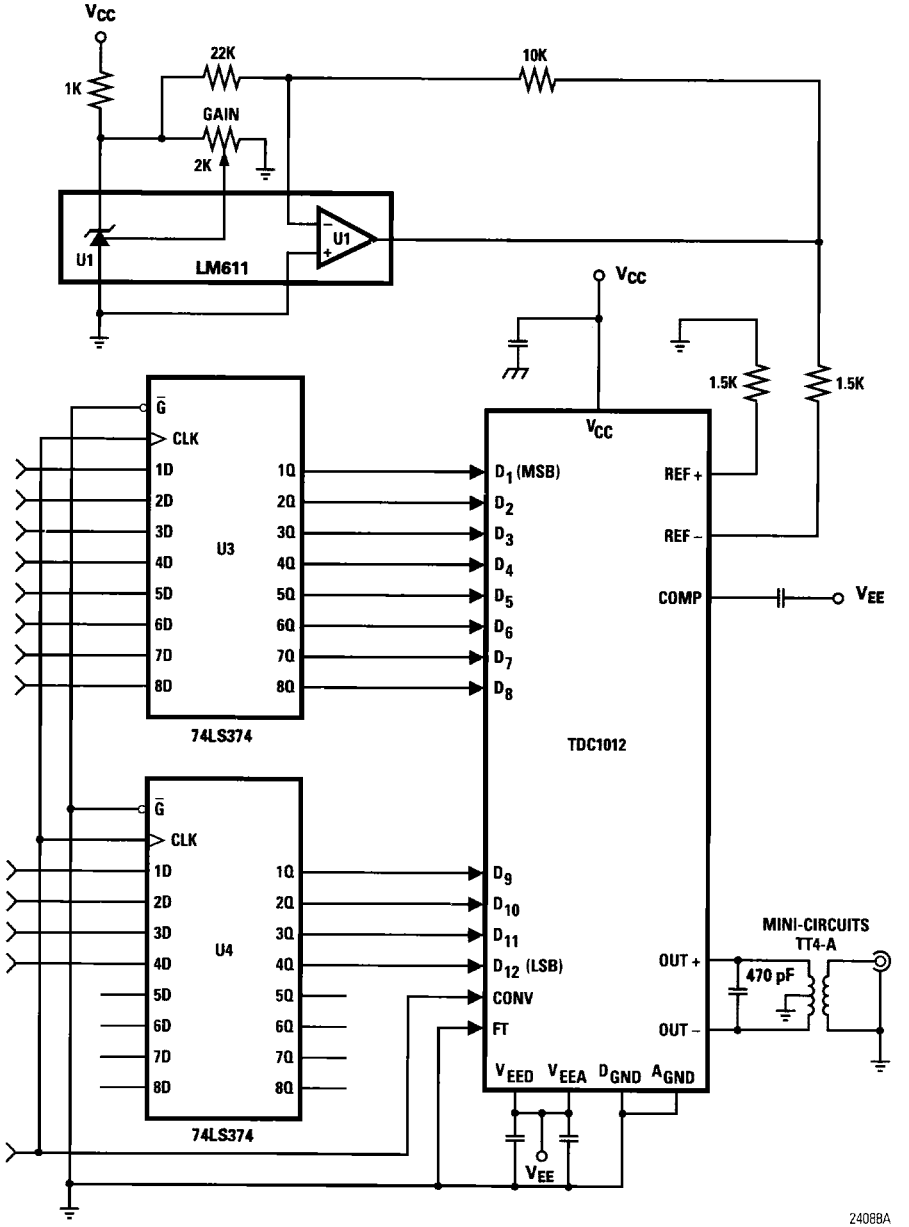


Figure 6. Typical Interface Circuit with Differential Amplifier Output

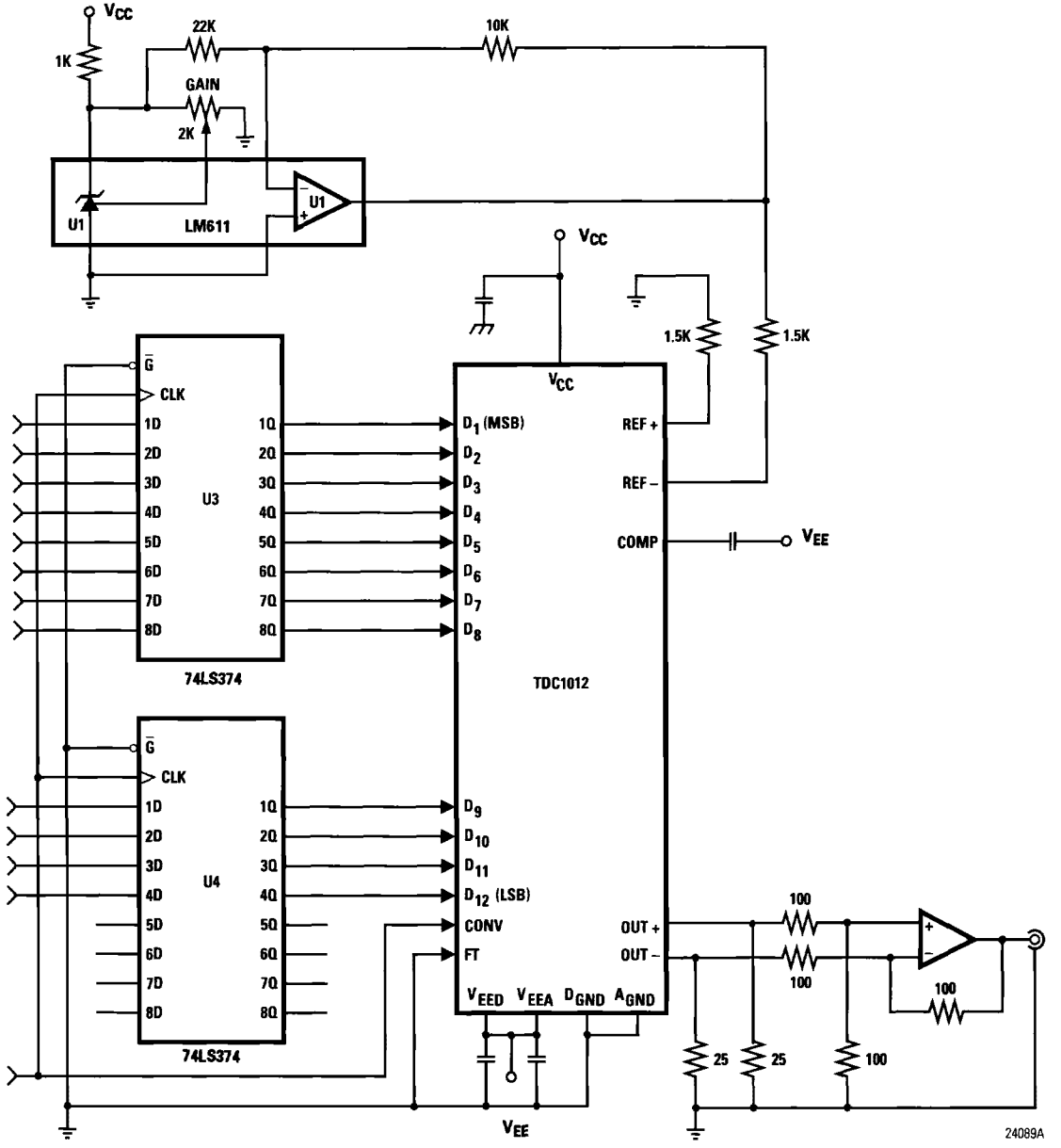
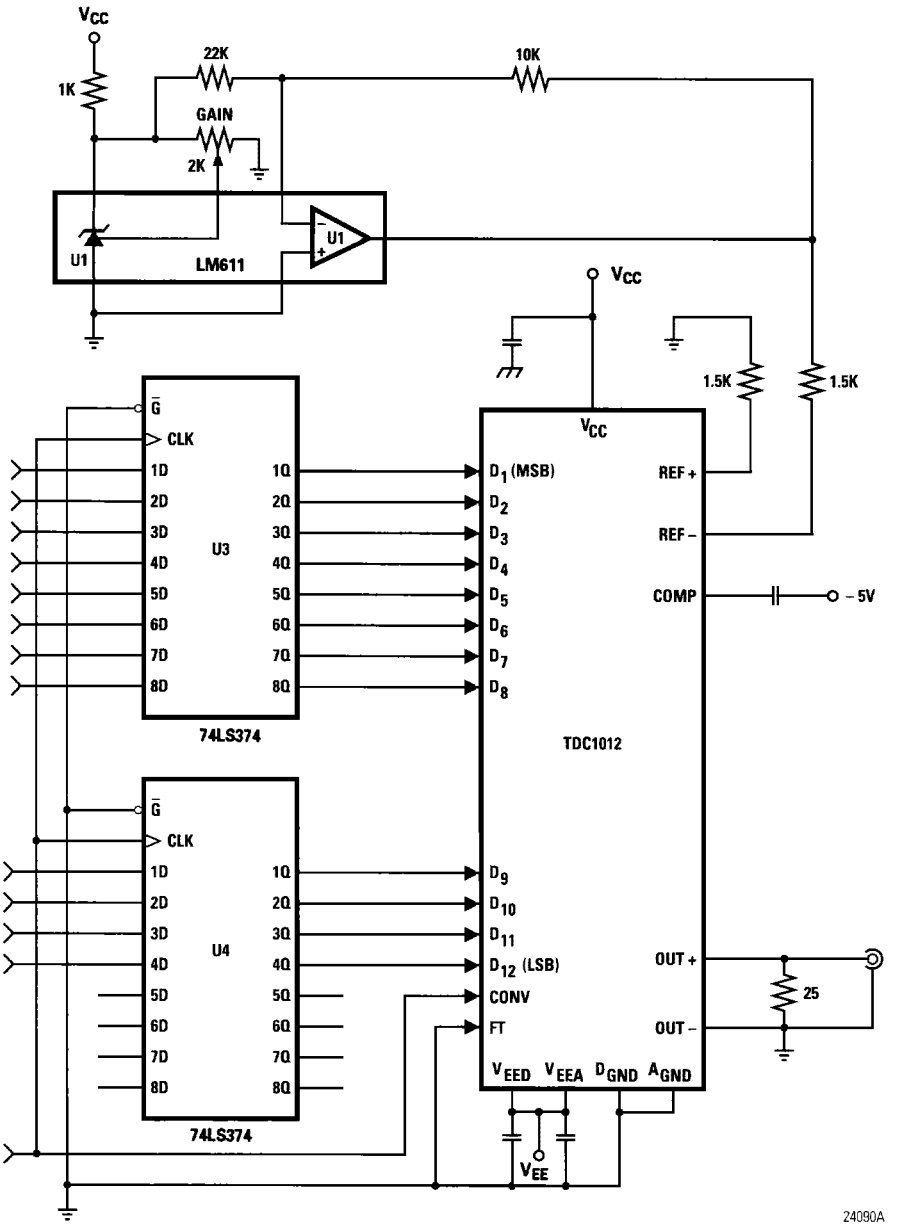


Figure 7. Typical Interface Circuit with Resistive Load Output



Using the TDC1012 and TDC1112 in Sinusoidal Synthesis Applications

In the past, most waveform synthesis was performed using analog oscillators, with their problems of drift, limited versatility, and design complexity. However, as the cost of high-performance digital circuits and digital-to-analog converters continues to fall, digital waveform synthesis is becoming increasingly popular. Direct digital synthesis (DDS) offers unprecedented levels of signal stability. Potential signal complexity for numerous applications including communications, instrumentation, radar, and medical imaging is also enhanced by DDS. This application note describes how exceptional spectral purity can be achieved with the TDC1012 and TDC1112 in sinewave synthesis applications. Board design techniques which optimize the performance of these D/A converters is also discussed.

In most applications, the performance of a digital synthesizer is limited by the digital-to-analog converter (D/A) employed. Specifications of interest include maximum allowable sampling (digital clock) rate, signal-to- [random] noise ratio, total harmonic distortion, and spurious-free dynamic range (SFDR).

With their high linearity and low glitch energy, the TRW TDC1012 and TDC1112 12-bit and TDC1018 8-bit D/A converters are particularly well suited to DDS applications. When used with the TRW TMC2340 Direct Digital Frequency Synthesizer, the TDC1012 becomes the output stage of a high-performance, low part count digital frequency synthesizer. The TDC1012 offers a 20MSPS clock rate and is TTL-compatible. The TDC1112 operates at up to 50MSPS and is ECL-compatible. Both parts offer 70dB SFDR for 8 MHz signals sampled at 20MSPS.

The circuit in Figure 10 can perform with spurs as low as -70dBc. To maintain a clean clock signal, a buffer should drive the clock to the direct digital synthesis circuitry. The clock oscillator should be powered from the same decoupled V_{CC} as the D/A converter.

Grounding is extremely important. A solid copper ground plane should be used and connected to digital ground at only one point to prevent the formation of ground loops. This minimizes the flow of digital switching current across the D/A ground plane.

The use of a balun across the D/A outputs significantly improves spectral purity, since it effectively cancels distortion due to the Early voltage and data feedthrough characteristics of the D/A converter. In some applications, a 470 picofarad capacitor connected between pin 6 and pin 7 as close to those pins as possible will be effective in reducing spurs.

The primary sources of 2nd-harmonic distortion are insufficient input setup and hold times (t_S and t_H) and data feedthrough. Minimum setup and hold times for the SFDR specification are shown in the "System Performance Characteristics" section of the data sheets for the TDC1012 and TDC1112.

Figure 10 shows a 74ALS374 8-bit register with a 2ns R-C delay (200 Ohm, 10 pF in the clock input line) that is designed to help meet setup and hold times for the TDC1012 (when it is operated at 20MSPS) while reducing output slew rates. For military applications, a 54F374 with a 3ns R-C delay will meet the extended temperature range setup and hold time specifications while maintaining reasonable output slew rates. Note that the military versions of the TDC1012 and TDC1112 are available in a 24-pin side brazed ceramic dual-in-line package which has been specifically designed to minimize data feedthrough. For optimum performance, the D/A converter should be soldered directly to the board. If a socket must be used, a low profile gold-insert socket such as Robinson-Nugent part number ICT-246-S-TG is recommended.

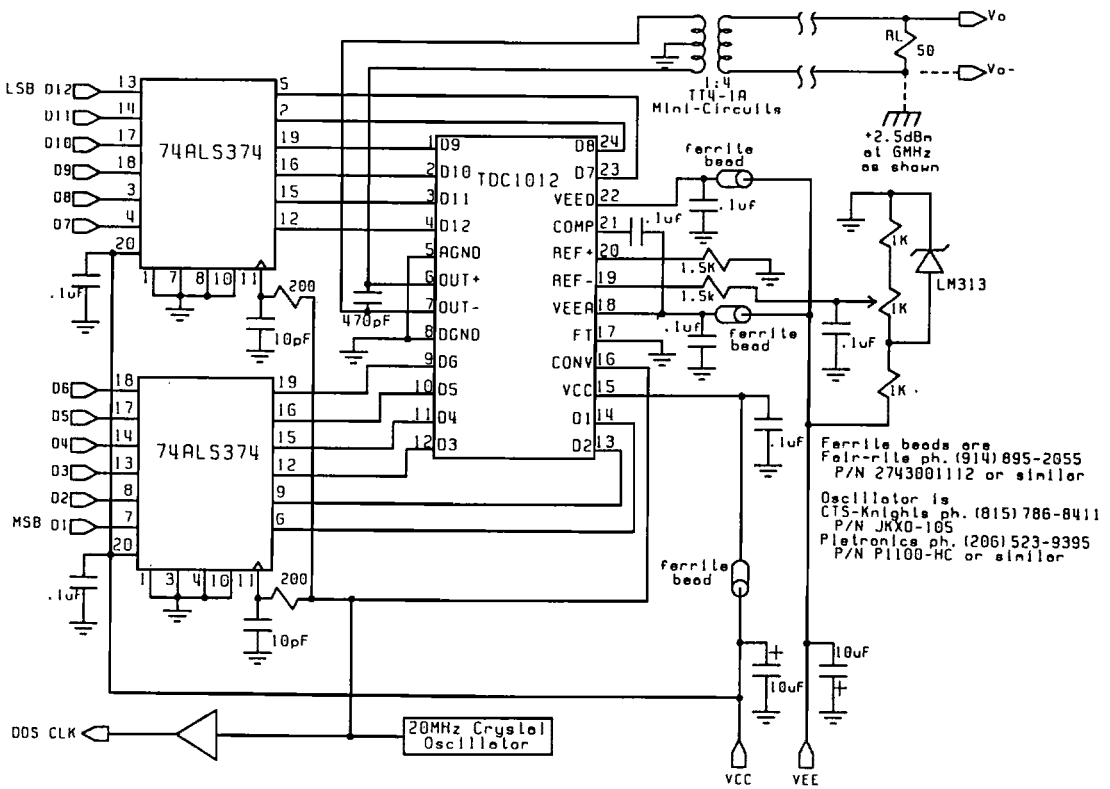
The primary source of 3rd-harmonic distortion is the small non-linear component of output capacitance of the D/A. This can be minimized by reducing the amplitude of the output voltage swing, e.g. with the 1:4 impedance ratio balun as shown in Figure 10. The center tap of the balun can be tied to a positive voltage generated by two diodes in series to ground. This will improve the 3rd-

harmonic distortion by around 2dB at the expense of the power dissipated by the diode biasing circuit. The D/A output voltage excursions should be limited to less than +1.2V.

The true harmonic distortion of these circuits can be masked by the spectrum analyzer under certain conditions. In particular, the circuit of Figure 10 generates a relatively high output power which can cause distortion in the internal circuitry of some spectrum analyzers. This can be avoided by setting the input attenuation to a higher level, typically 40dB.

The TDC1012 and TDC1112 D/A converters and TMC2340 Direct Digital Frequency Synthesizer make high-performance digital frequency synthesis cost-effective in applications requiring stability, spectral purity, and versatility.

Figure 8. The TDC1012 In a DDS Application



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1012N7CX	T_A=0°C to 70°C	Commercial	Plastic DIP	1012N7C-X
TDC1012J7CX	T_A=0°C to 70°C	Commercial	Ceramic DIP	1012J7C-X
TDC1012J7VX	T_C=–55°C to 125°C	MIL-STD-883	Ceramic DIP	1012J7V-X
TDC1012R3CX	T_A=0°C to 70°C	Commercial	Plastic Chip Carrier	1012R3C-X
TDC1012C3VX	T_C–55°C to 125°C	MIL-STD-883	Ceramic Chip Carrier	1012C3V-X

Linearity Grade (X)		None	1	2	3
E_{LD}	Linearity Error, Differential	±0.096% (4 LSB)	±0.048% (2 LSB)	±0.024% (1 LSB)	±0.012% (1/2 LSB)
E_{LI}	Linearity Error, Integral	±0.096% (4 LSB)	±0.048% (2 LSB)	±0.048% (2 LSB)	±0.024% (1 LSB)

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