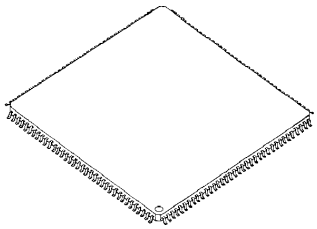
PRELIMINARY

MPEG-2 IMAGE PROCESSOR

■ GENERAL DESCRIPTION

The **NJU28001** is MPEG-2/DVD video decoding IC. It de-multiplexes MPEG-2 as well as DVD system (program) streams and holds them in its external DRAM. It decodes MPEG-2 compressed video and outputs digital video (in NTSC or PAL format) along with sub picture data while retrieving navigation data. In addition to these basic MPEG-2/DVD de-multiplexing and decoding functions, the **NJU28001** also supports a number of advanced features for the next generation products. It includes VBR operation, time stamp processing (for synchronization), error concealment and FF/FR modes. Since MPEG-2 and DVD are widely used in digital video application, the **NJU28001** forms a central core in decoder systems such as DVD player, digital TV, STB, computer multimedia system, etc.

■ PACKAGE OUTLINE

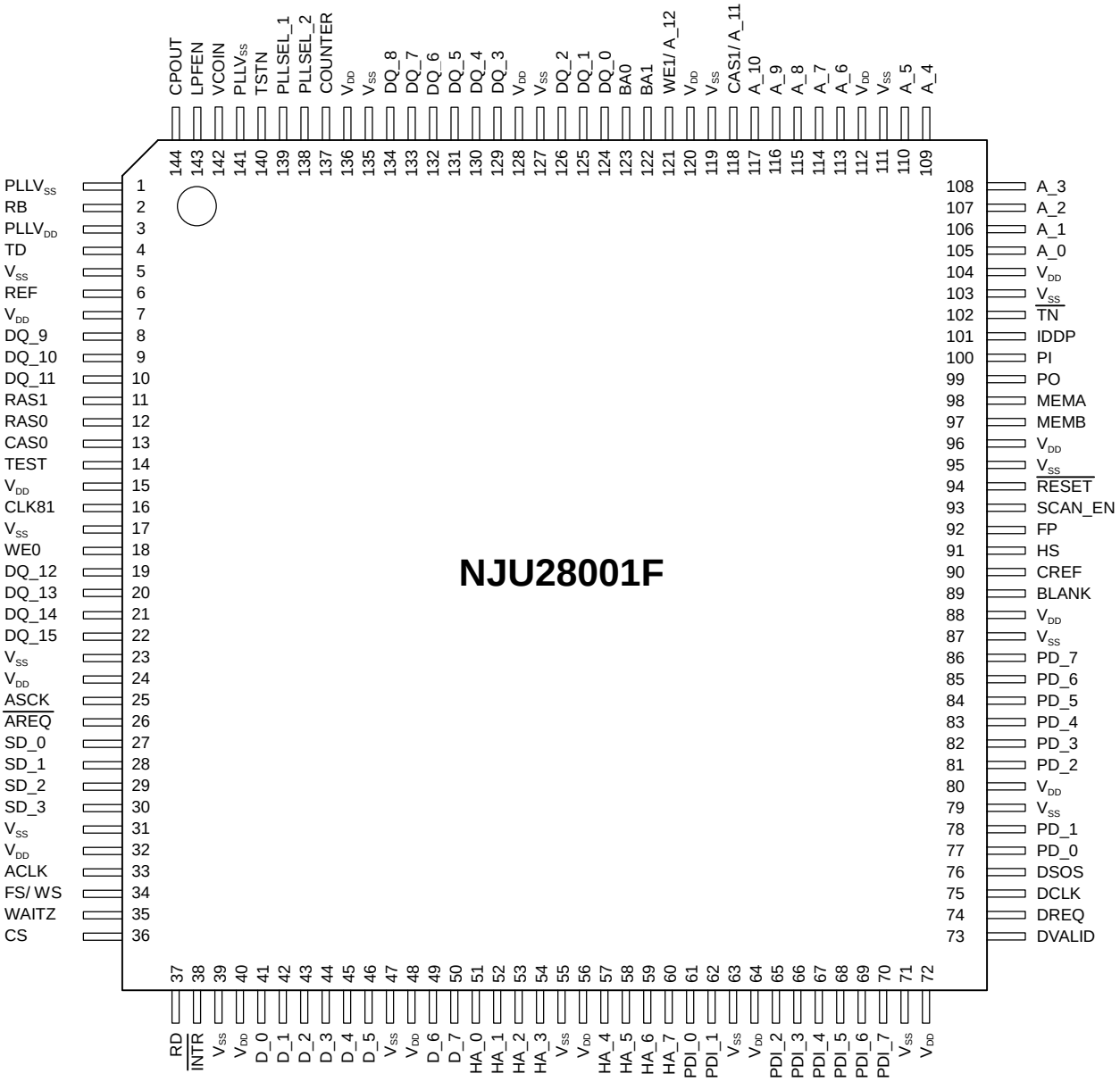


NJU28001F

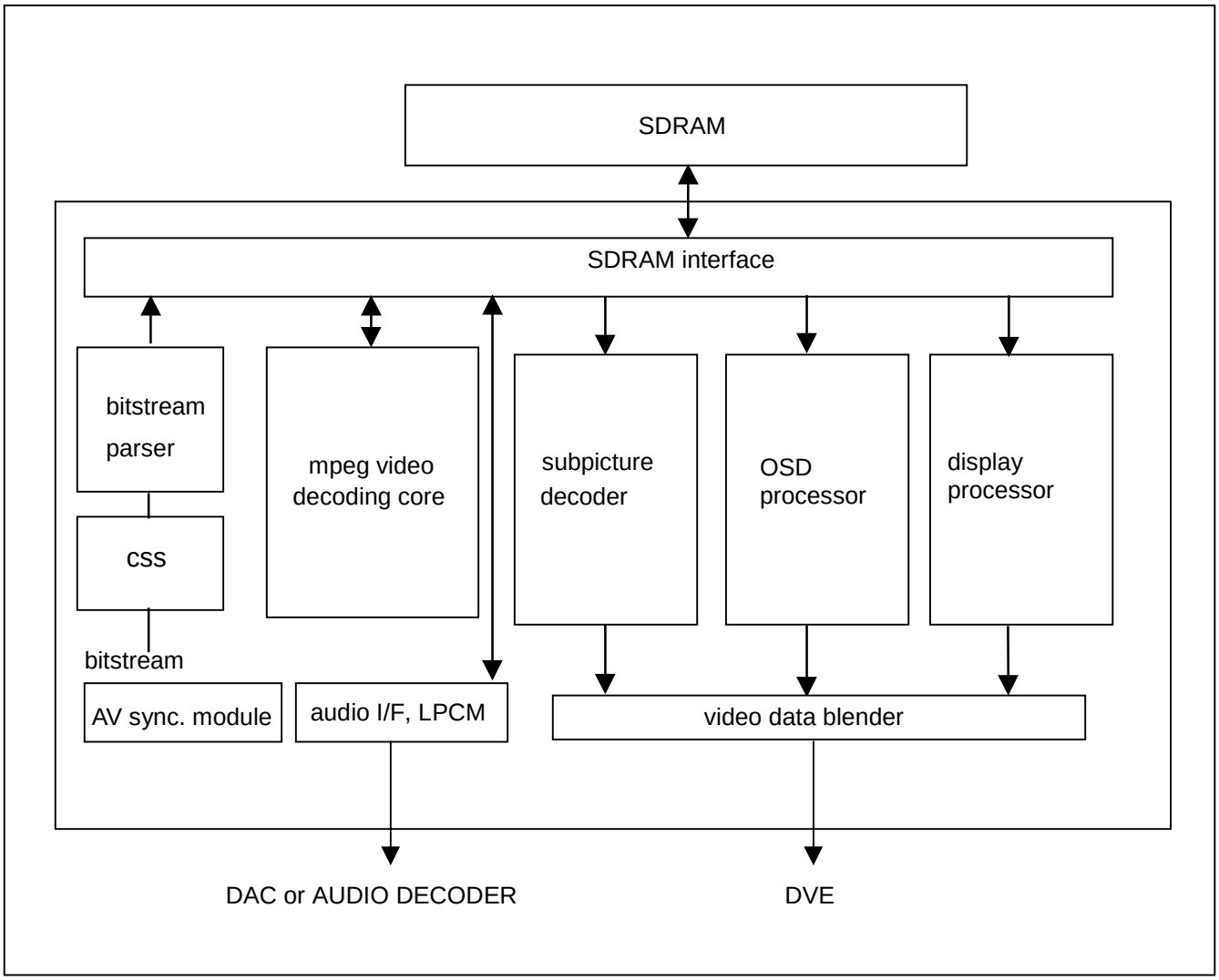
■ FEATURES

- Single 3.3V power supply
- Single 27MHz input clock
- Bit Stream Processor
  - ISO13818-1 MPEG-2 program stream de-multiplexing
  - ISO11172-1 MPEG-1 system stream de-multiplexing
  - Supports DVD program stream de-multiplexing including private_stream_1
  - Supports VBR operation
  - Supports CSS
- Audio Decoding
  - 16bit Linear PCM decoding
  - Extraction of audio data in PES layer or elementary layer
- Video Decoder
  - Decodes ISO13818-2 MPEG-2 (MP@ML)
  - Decodes ISO11172-2 MPEG-1 constrained parameter video stream
  - Supports Fast FW, Fast Reverse, skip/repeat frame, freeze in field/frame and slow FW
- Video Display Controller
  - Outputs digital video in NTSC or PAL format
  - Built-in OSD, Caption and Subpicture decoder
- C-MOS technology
- Package outline QFP144

■ PIN CONFIGURATION



■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION 1

NO	SYMBOLS	INPUT/OUTPUT	FUNCTION
35	WAITZ	OUTPUT	This signal indicates busy. When the output is low, it indicates the readiness of data while the host attempts to read it.
60 59 58 57 54 53 52 51	HA_7 (MSB) HA_6 HA_5 HA_4 HA_3 HA_2 HA_1 HA_0 (LSB)	INPUT	MPU data, address input
50 49 46 45 44 43 42 41	D_7 (MSB) D_6 D_5 D_4 D_3 D_2 D_1 D_0 (LSB)	INPUT/OUTPUT	MPU data, parallel input/output
36	CS	INPUT	Chip select
37	RD	INPUT	Read/Write strobe
38	$\overline{\text{INTR}}$	OUTPUT	INTERRUPT
74	DREQ	OUTPUT	It output becomes high when any of the following conditions happen: [1] the on-chip channel buffer fifo is full ,[2] the DRAM channel is full, this signal is de-asserted.
73	DVALID	INPUT	DVALID is an input pin that takes a signal which defines the validity of incoming coded data(on PDI_7 to PDI_0) at the rising of the DCLK pin input signal. The polarity of the input signal is programmable.
75	DCLK	INPUT	Channel Data Clock Input
76	DSOS	INPUT	DSOS is an input pin that takes a signal which indicates the start of the sector.
70 69 68 67 66 65 62 61	PDI_7 (MSB) PDI_6 PDI_5 PDI_4 PDI_3 PDI_2 PDI_1 PDI_0 (LSB)	INPUT	Channel Decode data input

■ TERMINAL DESCRIPTION 2

NO	SYMBOL	INPUT/OUTPUT	FUNCTION
22 21 20 19 10 9 8 134 133 132 131 130 129 126 125 124	DQ_15 (MSB) DQ_14 DQ_13 DQ_12 DQ_11 DQ_10 DQ_9 DQ_8 DQ_7 DQ_6 DQ_5 DQ_4 DQ_3 DQ_2 DQ_1 DQ_0 (LSB)	INPUT/OUTPUT	SDRAM data input / output
117 116 115 114 113 110 109 108 107 106 105	A_10 (MSB) A_9 A_8 A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0 (LSB)	OUTPUT	SDRAM address data
16	CLK81	OUTPUT	SDRAM clock data output
123	BA0	OUTPUT	SDRAM setting data for BANK0
12	RAS0	OUTPUT	RAS0
13	CAS0	OUTPUT	CAS0
18	WE0	OUTPUT	WE0
122	BA1	OUTPUT	SDRAM setting data for BANK1
11	RAS1	OUTPUT	RAS1
118	CAS1/A_11	OUTPUT	This is the drive CAS1 (or A_11) pin on SDRAM chip # 1 in 16 Mbit x 2 configuration. In 64 Mbit-2BANK and 64Mbit-4BANK configuration s, this pin serves as A11 of SDRAM chip.
121	WE1/A_12	OUTPUT	This is the drive WE1(or A_12) pin on SDRAM chip #1 in 16 Mbit x 2 configuration In 64 Mbit-2BANK configuration, this pin serves as A12 of SDRAM chip.
86 85 84 83 82 81 78 77	PD_7 (MSB) PD_6 PD_5 PD_4 PD_3 PD_2 PD_1 PD_0 (LSB)	OUTPUT	Digital Video Encoder data

■ TERMINAL DESCRIPTION 3

NO	SYMBOL	INPUT/OUTPUT	FUNCTION
89	BLANK	OUTPUT	The BLANK pin output signal becomes high during the video blanking period.
90	CREF	OUTPUT	The CREF pin output becomes high when Cb data is on PD7 to PD_0 pins. Else it outputs low when Cr data is on PD7 to PD_0.
91	HS	INPUT	HS is an input pin which takes horizontal sync from DVE.
92	FS	INPUT	The FP pin takes the Field Parity signal from a DVE.
30 29 28 27	SD_3 SD_2 SD_1 SD_0	OUTPUT OUTPUT OUTPUT OUTPUT	Audio data.
34	FS/WS	OUTPUT	The FS/FW pin outputs frame sync or word sync signal to the device which receives audio data.
25	ASCK	INPUT	Audio data input clock.
26	$\overline{\text{AREQ}}$	INPUT	The AREQ pin takes an audio data request signal.
33	ACLK	INPUT	Audio data input clock.
94	$\overline{\text{RESET}}$	INPUT	RESET
6	REF	INPUT	System Clock(27MHz)
2	RB	INPUT	The RD is the pin which takes the PLL loopfilter adj bias signal.
3	$PLLV_{DD}$	INPUT	Analog V_{DD} for PLL
1 141	$PLLV_{SS}$	——	Analog V_{SS} for PLL
138 139	PLLSEL_2 PLLSEL_1	INPUT	PLLSEL_2,PLLSEL_1 are pin which takes the PLL mode control signal.
143	LPFEN	INPUT	LPFEN is a pin that takes a signal which enables the low pass filter in PLL.
144	CPOUT	INPUT	CPOUT is charge pump output pin for the external loop filter.
137	COUNTER	OUTPUT	COUNTER PLL counter output signal
142	VCOIN	INPUT	VCOIN is the VCO input pin for the external loop ffilter.
4 15 24 32 40 48 56 64 72 80 88 96 104 112 120 128 136	V_{DD}		This is the power pin : 3.3V

■ TERMINAL DESCRIPTION 4

NO	SYMBOL	INPUT/OUTPUT	FUNCTION
5 17 23 31 39 47 55 63 71 79 87 95 103 111 119 127 135	V_{SS}	——	This is the ground : 0V

■ TERMINAL DESCRIPTION 5 (NOT USED BY USER)

NO	SYMBOL	INPUT/OUTPUT	FUNCTION
7	TD	INPUT	During the normal mode, this pin must be the ground : 0V.
14	TEST	OUTPUT	During the normal mode, this pin must be “OPEN”.
93	SCAN_EN	INPUT	During the normal mode, this pin must be the ground : 0V.
97	MEMB	INPUT	
98	MEMA	INPUT	
99	PO	OUTPUT	During the normal mode, this pin must be “OPEN”.
100	PI	INPUT	During the normal mode, this pin must be the ground : 0V.
101	IDDP	INPUT	During the normal mode, this pin must be V_{DD} : 3.3V.
102	$\overline{TN}$	INPUT	
140	TSTN	INPUT	During the normal mode, this pin must be the ground : 0V.

■ FUNCTION OVERVIEW

NJU28001 contains ninemain processing modules: CSS processor, Bitstream Paser, SDRAM controller, Video Decoder, OSD Processor, Video Display Processor, Sub Picture Processor, Audio video syncronizer, and audio i/f-LPCM decoder. For its proper operations, each module needs to be programmed by the external μcontroller. The incoming bitstream is fed to CSS modules first. If the bitstream is a DVD stream, DVD authentication process must be achieved between external host system and **NJU28001**. And CSS descrambling must be enabled. Otherwise it shall be set bypass mode. The output of CSS is fed to the bitstream parsing modules where an appropriate packet data are filtered out and sent to the external SDRAM. The mpeg video decoder is in charge of decoding MPEG video stream and reconstructs video image into the area in SDRAM. The sub-picture unit decodes data in subpicture stream and the decode image is send out to DVE after blended with the main decode video data. OSD processor decodes a OSD packet data stored in SDRAM. The display processor is in charge of displaying the decoded video image in SDRAM. It closely communicates the mpeg video decoding core to ensure synchronization of display with the video decoding activities. Also it controls the rest of display related modules: subpicture and OSD. Audio data extracted from the primary input bitstream is pass to the external audio decoder. If the bitstream is the LPCM data, the built in LPCM decoder can unpack it and sends out max 8 channels of LPCM data stream to D/A converters.

(1) SDRAM INTERFACE

NJU28001 can suports four SDRAM configulation: 1x16Mbit, 2x16Mbit, 1 x 64Mbit, 1x 64Mbit(2BANK). For example, a NTSC video decoding system with 16Mbit external SDRAM configulation

(2) Bitstream Processor

The most primitive bitstream is a MPEG video elementary stream. To take this stream, it is required to opening channel 1 path. If an incoming bitstream is MPEG1 system or MPEG2 program stream, the **NJU28001** parses its PES syntax. If stream id options are provided only matching video and/ or audio stream are fed to channel 1 and 2 in SDRAM. In case of the DVD bitstream, video PES packets are fed to channel 1, one of audio stream is fed to channel 2. And subpicture and navigation streams are fed to channel 3 and 4 respectively.

(3) Video Decoding

When enough amount of bitstream is accumulated in the video bitstream data area, decoding operation is issuued by the external controller. Down to the macro block layer, the micro controller processes the decoding operations. A picture is reconstructed by macroblock. Since the decoded image must be displayed, the video decode unit operates synchronuslly to the display processor. While the decoding operation is in progress, **NJU28001** may receive a trick mode command such as freeze display or skip display. When it occurs, depending on the type of each command, the video decoding unit will take a special operation.

(4) Audio bitstram Processing and decoding

NJU28001 contains an audio bitstream interfacing and LPCM decoding processor. When the direct read of the coded audio bitstream is selected by programming parameters, coded data interface module fetches the audio data in DRAM sends it out in **NJU28001**'s serial data format. If LPCM decoding is selected, the bitstream is fetched from SDRAM, decoded and sending out in I^2S or EIAJ format.

(5) System Synchronization

One unique feature of **NJU28001** is automatic of elementary bitstream from a system. It is acheived by VPES unit. The VPES unit extracts PTS time stamp embedded in PES packet header. The extracted PTS information is fed to sync unit which keeps track of PTS value and Picture.

(6) Video Display

NJU28001 operates its display as slave to the external digital video encoder. It receives horizontal sync(HS) and vertical sync(VS) signals. Depending on the type of signal (NTSC or PAL), all parameters must be defined accordingly.

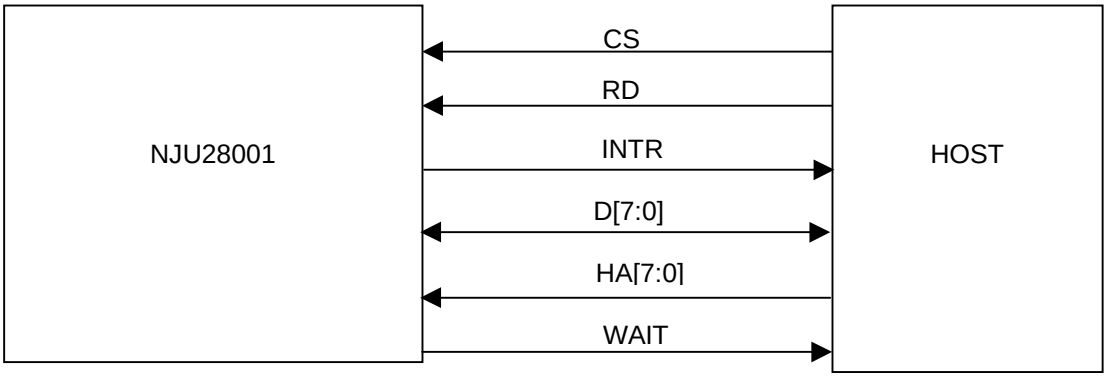
(7) Sub-Picture Data Display

To enable display of Subpicture data host must be bit 4 of reg to HIGH. With SP-palette information coded in PCI of Navigation data, the external HOST can program a color map register table inside SP contrpller otherwise the default values will be used.

■ Hardware Interface

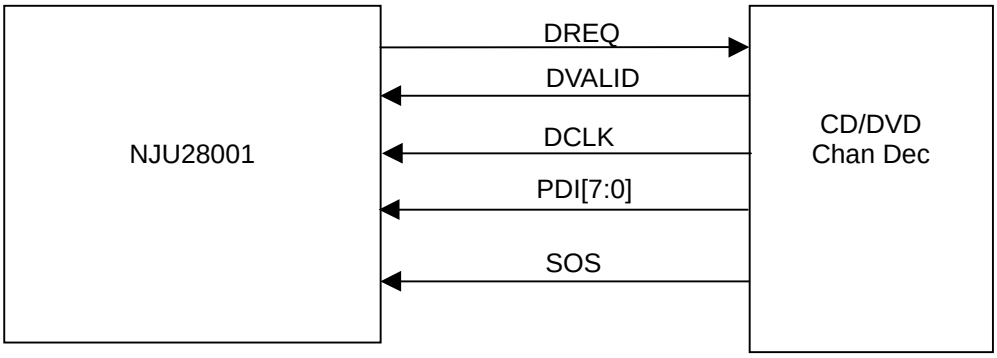
(1) Host Bus Interface

- 8-bit data bus (D7:0)
- 8-bit address bus(HA7:0)
- chip select(CS)
- read/write control(RD)
- interrupt(INTR)
- wait state indication for read cycle(WAIT)



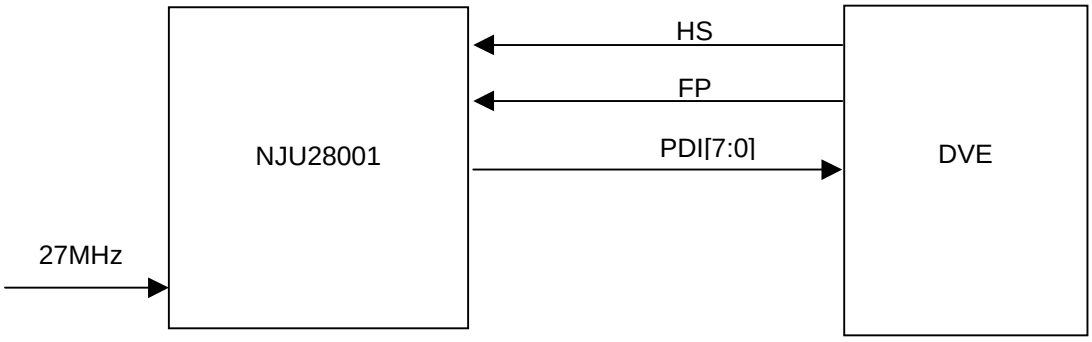
(2) Bitstream Interface

The Bitstream Input Interface is an 8-bit data port with 4 control signals. **NJU28001** support up to 23Mbps channel input rate.



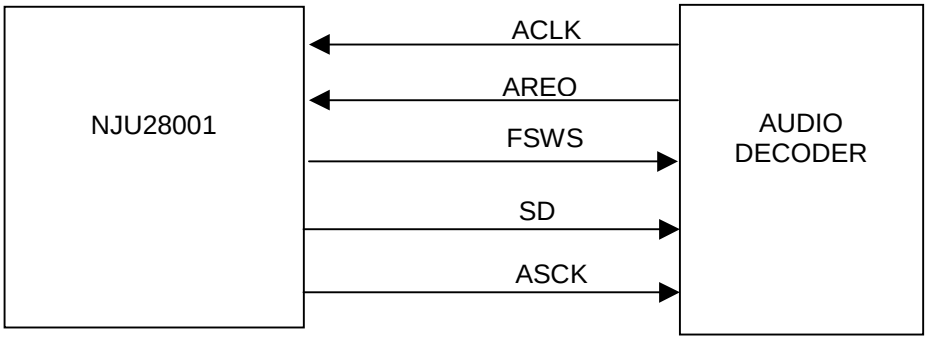
(3) Video Interface

Video Interface has an 8-bit

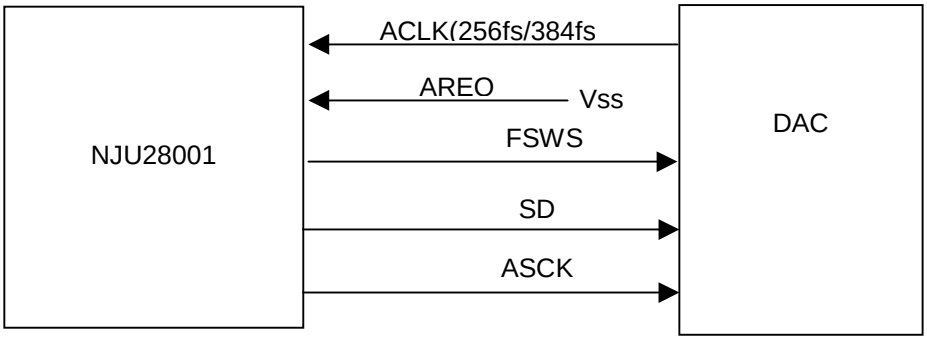


(4) Audio Interface

1. Type 1 : coded data audio interface
2. Type 2 : Linear PCM audio interface



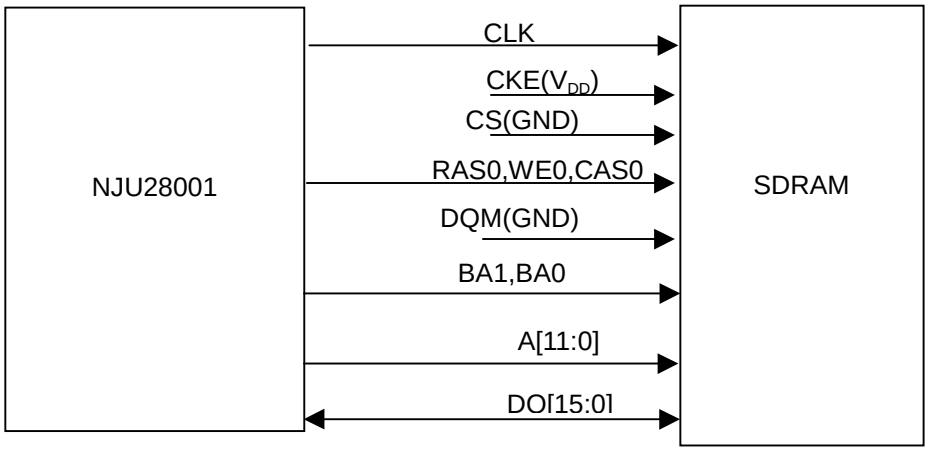
In case of using Audio Decoder



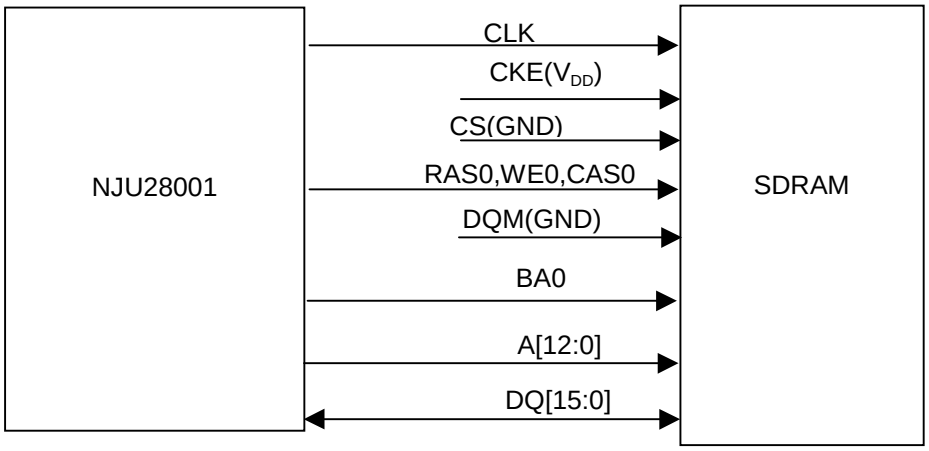
In case of using DAC

(5) SDRAM Interface

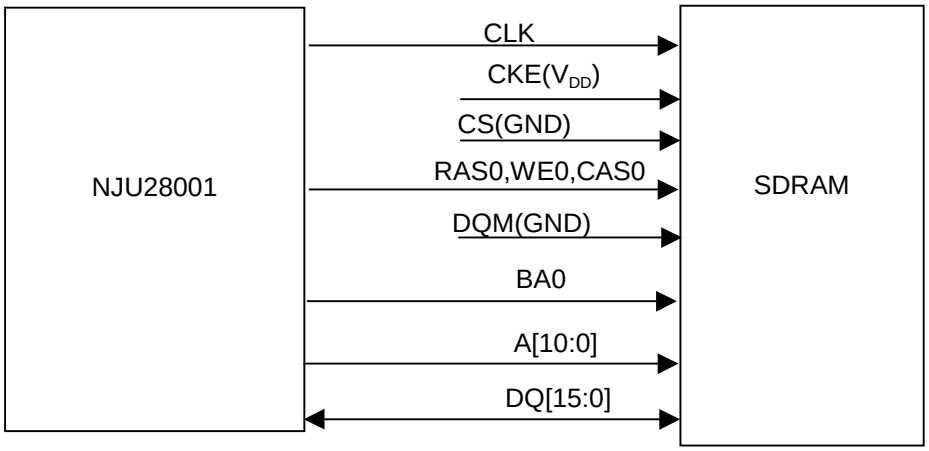
NJU28001 support single 16Mbits SDRAM, double 16Mbits SDRAM and single 64Mbits SDRAM of both 2-bank and 4-bank types.



64MbitDRAM X 1 (4BANKS)



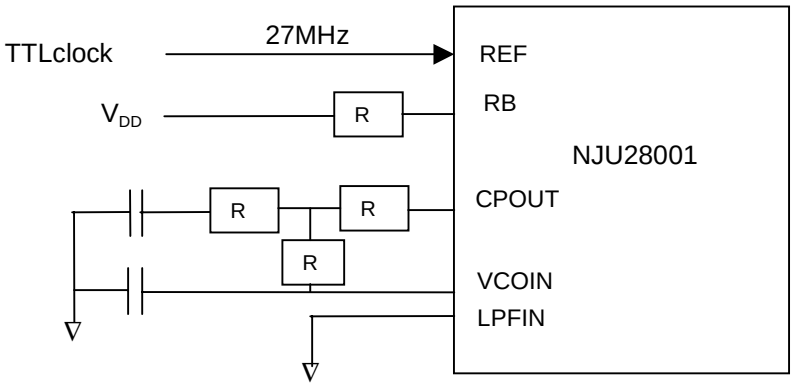
64MbitDRAM X 1(2BANKS)



16Mbit DRAM X 1

(6) PLL Interface

NJU28001 has PLL circuitry to generate an 81MHz SDRAM clock. A loop filter is controlled by the “lpfen” pin. If this pin is low, the internal loop filter is used. In this case “rb” pin should be connected to VDD via a register.



■ Programming Registers

[Control commands (Registers) Table]

Name	Address	R/W	Description	Reset State	Note
Data Chain Registers	00H	R/W	Data Chain Reg[7:0]	00h	
	01H		Data Chain Reg[15:8]	00h	
	02H		Data Chain Reg[23:16]	00h	
	03H		Data Chain Reg[31:24]	00h	
	04H		Data Chain Reg[39:32]	00h	
	05H		Data Chain Reg[47:40]	00h	
	06H		Data Chain Reg[55:48]	00h	
	07H		Data Chain Reg[63:56]	00h	

Name	Address	R/W	Description	Reset State	Note
Code Data Input	08H	R/W	Code Data Input control register	17h	
General Control Registers	09H	W	General Control Register	00h	
Interrupt Registers	0AH	R/W	Interrupt Register 0	00h	
	0BH		Interrupt Register 1	00h	
	0CH		Interrupt Register 2	00h	
Memory programming and S/DRAM access Registers	10H	R/W	Memory Partition Register 0	00h	
	11H		Memory Partition Register 1	00h	
	12H		Memory Partition Register 2	00h	
	13H		Memory Partition Register 3	00h	
	14H		Memory Status Register 1	00h	
	15H		Navigation Data Status Register	00h	
	16H		Memory Data Transfer Register	0000b	
	17H	W	Buffer RAM Write Address Register	0000b	
	18H		Buffer RAM Read Address Register	0000b	
	19H	R/W	Memory Configuration Register	00h	
Bitstream programming Registers	20H	W	CSS command Register	000b	
	21H	R	CSS Status Register	000b	
	22H	W	CSS Data Write Register	00h	
	23H	R	CSS Data Read Register	00h	
	24H	W	Channel Open Control Register	0000b	
	25H	W	Bitstream Selection Register	0100011b	
	26H	W	Video Stream ID Register	0000b	
	27H	W	Audio Stream ID Register	00000b	
	28H	W	Subpicture Stream ID Register	00000b	

Name	Address	R/W	Description	Reset State	Note
AV Synchronization Programming Registers	30H	R/W	Sync Unit control Register	0000000b	
	31H	W	Sync Unit Status 0 Register	00h	
	32H	W	Sync Unit Status 1 Register	000000b	
Video Programming Registers	40H	W	Video Display Control Register 0	0110b	
	41H	W	Video Display Control Register 1	000b	
	42H	W	Video Display Control Register 2	00b	
	43H	W	Video Display Control Register 3	00000b	
	44H	W	Video Display Control Register 4	00h	
	45H	W	Video Display Control Register 5	80h	
	46H	W	Video Display Control Register 6	00h	
	47H	W	Video Display Control Register 7	A8h	
	48H	W	Video Display Control Register 8	00h	
	49H	W	Video Display Control Register 9	00h	
	4AH	W	Video Display Control Register A	00h	
	4BH	W	Trick Mode Command Register 1	00h	
	4CH	W	Trick Mode Command Register 2	00h	
	4DH	W	Trick Mode Command Register 3	00h	
	4EH	R/W	Subpicture Status Register 1	00h	
	4FH	W	Subpicture Status Register 2	00b	
Audio Programming Registers	50H	W	Audio Stream Processor Register 1	4Ah	
	51H	W	Audio Stream Processor Register 2	0000b	
	52H	R	Audio Stream Processor Register 3	20h	
Debugging Registers	60H	W	VPES Debugging Register	T.B.D	
	61H	R/W	APES Debugging Register 1	23h	
	62H	W	APES Debugging Register 2	000b	
	63H	R	NBIT Status Register	--	
	64H	R/W	UC Debugging Register	00h	
	65H	W	Display Debugging Register	00h	
	66H	W	Module Reset Register	00h	
	67H	W	Module Reset Register	000b	
	68H	W	uC Debugging Register	0b	
	69H	W	SDC Debugging Register 1	00000b	

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.3 to +3.6	V
Input Voltage	V_{IN}	-0.3 to +3.6	V
Output Voltage	V_{OUT}	-0.3 to +3.6	V
Operating Temperature	T_{opr}	-20 to +75	°C
Storage Temperature	T_{stg}	-55 to +120	°C

■ DC CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Supply Voltage	V_{DD}	V_{DD}	3.15		3.45	V
Supply Current	I_{DD}	V_{DD}, V_{DD}=3.45V, f_{OSC}=27MHz			350	mA
High-Level Input Voltage	V_{IH}		2.0		V_{DD}	V
High-Level Output Voltage	V_{OH}	I_{OH}=-0.4mA	2.4			V
Low-Level Output Voltage	V_{OL}	I_{OL}=2mA			0.4	V