

## 128M-BIT MASK ROM (16/32 BIT OUTPUT)

### FEATURES

- Bit organization
  - 8M x 16 (byte mode)
  - 4M x 32 (double word mode)
- Fast access time (for VCC=3.3V±5%)
  - Random access: 100ns (max.)
  - Page access: 30ns (max.)
- Fast access time (for VCC=3.3V±10%)
  - Random access: 120ns (max.)
  - Page access: 50ns (max.)
- Page Size
  - 8 double words per page
- Current
  - Operating: 60mA (max.)
  - Standby: 5uA (max.)
- Supply voltage
  - 3.3V±10%
- Package
  - 70 pin SSOP (500 mil)
  - 86 pin TSOP(2)



### PIN CONFIGURATION

#### 70 SSOP

A0	0	70	NC
A1	2	69	A21
A2	3	68	A20
A3	4	67	WORD
A4	5	66	OE
A5	6	65	CE
VCC	7	64	VSS
D0	8	63	D31/A-1
D16	9	62	D15
D1	10	61	D30
D17	11	60	D14
VSS	12	59	VSS
VCC	13	58	VCC
D2	14	57	D29
D18	15	56	D13
D3	16	55	D28
D19	17	54	D12
D4	18	53	D27
D20	19	52	D11
D5	20	51	D26
D21	21	50	D10
VSS	22	49	VSS
VCC	23	48	VCC
D6	24	47	D25
D22	25	46	D9
D7	26	45	D24
D23	27	44	D8
VSS	28	43	VCC
A6	29	42	A19
A7	30	41	A18
A8	31	40	A17
A9	32	39	A16
A10	33	38	A15
A11	34	37	A14
A12	35	36	A13

#### 86 TSOP

NC	0	86	NC
A0	2	85	NC
A1	3	84	NC
A2	4	83	A21
A3	5	82	A20
A4	6	81	WORD
A5	7	80	OE
NC	8	79	CE
NC	9	78	NC
VCC	10	77	VSS
D0	11	76	NC
D16	12	75	D31
D1	13	74	D15
D17	14	73	D30
VSS	15	72	D14
VCC	16	71	VSS
D2	17	70	VCC
D18	18	69	D29
D3	19	68	D13
D19	20	67	D28
NC	21	66	D12
NC	22	65	NC
D4	23	64	D27
D20	24	63	D11
D5	25	62	D26
D21	26	61	D10
VSS	27	60	VSS
VCC	28	59	VCC
D6	29	58	D25
D22	30	57	D9
D7	31	56	D24
D23	32	55	D8
VSS	33	54	VCC
A6	34	53	A19
A7	35	52	A18
A8	36	51	A17
A9	37	50	A16
A10	38	49	A15
A11	39	48	A14
A12	40	47	NC
A13	41	46	NC
NC	42	45	NC
NC	43	44	NC

**ORDER INFORMATION**

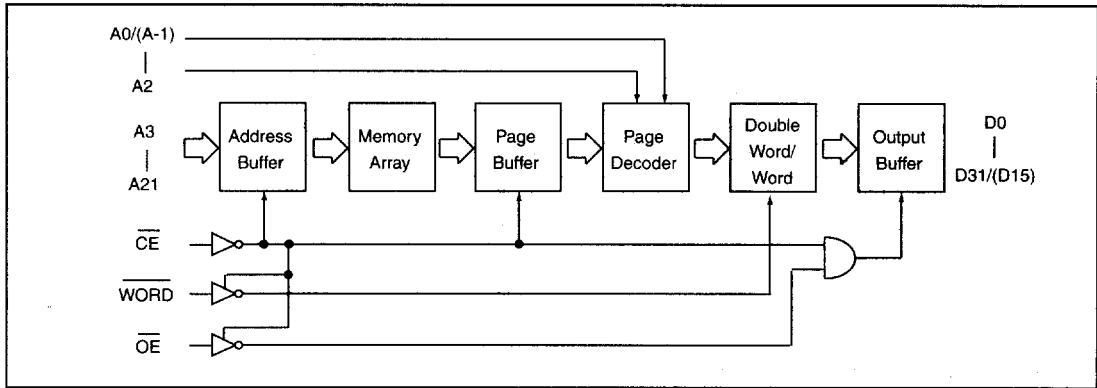
Part No.	Access Time	Page Access Time	Package
MX23L12822MC-10	100ns	30ns	70 pin SSOP
MX23L12822MC-12	120ns	50ns	70 pin SSOP
MX23L12822YC-10	100ns	30ns	86 pin TSOP
MX23L12822YC-12	120ns	50ns	86 pin TSOP

**PIN DESCRIPTION**

Symbol	Pin Function
A0~A21	Address Inputs
D0~D30	Data Outputs
D31/A-1	D31 (Double Word Mode)/ LSB Address (Word Mode)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
Word	Double Word/ Word Mode Selection
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

**MODE SELECTION**

$\overline{CE}$	$\overline{OE}$	Word	D31/A-1	D0~D15	D16~D31	Mode	Power
H	X	X	X	High Z	High Z	-	Stand-by
L	H	X	X	High Z	High Z	-	Active
L	L	H	Output	D0~D15	D16~D31	Double Word	Active
L	L	L	Input	D0~D15	High Z	Word	Active

**BLOCK DIAGRAM**

**2**
**ABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VIN	-1.3V to 2.0V
Ambient Operating Temperature	Topr	0°C to 70°C
Storage Temperature	Tstg	-65°C to 125°C

Note: Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may undershoot VSS to -1.3V for periods of up to 20ns. Maximum DC voltage on input or I/O pins is VCC+0.5V. During voltage transitions, input may overshoot VCC to VCC+2.0V for periods of up to 20ns.

**DC CHARACTERISTICS** (Ta = 0°C ~ 70°C, VCC = 3.3V±10%)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -0.4mA
Output Low Voltage	VOL	-	0.4V	IOL = 1.6mA
Input High Voltage	VIH	2.2V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.8V	
Input Leakage Current	ILI	-	5uA	0V, VCC
Output Leakage Current	ILO	-	5uA	0V, VCC
Operating Current	ICC1	-	60mA	tRC = 120ns, all output open, with normal sequential access testing pattern
Standby Current (TTL)	ISTB1	-	1mA	CE = VIH
Standby Current (CMOS)	ISTB2	-	5uA	CE > VCC-0.2V
Input Capacitance	CIN	-	10pF	Ta = 25°C, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25°C, f = 1MHZ

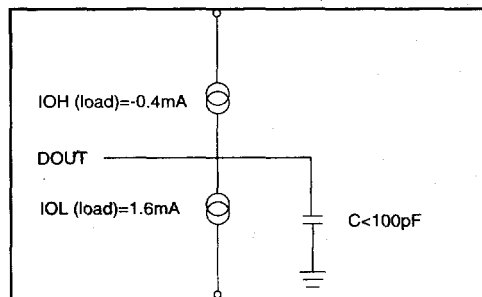
**AC CHARACTERISTICS** ( $T_a = 0^\circ\text{C} \sim 70^\circ\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 10\%$ )

Item	Symbol	23L12822-10		23L12822-12	
		MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	100ns	-	120ns	-
Address Access Time	tAA	-	100ns	-	120ns
Chip Enable Access Time	tACE	-	100ns	-	120ns
Page Mode Access Time	tPA	-	30ns	-	50ns
Output Enable Time	tOE	-	30ns	-	50ns
Output Hold After Address	tOH	0ns	-	0ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns

Note: Output high-impedance delay (tHZ) is measured from  $\overline{OE}$  or  $\overline{CE}$  going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

**AC Test Conditions**

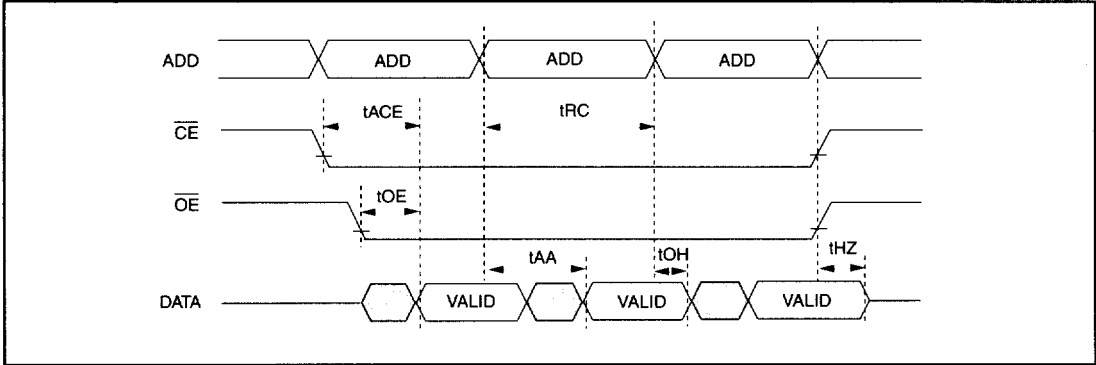
Input Pulse Levels	0.4V~2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.4V
Output Timing Level	1.4V
Output Load	See Figure



Note: No output loading is present in tester load board.

Active loading is used and under software programming control.

Output loading capacitance includes load board's and all stray capacitance.

**TIMING DIAGRAM**
**RANDOM READ**

**2**
**PAGE READ**
