SHARP

NEW PRODUCT INFORMATION

LZ98 Series

Channel-free Gate Array (Sea-of-gate)

Description

The LZ98 series is a channel-free gate array fabricated using silicon gate CMOS process technology.

It is developed to meet user's requirements such as large scale, high speed, high performance and multi-I/O function, which are suitable to consumer appliances to industrial equipment.

Furthermore, Sharp offers powerful lineup of cell libraries compatible with those of the LZ93, LZ95 series, which allow each series to be replaced by the LZ98 series.

Features

1. CMOS process
2. Sea-of-gate structure
3. Total gate count: 8000, 9000, 11000, 12000, 13000, 16000, 17000, 23000, 24000, 30000
4. Delay time: 0.6ns/gate (F.O. = 3, l = 1mm)
5. Output current: 12mA
6. Supply voltage: 2.0 to 5.5V
7. Usable gate count: 50%
8. I/O buffers of multi-I/O series

LZ989000	128
LZ9811000	136
LZ9813000	142
LZ9817000	156
LZ9823000	184

Packages

Series	Model No.	DIP					SDIP		QFP									SOP	CPGA			QFJ
		24	28	32	40	48	42	64	44	48	60	64	80 ▭	80 □	96	100	128	160	28	120	144	180	44
Normal Series	LZ988000	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●			●				●
	LZ9812000	●			●	●		●	●		●	●	●	●	●	●	●						
	LZ9816000	●			●			●			●		●	●	●	●	●	●				●	
	LZ9824000				●			●						●	●	○	●	●		●	●	●	
	LZ9830000				●									●	●	○	●	●		●	●	●	
Multi-I/O Series	LZ989000	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	○	●	●				●
	LZ9811000	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	○	●	●				●
	LZ9813000	●	●		●	●		●	●	●	●	●	●	●	●	○	●	●					
	LZ9817000	●	●		●			●			●	●	●	●	●	●	●					●	
	LZ9823000				●			●						●	●	●	●	●		●	●	●	

○:Under development

LZ98 Series Channel-free Gate Array (Sea-of-gate)

Electrical Characteristics

Parameter	Symbol	Conditions	TTL level			CMOS level			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input LOW voltage	V_{IL}				0.8			1.5	V
Input HIGH voltage	V_{IH}		2.0			3.5			V
Input HIGH threshold voltage	V_T^+	Schmitt input buffer			2.2			3.7	V
Input LOW threshold voltage	V_T^-	Schmitt input buffer	0.5			1.0			V
Hysteresis voltage	$V_T^+ - V_T^-$	Schmitt input buffer	0.2			0.4			V
Output LOW voltage	V_{OL}	I_{OL} = 1,2,4,6,8,12mA			0.4			0.4	V
Output HIGH voltage	V_{OH}	I_{OH} = −0.5, −1, −2, −3, −4, −6mA	4.0			4.0			V
Input leakage current	I_i	V_I = 0V - V_{CC}	−1.0		1.0	−1.0		1.0	μA
Output leakage current	I_{OZ}	Output high impedance	−1.0		1.0	−1.0		1.0	μA
Input LOW current	$\lvert I_{OL} \rvert$	Vi = 0V	8	20	60	8	20	60	μA
Input HIGH current	I_{OH}	Vi = V_{CC}	8	20	60	8	20	60	μA

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	-0.3 to 6.0	V
Input voltage	V_I	−0.3 to V_{CC} + 0.3	V
Output voltage	V_O	−0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	−40 to +85	°C
Storage temperature	Tstg	−55 to +150	°C

Recommended Operating Conditions

Parameter	Symbol	TTL level			CMOS level			Unit
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply voltage	V_{CC}	4.75	5	5.25	4.5	5	5.5	V
Operating temperature	Topr	−40		+85	−40		+85	°C

Macro Cells

(1) Internal standard macro cells

Name	Function	No. of gates
Inverters, non-inverters		
INV1	Single drive inverter	1
INV2	Double drive inverter	1
INV3	Tripple drive inverter	2
INV4	Quad drive inverter	2
INV6	6 times drive inverter	3
INV1P	Single drive inverter Pch Tr. PARA.	1
INV2P	Double drive inverter Pch Tr. PARA.	2
INV4P	Quad drive inverter Pch Tr. PARA.	4
NIN1	Single drive non-inverter	1
NIN2	Double drive non-inverter	2
NIN3	Tripple drive non-inverter	2
NIN4	Quad drive non-inverter	3
Internal bus buffers, delay elements		
CINV	High active clocked inverter (Half drive internal bus buffer)	2
CXINV	Low active clocked inverter (Half drive internal bus buffer)	2
INTB1	Single drive internal bus buffer	3
INTB2	Double drive internal bus buffer	4
INTB4	Quad drive internal bus buffer	5
DLY10	About 10nsec delay	12
DLY20	About 20nsec delay	24
DLY40	About 40nsec delay	48
NAND/NOR gates		
NA2	2-input NAND gate	1
NA3	3-input NAND gate	2
NA4	4-input NAND gate	2
NA5	5-input NAND gate	4
NA6	6-input NAND gate	5
NA7	7-input NAND gate	5
NA8	8-input NAND gate	6
NA2P	2-input POWER NAND gate	2
NA3P	3-input POWER NAND gate	3
NA4P	4-input POWER NAND gate	4
NO2	2-input NOR gate	1
NO3	3-input NOR gate	2
NO4	4-input NOR gate	2
NO5	5-input NOR gate	4
NO6	6-input NOR gate	5
NO7	7-input NOR gate	5
NO8	8-input NOR gate	6
NO2P	2-input POWER NOR gate	2
NO3P	3-input POWER NOR gate	3
NO4P	4-input POWER NOR gate	4
AND/OR/EX-NOR gates		
AN2	2-input AND gate	2
AN3	3-input AND gate	2
AN4	4-input AND gate	3
OR2	2-input OR gate	2
OR3	3-input OR gate	2
OR4	4-input OR gate	3

Name	Function	No. of gates
AND/OR/EX-NOR gates		
EXO	2-input EXCLUSIVE OR	3
EXN	2-input EXCLUSIVE NOR	3
Combined logic circuits, combined gate circuits		
ON1	2,1 input OR-NAND gate	2
DN1	2,1 input AND-NOR gate	2
DN22	2×2 input AND-NOR gate	2
OA1	2,1 input OR-AND gate	2
OA22	2×2 input OR-AND gate	3
AO1	2,1 input AND-OR gate	2
AO22	2×2 input AND-OR gate	3
AO23	2×3 input AND-OR gate	4
AO24	2×4 input AND-OR gate	5
AO25	2×5 input AND-OR gate	6
AO26	2×6 input AND-OR gate	7
AO32	3×2 input AND-OR gate	4
AO33	3×3 input AND-OR gate	5
AO34	3×4 input AND-OR gate	7
AO42	4×2 input AND-OR gate	5
AO43	4×3 input AND-OR gate	7
AO52	5×2 input AND-OR gate	7
AON	2,1,1 input AND-OR-NAND gate	2
OAN	2,1,1 input OR-AND-NOR gate	2
DS	2 to 1 data selector	3
DSN	2 to 1 inverting data selector	3
ADDH	Half adder	4
ADDF	Full adder	7
Latch, flip-flop cells		
DLT	D latch	4
DLTR	D latch with reset	5
D	D flip-flop	6
DR	D flip-flop with reset	8
DRS	D flip-flop with reset & set	10
DRS4	D flip-flop with reset & set	8
DAL3	D flip-flop with asynchronous load	10
TR	T flip-flop with reset	10
JK	JK flip-flop	9
JKRS	JK flip-flop with reset & set	12
Flip-flop cells for ATPG		
SD	D flip-flop for ATPG	Not fixed
SDR	D flip-flop with reset for ATPG	
SDRS	D flip-flop with reset & set for ATPG	
SDRS4	D flip-flop with reset & set for ATPG	
SDAL3	D flip-flop with asynchronous load for ATPG	
STR	T flip-flop with reset for ATPG	
SJK	JK flip-flop for ATPG	
SJKRS	JK flip-flop with reset & set for ATPG	

I/O Buffer Cells

(1) Standard I/O cells (Cells with pull-up/pull-down register are also available.)

Name	Function	No. of internal gates
Special input cells		
IBF	TTL level input buffer	1
IBFC	CMOS level input buffer	1
IBFS	TTL level schmitt-trigger input buffer	1
IBFCS	CMOS level schmitt-trigger input buffer	1
Special output cells		
OBF	Output buffer I_{OL} = 4mA (I_{OH} = – 2mA)	0
OBF1M	Output buffer I_{OL} = 1mA (I_{OH} = – 0.5mA)	0
OBF2M	Output buffer I_{OL} = 2mA (I_{OH} = – 1mA)	0
OBF6M	Output buffer I_{OL} = 6mA (I_{OH} = – 3mA)	0
OBF8M	Output buffer I_{OL} = 8mA (I_{OH} = – 4mA)	0
OBF12M	Output buffer I_{OL} = 12mA (I_{OH} = – 6mA)	0
OBFH	Output buffer I_{OL} = 4mA (I_{OH} = – 2mA, high speed version)	0
TOBF (4mA)	Output buffer I_{OL} = 4mA (I_{OH} = – 2mA, 3-state output)	0
OBFN (4mA)	Output buffer I_{OL} = 4mA (Nch open drain output)	0
OBFP (2mA)	Output buffer I_{OH} = 2mA (Pch open drain output)	0
Common I/O cell		
IOBF (4mA)	TTL level input and I_{OL} = 4mA (I_{OH} = 2mA) output buffer	1
IOBFC (4mA)	CMOS level input and I_{OL} = 4mA (I_{OH} = 2mA) output buffer	1
Special I/O cells		
OSC	Oscillator with IBF0 (Drive factor 4)	1
OSC1M	Oscillator with IBF0 (Drive factor 1)	1
OSC2M	Oscillator with IBF0 (Drive factor 2)	1
OSCL	Low power oscillator (with IBF0)	1
ASW	Analog switch (with OBF0)	0
OBF0	Analog switch (with ASW)	0
IBF0	Oscillator with OSC, OSC1M, OSC2M, or OSCL	0
XIBFC5	5 times drive inverting input buffer	0
XOBF1M	3 PAD C-R oscillator with IBFCS and OSC	0
NABF	Amplifier NAND input buffer with OBFC0	0
IOBF0C	Amplifier with NABF	1
BINV5	5 times drive inverter ON I/O cell	0

LZ98 Series Lineup

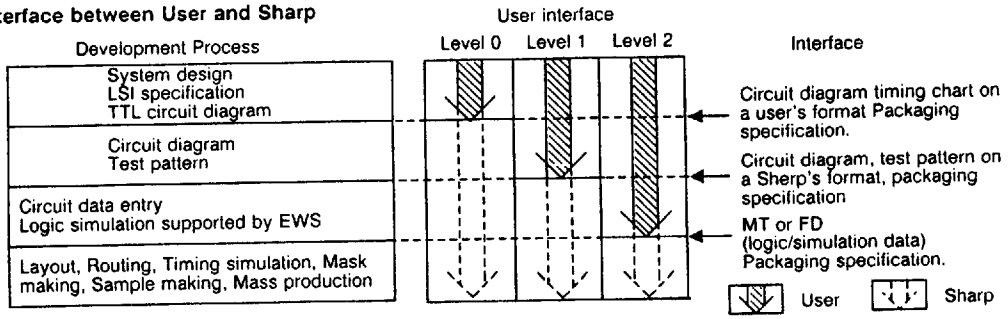
Model No.		LZ988000	LZ989000	LZ9811000	LZ9812000	LZ9813000	LZ9816000	LZ9817000	LZ9823000	LZ9824000	LZ9830000
Total gate count		8000	9000	11000	12000	13000	16000	17000	23000	24000	30000
Usable gate count		4000	4500	5500	6000	6500	8000	8500	11500	12000	15000
I/O buffers		96	128	136	116	142	130	156	184	158	178
Process		1 μm CMOS, double metal									
Delay time	Internal gate	0.6ns									
	Input buffer	2.2ns									
	Output buffer	2.7ns									
I/O level		TTL/CMOS									
Supply voltage		5V ± 5% (TTL interface)/5V ± 10% (CMOS interface)									

NEW PRODUCT INFORMATION

LZ98 Series Channel-free Gate Array (Sea-of-gate)

Support System

•Interface between User and Sharp



Support Tools for LZ98 series

SHARP will make a design support of user's development tools for the CAD interface at level 2.

User's development tool		Data to be submitted by SHARP
EWS	MENTOR	Basic cell library (95 cells) Macro cell library equivalent to TTL74 (140 cells)
	DAZIX	Basic cell library (95 cells)
	HP	Basic cell library (95 cells) Macro cell library equivalent to TTL74 (140 cells)
Personal computer	IBM PC AT	

Development Schedule (Target)

Mass production start ..... Dec., '90 (LZ988000, LZ9824000, LZ9830000, LZ9811000)
April, '91 (LZ9812000, LZ9816000, LZ989000, LZ9813000, LZ9817000, LZ9823000)

The information described herein is intended to introduce descriptions for products that are in development, and specifications and circuitry are subject to change upon final characterization.

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