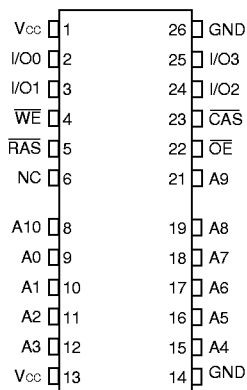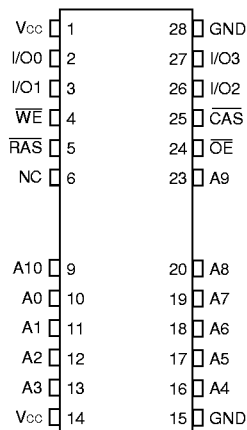## 4Mx4 CMOS FPM Dynamic RAM 3.3V   *ADVANCED**

FEATURES

- Fast Access Time (tRAC): 70, 80, 100ns
- Power Supply: 3.3V ± 0.3V
- Packaging:
  - 24/26 pin Ceramic Flatpack (FP)
  - 24/26 pin Ceramic Flatpack, Lead Formed (F1)
  - 24/28 pin Ceramic Flatpack (FB)
  - 24/28 pin Ceramic Flatpack, Lead Formed (F2)
- Commercial, Industrial and Military Temperature Ranges
- Fast Page Mode (FPM) Access Cycle

- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$-Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Common I/O
- 2K Cycle Refresh = 32ms
- Low Active Power Dissipation
- Low Standby Power Dissipation

 * *This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.*

PIN CONFIGURATION FOR WMD4M4-XXX

24/26 pin (FP, F1)
TOP VIEW

Vcc	1	26	GND
I/O0	2	25	I/O3
I/O1	3	24	I/O2
$\overline{WE}$	4	23	$\overline{CAS}$
$\overline{RAS}$	5	22	$\overline{OE}$
NC	6	21	A9
A10	8	19	A8
A0	9	18	A7
A1	10	17	A6
A2	11	16	A5
A3	12	15	A4
Vcc	13	14	GND

24/28 pin (FB, F2)
TOP VIEW

Vcc	1	28	GND
I/O0	2	27	I/O3
I/O1	3	26	I/O2
$\overline{WE}$	4	25	$\overline{CAS}$
$\overline{RAS}$	5	24	$\overline{OE}$
NC	6	23	A9
A10	9	20	A8
A0	10	19	A7
A1	11	18	A6
A2	12	17	A5
A3	13	16	A4
Vcc	14	15	GND

PIN DESCRIPTION

A0-10	Address Inputs
I/O0-3	Data Input/Outputs
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
Vcc	+3.3V Power Supply
GND	Ground
NC	Not Connected

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Short Circuit Output Current	I_{OS}		50	mA
Power Dissipation	P_D		1	W
Supply Voltage Range	V_{CC}	-1.0	4.6	V
Voltage Range on any Pin*	V_T	-1.0	5.5	V

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

* All voltage values are with respect to GND.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3.0	3.6	V
Input High Voltage	V_{IH}	2.0	5.5	V
Input Low Voltage	V_{IL}	-1.0	+0.8	V
Operating Temp. (Com.)	T_A	0	+70	°C
Operating Temp. (Ind.)	T_A	-40	+85	°C
Operating Temp. (Mil.)	T_A	-55	+125	°C

CAPACITANCE
(T_A = 25°C)

Parameter	Symbol	Max	Unit
A_{0-10} Input Capacitance	$C_{I(A)}$	6	pF
$\overline{RAS}$ and $\overline{CAS}$ Input Capacitance	$C_{I(RC)}$	7	pF
$\overline{OE}$ Input Capacitance	$C_{I(OE)}$	7	pF
$\overline{WE}$ Input Capacitance	$C_{I(WE)}$	7	pF
I/O Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	$C_{I/O}$	8	pF

This parameter is guaranteed by design but not tested.

TRUTH TABLE

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Address t_R	t_C	Data In/Out I/O_{0-3}
Standby		H	H→X	X	X	X	X	High-Z
Read		L	L	H	L	ROW	COL	Data-Out
Early Write		L	L	L	X	ROW	COL	Data-In
Read Write		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
Fast-Page-Mode Read	1st cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd cycle	L	H→L	H	L	n/a	COL	Data-Out
Fast-Page-Mode	1st cycle	L	H→L	L	X	ROW	COL	Data-In
Early-Write	2nd cycle	L	H→L	L	X	n/a	COL	Data-In
Fast-Page-Mode	1st cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
Read-Write	2nd cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
$\overline{RAS}$-Only Refresh		L	H	X	X	ROW	n/a	High-Z
Hidden Refresh (Read)		L→H→L	L	H	L	ROW	COL	Data-Out
Hidden Refresh (Write)		L→H→L	L	L	X	ROW	COL	Data-In
CBR Refresh		H→L	L	H	X	X	X	High-Z

AC TEST CIRCUIT
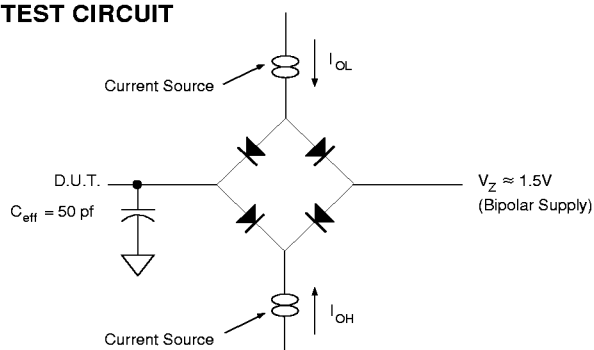
AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

DC CHARACTERISTICS

(Vcc = 3.3V, TA = -55°C to +125°C)

Parameter	Test Condition	Symbol	Min	Max	Units
High Level Output Voltage	IOH = -2mA	VOH	2.4		V
Low Level Output Voltage	IOL = 2mA	VOL		0.4	V
Input Current (Leakage)	VI = 0V to +3.6V All others = 0V	II		10	μA
Output current (Leakage)	VO = 0V to Vcc, data floating	Io		20	μA
Read or Write Cycle Current (1,2)	Vcc = 3.6V, minimum cycle	ICC1		80	mA
Standby Current	$\overline{RAS}$ and $\overline{CAS}$ = VIH, output open	ICC2		2	mA
Average Page Current (1,2)	$\overline{RAS}$ = VIL, $\overline{CAS}$ cycling, minimum cycle	ICC4		80	mA

NOTES:
1. ICC1 and ICC4 depend on cycle rate.
2. ICC1 and ICC4 depend on output loading, specified values are obtained with the output open.

AC CHARACTERISTICS FOR READ ONLY OPERATIONS

(Vcc = 3.3V ± 0.3V, TA = -55°C to +125°C) Note 1

Parameter	Symbol	-70		-80		-100		Units
		Min	Max	Min	Max	Min	Max	
Access Time from $\overline{CAS}$ (2,3)	tCAC		20		20		25	ns
Access Time from $\overline{RAS}$ (2,4)	tRAC		70		80		100	ns
Column Address Access Time (2)	tCAA		35		40		50	ns
Access Time from $\overline{CAS}$ Precharge	tCPA		40		45		50	ns
Access Time from $\overline{OE}$ (2)	tOEA		20		20		25	ns
Output Low Impedance Time from $\overline{CAS}$ Low (5)	tCLZ	3		3		3		ns
Output Disable Time after $\overline{CAS}$ High (6)	tOFF	3	20	3	20	3	20	ns
Output Disable Time after $\overline{OE}$ High (6)	tDISOE	3	20	3	20	3	20	ns

NOTES:
1. An initial pause of 100μs is required after power-up, followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-only or CBR with $\overline{WE}$ High), before proper device operation is ensured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the tREF requirement is exceeded.
2. Measured with a load circuit equivalent to 2tTTL loads 100pF, VOL = 0.8V and VOH = 2.0V.
3. Assumes that tRCD ≥ tRCD (max).
4. Assumes that tRCD ≤ tRCD (max).
5. Guaranteed by design, but not tested.
6. tOFF (max) defines the time at which the output achieves the high impedance state (IOUT ≤ ±10μA) and is not reference to VOH (min) or VOL (max).

AC OPERATIONS AND CHARACTERISTICS

(Vcc = 3.3V ± 0.3V, TA = -55°C to +125°C)

Parameter	Symbol	-70		-80		-100		Units
		Min	Max	Min	Max	Min	Max	
Refresh Cycle	tREF		32		32		32	ms
$\overline{RAS}$ Precharge Time	tRP	50		60		80		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time (9)	tRCD	20	50	20	60	25	75	ns
Delay $\overline{CAS}$ High to $\overline{RAS}$ Low	tCRP	5		5		5		ns
$\overline{CAS}$ Precharge Time (Non Page Mode)	tCP	10		10		10		ns
Column Address Delay Time from $\overline{RAS}$ Low (10)	tRAD	15	35	15	40	20	50	ns
Row Address Setup Time	tASR	0		0		0		ns
Column Address Setup Time (11)	tASC	0		0		0		ns
Row Address Hold Time	tRAH	10		10		15		ns
Column Address Hold Time	tCAH	15		15		20		ns
Transition Time (12)	tT	3	50	3	50	3	50	ns

NOTES:
7. The timing requirements are assumed tT = 5ns.
8. VIH (min) and VIL (max) are reference levels for measuring timing of input signals.
9. tRCD (max) is specified as a reference point only. If tRCD is less than tRCD (max), access time is tRAC. If tRCD is greater than tRCD (max), access time is defined as tCAC and tCAA as shown in note 3.
10. tRAD (max) is specified as a reference point only. If tRAD ≥ tRAD (max), access time is assumed by tCAA for read cycle.
11. tASC (max) is specified as a reference point only of address access time.
12. tT is measured between VIH (min) and VIL (max).

AC CHARACTERISTICS FOR READ OPERATIONS

(Vcc = 3.3V ± 0.3V, TA = -55°C to +125°C) Notes 1, 13, 14

Parameter	Symbol	-70		-80		-100		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	130		150		190		ns
$\overline{RAS}$ Low Pulse Width	tRAS	70	100,000	80	100,000	100	100,000	ns
$\overline{CAS}$ Low Pulse Width	tCAS	20	100,000	20	100,000	25	100,000	ns
$\overline{CAS}$ Hold Time after $\overline{RAS}$ Low	tCSH	70		80		100		ns
$\overline{RAS}$ Hold Time after $\overline{CAS}$ Low	tRSH	20		20		25		ns
Read Setup Time before $\overline{CAS}$ Low	tRCS	0		0		0		ns
Read Hold Time after $\overline{CAS}$ High (1)	tRCH	0		0		0		ns
Read Hold Time after $\overline{RAS}$ High (1)	tRRH	0		0		0		ns
Column Address to $\overline{RAS}$ Setup	tRAL	35		40		50		ns
Precharge to $\overline{CAS}$ Active	tRPC	0		0		0		ns
Delay Time, Data to $\overline{OE}$ Low	tDOEL	0		0		0		ns
Delay Time, $\overline{OE}$ High to Data	tOEHD	20		20		25		ns

NOTES:
1. Either tRCH or tRRH must be satisfied for a read cycle.

AC CHARACTERISTICS FOR WRITE OPERATIONS

(Vcc = 3.3V ± 0.3V, TA = -55°C to +125°C)

Parameter	Symbol	-70 Min	-70 Max	-80 Min	-80 Max	-100 Min	-100 Max	Units
Write Cycle Time	twc	130		150		190		ns
$\overline{RAS}$ Low Pulse Width	tRAS	70	100,000	80	100,000	100	100,000	ns
$\overline{CAS}$ Low Pulse Width	tCAS	20	100,000	20	100,000	25	100,000	ns
$\overline{CAS}$ Hold Time after $\overline{RAS}$ Low	tCSH	70		80		100		ns
$\overline{RAS}$ Hold Time after $\overline{CAS}$ Low	tRSH	20		20		25		ns
Write Setup Time before $\overline{CAS}$ Low (1)	twCS	0		0		0		ns
Write Hold Time after $\overline{CAS}$ Low	twCH	15		15		20		ns
$\overline{CAS}$ Hold Time after $\overline{WE}$ Low	tCWL	20		20		25		ns
$\overline{RAS}$ Hold Time after $\overline{WE}$ Low	tRWL	20		20		25		ns
Write Pulse Width	twP	15		15		20		ns
Data Setup Time (1)	tDS	0		0		0		ns
Data Hold Time after $\overline{CAS}$ Low (1)	tDH	15		15		20		ns
Delay Time, $\overline{OE}$ High to Data	tOEHD	20		20		25		ns
$\overline{OE}$ Hold Time after $\overline{WE}$ Low	tHWOE	20		20		25		ns

1. twcs , tRWD, tcwD, and tawD do not define the limits of operation, but are included as electrical characteristics only.
When twcs ≥ twcs (min), an early write cycle is performed, and the data output keeps the high-impedance state. When tRWD ≥ tRWD (min), tcwD ≥ tcwD (min) and tAWD ≥ tAWD (min), a read write cycle is performed, and the data of the selected address will be read out on the data output. If neither of the above conditions is satisfied, the condition of the output (at the access time and until $\overline{CAS}$ goes back to VIH) is indeterminate.

AC CHARACTERISTICS FOR READ-WRITE OPERATIONS

(Vcc = 3.3V ± 0.3V, TA = -55°C to +125°C)

Parameter	Symbol	-70 Min	-70 Max	-80 Min	-80 Max	-100 Min	-100 Max	Units
Read-ModifyWrite Cycle Time	tRWC	180		205		220		ns
$\overline{RAS}$ Low Pulse Width	tRASRW	70	100,000	80	100,000	100	100,000	ns
$\overline{CAS}$ Low Pulse Width	tCASRW	20	100,000	20	100,000	25	100,000	ns
$\overline{CAS}$ Hold Time after $\overline{RAS}$ Low	tCSHRW	70		80		100		ns
$\overline{RAS}$ Hold Time after $\overline{CAS}$ Low	tRSHRW	20		20		25		ns
Read Setup Time before $\overline{CAS}$ Low	tRCS	0		0		0		ns
$\overline{CAS}$ Low to $\overline{WE}$ Low Delay (1)	tCWD	50		50		55		ns
$\overline{RAS}$ Low to $\overline{WE}$ Low Delay (1)	tRWD	95		110		130		ns
$\overline{CAS}$ Hold after $\overline{WE}$ Low	tCWL	20		20		25		ns
$\overline{RAS}$ Hold after $\overline{WE}$ Low	tRWL	20		20		25		ns
Write Pulse Width	twP	15		15		20		ns
Data Setup Time	tDS	0		0		0		ns
Data Hold Time after $\overline{CAS}$ Low	tDH	15		15		20		ns
Address to $\overline{WE}$ Low Delay (1)	tAWD	65		70		80		ns
Delay Time, $\overline{OE}$ High to Data	tOEHD	20		20		25		ns
$\overline{OE}$ Hold Time after Write Low	tHWOE	20		20		25		ns

1. twcs, tRWD, tcwD, and tawD do not define the limits of operation, but are included as electrical characteristics only.
When twcs ≥ twcs (min), an early write cycle is performed, and the data output keeps the high-impedance state. When tRWD ≥ tRWD (min), tcwD ≥ tcwD (min) and tAWD ≥ tAWD (min), a read write cycle is performed, and the data of the selected address will be read out on the data output. If neither of the above conditions is satisfied, the condition of the output (at the access time and until $\overline{CAS}$ goes back to VIH) is indeterminate.

PAGE MODE OPERATIONS

(Vcc = 3.3V ± 0.3V, TA = -55°C to +125°C)

Parameter	Symbol	-70 Min	-70 Max	-80 Min	-80 Max	-100 Min	-100 Max	Units
Fast Page Mode Cycle Time	t_{PC}	40		45		55		ns
Fast Page Mode for R/W, R/M/W Cycle Time	t_{PRWC}	100		105		115		ns
$\overline{RAS}$ Low Pulse Width for Read, Write Cycle	t_{RASP}	70	100,000	80	100,000	100	100,000	ns
$\overline{CAS}$ Low Pulse Width for Read Cycle	t_{CAS}	20	100,000	20	100,000	25	100,000	ns
$\overline{CAS}$ Pulse Width (Page Mode)	t_{CP}	10		10		10		ns
$\overline{RAS}$ Hold Time after $\overline{CAS}$ Low	t_{RSH}	20		20		25		ns

WRITE REFRESH OPERATIONS *

(Vcc = 3.3V ± 0.3V, TA = -55°C to +125°C)

Parameter	Symbol	-70 Min	-70 Max	-80 Min	-80 Max	-100 Min	-100 Max	Units
$\overline{CAS}$ Setup for $\overline{CAS}$ before $\overline{RAS}$ Refresh	t_{CSR}	5		5		5		ns
$\overline{CAS}$ Hold for $\overline{CAS}$ before $\overline{RAS}$ Refresh	t_{CHR}	15		15		15		ns
Precharge to $\overline{CAS}$ Active	t_{RPC}	0		0		0		ns
Write Setup Time	t_{WRP}	10		10		10		ns
Write Hold Time	t_{WRH}	10		10		10		ns

* Eight or more CAS before RAS cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

GENERAL DESCRIPTION

The 4M x 4 DRAM is a randomly accessed, solid-state memory containing 16,777,216 bits organized in a x4 configuration. $\overline{RAS}$ is used to latch the row address. Once the page has been opened by $\overline{RAS}$, $\overline{CAS}$ is used to latch the column address. Read and Write cycles are selected with the $\overline{WE}$ input. A logic High on $\overline{WE}$ dictates Read mode while a logic Low on $\overline{WE}$ dictates Write mode. During a Write cycle, data-in (I) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes Low prior to $\overline{CAS}$ going Low, the output pins remain open (High-Z) until the next $\overline{CAS}$ cycle, regardless of $\overline{OE}$.

A logic High on $\overline{WE}$ dictates Read mode while logic Low on $\overline{WE}$ dictates Write mode. During a Write cycle, data-in is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. An Early Write occurs when $\overline{WE}$ is taken Low prior to $\overline{CAS}$ falling. A Late Write or Read-Modify-Write occurs when $\overline{WE}$ falls after $\overline{CAS}$ was taken Low. During Early Write cycles, the outputs (O) will remain High-Z regardless of the state of $\overline{OE}$. During Late Write or Read-Modify-Write cycles, $\overline{OE}$ must be taken High to disable the data outputs prior to applying input data. If a Late Write or Read-Modify-Write is attempted while keeping $\overline{OE}$ Low, no write will occur, and the data outputs will drive read data from the accessed location.

The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.
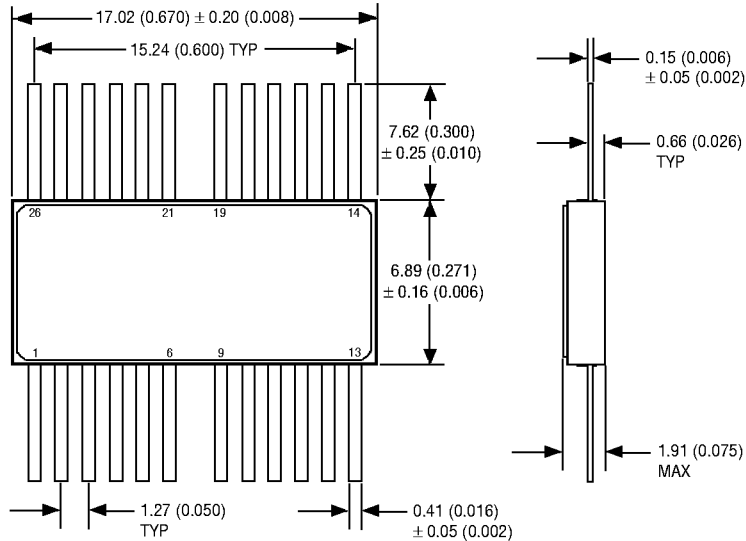
PAGE ACCESS

Page operations allow faster data operations (Read, Write or Read-Modify-Write) within a row-address-defined page boundary. The Page cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ Low and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ High terminates the Page Mode operation, i.e. closes the page.
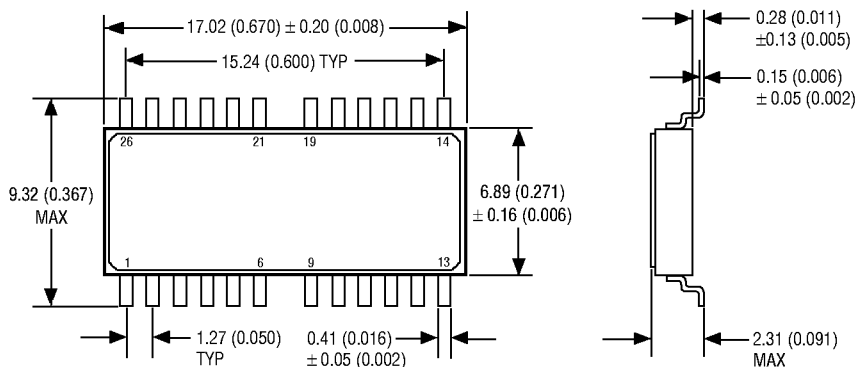
REFRESH

Preserve correct memory cell data by maintaining power and executing any $\overline{RAS}$ cycle (Read, Write) or $\overline{RAS}$ refresh CYCLE ($\overline{RAS}$-only, CBR, or Hidden) so that all combinations of $\overline{RAS}$ addresses (2,048) are executed within tREF (max), regardless of sequence. The CBR Refresh cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

STANDBY

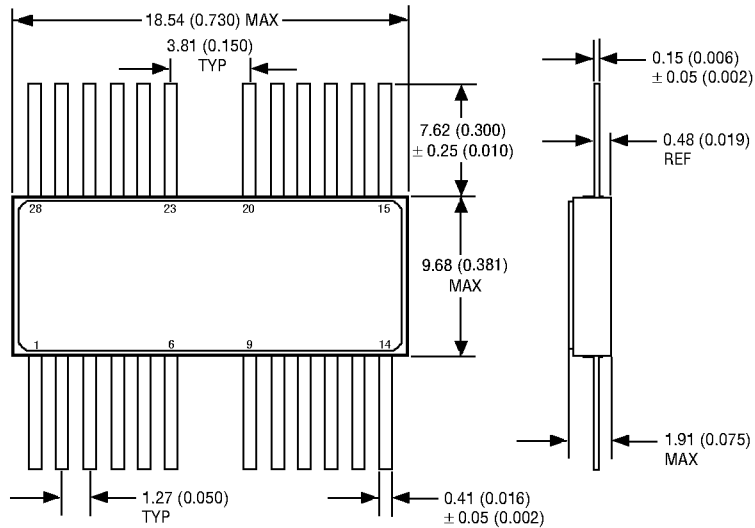Returning $\overline{RAS}$ and $\overline{CAS}$ High terminates a memory cycle and decreases chip current to a reduced standby level. The chip is preconditioned for the next cycle during the $\overline{RAS}$ High time.

PACKAGE DIMENSION: 24/26 PIN, CERAMIC FLATPACK (FP)

17.02 (0.670) ± 0.20 (0.008)

15.24 (0.600) TYP

7.62 (0.300)
± 0.25 (0.010)

6.89 (0.271)
± 0.16 (0.006)

26   21   19   14

1   6   9   13

0.15 (0.006)
± 0.05 (0.002)

0.66 (0.026)
TYP

1.91 (0.075)
MAX

1.27 (0.050)
TYP

0.41 (0.016)
± 0.05 (0.002)

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE DIMENSION: 24/26 PIN, CERAMIC FLATPACK, LEAD FORMED (F1)

17.02 (0.670) ± 0.20 (0.008)

15.24 (0.600) TYP

9.32 (0.367)
MAX

6.89 (0.271)
± 0.16 (0.006)

26   21   19   14

1   6   9   13

0.28 (0.011)
±0.13 (0.005)

0.15 (0.006)
± 0.05 (0.002)

2.31 (0.091)
MAX

1.27 (0.050)
TYP

0.41 (0.016)
± 0.05 (0.002)

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE DIMENSION: 24/28 PIN, CERAMIC FLATPACK (FB)

18.54 (0.730) MAX

3.81 (0.150) TYP

0.15 (0.006) ± 0.05 (0.002)

7.62 (0.300) ± 0.25 (0.010)

0.48 (0.019) REF

28   23   20   15

9.68 (0.381) MAX

1   6   9   14

1.91 (0.075) MAX

1.27 (0.050) TYP

0.41 (0.016) ± 0.05 (0.002)
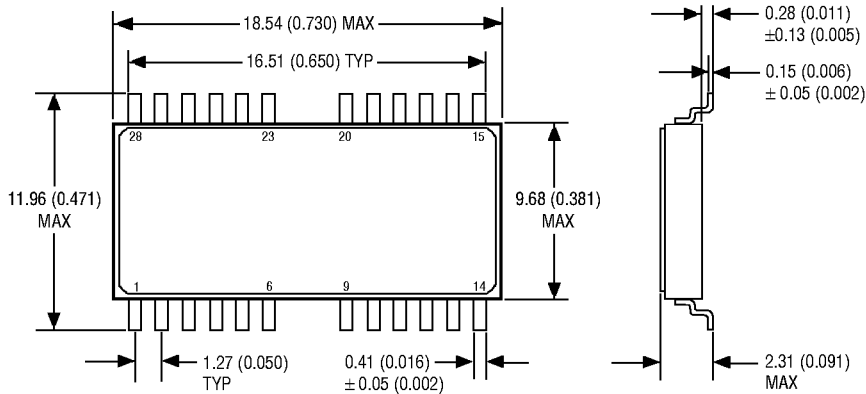
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE DIMENSION: 24/28 PIN, CERAMIC FLATPACK, LEAD FORMED (F2)

18.54 (0.730) MAX

16.51 (0.650) TYP

0.28 (0.011) ±0.13 (0.005)

0.15 (0.006) ± 0.05 (0.002)

28   23   20   15

11.96 (0.471) MAX

9.68 (0.381) MAX

1   6   9   14

1.27 (0.050) TYP

0.41 (0.016) ± 0.05 (0.002)

2.31 (0.091) MAX

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W M D   4M 4 V - XXX X X

DEVICE GRADE:

M = Military Screened   -55°C to +125°C
I = Industrial   -40°C to +85°C
C = Commercial   0°C to +70°C

PACKAGE:

FP = 24/26 pin, Ceramic Flatpack
F1 = 24/26 pin, Ceramic Flatpack, Lead Formed
FB = 24/28 pin, Ceramic Flatpack
F2 = 24/28 pin, Ceramic Flatpack, Lead Formed

ACCESS TIME (ns)

Low Voltage Supply 3.3V ± 0.3V

ORGANIZATION, 4M x 4

DRAM FPM

MONOLITHIC

WHITE MICROELECTRONICS