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N04L1630C2B

Advance Information

4Mb Ultra-Low Power Asynchronous CMOS SRAMs

256K × 16 bit POWER SAVER TECHNOLOGY™

Overview

The N04L1630C2B is an integrated memory device containing a 4 Mbit Static Random Access Memory organized as 262,144 words by 16 bits. The device is designed and fabricated using AMI Semiconductor's advanced CMOS technology to provide both high-speed performance and ultra-low power. The device operates with two chip enable ($\overline{CE1}$ and $\overline{CE2}$) controls and output enable (\overline{OE}) to allow for easy memory expansion. Byte controls (\overline{UB} and \overline{LB}) allow the upper and lower bytes to be accessed independently and can also be used to deselect the device. The N04L1630C2B is optimized for the ultimate in low power and is suited for various applications where ultra-low-power is critical such as medical applications, battery backup and power sensitive hand-held devices. The unique page mode operation saves operating power while improving the performance over standard SRAMs. The device can operate over a very wide temperature range of -40°C to +85°C and is available in JEDEC standard packages compatible with other standard 256Kb x 16 SRAMs.

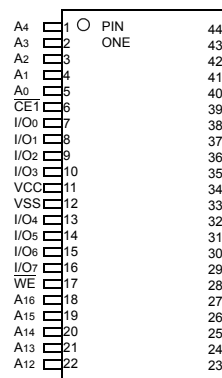
Features

- **Wide Power Supply Range**
2.7 to 3.6 Volts
- **Very low standby current**
1 μ A (Typical)
- **Very low operating current**
2.0mA at 1 μ s (Typical)
- **Very low Page Mode operating current**
0.8mA at 1 μ s (Typical)
- **Simple memory control**
Dual Chip Enables ($\overline{CE1}$ and $\overline{CE2}$)
Byte control for independent byte operation
Output Enable (\overline{OE}) for memory expansion
- **Very fast output enable access time**
30ns \overline{OE} Access Time
55ns Random Access Time
30ns Page Mode Access Time
- **Automatic power down to standby mode**
- **TTL compatible three-state output driver**
- **RoHS Compliant TSOP and BGA packages**

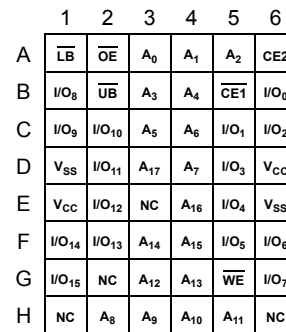
Product Family

| Part Number | Package Type | Operating Temperature | Power Supply (Vcc) | Speed Options | Standby Current (I_{SB}), Typical | Operating Current (I_{CC}), Typical |
|---------------|------------------|-----------------------|--------------------|---------------|---------------------------------------|---|
| N04L1630C2BB2 | 48-BGA Green | -40°C to +85°C | 2.7V - 3.6V | 55ns 70ns | 1 μ A | 2 mA @ 1MHz |
| N04L1630C2BT2 | 44-TSOP II Green | | | | | |

Pin Configurations (4Mb)



TSOP II

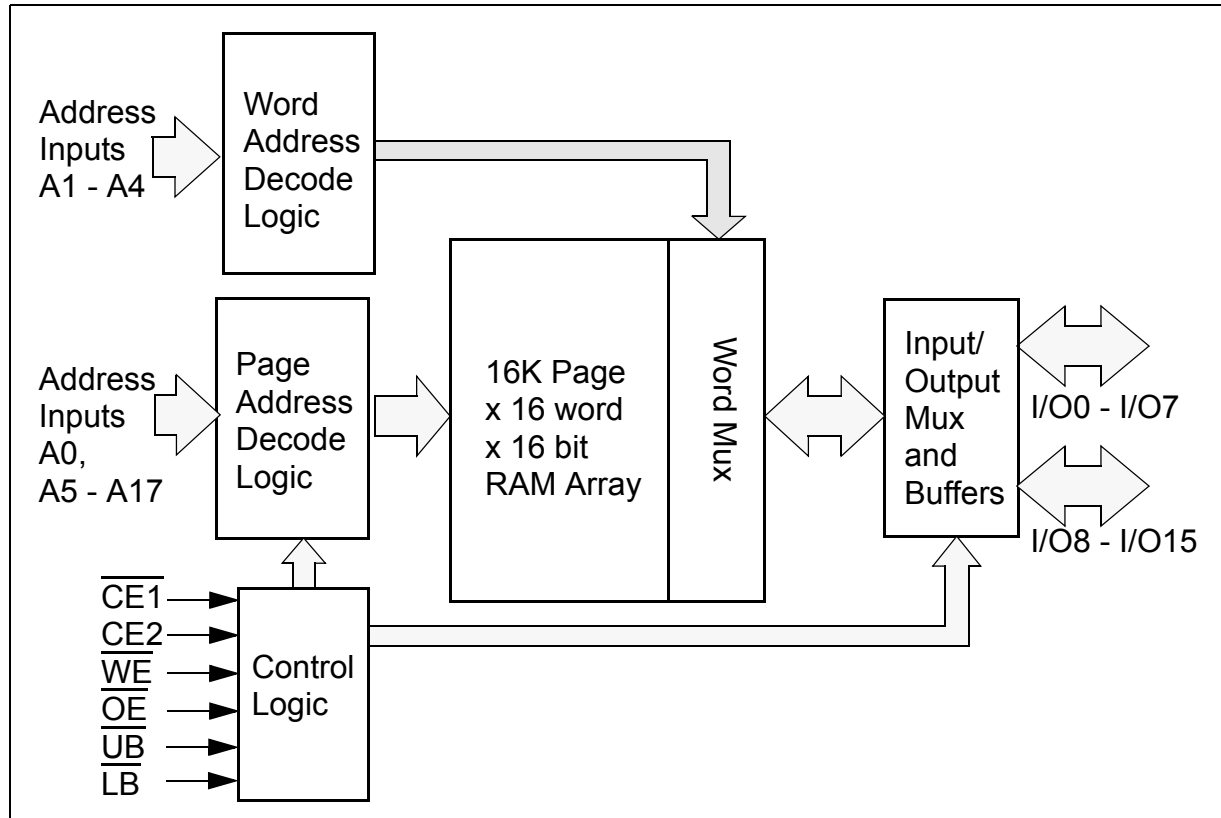


48 Pin BGA (top)

Pin Descriptions

| Pin Name | Pin Function |
|-------------------------------------|------------------------------|
| A ₀ -A ₁₇ | Address Inputs |
| WE | Write Enable Input |
| CE1 | Chip Enable 1 Input |
| CE2 | Chip Enable 2 Input |
| OE | Output Enable Input |
| LB | Lower Byte Enable Input |
| UB | Upper Byte Enable Input |
| I/O ₀ -I/O ₇ | Lower Byte Data Input/Output |
| I/O ₈ -I/O ₁₅ | Upper Byte Data Input/Output |
| V _{CC} | Power |
| V _{SS} | Ground |
| NC | Not Connected |

Functional Block Diagram



Functional Description

| $\overline{CE1}$ | $\overline{CE2}$ | \overline{WE} | \overline{OE} | \overline{UB} | \overline{LB} | I/O ₀ - I/O ₁₅ ¹ | MODE | POWER |
|------------------|------------------|-----------------|-----------------|-----------------|-----------------|---|----------------------|---------|
| H | X | X | X | X | X | High Z | Standby ² | Standby |
| X | L | X | X | X | X | High Z | Standby ² | Standby |
| L | H | X | X | H | H | High Z | Standby | Standby |
| L | H | L | X ³ | L ¹ | L ¹ | Data In | Write ³ | Active |
| L | H | H | L | L ¹ | L ¹ | Data Out | Read | Active |
| L | H | H | H | L ¹ | L ¹ | High Z | Active | Active |

1. When \overline{UB} and \overline{LB} are in select mode (low), I/O₀ - I/O₁₅ are affected as shown. When \overline{LB} only is in the select mode only I/O₀ - I/O₇ are affected as shown. When \overline{UB} is in the select mode only I/O₈ - I/O₁₅ are affected as shown.

2. When the device is in standby mode, control inputs (\overline{WE} , \overline{OE} , \overline{UB} , and \overline{LB}), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.

3. When \overline{WE} is invoked, the \overline{OE} input is internally disabled and has no effect on the circuit.

Capacitance¹

| Item | Symbol | Test Condition | Min | Max | Unit |
|-------------------|------------------|--|-----|-----|------|
| Input Capacitance | C _{IN} | V _{IN} = 0V, f = 1 MHz, T _A = 25°C | | 8 | pF |
| I/O Capacitance | C _{I/O} | V _{IN} = 0V, f = 1 MHz, T _A = 25°C | | 8 | pF |

1. These parameters are verified in device characterization and are not 100% tested

Absolute Maximum Ratings¹

| Item | Symbol | Rating | Unit |
|---|---------------------|------------------------------|------|
| Voltage on any pin relative to V _{SS} | V _{IN,OUT} | -0.3 to V _{CC} +0.3 | V |
| Voltage on V _{CC} Supply Relative to V _{SS} | V _{CC} | -0.3 to 4.5 | V |
| Power Dissipation | P _D | 500 | mW |
| Storage Temperature | T _{STG} | -40 to 125 | °C |
| Operating Temperature | T _A | -40 to +85 | °C |
| Soldering Temperature and Time | T _{SOLDER} | 260°C, 10sec | °C |

1. Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Characteristics (Over Specified Temperature Range)

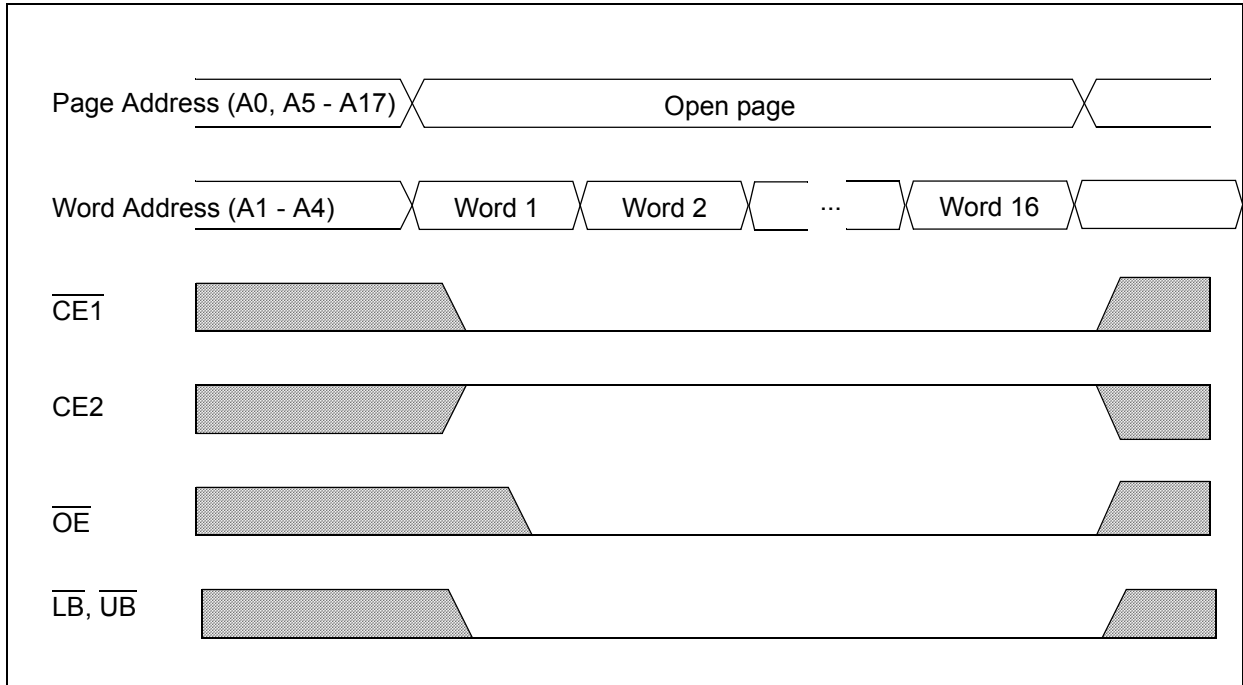
| Item | Symbol | Test Conditions | Min. | Typ ¹ | Max | Unit |
|---|------------------|---|----------------------|------------------|----------------------|------|
| Supply Voltage | V _{CC} | | 2.7 | 3.0 | 3.6 | V |
| Data Retention Voltage | V _{DR} | Chip Disabled ³ | 1.8 | | | V |
| Input High Voltage | V _{IH} | | 0.7V _{CC} | | V _{CC} +0.3 | V |
| Input Low Voltage | V _{IL} | | -0.3 | | 0.6 | V |
| Output High Voltage | V _{OH} | I _{OH} = -100uA | V _{CC} -0.2 | | | V |
| | | I _{OH} = -1mA | 2.4 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 100uA | | | 0.2 | V |
| | | I _{OL} = 2.1mA | | | 0.4 | V |
| Input Leakage Current | I _{LI} | V _{IN} = 0 to V _{CC} | | | 0.5 | μA |
| Output Leakage Current | I _{LO} | \overline{OE} = V _{IH} or Chip Disabled | | | 0.5 | μA |
| Read/Write Operating Supply Current @ 1 μs Cycle Time ² | I _{CC1} | V _{CC} =V _{CC} Max, V _{IN} =V _{IH} or V _{IL} Chip Enabled, I _{OUT} = 0 | | 2.5 | 3.0 | mA |
| Read/Write Operating Supply Current @ 70 ns Cycle Time ² | I _{CC2} | V _{CC} =V _{CC} Max, V _{IN} =V _{IH} or V _{IL} Chip Enabled, I _{OUT} = 0 | | 10 | 15.0 | mA |
| Page Mode Operating Supply Current @ 70ns Cycle Time ² (Refer to Power Savings with Page Mode Operation) | I _{CC3} | V _{CC} =V _{CC} Max, V _{IN} =V _{IH} or V _{IL} Chip Enabled, I _{OUT} = 0 | | 4 | 8 | mA |
| Maximum Standby Current ³ | I _{SB1} | V _{IN} = V _{CC} or 0V Chip Disabled t _A = 85°C, V _{CC} = 3.6 V | | 1 | 10.0 | μA |
| Maximum Data Retention Current ³ | I _{DR} | V _{CC} = 1.8V, V _{IN} = V _{CC} or 0 Chip Disabled, t _A = 85°C | | | 5 | μA |

1. Typical values are measured at V_{CC}=V_{CC} Typ., T_A=25°C and not 100% tested.

2. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.

3. This device assumes a standby mode if the chip is disabled ($\overline{CE1}$ high or CE2 low). In order to achieve low standby current all inputs must be within 0.2 volts of either V_{CC} or V_{SS}.

Power Savings with Page Mode Operation ($\overline{WE} = V_{IH}$)



Note: Page mode operation is a method of addressing the SRAM to save operating current. The internal organization of the SRAM is optimized to allow this unique operating mode to be used as a valuable power saving feature.

The only thing that needs to be done is to address the SRAM in a manner that the internal page is left open and 16-bit words of data are read from the open page. By treating addresses A1-A4 as the least significant bits and addressing the 16 words within the open page, power is reduced to the page mode value which is considerably lower than standard operating currents for low power SRAMs.

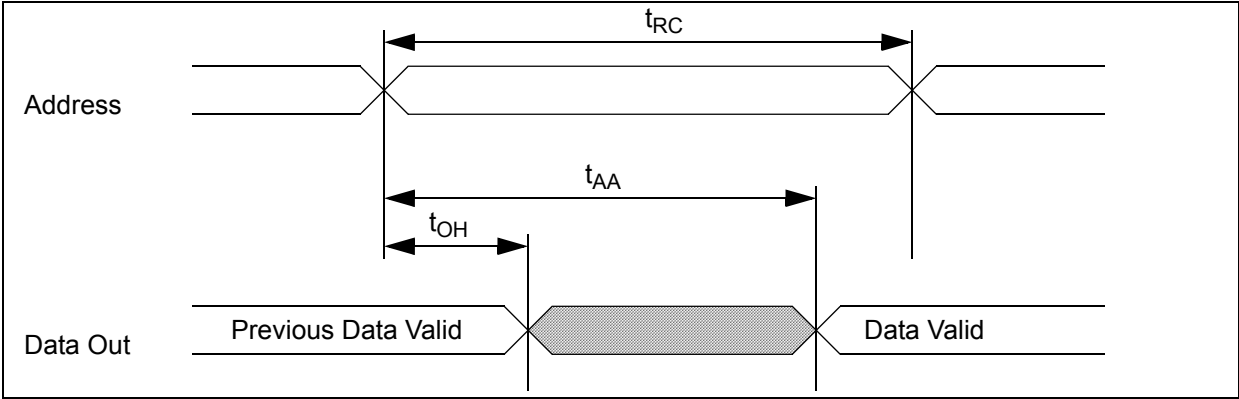
Timing Test Conditions

| Item | |
|--|---|
| Input Pulse Level | 0.1V _{CC} to 0.9 V _{CC} |
| Input Rise and Fall Time | 5ns |
| Input and Output Timing Reference Levels | 0.5 V _{CC} |
| Output Load | CL = 30pF |
| Operating Temperature | -40 to +85 °C |

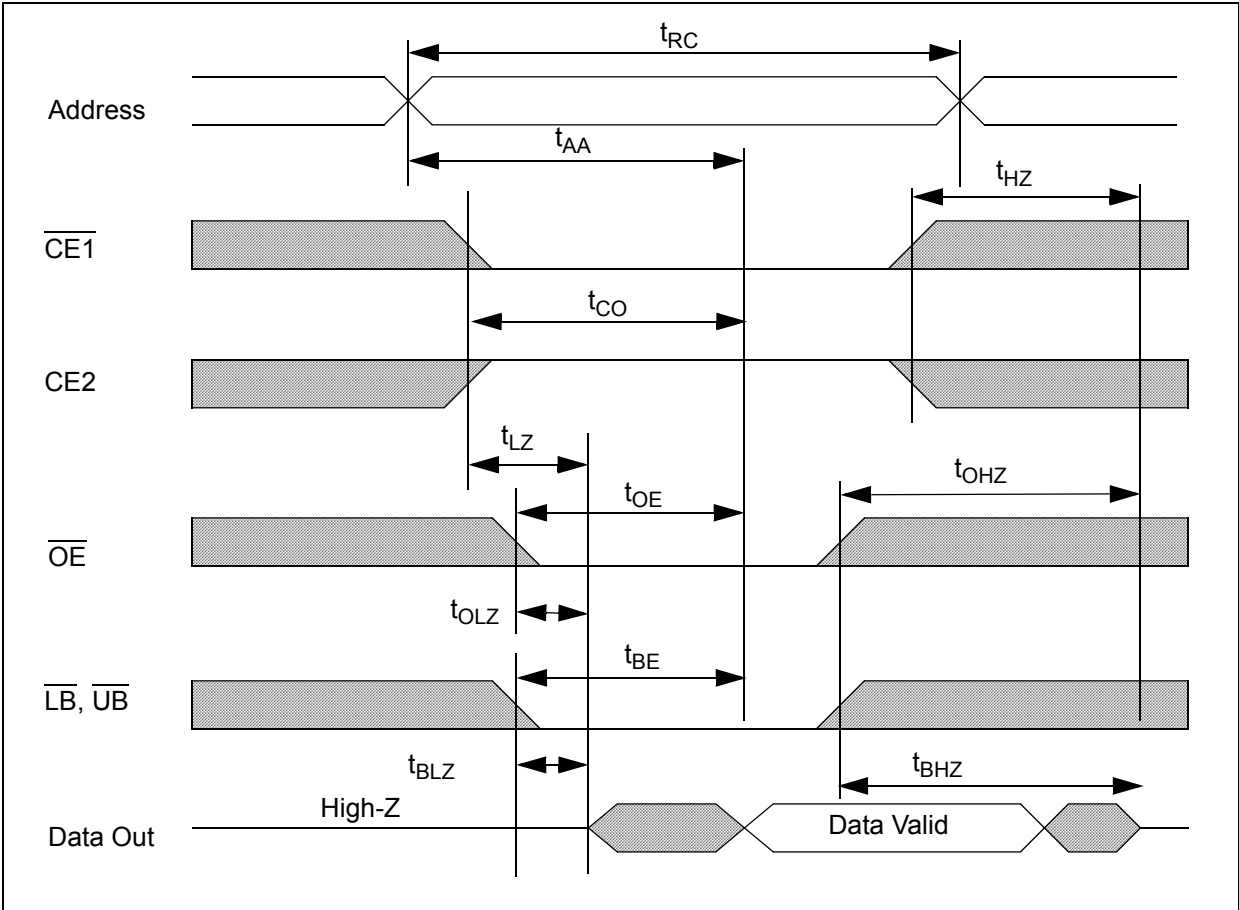
Timing

| Item | Symbol | -55 | | -70 | | Units |
|--------------------------------------|------------------|------|------|------|------|-------|
| | | Min. | Max. | Min. | Max. | |
| Read Cycle Time | t _{RC} | 55 | | 70 | | ns |
| Address Access Time | t _{AA} | | 55 | | 70 | ns |
| Page Mode Address Access Time | t _{AAP} | | 30 | | 35 | ns |
| Chip Enable to Valid Output | t _{CO} | | 55 | | 70 | ns |
| Output Enable to Valid Output | t _{OE} | | 30 | | 35 | ns |
| Byte Select to Valid Output | t _{BE} | | 55 | | 70 | ns |
| Chip Enable to Low-Z output | t _{LZ} | 10 | | 10 | | ns |
| Output Enable to Low-Z Output | t _{OLZ} | 5 | | 5 | | ns |
| Byte Select to Low-Z Output | t _{BZ} | 10 | | 10 | | ns |
| Chip Disable to High-Z Output | t _{HZ} | 0 | 20 | 0 | 20 | ns |
| Output Disable to High-Z Output | t _{OHZ} | 0 | 20 | 0 | 20 | ns |
| Byte Select Disable to High-Z Output | t _{BHZ} | 0 | 20 | 0 | 20 | ns |
| Output Hold from Address Change | t _{OH} | 10 | | 10 | | ns |
| | | | | | | |
| Write Cycle Time | t _{WC} | 55 | | 70 | | ns |
| Chip Enable to End of Write | t _{CW} | 45 | | 50 | | ns |
| Address Valid to End of Write | t _{AW} | 45 | | 50 | | ns |
| Byte Select to End of Write | t _{BW} | 45 | | 50 | | ns |
| Write Pulse Width | t _{WP} | 40 | | 40 | | ns |
| Address Setup Time | t _{AS} | 0 | | 0 | | ns |
| Write Recovery Time | t _{WR} | 0 | | 0 | | ns |
| Write to High-Z Output | t _{WHZ} | | 20 | | 20 | ns |
| Data to Write Time Overlap | t _{DW} | 40 | | 40 | | ns |
| Data Hold from Write Time | t _{DH} | 0 | | 0 | | ns |
| End Write to Low-Z Output | t _{OW} | 5 | | 5 | | ns |

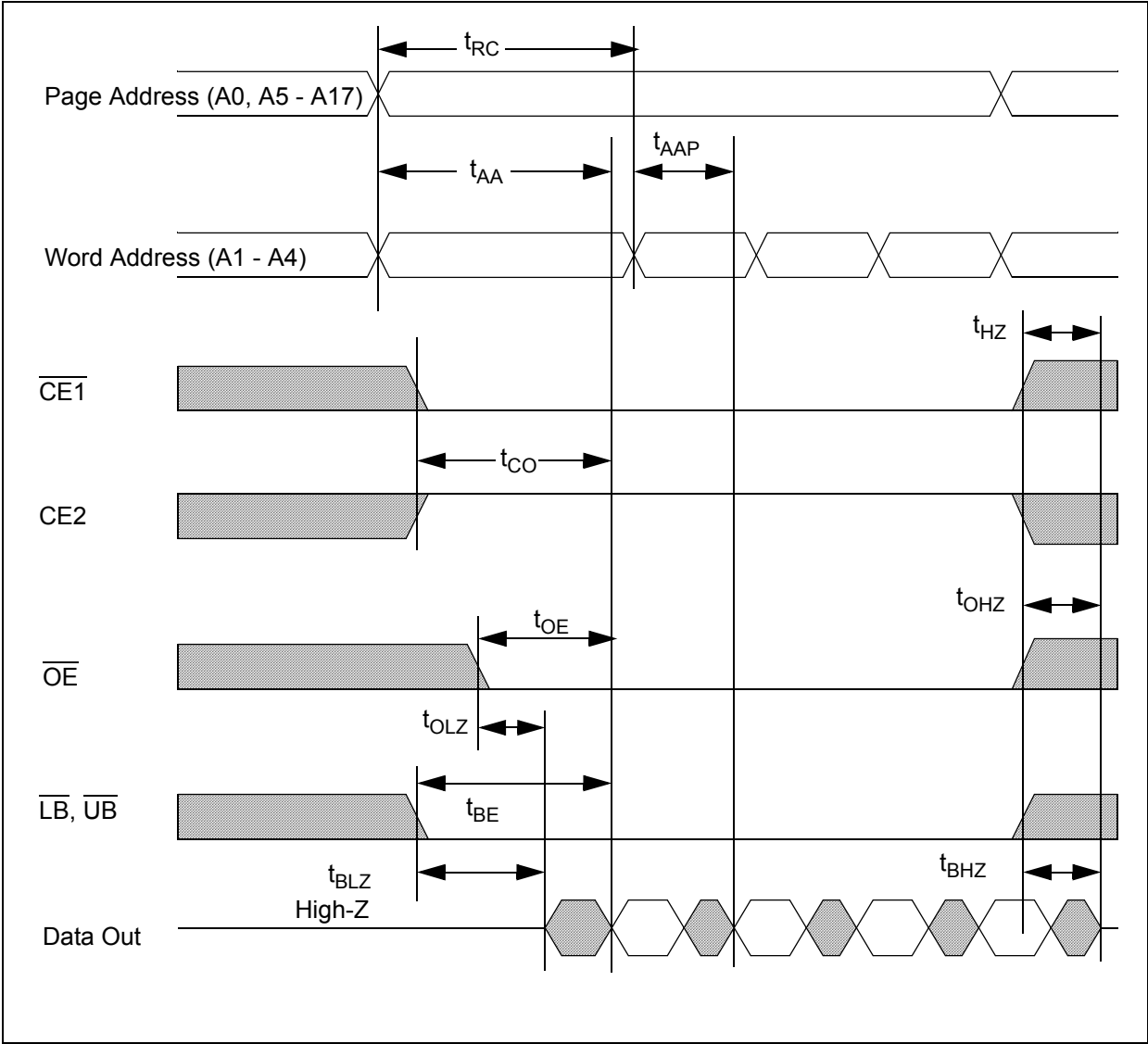
Timing of Read Cycle ($\overline{\text{CE1}} = \overline{\text{OE}} = V_{\text{IL}}, \overline{\text{WE}} = \text{CE2} = V_{\text{IH}}$)



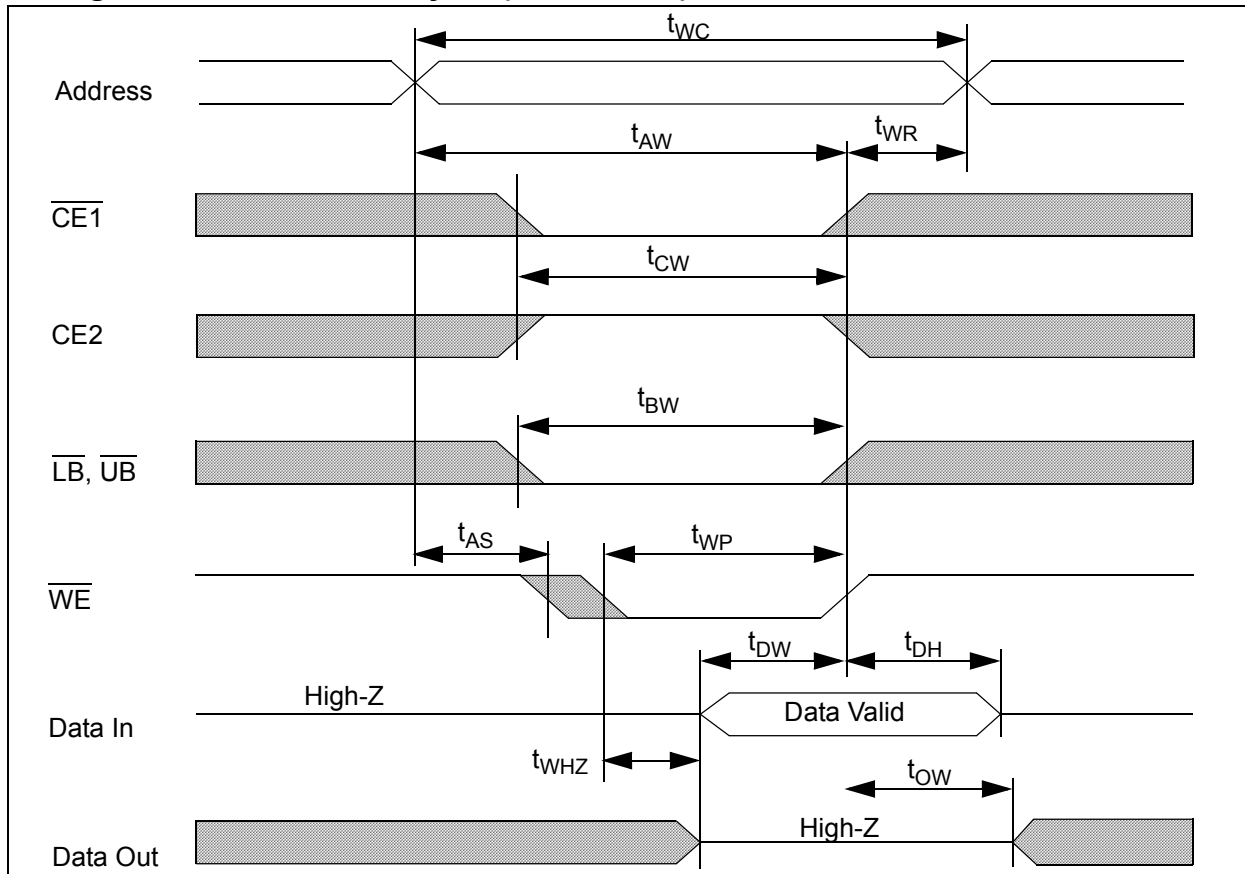
Timing Waveform of Read Cycle ($\overline{\text{WE}} = V_{\text{IH}}$)



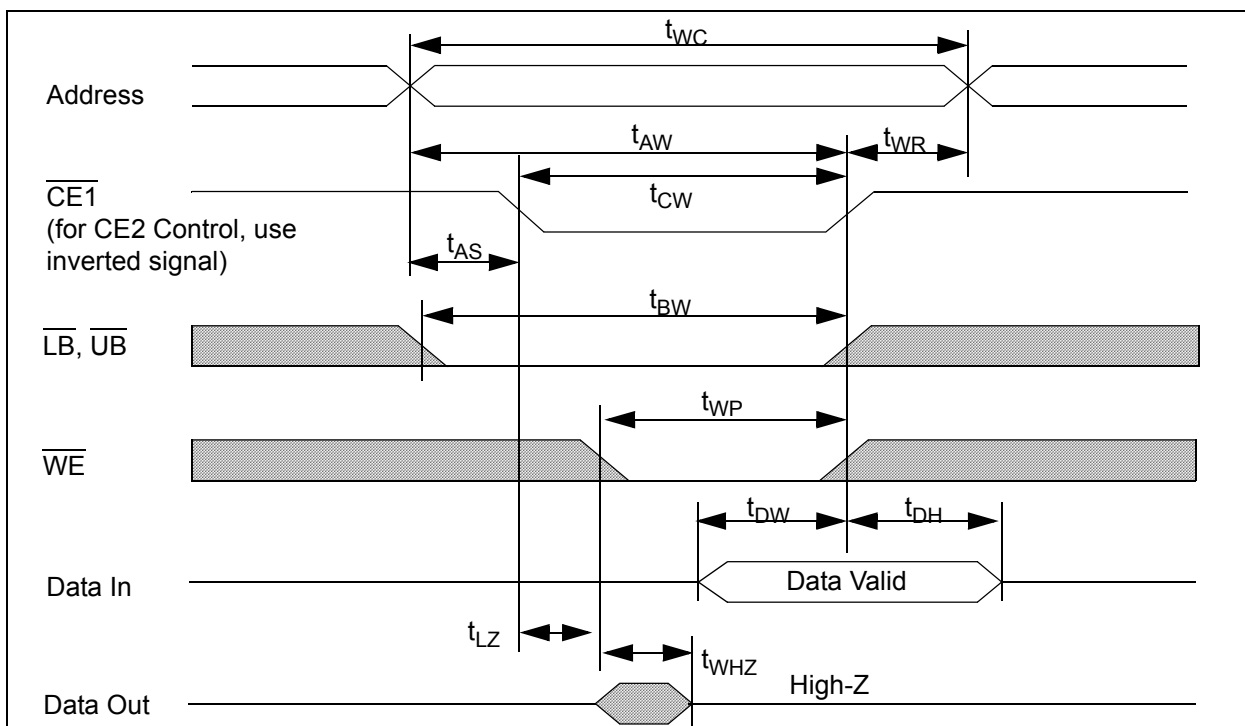
Timing Waveform of Page Mode Read Cycle ($\overline{WE} = V_{IH}$)



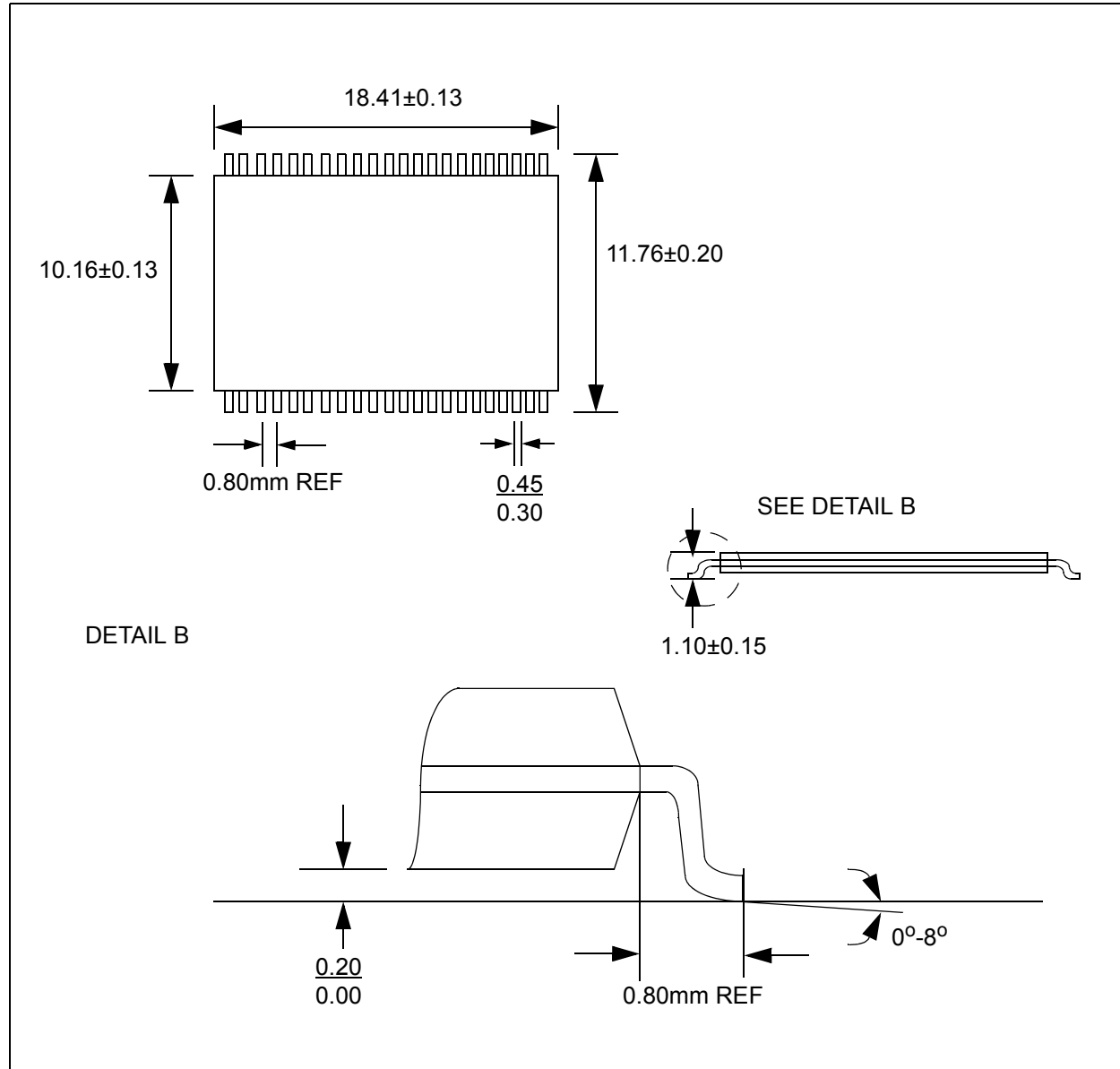
Timing Waveform of Write Cycle ($\overline{\text{WE}}$ control)



Timing Waveform of Write Cycle ($\overline{\text{CE1}}$ Control)



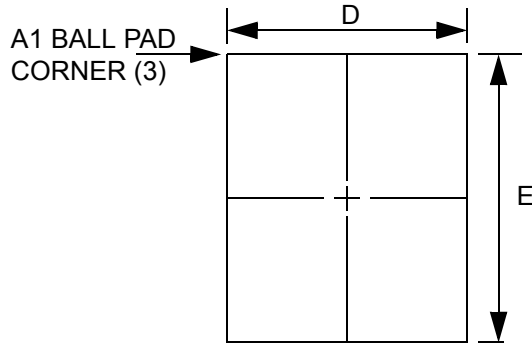
44-Lead TSOP II Package (T44)



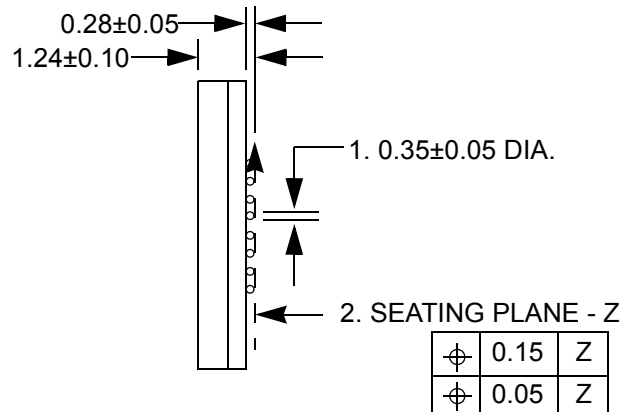
Note:

1. All dimensions in inches (Millimeters)

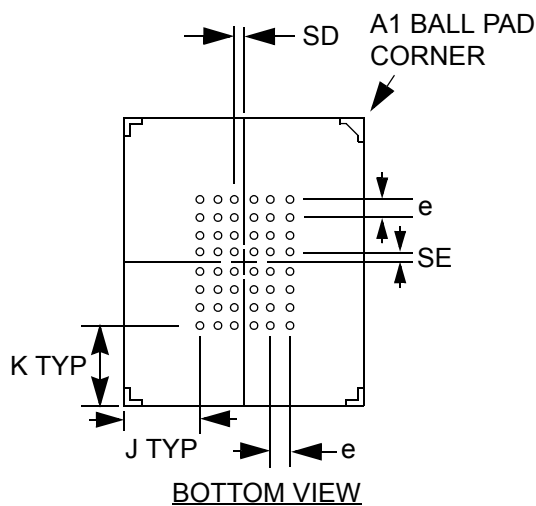
Ball Grid Array Package



TOP VIEW



SIDE VIEW



BOTTOM VIEW

1. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER. PARALLEL TO PRIMARY Z.

2. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

3. A1 BALL PAD CORNER I.D. TO BE MARKED BY INK.

Ordering Information**N04L1630C2BX-XX I****Performance**55 = 55ns
70 = 70ns**Package Type**B2 = 48-ball BGA Green (RoHS Compliant)
T2 = 44-pin TSOP II Green (RoHS Compliant)**Revision History**

| Revision | Date | Change Description |
|----------|----------------|---|
| A | April 2003 | Initial Advanced Release |
| B | August 2004 | Changed part number to -30 from -3W and V _{CC} range to 2.7 V - 3.6V |
| C | January 2005 | Change I _{DR} = 5 μ A, I _{CC} (typ) = 2.5mA. Modified page mode address A1-A4 configuration. |
| D | January 2005 | General Update |
| E | March 22, 2005 | Changed tWP and tDW to 40ns for -55 and -70, to 45ns for -85 |
| F | June 9, 2005 | Added TSOP II Green Package Ordering Option |
| G | Dec. 2005 | Added RoHS Compliant |
| H | July 2006 | Added BGA package |
| I | September 2006 | Converted to AMI Semiconductor |

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