M54740AP, S/P, S-1/P, S-2
M54741AP, S/P, S-1/P, S-2

4096-BIT(1024-WORD BY 4-BIT)FIELD PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The M54740AP,S (open collector output) and the M54741AP,S (three-state output) are field programmable ROM's with fuse links type 4096 bit (1,024 words x 4 bits) memories.

FEATURES

- Access time
  M54740AP, S-1/M54741AP, S-1 ..... 30ns (Max)
  M54740AP, S-2/M54741AP, S-2 ..... 35ns (Max)
  M54740AP, S/M54741AP, S ..... 50ns (Max)
- Unique built-in test circuits guarrantee high programming yield as well as various performance characteristics after programming
- Fuse technology is used
- Memory capacity: 4,096 bits (1,024 words × 4 bits)
- Output type: M54740AP,S (open collector output)
  M54741AP,S (three state output)
- Output level before programming is high
- Chip enable pin $\overline{E}_1$, $\overline{E}_2$ provided for easy expansion of memory capacity
- Input and output are TTL compatible
- Package is 18-pin DIL ceramic or plastic

APPLICATION

General purpose, for use in industrial and consumer equipment

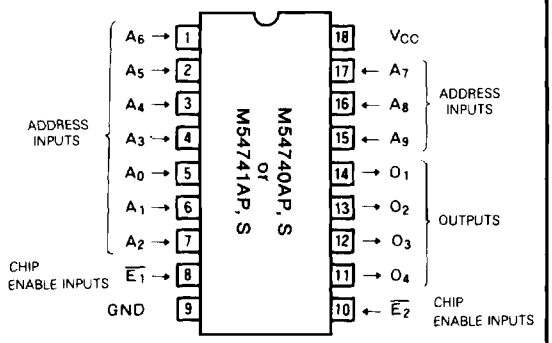
SUMMARY OF OPERATION

The unit consists of an address circuit, decoder circuit, memory circuit, output circuit, and a chip enable circuit. The memory cells are structured from fuses and diodes. Data can be programmed into the PROM by the user using a writer by cutting the fuses of the memory cells. Before programming the output level is high. After programming, the output level becomes low.

The 4,096 bit memory is made up of 1,024 words with 4 bits associated with each word. Through the address inputs ($A_0 \sim A_9$) one word out of the 1,024 is chosen and a 4-bit parallel output, $O_1 \sim O_4$, is obtained.

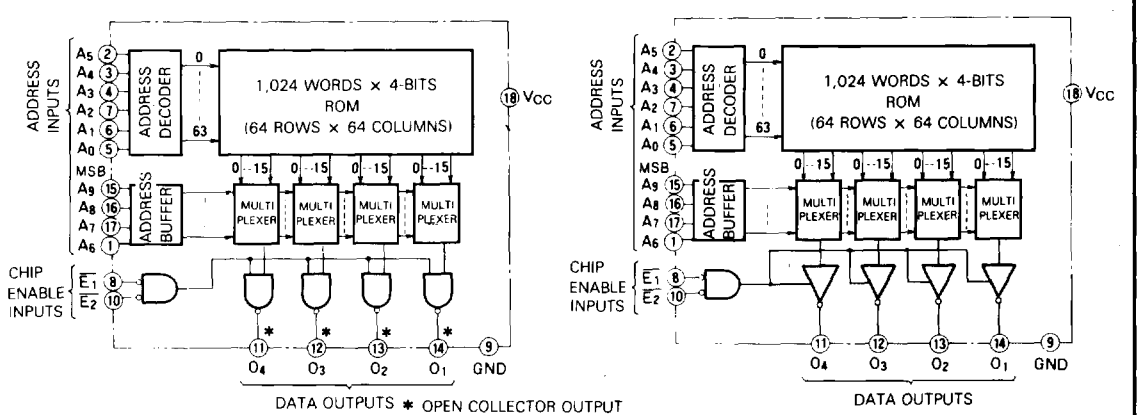
Input and output threshold voltages are the same as that for a TTL system and thus direct coupling can be made with TTL logic (M54740AP,S) or 3-state (M54741AP, S) so AND ties are possible.

PIN CONFIGURATION (TOP VIEW)



Outline **18S1** (M54740AS, M54741AS)
18P4 (M54740AP, M54741AP)

BLOCK DIAGRAM



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When both of the chip enable inputs $\overline{E}_1$ and $\overline{E}_2$ are at low level the output is enabled and the content of the memory selected by the address input appears as output. If either $\overline{E}_1$ or $\overline{E}_2$ is at high level, the output is disabled and regardless of the address input, the output is "H" (open collector output) or high impedance (three-state output).

READ-OUT FUNCTION TABLE (Note 1)

M54740AP,S Read-Out Funciton Table

$\overline{E_1}$	$\overline{E_2}$	$O_1 \sim O_4$
L	L	Wn
H	L	H
L	H	H
H	H	H

M54740AP,S Read-Out Function Table

$\overline{E_1}$	$\overline{E_2}$	$O_1 \sim O_4$
L	L	Wn
H	L	Z
L	H	Z
H	H	Z

Note 1: Wn: The memory content programmed in Wn word appears as output
Z: High impedance state

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +5.5	V
V_O	Output voltage	When output is high level	−0.5 ~ +5.5	V
V_{OP}	Applied output voltage	During programming	21	V
$t_{W(P)}/t_{C(P)}$	Duty cycle		25	%
Topr	Operating temperature		0 ~ +75	°C
Tstg	Storage temperature		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = 0 ~ 75°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
I_{OH}	High level output current (M5474IAP/S) $V_{OH} \geq 2.4V$	0		−2	mA
I_{OH}	High level output current (M54740AP/S) $V_O = 5V$	0		50	μA
I_{OL}	Low level output current $V_{OL} \leq 0.45V$	0		16	mA

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ *	Max	
V_{IH}	High level input voltage		2			V
V_{IL}	Low level input voltage				0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = 4.75V$, $I_{IC} = -18mA$			−1.2	V
V_{OH}	High level output voltage (M54741AP, S)	$V_{CC} = 4.75V$, $V_I = 2V$, $V_I = 0.8V$, $I_{OH} = -2mA$	2.4	3.1		V
I_{OH}	High level output current (M54740AP, S)	$V_{CC} = 5.25V$, $V_I = 2V$, $V_I = 0.8V$, $V_O = 5V$			50	μA
V_{OL}	Low level output voltage	$V_{CC} = 4.75V$, $V_I = 2V$, $V_I = 0.8V$, $I_{OL} = 16mA$		0.3	0.45	V
I_{OZH}	Off-state high level output current (M54741AP, S)	$V_{CC} = 5.25V$, $V_I = 0.8V$, $V_I = 2V$, $V_O = 2.4V$			50	μA
I_{OZL}	Off-state low level output current (M54741AP, S)	$V_{CC} = 5.25V$, $V_I = 0.8V$, $V_I = 2V$, $V_O = 0.4V$			−50	μA
I_{IH}	High level input current	$V_{CC} = 5.25V$, $V_I = 2.4V$			40	μA
I_{IL}	Low level input current	$V_{CC} = 5.25V$, $V_I = 0.4V$		−160	−250	μA
I_{OS}	Output short-circuit current (M54741AP, S)(Note 2)	$V_{CC} = 5.25V$, $V_O = 0V$	−15		−100	mA
I_{CC}	Supply current (Note 3)	$V_{CC} = 5.25V$, $V_I = 0V$		120	170	mA
C_{IN}	Input capacitance	$V_{CC} = 5V$, $V_I = 2V$, $f = 1MHz$		4		pF
C_{OUT}	Output capacitance	$V_{CC} = 5V$, $V_O = 2V$, $f = 1MHz$		7		pF

* : A typical value at T_a=25℃

Note 2. All measurements should be done quickly and not more than one output should be shorted at a time.
3. Icc is measured with all inputs at GND.

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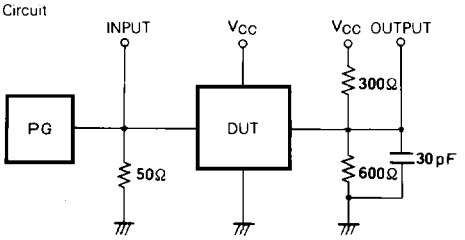
SWITCHING CHARACTERISTICS (V_{CC} = 5V ± 5%, T_a = 0 ~ 75°C, unless otherwise noted) (Note 4)

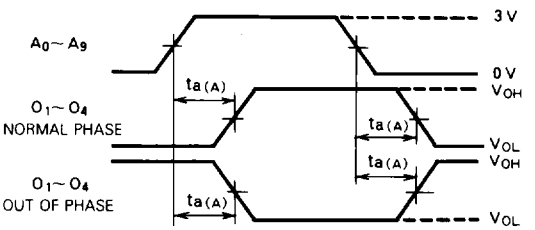
Symbol	Parameter	Limits									Unit
		M54740AP, S-1 M54741AP, S-1			M54740AP, S-2 M54741AP, S-2			M54740AP, S M54741AP, S			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{a(A)}$	Address access time		25	30		25	35		25	50	ns
$t_{a(\overline{E})}$	Chip enable access time		15	25		15	25		15	25	ns
$t_{CD(\overline{E})}$	Chip disable time		15	25		15	25		15	25	ns

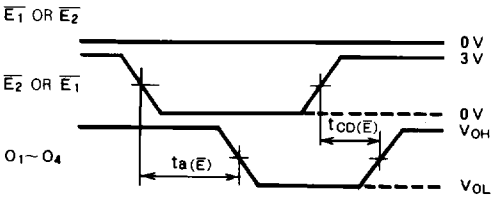
Note 4. Test Circuit



1. PG characteristics: t_r = 6ns, t_f = 6ns, PRR = 1MHz, t_{PW} = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω
2. The electrostatic capacitance of the load includes probe and jig capacitance.

TIMING DIAGRAMS (Reference voltage = 1.5V)

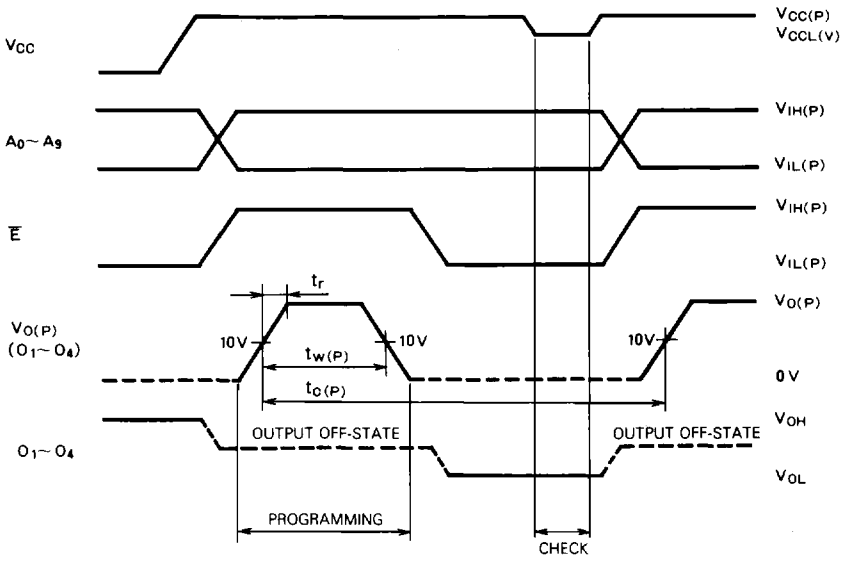




RECOMMENDED OPERATING CONDITIONS FOR PROGRAMMING (T_a = 25°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$V_{IH(P)}$	High level input voltage	2.4	5	5	V
$V_{IL(P)}$	Low level input voltage	0	0	0.4	V
$V_{O(P)}$	Applied output voltage	20	21	21	V
$t_{W(P)}$	Applied pulse width	0.05	0.18	50	ms
$t_{W(P)}/t_{C(P)}$	Duty Cycle		20	25	%
t_r	Pulse rise time	5	10	30	μs
$N_{(P)}$	Number of pulse applied	1	4	4	—
$V_{CC(P)}$	Supply voltage during programming	4.9	5	5.1	V
I_{OP}	Applied output current			100	mA
$V_{CCL(V)}$	Low level supply voltage for check after programming	4.4	4.4	4.5	V

PROGRAMMING TIMING DIAGRAM



Note 5. $V_{O(P)}$ is the waveform applied to the output during programming. $O_1 \sim O_4$ are the waveforms showing the output of the element itself.

6. $\bar{E}$ is the waveform for either $\bar{E}_1$ or $\bar{E}_2$, the other being taken as $V_{IL(P)}$.

PROGRAMMING METHOD

The elements actually programmed are the fuses making up the 4,096 memory cells. When the memory cell is not programmed, the output is logic high level (fuse closed). To put these at logic low level (fuse open), the following steps are taken.

(1) Apply $V_{CC(P)}$ supply voltage (5V Typ)
(2) Select the word to be programmed by using the address inputs $A_0 \sim A_9$ (Input voltage: $V_{IH(P)}$ 5V Typ, $V_{IL(P)}$ 5V Typ).
(3) Put at least one of the enable inputs $\overline{E_1}$, $\overline{E_2}$ at "H" ($V_{IH(P)}$ 0V Typ) and put the output in the OFF state.
(4) An output pulse $V_{O(P)}$ (21V Typ) is applied to the output corresponding to the bit to be programmed. $V_{O(P)}$ must be applied to each individual output, do not apply it to two or more outputs at same time.
(5) Put both E_1 and E_2 to "L" ($V_{IL(P)}$ 0V Typ).
(6) Put the supply voltage at $V_{CCL(P)}$ (4.4V Typ) and check whether programming was completed or not.
(7) If the test in step (6) is passed, repeat steps (1) through (6) for the next bit or word to be programmed. If the test in step (6) is not passed, repeat steps (1) through (6). If these steps are repeated four times and test results are not positive, the IC can be considered defective. For timing, refer to the programming timing diagrams.