To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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HD74AC538

1-of-8 Decoder with 3-State Output

REJ03D0276–0200Z
(Previous ADE-205-397 (Z))
Rev.2.00
Jul.16.2004

Description

The HD74AC538 decoder/demultiplexer accepts three Address (A0 to A2) input signal and decodes them to select one of eight mutually exclusive outputs. A polarity control input (P) determines whether the outputs are active LOW or active HIGH. A HIGH signal on either of the active LOW output Enable ($\overline{OE}$) inputs forces all outputs to the high impedance state. Two active HIGH and two active LOW input enables are available for easy expansion to 1-of-32 decoding with four packages, or for data demultiplexing to 1-of-8 or 1-of-16 destinations.

Features

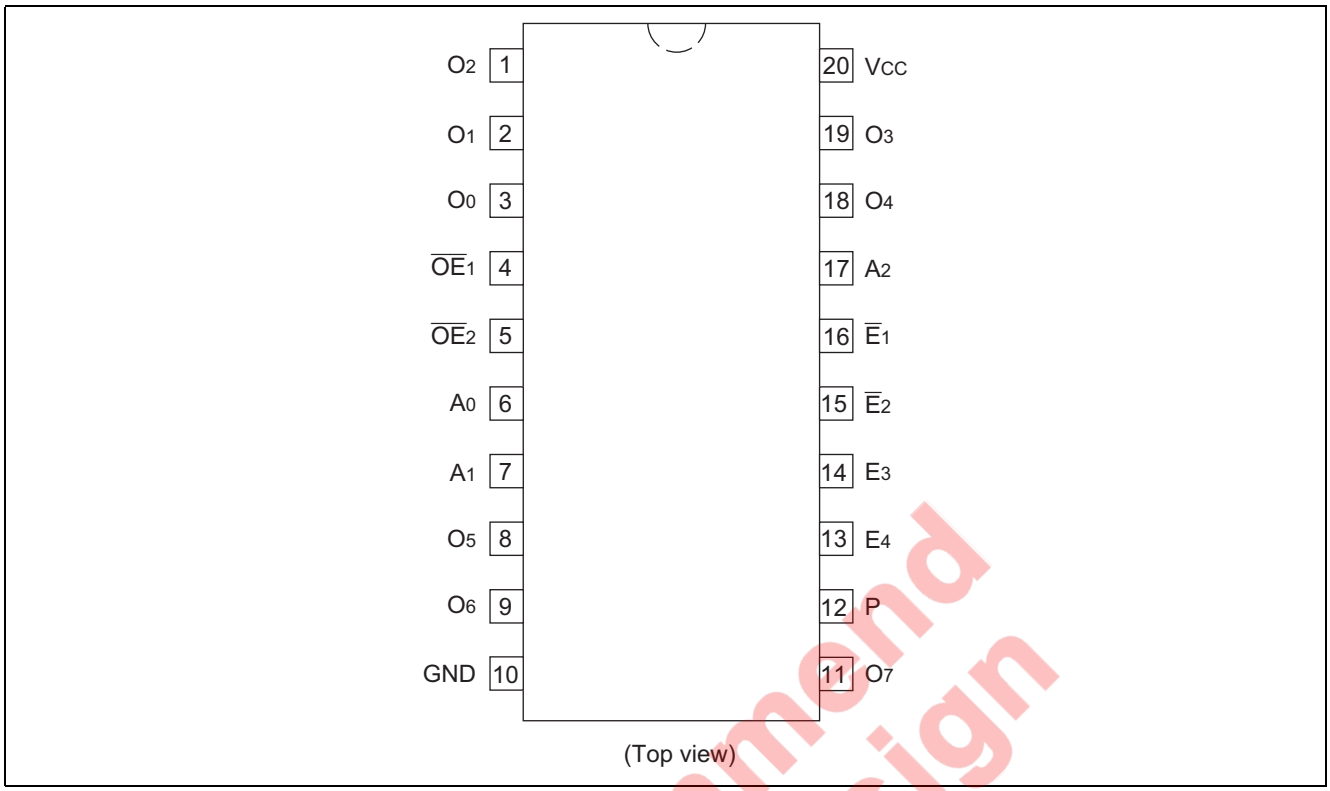
- Output Polarity Control
- Data Demultiplexing Capability
- Multiple Enables for Expansion
- Outputs Source/Sink 24 mA

- Ordering Information

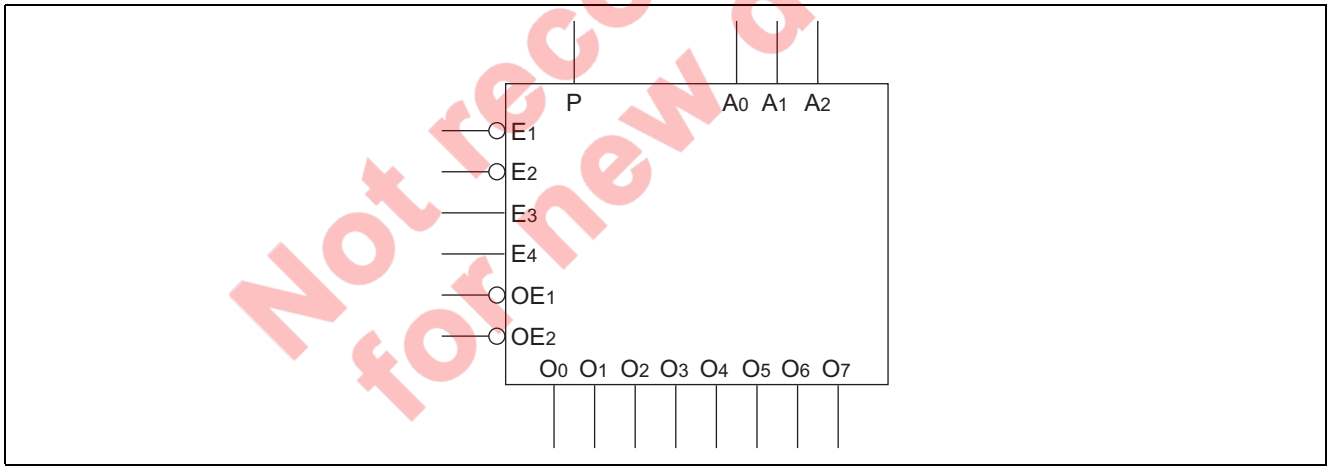
Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74AC538FPEL	SOP-20 pin (JEITA)	FP-20DAV	FP	EL (2,000 pcs/reel)
HD74AC538RPEL	SOP-20 pin (JEDEC)	FP-20DBV	RP	EL (1,000 pcs/reel)

Notes: 1. Please consult the sales office for the above package availability.
2. The packages with lead-free pins are distinguished from the conventional products by adding V at the end of the package code.

Pin Arrangement



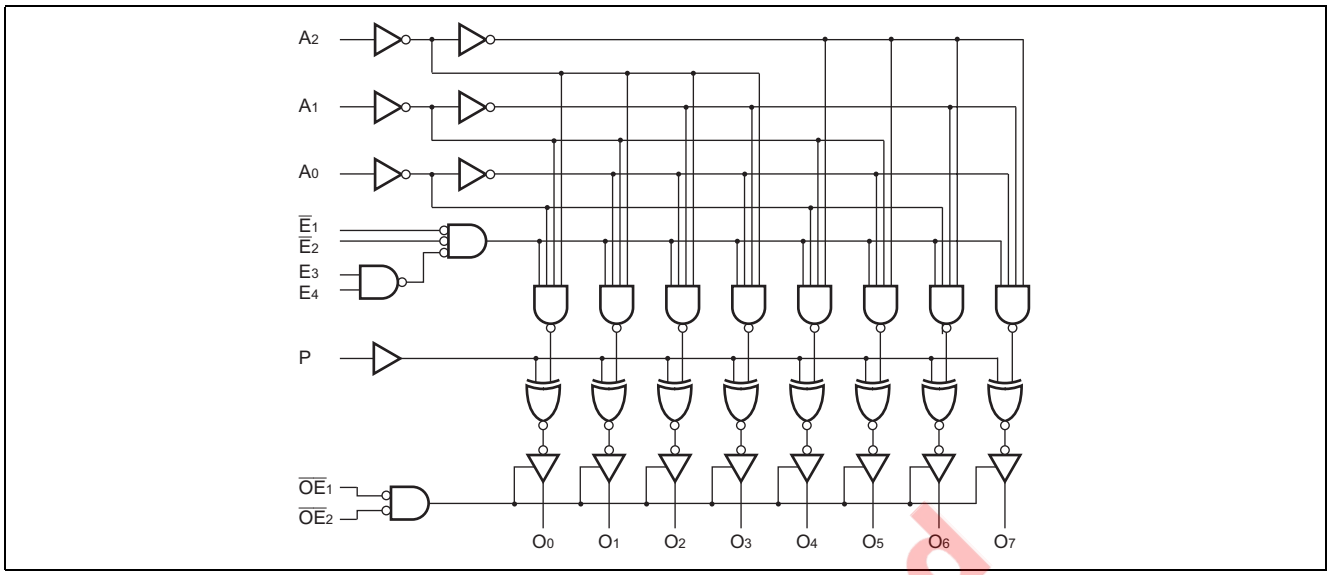
Logic Symbol



Pin Names

A_0 to A_2	Address Inputs
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)
E_3, E_4	Enable Inputs (Active HIGH)
P	Polarity Control Input
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable Inputs (Active LOW)
O_0 to O_7	3-State Outputs

Logic Diagram



Truth Table

Function	Inputs									Outputs							
	$\overline{OE}_1$	$\overline{OE}_2$	$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
High impedance	H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z
	Z	H	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
Disable	L	L	H	X	X	X	X	X	X	Outputs equal input							
	L	L	X	H	X	X	X	X	X								
	L	L	X	X	L	X	X	X	X								
	L	L	X	X	X	L	X	X	X								
Active HIGH output (P = L)	L	L	L	L	H	H	L	L	L	H	L	L	L	L	L	L	L
	L	L	L	L	H	H	L	L	H	L	H	L	L	L	L	L	L
	L	L	L	L	H	H	L	H	L	L	L	H	L	L	L	L	L
	L	L	L	L	H	H	L	H	H	L	L	L	H	L	L	L	L
	L	L	L	L	H	H	H	L	L	L	L	L	L	H	L	L	L
	L	L	L	L	H	H	H	L	H	L	L	L	L	L	H	L	L
	L	L	L	L	H	H	H	H	L	L	L	L	L	L	L	H	L
	L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L	H
Active LOW output (P = L)	L	L	L	L	H	H	L	L	L	L	H	H	H	H	H	H	H
	L	L	L	L	H	H	L	L	H	H	L	H	H	H	H	H	H
	L	L	L	L	H	H	L	H	L	H	H	L	H	H	H	H	H
	L	L	L	L	H	H	L	H	H	H	H	H	L	H	H	H	H
	L	L	L	L	H	H	H	L	L	H	H	H	H	L	H	H	H
	L	L	L	L	H	H	H	L	H	H	H	H	H	H	L	H	H
	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	L	H
	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L

H : High Voltage Level
L : Low Voltage Level
X : Immaterial
Z : High Impedance

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	–0.5 to 7	V	
DC input diode current	I_{IK}	–20	mA	V_I = –0.5V
		20	mA	V_I = Vcc+0.5V
DC input voltage	V_I	–0.5 to Vcc+0.5	V	
DC output diode current	I_{OK}	–50	mA	V_O = –0.5V
		50	mA	V_O = Vcc+0.5V
DC output voltage	V_O	–0.5 to Vcc+0.5	V	
DC output source or sink current	I_O	±50	mA	
DC V_{CC} or ground current per output pin	I_{CC}, I_{GND}	±50	mA	
Storage temperature	Tstg	–65 to +150	°C	

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	2 to 6	V	
Input and Output voltage	V_I, V_O	0 to V_{CC}	V	
Operating temperature	Ta	–40 to +85	°C	
Input rise and fall time (except Schmitt inputs) V_{IN} 30% to 70% V_{CC}	tr, tf	8	ns/V	V_{CC} = 3.0V
				V_{CC} = 4.5 V
				V_{CC} = 5.5 V

DC Characteristics

Item	Sym-bol	Vcc (V)	Ta = 25°C			Ta = –40 to +85°C		Unit	Condition	
			min.	typ.	max.	min.	max.			
Input Voltage	V_{IH}	3.0	2.1	1.5	—	2.1	—	V	V_{OUT} = 0.1 V or V_{CC} –0.1 V	
		4.5	3.15	2.25	—	3.15	—			
		5.5	3.85	2.75	—	3.85	—			
	V_{IL}	3.0	—	1.50	0.9	—	0.9		V_{OUT} = 0.1 V or V_{CC} –0.1 V	
		4.5	—	2.25	1.35	—	1.35			
		5.5	—	2.75	1.65	—	1.65			
Output voltage	V_{OH}	3.0	2.9	2.99	—	2.9	—	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = –50 µA	
		4.5	4.4	4.49	—	4.4	—			
		5.5	5.4	5.49	—	5.4	—			
		3.0	2.58	—	—	2.48	—		V_{IN} = V_{IL} or V_{IH}	I_{OH} = –12 mA
		4.5	3.94	—	—	3.80	—			I_{OH} = –24 mA
		5.5	4.94	—	—	4.80	—			I_{OH} = –24 mA
	V_{OL}	3.0	—	0.002	0.1	—	0.1		V_{IN} = V_{IL} or V_{IH} I_{OUT} = 50 µA	
		4.5	—	0.001	0.1	—	0.1			
		5.5	—	0.001	0.1	—	0.1			
		3.0	—	—	0.32	—	0.37		V_{IN} = V_{IL} or V_{IH}	I_{OL} = 12 mA
		4.5	—	—	0.32	—	0.37			I_{OL} = 24 mA
		5.5	—	—	0.32	—	0.37			I_{OL} = 24 mA
Input leakage current	I_{IN}	5.5	—	—	±0.1	—	±1.0	µA	V_{IN} = V_{CC} or GND	
3 State current	I_{OZ}	5.5	—	—	±0.5	—	±5.0	µA	$V_{IN(OE)}$ = V_{IL}, V_{IH} V_{IN} = V_{CC} or GND V_{OUT} = V_{CC} or GND	
Dynamic output current*	I_{OLD}	5.5	—	—	—	86	—	mA	V_{OLD} = 1.1 V	
	I_{OHD}	5.5	—	—	—	–75	—	mA	V_{OHD} = 3.85 V	
Quiescent supply current	I_{CC}	5.5	—	—	8.0	—	80	µA	V_{IN} = V_{CC} or ground	

*Maximum test duration 2.0 ms, one output loaded at a time.

AC Characteristics

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C, C_L = 50 pF			Ta = –40°C to +85°C, C_L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Propagation delay	t_{PLH}	3.3	1.0	10.5	17.5	1.0	20.0	ns
A_n to O_n		5.0	1.0	8.0	12.5	1.0	14.0	
Propagation delay	t_{PHL}	3.3	1.0	9.5	17.5	1.0	20.0	ns
A_n to O_n		5.0	1.0	7.0	12.0	1.0	14.0	
Propagation delay	t_{PLH}	3.3	1.0	11.0	19.5	1.0	23.0	ns
$\overline{E}_1$, or $\overline{E}_2$ to O_n		5.0	1.0	8.0	14.5	1.0	16.5	
Propagation delay	t_{PHL}	3.3	1.0	10.0	19.5	1.0	23.0	ns
$\overline{E}_1$, or $\overline{E}_2$ to O_n		5.0	1.0	8.0	14.5	1.0	16.5	
Propagation delay	t_{PLH}	3.3	1.0	11.0	19.5	1.0	23.0	ns
$\overline{E}_3$, or $\overline{E}_4$ to O_n		5.0	1.0	8.5	14.5	1.0	17.0	
Propagation delay	t_{PHL}	3.3	1.0	10.5	20.0	1.0	23.5	ns
$\overline{E}_3$, or $\overline{E}_4$ to O_n		5.0	1.0	8.0	15.0	1.0	18.0	
Propagation delay	t_{PLH}	3.3	1.0	10.5	15.5	1.0	17.5	ns
P to O_n		5.0	1.0	9.0	11.0	1.0	12.5	
Propagation delay	t_{PHL}	3.3	1.0	9.0	15.0	1.0	17.0	ns
P to O_n		5.0	1.0	7.5	10.5	1.0	11.5	
Propagation delay	t_{PZH}	3.3	1.0	7.0	14.0	1.0	15.5	ns
$\overline{OE}_n$ to O_n		5.0	1.0	5.0	8.5	1.0	9.5	
Propagation delay	t_{PZL}	3.3	1.0	8.5	16.5	1.0	19.0	ns
$\overline{OE}_n$ to O_n		5.0	1.0	5.5	9.5	1.0	11.5	
Propagation delay	t_{PHZ}	3.3	1.0	7.0	14.0	1.0	15.5	ns
$\overline{OE}_n$ to O_n		5.0	1.0	6.0	10.5	1.0	11.5	
Propagation delay	t_{PLZ}	3.3	1.0	9.0	14.5	1.0	17.0	ns
$\overline{OE}_n$ to O_n		5.0	1.0	7.0	10.5	1.0	12.0	

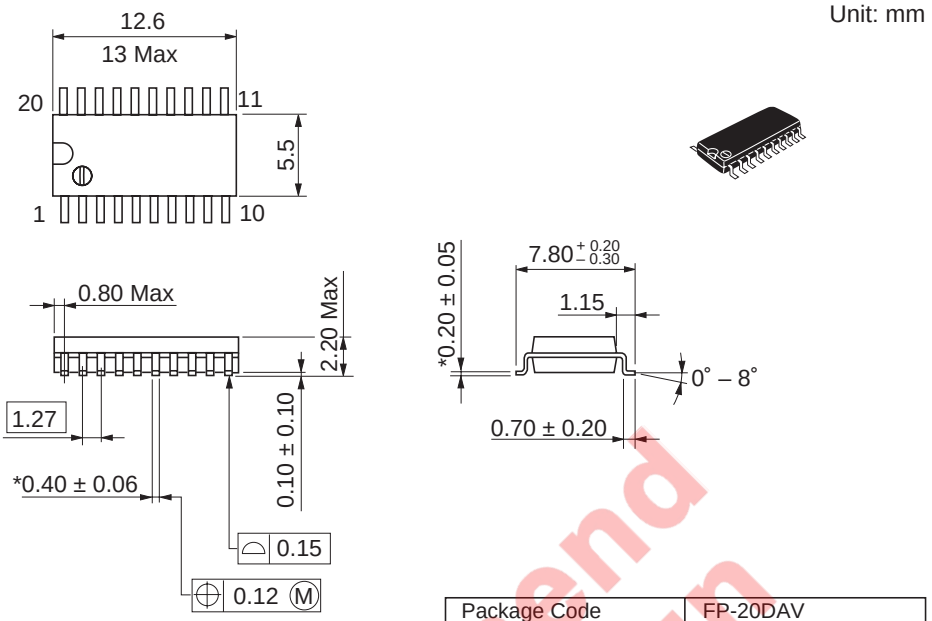
Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C_{IN}	4.5	pF	V_{CC} = 5.5 V
Power dissipation capacitance	C_{PD}	100	pF	V_{CC} = 5.0 V

Package Dimensions

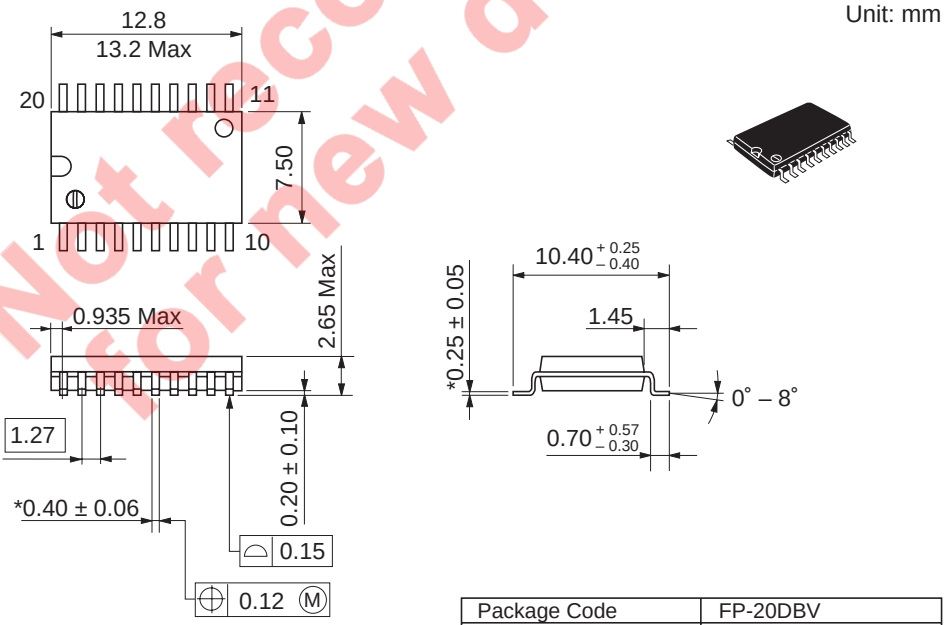
As of January, 2003
Unit: mm



*Ni/Pd/Au plating

Package Code	FP-20DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.31 g

As of January, 2003
Unit: mm



*Ni/Pd/Au plating

Package Code	FP-20DBV
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.52 g

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