FX-500
Low Jitter Frequency Translator

Features

- Complete Frequency Translator to 77.760 MHz
- 3.3 Volt or 5.0 Volt Supply
- Capable of locking to an 8 kHz pulse/BITS clock
- Tri-State Output allows board test
- J-lead Ceramic Package
- Advanced Customer ASIC Technology
- Absolute Pull Range Performance to ±100 ppm
- CMOS Output
- Commercial or Industrial Temperature Range
- EIA Compatible Tape and Reel Packaging
- RoHS/Lead Free Compliant

Description

The FX-500 is a complete crystal-based frequency translator used in communications applications where low jitter is paramount.

Performance advantages include superior jitter performance, high output frequencies and small package size. Advanced custom ASIC technology results in a highly robust, reliable and predictable device.

The device is packaged in a 6 pin J-Lead ceramic package with a hermetic seam welded lid.

Applications

- Frequency Translation, Clock Smoothing
- Telecom – SONET/SDH/ATM
- Datacom – DSLAM, DSLAR, Access Nodes
- Cable Modem Head End
- Base Station – GSM, CDMA
- Military Communications

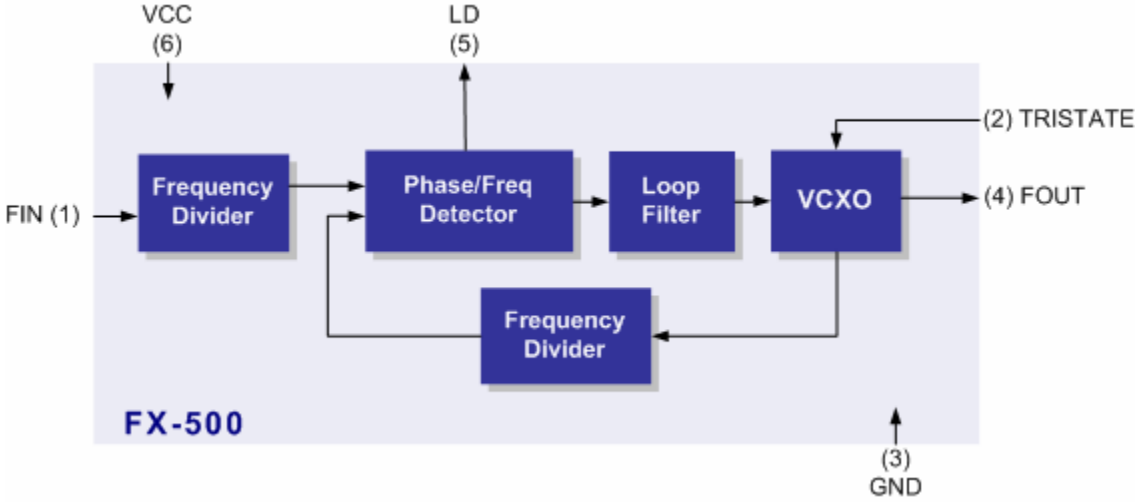


Figure 1. Functional Block Diagram

Electrical Performance

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Supply Voltage	V_{DD} V_{DD}	3.0 4.5	3.3 5.0	3.6 5.5	V V	1,5
Supply Current @ 19.44 MHz 48.408 MHz 77.760 MHz	I_{DD} I_{DD} I_{DD}		15 25 35	20 30 40	mA mA mA	
Input Input Low Level Voltage Input High Level Voltage Frequency Pulse Width	 V_{IL} V_{IH} f_{IN}	 0.7* V_{DD} 1k 6	 	 0.3* V_{DD} 77.76 M	 V V Hz Ns	
Output Output High Level Voltage Output Low Level Voltage	 V_{OH} V_{OL}	 0.9*V_{DD}	 	 0.1*V_{DD}	 V V	
Transition Times Rise Time Fall Time	 t_R t_F	 	 1.8 1.8	 3.0 3.0	 ns ns	 2
Duty Cycle ≤ 60 MHz ≥ 60 MHz	D	 45 40	 	 55 60	% 	 3,5
Nominal Output Frequency	f_O	0.100		77.76	MHz	4
Absolute Pull Range	APR	See Part Numbering			ppm	
Leakage Current of Input	I_C	-1		1	µA	
Loop Bandwidth (-3 dB), 8 kHz Input	BW		10		Hz	
Jitter (Application: 8 kHz to 77.76 MHz) rms peak/peak peak/peak	Φ_J		 4.7 44 0.003		 ps ps UI	
Operating Temperature	T_{OP}	-40		+85	°C	5
Package Size		9.0 x 14.0 x 4.5			Mm	

1. A 0.1 µF low frequency tantalum bypass capacitor in parallel with a 0.01 µF high frequency ceramic capacitor is recommended.
2. Figure 3 defines the waveform parameters. Figure 2 illustrates the standard test conditions under which these parameters are specified and tested.
3. Duty cycle is defined as (on time÷period), with VS = VDD/2, per figure 3. Duty cycle is measured with a 15pf load per figure 2.
4. Other frequencies may be available, please contact factory.
5. See Standard Frequencies and Ordering Information (Pg 6).

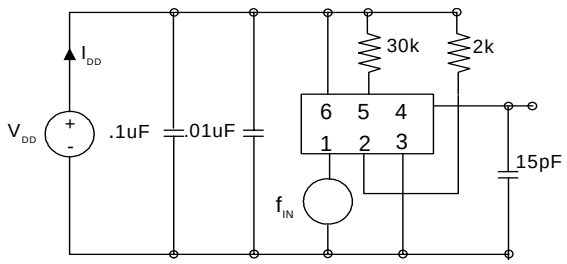


Figure 2. Test Circuit

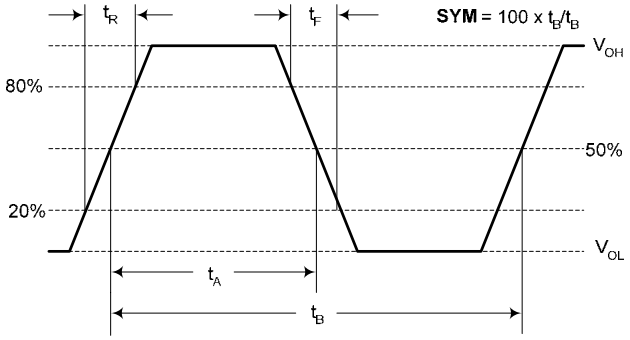


Figure 3. Output Waveform

Outline Diagram

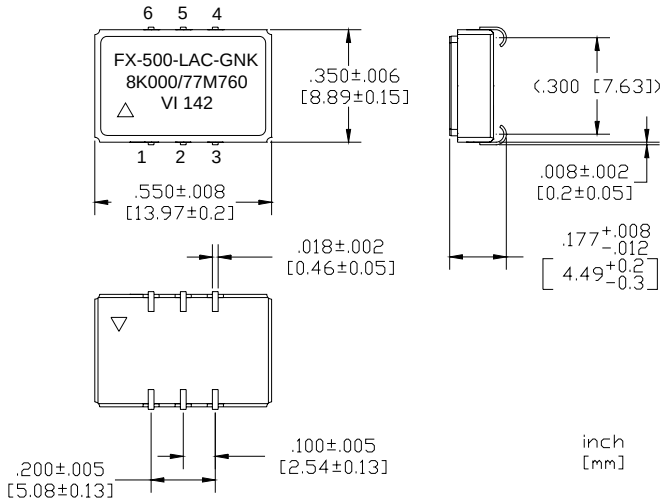


Figure 4.

Suggested Pad Layout

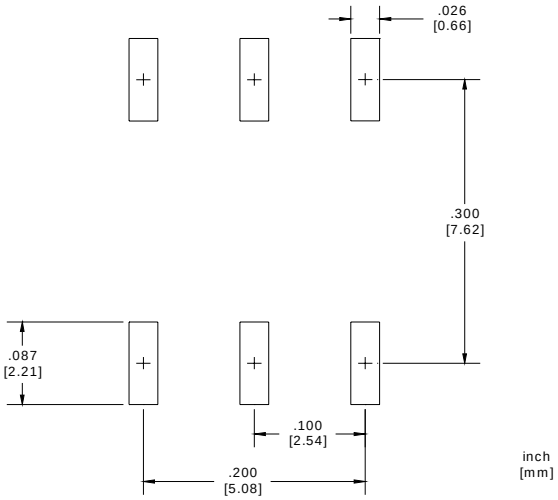


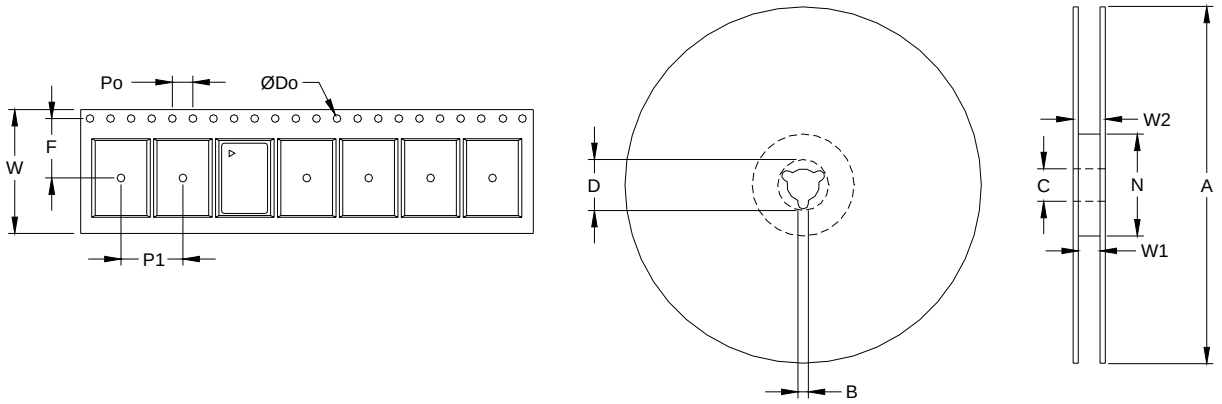
Figure 5.

Pin Out

Pin #	Symbol	Function
1	f_{IN}	Input Frequency
2	Tri-state[1]	Logic Low = Output Disable Logic High = Output Enabled
3	GND	Case and Electrical Ground
4	f_O	Output Frequency
5	LD[2]	Lock Detect
6	V_{DD}	Power Supply Voltage (3.3 V ± 0.3 or 5.0 V ± 0.5)

1. Tristate is driven to logic high or logic low; there is no internal pull up or pull down resistor.
2. LD is an open collector output requiring a 30k ohm pullup resistor to V_{DD}. LD output is logic high under locked condition, logic low for no input at f_{IN}, and for "out-of-lock" condition LD transitions between logic low and logic high at the phase detector frequency.

Tape and Reel (EIA-481-2-A)



Tape Dimensions (mm)						Reel Dimensions (mm)							
Dimension	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	# Per
Tolerance	Typ	Typ	Typ	Typ	Typ	Typ	Min	Typ	Min	Min	Typ	Max	Reel
FX-500	24	11.5	1.5	4	12	330	1.78	13	20.2	100	24.4	30.4	200

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Power Supply	V_{CC}	0 to 7	Vdc
Storage Temperature	TS	-55 to 125	°C
Soldering Temp/Time	T_{LS}	260/40	°C/sec

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Reliability

The FX-500 family is capable of meeting the following qualification tests:

Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016

Handling Precautions

Although ESD protection circuitry has been designed into the FX-500 proper precautions should be taken when handling and mounting. VI employs a human body model and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation.

ESD Ratings

Model	Minimum	Conditions
Human Body Model	1000 V	MIL-STD 883, Method 3015
Charged Device Model	1000 V	JEDEC, JESD22-C101

Reflow Profile (IPC/JEDEC J-STD-020C)

Parameter	Symbol	Value
PreHeat Time	t_S	60 sec Min, 180 sec Max
Ramp Up	R_{UP}	3 °C/sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	t_{AMB-P}	480 sec Max
Time At 260 °C	t_P	20 sec Min, 40 sec Max
Ramp Down	R_{DN}	6 °C/sec Max

The FX-500 has been qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The temperatures refer to the topside of the package, measured on the package body surface. The FX-500 device is hermetically sealed so an aqueous wash is not an issue.

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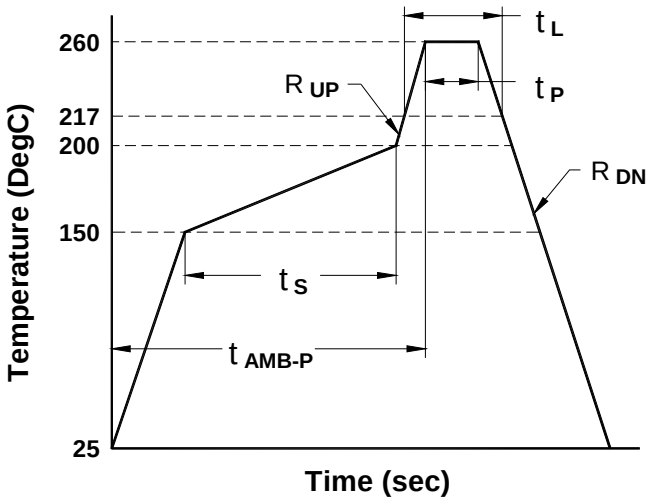
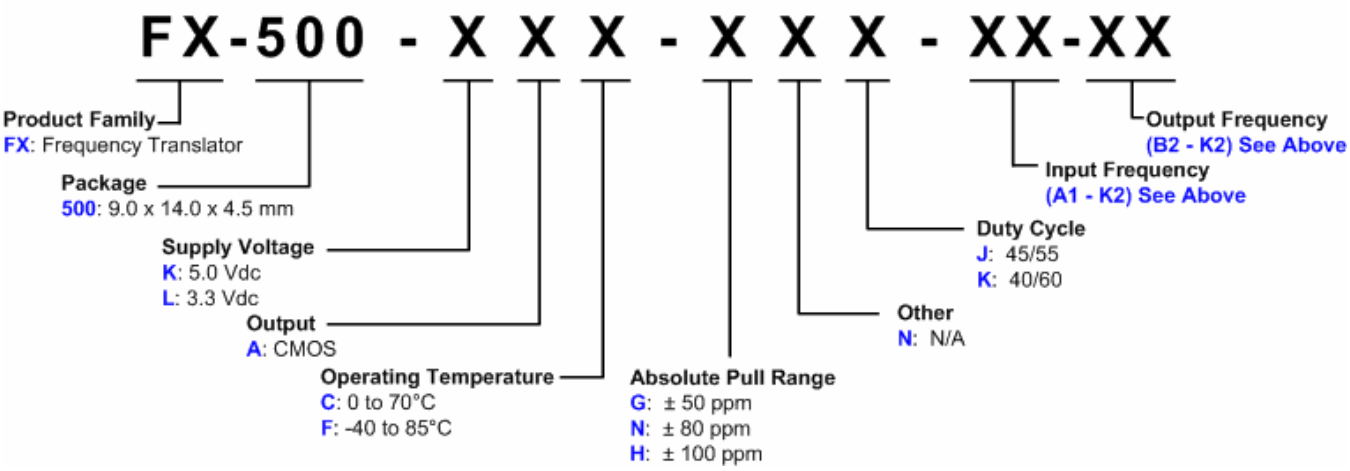


Standard Frequencies (MHz)*											
0.00100	A1	0.40000	AF	10.00000	C4	20.48000	E4	38.88000	H5	62.20800	J8
0.00400	A2	0.48000	AK	10.48720	DN	24.57600	E6	40.00000	JF	65.53600	J6
0.00800	A3	0.51200	AJ	12.28800	D8	24.70400	E7	44.73600	J3	73.72800	K8
0.01000	A6	0.65545	AE	12.35200	D1	25.00000	F7	44.92800	JE	77.76000	K2
0.01573	AD	1.02400	B2	16.00000	D9	25.60000	F6	49.15200	J7		
0.01575	AC	1.22880	BK	16.38400	D5	27.00000	F4	49.40800	J2		
0.04800	AB	1.54400	B3	19.44000	D6	32.00000	H2	50.00000	JD		
0.06400	A5	2.04800	B4	19.69897	DK	32.76800	H3	51.84000	J4		
0.10000	AH	6.31200	C7	19.71900	DH	34.36800	H6	60.00000	JR		
0.25600	AM	7.68000	C9	20.00000	E2	37.05600	H4	61.44000	J5		

Note 1: Other frequencies are available upon request, please contact VI for details.
SS is code for non-standard frequencies, list the frequency after the part number.
Note 2: Not all combinations are possible.
Note 3: Output frequency must be equal to or greater than the input frequency. The ratio of f_O/f_{IN} must be an integer. Also, the output frequency must be equal to greater than 100 kHz.

Ordering Information



EXAMPLE: FX-500-LAC-GNK-A3-K2
FX-500, 3.3V, CMOS output, 0 to 70°C operating temperature, ±50 ppm APR, 40/60% duty cycle with an 8 kHz input and 77.760 MHz output.

For Additional Information, Please Contact:

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