Am99C134

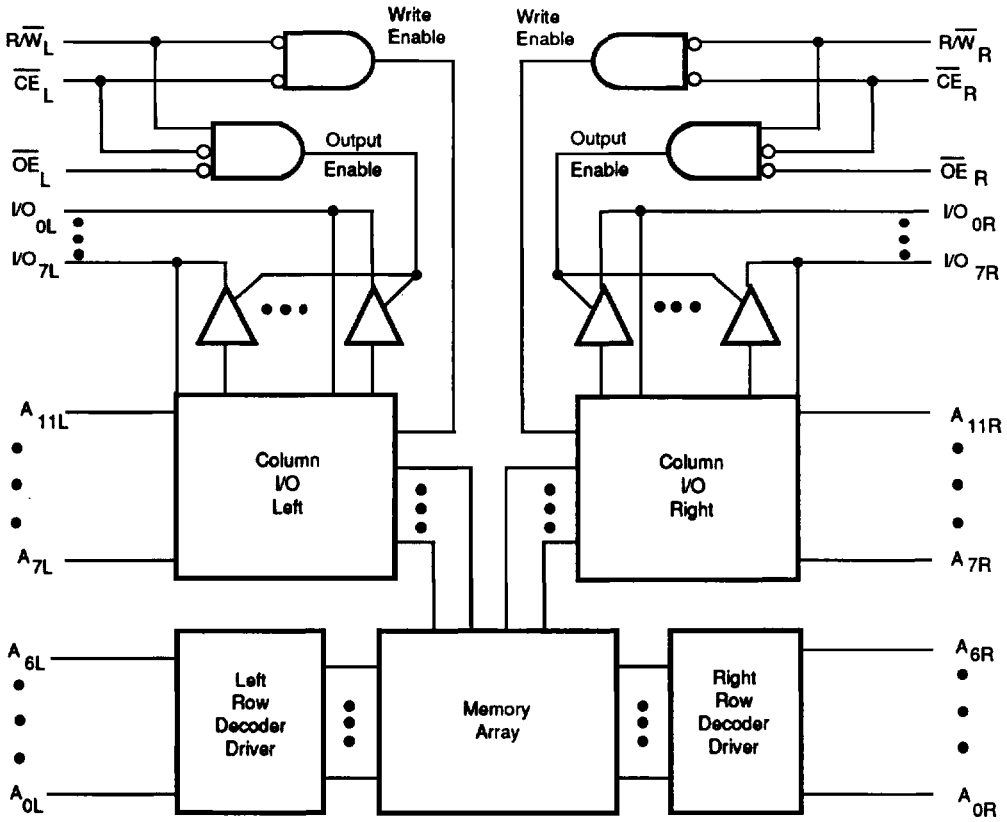
4K x 8 Dual-Port Static Random Access Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **True dual port operation**
- **Access time as fast as 35ns**
- **Low power dissipation**
  - 900 mW max. operating power
  - 2.5 mW max. standby power for CMOS interface levels
- **2V Data retention capability**
- **Automatic power-down feature**
- **All inputs and outputs are TTL-compatible**
- **48-pin DIP or 52-pin LCC/PLCC**
- **Single +5V power supply**
- **Advanced CMOS technology**

BLOCK DIAGRAM



11690-001A

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GENERAL DESCRIPTION

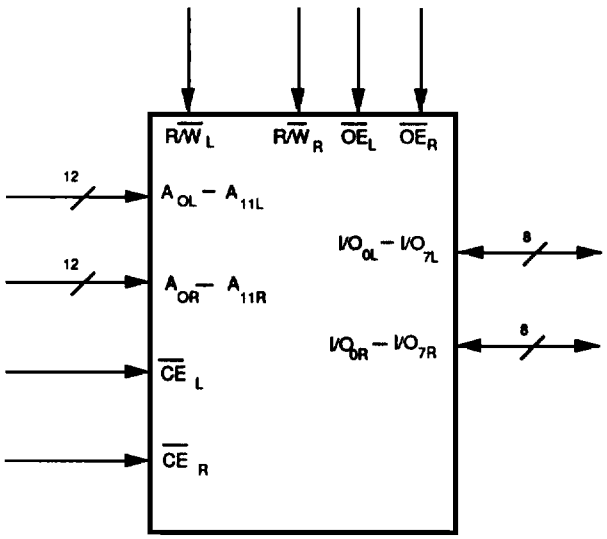
The AM99C134 is an extremely high-speed 4K X 8 Dual-Port static RAM designed to be used in systems where on-chip hardware arbitration is not needed. This part is suitable for those systems which are to be able to externally arbitrate when both ports simultaneously access the same dual-port RAM location.

The AM99C134 has two independent ports called Left and Right port. Each port consists of an 8-bit bidirectional data bus and a 12-bit address input and necessary control signals.

The AM99C134 also has two chip enable signals corresponding to the left and right ports. Before any transaction on a port takes place, the corresponding chip enable input must be activated. If a chip enable signal is not active, the circuitry corresponding to its side automatically powers down and enters standby mode.

The AM99C134 is packaged in 48-pin DIPs or 52-pin chip carriers. All inputs and outputs are TTL-compatible and the device requires a single +5-volt power supply while operating, but will hold the data when the power supply level is maintained as low as 2V.

LOGIC SYMBOL



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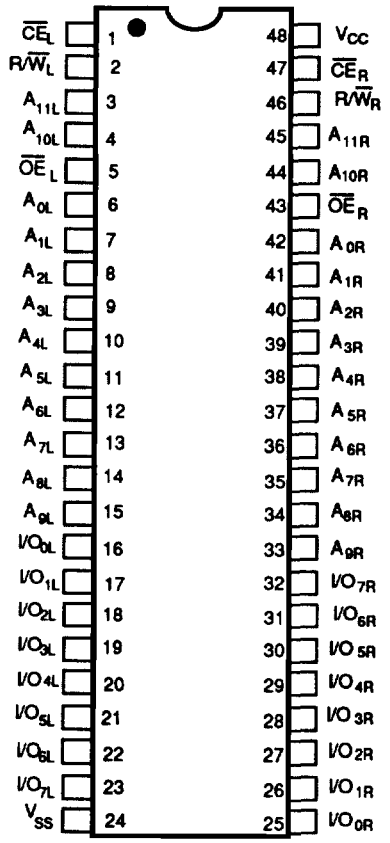
CONNECTION DIAGRAM



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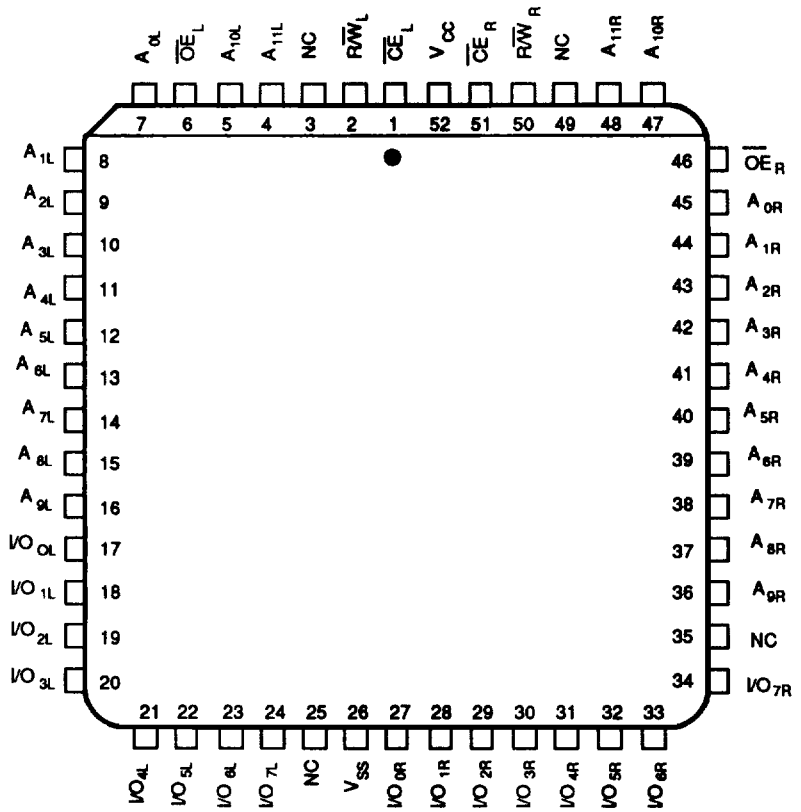
PLCC PIN CONNECTION



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PIN DESRCRIPTION

A_{OL} - A_{11L}

Left Port Address (Inputs)

These twelve (12) inputs constitute the memory address for the left port. A_0 is the least significant bit position and A_{11} is the most significant position. A HIGH level on any of these inputs represents a logic 1 at that position and low represents a logic 0. The sequence of events and related timing for the address inputs during read and write operations will be discussed in later sections of this data sheet.

A_{OR} - A_{11R}

Right Port Address (Inputs)

These twelve (12) inputs constitute the memory address for the right port. A_0 is the least significant bit position and A_{11} is the most significant position. A HIGH level on any of these inputs represents a logic 1 at that position and low represents a logic 0. The sequence of events and related timing for the address inputs during read and write operations will be discussed in later sections of this data sheet.

$\overline{CE}_L$

Left Port Chip Enable (Input)

This input must be LOW before any transaction from the left port and remain LOW for the duration of the transaction. When this input goes HIGH, left port logic circuits enter standby power mode and remain in this mode as long as this input remains HIGH.

$\overline{CE}_R$

Right Port Chip Enable (Input)

Operation of this input is identical to CE_L except that the CE_R input controls the right port.

GND

V_{SS} Ground.

I/O_{OL} - I/O_{7L}

Left Port Input/Output Bus (Input/Output; Three State)

These eight lines constitute the data bus for the left port. If a read operation is performed using the left port, data from the location addressed by the left port address will be available on these lines. Similarly, to perform a write operation using the left port, data to be written into the memory must be presented on these lines. The drivers on the chip to drive these lines are enabled only when the $\overline{CE}_L$ is LOW, $\overline{OE}_L$ is LOW and $R/\overline{W}_L$ is HIGH.

I/O_{OR} - I/O_{7R}

Right Port Input/Output Bus (Input/Output; Three State)

These eight lines constitute the data bus for the right port. If a read operation is performed using the right port, data from the location addressed by the right port address will be available on these lines. Similarly, to perform a write operation using the left port, data to be written into the memory must be presented on these lines. The drivers on the chip to drive these lines are enabled only when the $\overline{CE}_R$ is LOW, $\overline{OE}_R$ is LOW and $R/\overline{W}_R$ is HIGH.

$\overline{OE}_L$

Output Enable Left I/O Port (Input)

When this input is HIGH, the left port I/O bus lines are in high impedance state. If this input is LOW and $\overline{CE}_L$ is LOW and $R/\overline{W}_L$ is HIGH, the left port drivers are enabled and data from the location addressed by the $A_{OL} - A_{11L}$ inputs will be available on the I/O bus lines of the left port.

$\overline{OE}_R$

Output Enable Right I/O Port (Input)

When this input is HIGH, the right port I/O bus lines are in high impedance state. If this input is LOW and $\overline{CE}_R$ is LOW and $R/\overline{W}_R$ is HIGH, the right port drivers are enabled and data from the location addressed by the A_{OR} - A_{11R} inputs will be available on the I/O bus lines of the right port.

$R/\overline{W}_L$

Left Port Read/Write Enable (Input)

This input is used to specify the left port function to be performed. HIGH indicates a read and LOW indicates a write function.

When the $\overline{CE}_L$ is LOW and the $\overline{OE}_L$ is LOW and the $R/\overline{W}_L$ is HIGH, data from the location addressed by the A_{OL} - A_{11L} will be available on the I/O_{OL} - I/O_{7L} lines.

When the $\overline{CE}_L$ is LOW and the $R/\overline{W}_L$ goes LOW, data present on the I/O_{OL} - I/O_{7L} lines will be written into the location addressed by the A_{OL} - A_{11L} inputs. It should be noted that the write operation is not effected by the $\overline{OE}_L$ input. However, it is recommended that the $\overline{OE}_L$ input be held HIGH during a write operation.

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$R/\overline{W}_R$

Right Port Read/Write Enable (Input)

This input is used to specify the right port function to be performed. HIGH indicates a read and LOW indicates a write function.

When the $\overline{CE}_R$ is LOW and the $\overline{OE}_R$ is LOW and the $R/\overline{W}_R$ is HIGH, data from the location addressed by the A_{0R} - A_{11R} will be available on the I/O_{0R} - I/O_{7R} lines.

When the $\overline{CE}_R$ is LOW and the $R/\overline{W}_R$ goes LOW, data present on the I/O_{0R} - I/O_{7R} lines will be written into the location addressed by the A_{0R} - A_{11R} inputs. It should be noted that the write operation is not effected by the $\overline{OE}_R$ input. However, it is recommended that the $\overline{OE}_R$ input be held HIGH during a write operation.

V_{CC}

+5-Volt Power Supply.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A)	0 to 70°C
Supply Voltage (V_{CC})	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.